### 1 Features
- $V_{IN}$ Range From 4.5 V to 75 V
- High-Side Adjustable Current Sense
- 2-$\Omega$, 1-A Peak MOSFET Gate Driver
- Input Undervoltage and Output Overvoltage Protection
- PWM and Analog Dimming
- Cycle-by-Cycle Current Limit
- Programmable Switching Frequency
- Zero Current Shutdown and Thermal Shutdown
- LED Output Status Flag (LM3423 and LM3423-Q0 Only)
- Fault Status Flag and Timer (LM3423 and LM3423-Q0 Only)

### 2 Applications
- LED Drivers: Buck, Boost, Buck-Boost, and SEPIC
- Indoor and Outdoor Area SSL
- Automotive
- General Illumination
- Constant-Current Regulators

### 3 Description
The LM3421 and LM3423 family of devices are versatile high voltage N-channel MOSFET controllers for LED drivers. They can be easily configured in buck, boost, buck-boost and SEPIC topologies. This flexibility, along with an input voltage rating of 75 V, makes these controllers ideal for illuminating LEDs in a large family of applications.

Adjustable high-side current sense voltage allows for tight regulation of the LED current with the highest efficiency possible. The LM3421 and LM3423 devices use predictive off-time (PRO) control, which is a combination of peak current-mode control and a predictive off-timer. This method of control eases the design of loop compensation while providing inherent input voltage feed-forward compensation.

The LM3421 and LM3423 devices include a high-voltage start-up regulator that operates over a wide input range of 4.5 V to 75 V. The internal PWM controller is designed for adjustable switching frequencies of up to 2 MHz, thus enabling compact solutions.

### Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421</td>
<td>HTSSOP (16)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
<tr>
<td>LM3423</td>
<td>HTSSOP (20)</td>
<td>6.50 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Typical Boost Application**
Table of Contents

1 Features .......................................................... 1
2 Applications .................................................. 1
3 Description .................................................. 1
4 Revision History ........................................... 2
5 Device Comparison ....................................... 3
6 Pin Configuration and Functions ....................... 4
7 Specifications ............................................... 5
   7.1 Absolute Maximum Ratings ..................... 5
   7.2 ESD Ratings ............................................ 6
   7.3 Recommended Operating Conditions .......... 6
   7.4 Thermal Information ................................ 6
   7.5 Electrical Characteristics ....................... 7
   7.6 Typical Characteristics ......................... 11
8 Detailed Description ...................................... 13
   8.1 Overview ............................................. 13
   8.2 Functional Block Diagram ....................... 13
   8.3 Feature Description ................................ 14
9 Application and Implementation ...................... 28
   9.1 Application Information ......................... 28
   9.2 Typical Applications ............................ 32
10 Power Supply Recommendations .................... 65
   10.1 General Recommendations .................... 65
   10.2 Input Supply Current Limit .................... 65
11 Layout ..................................................... 65
   11.1 Layout Guidelines ............................. 65
   11.2 Layout Example .................................. 66
12 Device and Documentation Support .................. 67
   12.1 Device Support .................................. 67
   12.2 Related Links .................................. 67
   12.3 Community Resources ........................ 67
   12.4 Trademarks ..................................... 67
   12.5 Electrostatic Discharge Caution ............. 67
   12.6 Glossary .......................................... 67
13 Mechanical, Packaging, and Orderable Information ........................................ 67

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2015) to Revision G Page

- Deleted references to automotive grade (LM342x-Q1 and LM342x-Q0) devices, now available in data sheet SNVSB95... 1
- Corrected typographic error in Table 1 .................................................................................................................. 3
- Changed EN pulldown resistance specification minimum value from: 0.45 MΩ to: 0.245 MΩ Electrical Characteristics table. ........................................................................................................................................... 7
- Changed EN pulldown resistance specification maximum value from: 1.3 MΩ to: 2.85 MΩ in Electrical Characteristics table. ........................................................................................................................................... 7

Changes from Revision E (April 2013) to Revision F Page

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ........................................................................................................ 1

Changes from Revision D (May 2013) to Revision E Page

- Changed layout of National Data Sheet to TI format .................................................................................................................. 64
# 5 Device Comparison

## Table 1. Device Comparison

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>LED OUTPUT</th>
<th>FAULT STATUS</th>
<th>QUALIFICATION</th>
<th>TEMPERATURE RANGE, $T_A$</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421-Q0</td>
<td>No</td>
<td>No</td>
<td>AEC-Q100 Grade 0</td>
<td>-40°C to +150°C</td>
</tr>
<tr>
<td>LM3421-Q1</td>
<td>No</td>
<td>No</td>
<td>AEC-Q100 Grade 1</td>
<td>-40°C to +125°C</td>
</tr>
<tr>
<td>LM3423-Q0</td>
<td>Yes</td>
<td>Yes</td>
<td>AEC-Q100 Grade 0</td>
<td>-40°C to +150°C</td>
</tr>
<tr>
<td>LM3423-Q1</td>
<td>Yes</td>
<td>Yes</td>
<td>AEC-Q100 Grade 1</td>
<td>-40°C to +125°C</td>
</tr>
<tr>
<td>LM3421</td>
<td>No</td>
<td>No</td>
<td>Commercial Grade</td>
<td>-40°C to +125°C</td>
</tr>
<tr>
<td>LM3423</td>
<td>Yes</td>
<td>Yes</td>
<td>Commercial Grade</td>
<td>-40°C to +125°C</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

![Pin Configuration Diagram](image)

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O(1)</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>LM3423</td>
<td>LM3421</td>
</tr>
<tr>
<td>AGND</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>COMP</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>CSH</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>DDRV</td>
<td>13</td>
<td>9</td>
</tr>
<tr>
<td>DPOL</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>EN</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>FLT</td>
<td>9</td>
<td>—</td>
</tr>
<tr>
<td>GATE</td>
<td>15</td>
<td>11</td>
</tr>
<tr>
<td>HSN</td>
<td>20</td>
<td>16</td>
</tr>
<tr>
<td>HSP</td>
<td>19</td>
<td>15</td>
</tr>
<tr>
<td>IS</td>
<td>17</td>
<td>13</td>
</tr>
<tr>
<td>LRDY</td>
<td>11</td>
<td>—</td>
</tr>
<tr>
<td>nDIM</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>OVP</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>PGND</td>
<td>14</td>
<td>10</td>
</tr>
<tr>
<td>RCT</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

(1) G = Ground, I = Input, O = Output

---

Copyright © 2008–2019, Texas Instruments Incorporated

Product Folder Links: LM3421 LM3423
### Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O(1)</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPD</td>
<td>18</td>
<td>14</td>
</tr>
<tr>
<td>TIMR</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>VIN</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>VCC</td>
<td>16</td>
<td>12</td>
</tr>
<tr>
<td>Thermal PAD</td>
<td>G</td>
<td>Thermal PAD on bottom of IC. Star ground, connecting AGND and PGND.</td>
</tr>
<tr>
<td>DAP</td>
<td>DAP (21)</td>
<td>DAP (17)</td>
</tr>
</tbody>
</table>

### 7 Specifications

#### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN, EN, RPD, nDIM</td>
<td>–0.3</td>
<td>76</td>
</tr>
<tr>
<td>OVP, HSP, HSN, LRDY, FLT, DPOL</td>
<td>–0.3</td>
<td>76</td>
</tr>
<tr>
<td>RCT</td>
<td>–0.3</td>
<td>76</td>
</tr>
<tr>
<td>IS</td>
<td>–0.3</td>
<td>76</td>
</tr>
<tr>
<td>VCC</td>
<td>–0.3</td>
<td>8</td>
</tr>
<tr>
<td>TIMR</td>
<td>–0.3</td>
<td>7</td>
</tr>
<tr>
<td>COMP, CSH</td>
<td>–0.3</td>
<td>6</td>
</tr>
<tr>
<td>GATE, DDRV</td>
<td>–0.3</td>
<td>VCC+2.5 for 100 ns</td>
</tr>
<tr>
<td>PGND</td>
<td>–0.3</td>
<td>0.3</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) Refer to [http://www.ti.com/packaging](http://www.ti.com/packaging) for more detailed information and mounting techniques.
7.2 ESD Ratings

<table>
<thead>
<tr>
<th>$V_{(ESD)}$</th>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101</td>
<td>±500</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Operating junction temperature, $T_J$</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421, LM3423</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Input voltage, $V_{IN}$</td>
<td>4.5</td>
<td>75</td>
<td>V</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LM3421 PWP (HTSSOP)</th>
<th>LM3423 PWP (HTSSOP)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUA}$ Junction-to-ambient thermal resistance</td>
<td>38.9</td>
<td>36.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{J(U_{C(top))}}$ Junction-to-case (top) thermal resistance</td>
<td>23.1</td>
<td>21.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JUB}$ Junction-to-board thermal resistance</td>
<td>16.8</td>
<td>18</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>0.6</td>
<td>0.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JUB}$ Junction-to-board characterization parameter</td>
<td>16.6</td>
<td>17.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{J(U_{C(bot))}}$ Junction-to-case (bottom) thermal resistance</td>
<td>1.7</td>
<td>1.9</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 7.5 Electrical Characteristics

$V_{IN} = 14, \ -40^\circ C \leq T_J \leq 125^\circ C$ unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ C$, and are provided for reference purposes only.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>START-UP REGULATOR</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CCREG}$</td>
<td>$V_{CC}$ regulation</td>
<td>$I_{CC} = 0 \ mA$</td>
<td>6.3</td>
<td>7.35</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{CC} = 0 \ mA, T_A = 25^\circ C$</td>
<td></td>
<td>6.9</td>
<td></td>
</tr>
<tr>
<td>$I_{CCLIM}$</td>
<td>$V_{CC}$ current limit</td>
<td>$V_{CC} = 0 \ V$</td>
<td>20</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 0 \ V, T_A = 25^\circ C$</td>
<td></td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent Current</td>
<td>$V_{EN} = 3 \ V, Static$</td>
<td>3</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{EN} = 3 \ V, Static, T_A = 25^\circ C$</td>
<td></td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>$I_{SD}$</td>
<td>Shutdown current</td>
<td>$V_{EN} = 0 \ V$</td>
<td>1</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{EN} = 0 \ V, T_A = 25^\circ C$</td>
<td></td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td><strong>$V_{CC}$ SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV}$</td>
<td>$V_{CC}$ UVLO Threshold</td>
<td>$V_{CC}$ Increasing</td>
<td>4.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC}$ Increasing, $T_A = 25^\circ C$</td>
<td></td>
<td>4.17</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC}$ Decreasing</td>
<td></td>
<td>3.7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC}$ Decreasing, $T_A = 25^\circ C$</td>
<td></td>
<td>4.08</td>
<td></td>
</tr>
<tr>
<td>$V_{CCHYS}$</td>
<td>$V_{CC}$ UVLO Hysteresis</td>
<td>$T_A = 25^\circ C$</td>
<td></td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td><strong>ENABLE THRESHOLDS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$EN_{ST}$</td>
<td>EN start-up threshold</td>
<td>$V_{EN}$ Increasing</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{EN}$ Increasing, $T_A = 25^\circ C$</td>
<td></td>
<td>1.75</td>
<td></td>
</tr>
<tr>
<td>$EN_{ST}$</td>
<td>EN start-up threshold</td>
<td>$V_{EN}$ Decreasing</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{EN}$ Decreasing, $T_A = 25^\circ C$</td>
<td></td>
<td>1.63</td>
<td></td>
</tr>
<tr>
<td>$EN_{STHYS}$</td>
<td>EN start-up hysteresis</td>
<td>$T_A = 25^\circ C$</td>
<td></td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td>$R_{EN}$</td>
<td>EN pulldown resistance</td>
<td>$V_{EN} = 1 \ V$</td>
<td>0.245</td>
<td>2.85</td>
<td>M$\Omega$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{EN} = 1 \ V, T_A = 25^\circ C$</td>
<td></td>
<td>0.82</td>
<td></td>
</tr>
<tr>
<td><strong>CSH THRESHOLDS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CSH high fault</td>
<td>$CSH$ Increasing, $T_A = 25^\circ C$</td>
<td>1.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CSH low condition on LRDY Pin</td>
<td>$CSH$ increasing, $T_A = 25^\circ C$, LM3423</td>
<td>1</td>
<td>V</td>
</tr>
<tr>
<td><strong>OV THRESHOLDS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$OVP_{CB}$</td>
<td>OVP OVLO threshold</td>
<td>OVP Increasing</td>
<td>1.185</td>
<td>1.285</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OVP Increasing, $T_A = 25^\circ C$</td>
<td></td>
<td>1.24</td>
<td></td>
</tr>
<tr>
<td>$OVP_{HYS}$</td>
<td>OVP hysteresis source current</td>
<td>OVP Active (high)</td>
<td>20</td>
<td>25</td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OVP Active (high), $T_A = 25^\circ C$</td>
<td></td>
<td>23</td>
<td></td>
</tr>
</tbody>
</table>
## Electrical Characteristics (continued)

$V_{IN} = 14, -40^\circ C \leq T_J \leq 125^\circ C$ unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ C$, and are provided for reference purposes only.

### DPOL Thresholds

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPOL-THRESH</td>
<td>DPOL logic threshold</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>DPOL Increasing</td>
<td>2</td>
<td>2.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DPOL Increasing, $T_A = 25^\circ C$</td>
<td>2.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{DPOL}$</td>
<td>DPOL pullup resistance</td>
<td>$T_A = 25^\circ C$</td>
<td>1200</td>
<td>500</td>
<td>kΩ</td>
</tr>
</tbody>
</table>

### Fault Timer

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FLTTH}$</td>
<td>Fault threshold</td>
<td>$T_A = 25^\circ C$</td>
<td>1.185</td>
<td>1.24</td>
<td>V</td>
</tr>
<tr>
<td>$I_{FLT}$</td>
<td>FAULT pin source current</td>
<td>$T_A = 25^\circ C$</td>
<td>10</td>
<td>13</td>
<td>µA</td>
</tr>
</tbody>
</table>

### Error Amplifier

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{REF}$</td>
<td>CSH reference voltage</td>
<td>w/r/t to AGND</td>
<td>1.21</td>
<td>1.26</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>w/r/t to AGND, $T_J = 25^\circ C$</td>
<td></td>
<td>1.235</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Error amplifier input bias current</td>
<td>$T_J = 25^\circ C$</td>
<td>−0.6</td>
<td>0</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td>COMP sink or source current</td>
<td>$T_J = 25^\circ C$</td>
<td>22</td>
<td>35</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transconductance</td>
<td>$T_J = 25^\circ C$</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Linear input range</td>
<td>$T_J = 25^\circ C$</td>
<td>±125</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transconductance bandwidth</td>
<td>$T_J = 25^\circ C$</td>
<td>0.5</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

### Off Timer

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OFF(min)}$</td>
<td>Minimum OFF-time</td>
<td></td>
<td></td>
<td>75</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>RCT = 1 V through 1 kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RCT = 1 V through 1 kΩ, $T_J = 25^\circ C$</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{RCT}$</td>
<td>RCT reset pulldown resistance</td>
<td>$T_J = 25^\circ C$</td>
<td>120</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{RST}$</td>
<td>$V_{IN}/25$ reference voltage</td>
<td>$V_{IN} = 14$ V</td>
<td>540</td>
<td>585</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$V_{IN} = 14$ V, $T_J = 25^\circ C$</td>
<td>565</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f$</td>
<td>Continuous conduction switching frequency</td>
<td>$2.2$ nF &gt; $C_T &gt; 470$ pF, $T_J = 25^\circ C$</td>
<td>(See (2))</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### PWM Comparator

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP-to-PWM offset voltage</td>
<td>$T_J = 25^\circ C$</td>
<td>700</td>
<td>900</td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

### Current Limit (IS)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{LIM}$</td>
<td>Current limit threshold</td>
<td>$T_J = 25^\circ C$</td>
<td>215</td>
<td>275</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>Current limit delay-to-output</td>
<td>$T_J = 25^\circ C$</td>
<td>75</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{LEB}$</td>
<td>Leading edge blanking (LEB) time</td>
<td>$T_J = 25^\circ C$</td>
<td>115</td>
<td>325</td>
<td>ns</td>
</tr>
</tbody>
</table>

### High Side Transconductance Amplifier

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_B$</td>
<td>Input bias current</td>
<td>$T_J = 25^\circ C$</td>
<td>11.5</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$g_M$</td>
<td>Transconductance</td>
<td>$T_J = 25^\circ C$</td>
<td>20</td>
<td>119</td>
<td>mA/V</td>
</tr>
</tbody>
</table>

(1) Specified by design. Not production tested.
(2) $f = f_{C_T} R_T$
## Electrical Characteristics (continued)

\( V_{IN} = 14, \ -40^\circ C \leq T_J \leq 125^\circ C \) unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at \( T_J = 25^\circ C \), and are provided for reference purposes only.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input offset current</td>
<td>( T_J = 25^\circ C )</td>
<td>(-1.5)</td>
<td>(0)</td>
<td>(1.5)</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>( T_J = 25^\circ C )</td>
<td>(-7)</td>
<td>(7)</td>
<td>(0)</td>
<td>(mV)</td>
</tr>
<tr>
<td>Transconductance bandwidth</td>
<td>( I_{CSH} = 100 \mu A^{(1)}, T_J = 25^\circ C )</td>
<td>(250)</td>
<td>(500)</td>
<td></td>
<td>(kHz)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GATE DRIVER (GATE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{SRC(GATE)} )</td>
</tr>
<tr>
<td>( R_{SRC(GATE)} )</td>
</tr>
<tr>
<td>( R_{SNK(GATE)} )</td>
</tr>
<tr>
<td>( R_{SNK(GATE)} )</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DIM DRIVER (DIM, DDRV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( nDIMVTH )</td>
</tr>
<tr>
<td>( T_J = 25^\circ C )</td>
</tr>
<tr>
<td>( nDIMHYS )</td>
</tr>
<tr>
<td>( T_J = 25^\circ C )</td>
</tr>
<tr>
<td>( R_{SRC(DDRV)} )</td>
</tr>
<tr>
<td>( DDRV = High, T_J = 25^\circ C )</td>
</tr>
<tr>
<td>( R_{SNK(DDRV)} )</td>
</tr>
<tr>
<td>( DDRV = Low, T_J = 25^\circ C )</td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)

$V_{IN} = 14, -40°C \leq T_J \leq 125°C$ unless otherwise specified. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{RPD}$</td>
<td>RPD pulldown resistance</td>
<td>$T_J = 25°C$</td>
<td>300 $\Omega$</td>
<td>145 $\Omega$</td>
<td></td>
</tr>
<tr>
<td>$R_{FLT}$</td>
<td>FLT pulldown resistance</td>
<td>$T_J = 25°C$</td>
<td>300 $\Omega$</td>
<td>145 $\Omega$</td>
<td></td>
</tr>
<tr>
<td>$R_{LRDY}$</td>
<td>LRDY pulldown resistance</td>
<td>$T_J = 25°C$</td>
<td>300 $\Omega$</td>
<td>135 $\Omega$</td>
<td></td>
</tr>
<tr>
<td>$T_{SD}$</td>
<td>Thermal shutdown threshold(1)</td>
<td>$T_J = 25°C$</td>
<td>165 °C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{HYS}$</td>
<td>Thermal shutdown hysteresis(1)</td>
<td>$T_J = 25°C$</td>
<td>25 °C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
7.6 Typical Characteristics

\( T_A = 25^\circ C, \ V_{\text{IN}} = 14 \ V \) unless otherwise specified

- **Figure 1. Boost Efficiency vs. Input Voltage**
  - \( V_O = 32 \ V \) (9 LEDs)

- **Figure 2. Buck-Boost Efficiency vs. Input Voltage**
  - \( V_O = 21 \ V \) (6 LEDs)

- **Figure 3. Boost LED Current vs. Input Voltage**
  - \( V_O = 32 \ V \) (9 LEDs)

- **Figure 4. Buck-Boost LED Current vs. Input Voltage**
  - \( V_O = 21 \ V \) (6 LEDs)

- **Figure 5. Analog Dimming**
  - \( V_O = 21 \ V \) (6 LEDs), \( V_{\text{IN}} = 24 \ V \)

- **Figure 6. PWM Dimming**
  - \( V_O = 32 \ V \) (9 LEDs), \( V_{\text{IN}} = 24 \ V \)
Typical Characteristics (continued)

\[ T_A = 25^\circ C, \ V_{IN} = 14 \text{ V unless otherwise specified} \]

![Figure 7. \( V_{CSH} \) vs Junction Temperature](image1)

![Figure 8. \( V_{CC} \) vs Junction Temperature](image2)

![Figure 9. \( V_{RCT} \) vs Junction Temperature](image3)

![Figure 10. \( V_{LIM} \) vs Junction Temperature](image4)

![Figure 11. \( t_{ON(min)} \) vs Junction Temperature](image5)
8 Detailed Description

8.1 Overview

The LM3421 and LM3423 are N-channel MOSFET (N-channel FET) controllers for buck, boost and buck-boost current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency.

The devices use a Predictive Off-time (PRO) control architecture that allows the regulator to be operated using minimal external control loop compensation, while providing an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current and the output enable and disable function with external dimming FET driver allows for fast PWM dimming of the LED load. The maximum attainable LED current is not internally limited because the device is a controller. Instead, current is a function of the system operating point, component choices, and switching frequency that allows the device to easily provide constant currents up to 5 A. This controller contains all the features necessary to implement a high-efficiency versatile LED driver.

8.2 Functional Block Diagram

Grey pins are available in the LM3423 only. In the LM3421, TIMR is internally shorted to AGND.
8.3 Feature Description

8.3.1 Current Regulators

Current regulators can create three basic topologies: buck, boost, or buck-boost. All three topologies in their most basic form contain a main switching MOSFET, a recirculating diode, an inductor and capacitors. The controller is designed to drive a ground referenced N-channel FET which is perfect for a standard boost regulator. However, buck and buck-boost regulators usually have a high-side switch. When driving an LED load, a ground referenced load is often not necessary, therefore a ground referenced switch drives a floating load instead. The controller can then be used to drive all three basic topologies as shown in the Basic Topology Schematics section. Other topologies such as the SEPIC and flyback converter (both derivatives of the buck-boost) can be implemented as well.

Looking at the buck-boost design, the basic operation of a current regulator can be analyzed. During the time that the N-channel FET (Q1) is turned on ($t_{ON}$), the input voltage source stores energy in the inductor ($L_1$) while the output capacitor ($C_O$) provides energy to the LED load. When Q1 is turned off ($t_{OFF}$), the re-circulating diode (D1) becomes forward biased and $L_1$ provides energy to both $C_O$ and the LED load. Figure 12 shows the inductor current ($i_L(t)$) waveform for a regulator operating in CCM.

The average output LED current ($I_{LED}$) is proportional to the average inductor current ($i_L$), therefore if $i_L$ is tightly controlled, $I_{LED}$ is well regulated. As the system changes input voltage or output voltage, the ideal duty cycle ($D$) is varied to regulate $i_L$ and ultimately $I_{LED}$. For any current regulator, $D$ is a function of the conversion ratio:

**Buck**

$$D = \frac{V_O}{V_{IN}}$$

**Boost**

$$D = \frac{V_O - V_{IN}}{V_O}$$

**Buck-boost**

$$D = \frac{V_O}{V_O + V_{IN}}$$

8.3.2 Predictive Off-Time (PRO) Control

PRO control is used by the device to control $I_{LED}$. It is a combination of average peak current control and a one-shot off-timer that varies with input voltage. The LM3421 and LM3423 use peak current control to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MOSFET path or the MOSFET $R_{DS-ON}$ for both cycle-by-cycle current limit and input voltage feed forward. $D$ is indirectly controlled by changes in both $t_{OFF}$ and $t_{ON}$, which vary depending on the operating point.
Feature Description (continued)

Even though the off-time control is quasi-hysteretic, the input voltage proportionality in the off-timer creates an essentially constant switching frequency over the entire operating range for boost and buck-boost topologies. The buck topology can be designed to give constant ripple over either input voltage or output voltage, however switching frequency is only constant at a specific operating point.

This type of control minimizes the control loop compensation necessary in many switching regulators, simplifying the design process. The averaging mechanism in the peak detection control loop provides extremely accurate LED current regulation over the entire operating range.

PRO control was designed to mitigate current mode instability (also called sub-harmonic oscillation) found in standard peak current mode control when operating near or above 50% duty cycles. When using standard peak current mode control with a fixed switching frequency, this condition is present, regardless of the topology. However, using a constant off-time approach, current mode instability cannot occur, enabling easier design and control.

Predictive off-time advantages:
• There is no current mode instability at any duty cycle.
• Higher duty cycles or voltage transformation ratios are possible, especially in the boost regulator.

The only disadvantage is that synchronization to an external reference frequency is generally not available.

8.3.3 Average LED Current

The LM3421 and LM3423 use an external current sense resistor ($R_{\text{SNS}}$) placed in series with the LED load to convert the LED current ($I_{\text{LED}}$) into a voltage ($V_{\text{SNS}}$) as shown in Figure 13. The HSP and HSN pins are the inputs to the high-side sense amplifier which are forced to be equal potential ($V_{\text{HSP}}=V_{\text{HSN}}$) through negative feedback. Because of this, the $V_{\text{SNS}}$ voltage is forced across $R_{\text{HSP}}$ to generate the signal current ($I_{\text{CSH}}$) which flows out of the CSH pin and through the $R_{\text{CSH}}$ resistor. The error amplifier regulates the CSH pin to 1.24 V, therefore $I_{\text{CSH}}$ can be calculated using Equation 4.

$$I_{\text{CSH}} = \frac{V_{\text{SNS}}}{R_{\text{HSP}}} \quad (4)$$

This application regulates $V_{\text{SNS}}$ as described in Equation 5.

$$V_{\text{SNS}} = 1.24V \times \frac{R_{\text{HSP}}}{R_{\text{CSH}}} \quad (5)$$

Calculate $I_{\text{LED}}$ using Equation 6.
Feature Description (continued)

\[
I_{\text{LED}} = \frac{V_{\text{SNS}}}{R_{\text{SNS}}} = \frac{1.24V}{R_{\text{SNS}}} \times R_{\text{HSP}} \tag{6}
\]

The selection of the three resistors (R\text{SNS}, R\text{CSH}, and R\text{HSP}) is not arbitrary. For matching and noise performance, the suggested signal current \(I_{\text{CSH}}\) is approximately 100 µA. This current does not flow in the LEDs and does not affect either the off-state LED current or the regulated LED current. \(I_{\text{CSH}}\) can be above or below this value, but the high-side amplifier offset characteristics may be affected slightly. In addition, to minimize the effect of the high-side amplifier voltage offset on LED current accuracy, the minimum \(V_{\text{SNS}}\) is suggested to be 50 mV. Place a resistor (\(R_{\text{HSN}} = R_{\text{HSP}}\)) in series with the HSN pin to cancel out the effects of the input bias current (approximately 10 µA) of both inputs of the high-side sense amplifier.

The sense resistor (\(R_{\text{SNS}}\)) can be placed anywhere in the series string of LEDs as long as the voltage at the HSN and HSP pins (\(V_{\text{HSP}}\) and \(V_{\text{HSN}}\)) satisfies the following conditions:

\[
\begin{align*}
V_{\text{HSP}} &< 76V \\
V_{\text{HSN}} &> 3.5V 
\end{align*} \tag{7}
\]

Typically, for a buck-boost configuration, \(R_{\text{SNS}}\) is placed at the bottom of the string (LED-) which allows for greater flexibility of input and output voltage. However, if there is substantial input voltage ripple allowed, it can help to place \(R_{\text{SNS}}\) at the top of the string (LED+) which limits the output voltage of the string to:

\[
V_O = 76V - V_{\text{IN}} \tag{8}
\]

The CSH pin can also be used as a low-side current sense input regulated to 1.24 V. The high-side sense amplifier is disabled if HSP and HSN are tied to AGND (or \(V_{\text{HSN}} > V_{\text{HSP}}\)).

8.3.4 Analog Dimming

The CSH pin can be used to analog dim the LED current by adjusting the current sense voltage (\(V_{\text{SNS}}\)). There are several different methods to adjust \(V_{\text{SNS}}\) using the CSH pin:

1. External variable resistance: Adjust a potentiometer placed in series with \(R_{\text{CSH}}\) to vary \(V_{\text{SNS}}\).
2. External variable current source: Source current (0 µA to \(I_{\text{CSH}}\)) into the CSH pin to adjust \(V_{\text{SNS}}\).

![Figure 14. Analog Dimming Circuitry](image)

In general, analog dimming applications require a lower switching frequency to minimize the effect of the leading edge blanking circuit. As the LED current is reduced, the output voltage and the duty cycle decreases. Eventually, the minimum on-time is reached. The lower the switching frequency, the wider the linear dimming range. Figure 14 shows how both CSH methods are physically implemented.

Method 1 uses an external potentiometer in the CSH path which is a simple addition to the existing circuitry. However, the LEDs cannot dim completely because there is always some resistance causing signal current to flow. This method is also susceptible to noise coupling at the CSH pin because the potentiometer increases the size of the signal current loop.
Feature Description (continued)

Method 2 provides a complete dimming range and better noise performance, though it is more complex. It consists of a PNP current mirror and a bias network consisting of an NPN, 2 resistors and a potentiometer \((R_{\text{ADJ}})\), where \(R_{\text{ADJ}}\) controls the amount of current sourced into the CSH pin. A higher resistance value sources more current into the CSH pin, causing less regulated signal current through \(R_{\text{HSP}}\), effectively dimming the LEDs. \(V_{\text{REF}}\) should be a precise external voltage reference, while Q7 and Q8 should be a dual pair PNP for best matching and performance. The additional current \((I_{\text{ADD}})\) sourced into the CSH pin can be calculated using Equation 9.

\[
I_{\text{ADD}} = \frac{R_{\text{ADJ}} \times V_{\text{REF}}}{R_{\text{ADJ}} + R_{\text{MAX}}} - V_{\text{BE-Q6}}
\]

\(R_{\text{BIAS}}\)

(9)

The corresponding LED current \((I_{\text{LED}})\) for a specific \(I_{\text{ADD}}\) is:

\[
I_{\text{LED}} = (I_{\text{CSH}} - I_{\text{ADD}}) \times \left(\frac{R_{\text{HSP}}}{R_{\text{SNS}}}\right)
\]

(10)

8.3.5 Current Sense and Current Limit

The LM3421 and LM3423 achieve peak current mode control using a comparator that monitors the main MOSFET (Q1) transistor current, comparing it with the COMP pin voltage as shown in Figure 15. The controller incorporates a cycle-by-cycle overcurrent protection function. A redundant internal current sense comparator provides the current limit functionality. If the voltage at the current sense comparator input (IS pin) exceeds 245 mV (typical), the on cycle is immediately terminated. The IS input pin has an internal N-channel MOSFET which pulls it down at the conclusion of every cycle. The discharge device remains on for an additional 210 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. The leading edge blanking (LEB) determines the minimum achievable on-time \((t_{\text{ON-MIN}})\).

There are two possible methods to sense the transistor current. The \(R_{\text{DS-ON}}\) of the main power MOSFET can be used as the current sense resistance because the IS pin was designed to withstand the high voltages present on the drain when the MOSFET is in the off state. Alternatively, a sense resistor located in the source of the MOSFET may be used for current sensing; however, TI suggests a low inductance (ESL) type. The cycle-by-cycle current limit \((I_{\text{LIM}})\) can be calculated using either method as the limiting resistance \((R_{\text{LIM}})\):

\[
I_{\text{LIM}} = \frac{245 \text{ mV}}{R_{\text{LIM}}}
\]

(11)

![Figure 15. Current Sense / Current Limit Circuitry](image-url)
Feature Description (continued)

8.3.6 Overcurrent Protection

The LM3421 and LM3423 controllers have a secondary method of overcurrent protection. Switching action is disabled whenever the current in the LEDs is more than 30% above the regulation set point. The dimming MOSFET switch driver (DDRV) is not disabled however as this would immediately remove the fault condition and cause oscillatory behavior.

8.3.7 Zero Current Shutdown

The LM3421 and LM3423 controllers implement zero current shutdown through the EN and RPD pins. When pulled low, the EN pin places the devices into near-zero current state, where only the leakage currents occurs at the pins (typical 0.1 µA). The applications circuits frequently have resistor dividers to set UVLO, OVLO, or other similar functions. The RPD pin is an open-drain N-channel MOSFET that is enabled only when the device is enabled. Tying the bottom of all resistor dividers to the RPD pin as shown in Figure 16 allows them to float during shutdown, thus removing their current paths and providing true application-wide zero current shutdown.

![Figure 16. Zero Current Shutdown Circuit](image)

8.3.8 Control Loop Compensation

The control loop is modeled as most typical current mode controllers. Using a first order approximation, the uncompensated loop can be modeled as a single pole created by the output capacitor and, in the boost and buck-boost topologies, a right half plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance. There is also a high-frequency pole in the model; however, it is near the switching frequency and plays no part in the compensation design process. Therefore, it is neglected. Because ceramic capacitance is recommended for use with LED drivers, due to long lifetimes and high ripple current rating, the ESR of the output capacitor can also be neglected in the loop analysis. The DC gain of the uncompensated loop depends on internal controller gains and the external sensing network.

This section describes a buck-boost regulator as an example case.

Use Equation 12 to calculate the uncompensated loop gain for a buck-boost regulator.

\[
T_u = T_{uo} \times \frac{1 - \frac{S}{\omega_{z1}}}{1 + \frac{S}{\omega_{p1}}}
\]

(12)

Where the uncompensated DC loop gain of the system is calculated using Equation 13.

\[
T_{uo} = \frac{D' \times 500V \times R_{CSH} \times R_{OVS} - D' \times 620V}{(1+D) \times R_{HS} \times R_{LM} - (1+D) \times I_{LED} \times R_{LM}}
\]

(13)

And the output pole (\(\omega_{p1}\)) is approximated using Equation 14.

\[
\omega_{p1} = \frac{1+D}{r_D \times C_D}
\]

(14)
Feature Description (continued)

And the right half plane zero ($\omega_{Z1}$) is:

$$\omega_{Z1} = \frac{r_D D^C}{D x L_1}$$

(15)

Figure 17. Uncompensated Loop Gain Frequency Response

Figure 17 shows the uncompensated loop gain in a worst-case scenario when the RHP zero is below the output pole. This occurs at high duty cycles when the regulator is trying to boost the output voltage significantly. The RHP zero adds 20dB/decade of gain while losing 45°/decade of phase, which places the crossover frequency (when the gain is zero dB) extremely high because the gain only starts falling again due to the high-frequency pole (not shown in Figure 17). The phase is below –180° at the crossover frequency, which means there is no phase margin (180° + phase at crossover frequency) causing system instability. Even if the output pole is below the RHP zero, the phase reaches –180° before the crossover frequency in most cases yielding instability.

Figure 18. Compensation Circuitry
Feature Description (continued)

To mitigate this problem, a compensator should be designed to give adequate phase margin (above 45°) at the
crossover frequency. A simple compensator using a single capacitor at the COMP pin (C_CMP) adds a
dominant pole to the system, which ensures adequate phase margin if placed low enough. At high duty cycles (as shown
in Figure 17), the RHP zero places extreme limits on the achievable bandwidth with this type of compensation.
However, because an LED driver is essentially free of output transients (except catastrophic failures open or
short), the dominant pole approach, even with reduced bandwidth, is usually the best approach. The dominant
compensation pole (\(\omega_{P2}\)) is determined by C_CMP and the output resistance (R_O) of the error amplifier (typically 5
M\(\Omega\)) as demonstrated in Equation 16.

\[
\omega_{P2} = \frac{1}{5 \times 10^6 \times C_{CMP}}
\]  

(16)

It may also be necessary to add one final pole at least one decade above the crossover frequency to attenuate
switching noise and, in some cases, provide better gain margin. This pole can be placed across R_SNS to filter the
ESL of the sense resistor at the same time. Figure 18 shows how the compensation is physically implemented in
the system.

The high-frequency pole (\(\omega_{P3}\)) can be calculated using Equation 17.

\[
\omega_{P3} = \frac{1}{R_{FS} \times C_{FS}}
\]  

(17)

The total system transfer function becomes:

\[
T = \frac{1}{T_{UT}} \times \left( \frac{1 - S}{\omega_{P2}} \right) \times \left( \frac{1}{\omega_{P3}} \right) + 1
\]  

(18)

The resulting compensated loop gain frequency response shown in Figure 19 indicates that the system has
adequate phase margin (above 45°) if the dominant compensation pole is placed low enough, ensuring stability.

![Figure 19. Compensated Loop Gain Frequency Response](image)

8.3.9 Start-Up Regulator

The controller includes a high voltage, low dropout bias regulator. When power is applied, the regulator is
enabled and sources current into an external capacitor (C_BYP) connected to the V_CC pin. The recommended
bypass capacitance for the V_CC regulator is 2.2 \(\mu\)F to 3.3 \(\mu\)F. The output of the V_CC regulator is monitored by an
internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the
supply is also internally current limited. Figure 20 shows the typical start-up waveforms.
Feature Description (continued)

First, $C_{BYP}$ is charged to be above $V_{CC}$ UVLO threshold (approximately 4.2 V). The $C_{VCC}$ charging time ($t_{VCC}$) can be estimated using Equation 19.

$$t_{VCC} = \frac{4.2V}{25\text{ mA}} \times C_{BYP} = 168\Omega \times C_{BYP}$$  \hspace{1cm} (19)

$C_{CMP}$ is then charged to 0.9 V over the charging time ($t_{CMP}$), which can be estimated using Equation 20.

$$t_{CMP} = \frac{0.9V}{25\mu A} \times C_{CMP} = 36k\Omega \times C_{CMP}$$  \hspace{1cm} (20)

Once $C_{CMP} = 0.9$ V, the part starts switching to charge $C_O$ until the LED current is in regulation. The $C_O$ charging time ($t_{CO}$) can be roughly estimated using Equation 21.

$$t_{CO} = C_O \times \frac{V_O}{I_{LED}}$$  \hspace{1cm} (21)

The system start-up time ($t_{SU}$) is defined using Equation 22.

$$t_{SU} = t_{VCC} + t_{CMP} + t_{CO}$$  \hspace{1cm} (22)

In some configurations, the start-up waveform overshoots the steady state COMP pin voltage. In this case, the LED current and output voltage overshoots also, which can trip the overvoltage or protection, causing a race condition. The easiest way to prevent this is to use a larger compensation capacitor ($C_{CMP}$), thereby slowing down the control loop.

8.3.10 Overvoltage Lockout (OVLO)

The LM3421 and LM3423 can be configured to detect an output (or input) overvoltage condition through the OVP pin. The pin features a precision 1.24-V threshold with 23 µA (typical) of hysteresis current as shown in Figure 21. When the OVLO threshold is exceeded, the GATE pin is immediately pulled low and a 23-µA current source provides hysteresis to the lower threshold of the OVLO hysteretic band.

If the LEDs are referenced to a potential other than ground (floating), as in the buck-boost and buck configuration, the output voltage ($V_O$) should be sensed and translated to ground by using a single PNP as shown in Figure 22.

The overvoltage turnoff threshold ($V_{TURN-OFF}$) is defined:

**Ground Referenced**

$$V_{TURN-OFF} = 1.24V \times \left( \frac{R_{OVT} + R_{OVS}}{R_{OVT}} \right)$$  \hspace{1cm} (23)

**Floating**

$$V_{TURN-OFF} = 1.24V \times \left( \frac{0.5 \times R_{OVT} + R_{OVS}}{R_{OVT}} \right)$$  \hspace{1cm} (24)
Feature Description (continued)

In the ground referenced configuration, the voltage across $R_{OV2}$ is $V_O - 1.24 \text{ V}$ whereas in the floating configuration it is $V_O - 620 \text{ mV}$ where $620 \text{ mV}$ approximates $V_{BE}$ of the PNP.

The overvoltage hysteresis ($V_{HYSO}$) is defined using Equation 25.

$$V_{HYSO} = 23 \mu A \times R_{OV2}$$

(25)

![Figure 21. Overvoltage Protection Circuitry](image)

The OVLO feature can cause some interesting results if the OVLO trip-point is set too close to $V_O$. At turnon, the converter has a modest amount of voltage overshoot before the control loop gains control of $I_{LED}$. If the overshoot exceeds the OVLO threshold, the controller shuts down, opening the dimming MOSFET. This isolates the LED load from the converter and the output capacitance. The voltage then discharges very slowly through the HSP and HSN pins until $V_O$ drops below the lower threshold, where the process repeats. This looks like the LEDs are blinking at around 2 Hz. This mode can be escaped if the input voltage is reduced.

8.3.11 Input Undervoltage Lockout (UVLO)

The nDIM pin is a dual-function input that features an accurate 1.24-V threshold with programmable hysteresis as shown in Figure 23. This pin functions as both the PWM dimming input for the LEDs and as a $V_{IN}$ UVLO. When the pin voltage rises and exceeds the 1.24-V threshold, 23 $\mu$A (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.
Feature Description (continued)

Figure 23. UVLO Circuit

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra series resistor to set the hysteresis. This allows the standard resistor divider to have smaller resistor values minimizing PWM delays due to a pulldown MOSFET at the nDIM pin (see PWM Dimming section). In general, at least 3 V of hysteresis is preferable when PWM dimming, if operating near the UVLO threshold.

The turnon threshold ($V_{\text{TURN-ON}}$) is defined using Equation 26.

$$V_{\text{TURN-ON}} = 1.24V \times \left( \frac{R_{\text{UV1}} + R_{\text{UV2}}}{R_{\text{UV1}}} \right)$$

(26)

The hysteresis ($V_{\text{HYS}}$) is defined as follows:

- **8.3.11.1 UVLO Only**
  $$V_{\text{HYS}} = 23 \mu A \times R_{\text{UV2}}$$
  (27)

- **8.3.11.2 PWM Dimming and UVLO**
  $$V_{\text{HYS}} = 23 \mu A \times \left( R_{\text{UV2}} + \frac{R_{\text{UV4}} \times (R_{\text{UV1}} + R_{\text{UV2}})}{R_{\text{UV1}}} \right)$$
  (28)

When zero current shutdown and UVLO are implemented together, the EN pin can be used to escape UVLO. The nDIM pin pulls up to $V_{\text{IN}}$ when EN is pulled low. Therefore, if $V_{\text{IN}}$ is within the UVLO hysteretic window when EN is pulled high again, the controller starts-up even though $V_{\text{TURN-ON}}$ is not exceeded.

**8.3.12 PWM Dimming**

The active low nDIM pin can be driven with a PWM signal which controls the main N-channel FET and the dimming FET (dimFET). The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle, (that is, 30% duty cycle equals approximately 30% LED brightness). This function can be ignored if PWM dimming is not required by using nDIM solely as a $V_{\text{IN}}$ UVLO input as described in Input Undervoltage Lockout (UVLO) or by tying it directly to $V_{\text{CC}}$ or $V_{\text{IN}}$. 
Feature Description (continued)

Figure 24. PWM Dimming Circuit

STOPPED DD EDITING HERELM3421 and LM3423

Figure 24 shows how the PWM signal is applied to nDIM:

1. Connect the dimming MOSFET (Q\textsubscript{DIM}) with the drain to the nDIM pin and the source to AGND. Apply an external logic-level PWM signal to the gate of Q\textsubscript{DIM}.

2. Connect the anode of a Schottky diode (D\textsubscript{DIM}) to the nDIM pin. Apply an inverted external logic-level PWM signal to the cathode of the same diode.

The DDRV pin is a PWM output that follows the nDIM PWM input signal. When the nDIM pin rises, the DDRV pin rises and the PWM latch reset signal is removed allowing the main MOSFET Q1 to turn on at the beginning of the next clock set pulse. In boost and buck-boost topologies, the DDRV pin is used to control a N-channel MOSFET placed in series with the LED load, while it would control a P-channel MOSFET in parallel with the load for a buck topology.

The dimFET opens the LED load, when nDIM is low, effectively speeding up the rise and fall times of the LED current. Without any dimFET, the rise and fall times are limited by the inductor slew rate and dimming frequencies above 1 kHz are impractical. Using the series dimFET, dimming frequencies up to 30 kHz are achievable. With a parallel dimFET (buck topology), even higher dimming frequencies are achievable.

When using the PWM functionality in a boost regulator, the PWM signal can drive a ground referenced FET. However, with buck-boost and buck topologies, level shifting circuitry is necessary to translate the PWM dim signal to the floating dimFET as shown in Figure 25 and Figure 26. If high side dimming is necessary in a boost regulator using the LM3423, level shifting can be added providing the polarity inverting DPOL pin is pulled low (see LM3423 Only: DPOL, FLT, TIMR, and LRDY section) as shown in Figure 27.

When using a series dimFET to PWM dim the LED current, more output capacitance is always better. Typical applications use a minimum of 40 µF for PWM dimming. For most applications, a capacitance of 40 µF provides adequate energy storage at the output when the dimFET turns off and opens the LED load. Then when the dimFET is turned back on, the capacitance helps source current into the load, improving the LED current rise time.

A minimum on-time must be maintained in order for PWM dimming to operate in the linear region of its transfer function. Because the controller is disabled during dimming, the PWM pulse must be long enough such that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and buck-boost regulators, the minimum dimming pulse length in seconds (t\textsubscript{PULSE}) is:

$$t_{\text{PULSE}} = \frac{2 \times I_{\text{LED}} \times V_{\text{O}} \times L_{1}}{V_{\text{IN}}^2}$$

(29)

Even maintaining a dimming pulse greater than t\textsubscript{PULSE}, preserving linearity at low dimming duty cycles is difficult.
Feature Description (continued)

The second helpful modification is to remove the \( C_{FS} \) capacitor and \( R_{FS} \) resistor, eliminating the high-frequency compensation pole. Typically, this does not affect stability, but it speeds up the response of the CSH pin, specifically at the rising edge of the LED current when PWM dimming, thus improving the achievable linearity at low dimming duty cycles.
Feature Description (continued)

8.3.13 LM3423 Only: DPOL, FLT, TIMR, and LRDY

The LM3423 has four additional pins: DPOL, FLT, TIMR, and LRDY. The DPOL pin is simply used to invert the DDRV polarity. If DPOL is left open, then it is internally pulled high and the polarity is correct for driving a series N-channel dimFET. If DPOL is pulled low then the polarity is correct for using a series P-channel dimFET in high-side dimming applications. For a parallel P-channel dimFET, as used in the buck topology, leave DPOL open for proper polarity.

The additional TIMR and FLT pins can be used in conjunction with an input disconnect MOSFET switch as shown in Figure 28 to protect the module from various fault conditions.

A fault is detected and an 11.5 µA (typical) current is sourced from the TIMR pin whenever any one of the following conditions exists.

- LED current is above regulation by more than 30%.
- OVLO has engaged.
- Thermal shutdown has engaged.

An external capacitor ($C_{\text{TMR}}$) from TIMR to AGND programs the fault filter time as follows:

$$C_{\text{TMR}} = \frac{t_{\text{FLT}} \times 11.5 \mu\text{A}}{1.24\text{V}}$$

When the voltage on the TIMR pin reaches 1.24 V, the device is latched off and the N-channel MOSFET open-drain FLT pin transitions to a high impedance state. The controller immediately pulls the TIMR pin to ground (resets) if the fault condition is removed at any point during the filter period. Otherwise, if the timer expires, the fault remains latched until one of these situations occurs:

- The EN pin is pulled low long enough for the $V_{\text{CC}}$ pin to drop below 4.1 V (approximately 200 ms) or
- the TIMR pin is pulled to ground or
- a complete power cycle occurs

When using the EN and OVP pins in conjunction with the RPD pulldown pin, a race condition exists when exiting the disabled (EN low) state. When disabled, controller pulls up the OVP pin to the output voltage because the RPD pulldown is disabled, and this appears as if it is a real OVLO condition. The timer pin immediately rises and latches the controller to the fault state. To protect against this behavior, a minimum timer capacitor ($C_{\text{TMR}} = 220 \mu\text{F}$) should be used. If fault latching is not required, short the TMR pin to AGND, which disables the FLT flag function.

The LM3423 also includes an LED Ready (LRDY) flag to notify the system that the LEDs are in proper regulation. The N-channel MOSFET open-drain LRDY pin is pulled low whenever any of the following conditions are met:

1. $V_{\text{CC}}$ UVLO has engaged.
2. LED current is below regulation by more than 20%.
3. LED current is above regulation by more than 30%.
4. Overvoltage protection has engaged
5. Thermal shutdown has engaged.
6. A fault has latched the device off.

The LRDY pin is pulled low during start-up of the device and remains low until the LED current is in regulation.
Feature Description (continued)

Figure 28. Fault Detection and LED Status Circuit

High = LED in regulation
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Inductor

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transferred to the load in different ways (as an example, buck-boost operation is detailed in the Current Regulators section). The size of the inductor, the voltage across it, and the length of the switching subinterval \( t_{\text{ON}} \) or \( t_{\text{OFF}} \) determines the inductor current ripple \( \Delta i_{\text{L-PP}} \). In the design process, L1 is chosen to provide a desired \( \Delta i_{\text{L-PP}} \). For a buck regulator the inductor has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore \( \Delta i_{\text{L-PP}} \) is basically equal to the LED ripple current \( \Delta i_{\text{LED-PP}} \). However, for boost and buck-boost regulators, there is always an output capacitor which reduces \( \Delta i_{\text{LED-PP}} \); therefore, the inductor ripple can be larger than in the buck regulator case where output capacitance is minimal or completely absent.

In general, \( \Delta i_{\text{LED-PP}} \) is recommended by manufacturers to be less than 40% of the average LED current \( i_{\text{LED}} \). Therefore, for the buck regulator with no output capacitance, \( \Delta i_{\text{L-PP}} \) should also be less than 40% of \( i_{\text{LED}} \). For the boost and buck-boost topologies, \( \Delta i_{\text{L-PP}} \) can be much higher depending on the output capacitance value. However, \( \Delta i_{\text{L-PP}} \) is suggested to be less than 100% of the average inductor current \( i_{\text{L}} \) to limit the RMS inductor current.

L1 is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current \( i_{\text{L-RMS}} \).

9.1.2 LED Dynamic Resistance

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus \( R_{\text{SNS}} \). LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED \( V_{\text{LED}} \) by the forward current \( i_{\text{LED}} \) leads to an incorrect calculation of the dynamic resistance of a single LED \( r_{\text{LED}} \). The result can be 5 to 10 times higher than the true \( r_{\text{LED}} \) value.

![Figure 29. Dynamic Resistance](image)

Obtaining \( r_{\text{LED}} \) is accomplished by referring to the manufacturer’s LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 29. For any application with more than 2 series LEDs, \( R_{\text{SNS}} \) can be neglected allowing \( r_{\text{D}} \) to be approximated as the number of LEDs multiplied by \( r_{\text{LED}} \).
Application Information (continued)

9.1.3 Output Capacitor

For boost and buck-boost regulators, the output capacitor (C\text{O}) provides energy to the load when the recirculating diode (D1) is reverse biased during the first switching subinterval. An output capacitor in a buck topology simply reduces the LED current ripple (\Delta i_{\text{LED,PP}}) below the inductor current ripple (\Delta i_{\text{L,PP}}). In all cases, C\text{O} is sized to provide a desired \Delta i_{\text{LED,PP}}. As mentioned in the Inductor section, \Delta i_{\text{LED,PP}} is recommended by manufacturers to be less than 40% of the average LED current (I_{\text{LED}}).

C\text{O} should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

9.1.4 Input Capacitors

The input capacitance (C\text{IN}) provides energy during the discontinuous portions of the switching period. For buck and buck-boost regulators, C\text{IN} provides energy during t\text{ON} and during t\text{OFF}, the input voltage source charges up C\text{IN} with the average input current (I_{\text{IN}}). For boost regulators, C\text{IN} only needs to provide the ripple current due to the direct connection to the inductor. C\text{IN} is selected given the maximum input voltage ripple (\Delta v_{\text{IN,PP}}) which can be tolerated. \Delta v_{\text{IN,PP}} is suggested to be less than 10% of the input voltage (V_{\text{IN}}).

An input capacitance at least 100% greater than the calculated C\text{IN} value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transition of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

For most applications, TI recommends bypassing the V\text{IN} pin with an 0.1 \mu F ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the controller, a 10-\Omega series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150-kHz filter to eliminate undesired high-frequency noise.

9.1.5 Main MOSFET / Dimming MOSFET

The controller requires an external N-channel FET (Q1) as the main power MOSFET for the switching regulator. TI recommends Q1 have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. TI recommends the current rating be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the RMS transistor current and the N-channel FET on-resistance (R_{\text{DS-ON}}).

When PWM dimming, the controller requires another MOSFET (Q2) placed in series (or parallel for a buck regulator) with the LED load. This MOSFET should have a voltage rating greater than the output voltage (V_{\text{O}}) and a current rating at least 10% higher than the nominal LED current (I_{\text{LED}}). The power rating is simply R_{\text{DS-ON}} multiplied by I_{\text{LED}} assuming 100% dimming duty cycle (continuous operation) occurs.

For most applications, choose an N-channel FET that minimizes total gate charge (Q_g) when f_{\text{SW}} is high. It that is not possible, minimize the on-resistance R_{\text{DS(on)}} to minimize the dominant power losses in the system. Frequently, higher current N-channel FETs in larger packages yield better thermal performance.

9.1.6 Re-Circulating Diode

The controller requires a recirculating diode (D1) to carry the inductor current during the off time (t\text{OFF}). The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, TI recommends D1 have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product data sheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.
Application Information (continued)

9.1.7 Boost Inrush Current

When configured as a boost converter, there is a phantom power path comprised of the inductor, the output diode, and the output capacitor. This path causes two things to happen when power is applied:

1. a very large inrush of current to charge the output capacitor
2. the energy stored in the inductor during this inrush collects in the output capacitor, charging it to a higher potential than the input voltage

Depending on the state of the EN pin, the output capacitor discharges by:

1. EN < 1.3 V: no discharge path (leakage only).
2. EN > 1.3 V, the OVP divider resistor path, if present, and 10 µA into each of the HSP & HSN pins.

In applications using the OVP divider and with EN > 1.3 V, the output capacitor voltage can charge higher than V\text{TURN-OFF}. In this situation, the FLT pin (LM3423 only) is open and the PWM dimming MOSFET is turned off. This condition (the system appearing disabled) can persist for an undesirably long time. Possible solutions to this condition include:

- Add an inrush diode from V\text{IN} to the output as shown in Figure 30.
- Add an NTC thermistor in series with the input to prevent the inrush from overcharging the output capacitor too high.
- Use a current limited source supply.
- Raise the OVP threshold.

![Figure 30. Boost Topology with Inrush Diode](image)

9.1.8 Switching Frequency

An external resistor (R\text{T}) connected between the RCT pin and the switch node (where D1, Q1, and L1 connect), in combination with a capacitor (C\text{T}) between the RCT and AGND pins, sets the off-time (t\text{OFF}) as shown in Figure 31. For boost and buck-boost topologies, the V\text{IN} proportionality ensures a virtually constant switching frequency (f\text{SW}).

For a buck topology, R\text{T} and C\text{T} are also used to set t\text{OFF}, however the input voltage (V\text{IN}) proportionality does not ensure a constant switching frequency. Instead, constant ripple operation can be achieved. Changing the connection of R\text{T} in Figure 31 from V\text{SW} to V\text{IN} provides a constant ripple over varying V\text{IN}. Adding a PNP transistor as shown in Figure 32 provides constant ripple over varying V\text{O}.

The switching frequency is defined:

**Buck (Constant Ripple vs. V\text{IN})**

\[
f_{SW} = \frac{25 \times (V_{IN} - V_O)}{R_T \times C_T \times V_{IN}}
\]

(31)

**Buck (Constant Ripple vs. V\text{O})**

\[
f_{SW} = \frac{25 \times (V_{IN} \times V_O - V_O^2)}{R_T \times C_T \times V_{IN}^2}
\]

(32)

**Boost and Buck-boost**
Application Information (continued)

\[
 f_{SW} = \frac{25}{R_T \times C_T}
\]  

(33)

For all topologies, the \( C_T \) capacitor is recommended to be 1 nF and should be located very close to the LM34xx-Q1.

![Figure 31. Off-timer Circuitry for Boost and Buck-boost Regulators](image)

![Figure 32. Off-timer Circuitry for Buck Regulators](image)
9.2 Typical Applications

9.2.1 Basic Topology Schematics

Figure 33. Boost Regulator ($V_{IN} < V_O$)
Typical Applications (continued)

Figure 34. Buck Regulator ($V_{\text{IN}} > V_{\text{O}}$)
Typical Applications (continued)

Figure 35. Buck-Boost Regulator
Typical Applications (continued)

9.2.1.1 Design Requirements

Number of series LEDs: \( N \)

Single LED forward voltage: \( V_{\text{LED}} \)

Single LED dynamic resistance: \( r_{\text{LED}} \)

Nominal input voltage: \( V_{\text{IN}} \)

Input voltage range: \( V_{\text{IN-MAX}}, V_{\text{IN-MIN}} \)

Switching frequency: \( f_{\text{SW}} \)

Current sense voltage: \( V_{\text{SNS}} \)

Average LED current: \( I_{\text{LED}} \)

Inductor current ripple: \( \Delta i_{\text{L-PP}} \)

LED current ripple: \( \Delta i_{\text{LED-PP}} \)

Peak current limit: \( I_{\text{LIM}} \)

Input voltage ripple: \( \Delta V_{\text{IN-PP}} \)

Output OVLO characteristics: \( V_{\text{TURN-OFF}}, V_{\text{HYSO}} \)

Input UVLO characteristics: \( V_{\text{TURN-ON}}, V_{\text{HYS}} \)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Operating Point

Given the number of series LEDs (\( N \)), the forward voltage (\( V_{\text{LED}} \)) and dynamic resistance (\( r_{\text{LED}} \)) for a single LED, solve for the nominal output voltage (\( V_f \)) and the nominal LED string dynamic resistance (\( r_D \)):

\[
V_f = N \times V_{\text{LED}}
\]

\[
r_D = N \times r_{\text{LED}}
\]

Solve for the ideal nominal duty cycle (\( D \)):

Buck:

\[
D = \frac{V_f}{V_{\text{IN}}}
\]

Boost:

\[
D = \frac{V_f - V_{\text{IN}}}{V_f}
\]

Buck-Boost:

\[
D = \frac{V_f}{V_f + V_{\text{IN}}}
\]

Using the same equations, find the minimum duty cycle (\( D_{\text{MIN}} \)) using maximum input voltage (\( V_{\text{IN-MAX}} \)) and the maximum duty cycle (\( D_{\text{MAX}} \)) using the minimum input voltage (\( V_{\text{IN-MIN}} \)). Also, remember that \( D' = 1 - D \).

9.2.1.2.2 Switching Frequency

Set the switching frequency (\( f_{\text{SW}} \)) by assuming a \( C_T \) value of 1 nF and solving for \( R_T \):

Buck (Constant Ripple vs. \( V_{\text{IN}} \))
Typical Applications (continued)

\[ R_T = \frac{25 \times (V_{IN} - V_O)}{f_{SW} \times C_T \times V_{IN}} \]  \hspace{1cm} (39)

\[ \text{Buck (Constant Ripple vs. } V_O) \]
\[ R_T = \frac{25 \times (V_{IN} \times V_O - V_O^2)}{f_{SW} \times C_T \times V_{IN}^2} \]  \hspace{1cm} (40)

\[ \text{Boost and Buck-Boost} \]
\[ R_T = \frac{25}{f_{SW} \times C_T} \]  \hspace{1cm} (41)

9.2.1.2.3 Average LED Current

For all topologies, set the average LED current (I_{LED}) knowing the desired current sense voltage (V_{SNS}) and solving for R_{SNS}:
\[ R_{SNS} = \frac{V_{SNS}}{I_{LED}} \]  \hspace{1cm} (42)

If the calculated R_{SNS} is too far from a desired standard value, then V_{SNS} requires adjustment to obtain a standard value.

Setup the suggested signal current of 100 µA by assuming R_{CSH} = 12.4 kΩ and solving for R_{HSP}:
\[ R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24V} \]  \hspace{1cm} (43)

If the calculated R_{HSP} is too far from a desired standard value, then R_{CSH} can be adjusted to obtain a standard value.

9.2.1.2.4 Inductor Ripple Current

Set the nominal inductor ripple current (\Delta i_{L-PP}) by solving for the appropriate inductor (L1):

\[ L1 = \frac{(V_{IN} - V_O) \times D}{\Delta i_{L-PP} \times f_{SW}} \]  \hspace{1cm} (44)

\[ \text{Boost and Buck-Boost} \]
\[ L1 = \frac{V_{IN} \times D}{\Delta i_{L-PP} \times f_{SW}} \]  \hspace{1cm} (45)

To set the worst case inductor ripple current, use V_{IN-MAX} and D_{MIN} when solving for L1.

The minimum allowable inductor RMS current rating (I_{L-RMS}) can be calculated as:

\[ I_{L-RMS} = I_{LED} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta i_{L-PP}}{I_{LED}}\right)^2} \]  \hspace{1cm} (46)

\[ \text{Boost and Buck-Boost} \]
\[ I_{L-RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta i_{L-PP} \times D'}{I_{LED}}\right)^2} \]  \hspace{1cm} (47)
Typical Applications (continued)

9.2.1.2.5 LED Ripple Current

Set the nominal LED ripple current ($\Delta_i_{LED-PP}$), by solving for the output capacitance ($C_O$):

**Buck**

$$C_O = \frac{\Delta i_{LED-PP}}{8 \times f_{SW} \times f_D \times \Delta i_{LED-PP}}$$  \hspace{1cm} (48)

**Boost and Buck-boost**

$$C_O = \frac{i_{LED} \times D}{f_D \times \Delta i_{LED-PP} \times f_{SW}}$$  \hspace{1cm} (49)

To set the worst case LED ripple current, use $D_{MAX}$ when solving for $C_O$. Remember, when PWM dimming, TI recommends using a minimum of 40 µF of output capacitance to improve performance.

The minimum allowable RMS output capacitor current rating ($I_{CO-RMS}$) can be approximated:

**Buck**

$$I_{CO-RMS} = \frac{\Delta i_{LED-PP}}{\sqrt{12}}$$  \hspace{1cm} (50)

**Boost and Buck-boost**

$$I_{CO-RMS} = i_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$  \hspace{1cm} (51)

9.2.1.2.6 Peak Current Limit

Set the peak current limit ($I_{LIM}$) by solving for the transistor path sense resistor ($R_{LIM}$):

$$R_{LIM} = \frac{245 \text{ mV}}{I_{LIM}}$$  \hspace{1cm} (52)

9.2.1.2.7 Loop Compensation

Using a simple first order peak current mode control model, neglecting any output capacitor ESR dynamics, the necessary loop compensation can be determined.

First, the uncompensated loop gain ($T_U$) of the regulator can be approximated:

**Buck**

$$T_U = T_{U0} \times \frac{1}{1 + \frac{S}{\omega_{p1}}}$$  \hspace{1cm} (53)

**Boost and Buck-Boost**

$$T_U = T_{U0} \times \frac{1 - \frac{S}{\omega_{z1}}}{1 + \frac{S}{\omega_{p1}}}$$  \hspace{1cm} (54)

Where the pole ($\omega_{p1}$) is approximated:

**Buck**

$$\omega_{p1} = \frac{1}{r_D \times C_O}$$  \hspace{1cm} (55)
Typical Applications (continued)

Boost

\[ \omega_{p1} = \frac{2}{r_D \times C_O} \]  \hspace{1cm} (56)

Buck-Boost

\[ \omega_{p1} = \frac{1+D}{r_D \times C_O} \]  \hspace{1cm} (57)

And the RHP zero (\( \omega_{z1} \)) is approximated:

Boost

\[ \omega_{z1} = \frac{r_D \times D^2}{L1} \]  \hspace{1cm} (58)

Buck-Boost

\[ \omega_{z1} = \frac{r_D \times D^2}{D \times L1} \]  \hspace{1cm} (59)

And the uncompensated DC loop gain (\( T_{U0} \)) is approximated:

Buck

\[ T_{U0} = \frac{500V \times R_{CSH} \times R_{SNS}}{R_{HSP} \times R_{LIM}} = \frac{620V}{I_{LED} \times R_{LIM}} \]  \hspace{1cm} (60)

Boost

\[ T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{2 \times R_{HSP} \times R_{LIM}} = \frac{D' \times 310V}{I_{LED} \times R_{LIM}} \]  \hspace{1cm} (61)

Buck-Boost

\[ T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \]  \hspace{1cm} (62)

For all topologies, the primary method of compensation is to place a low frequency dominant pole (\( \omega_{p2} \)), which ensures that there is ample phase margin at the crossover frequency. This is accomplished by placing a capacitor (\( C_{CMP} \)) from the COMP pin to AGND, which is calculated according to the lower value of the pole and the RHP zero of the system (shown as a minimizing function):

\[ \omega_{p2} = \min(\omega_{p1}, \omega_{z1}) \times 5 \times T_{U0} \]  \hspace{1cm} (63)

\[ C_{CMP} = \frac{1}{\omega_{p2} \times 5 \times 10^6} \]  \hspace{1cm} (64)

If analog dimming is used, \( C_{CMP} \) should be approximately 4\( \times \) larger to maintain stability as the LEDs are dimmed to zero.

A high-frequency compensation pole (\( \omega_{p3} \)) can be used to attenuate switching noise and provide better gain margin. Assuming \( R_{FS} = 10 \Omega \), \( C_{FS} \) is calculated according to the higher value of the pole and the RHP zero of the system (shown as a maximizing function):

\[ \omega_{p3} = \max(\omega_{p1}, \omega_{z1}) \times 10 \]  \hspace{1cm} (65)

\[ C_{FS} = \frac{1}{10 \times \omega_{p3}} \]  \hspace{1cm} (66)

The total system loop gain (\( T \)) can then be written as:
Typical Applications (continued)

Buck

\[ T = T_{U0} x \frac{1}{\left(1 + \frac{s}{\omega_{p1}}\right) x \left(1 + \frac{s}{\omega_{p2}}\right) x \left(1 + \frac{s}{\omega_{p3}}\right)} \]  \hspace{1cm} (67)

Boost and Buck-Boost

\[ T = T_{U0} x \frac{1 - \frac{s}{\omega_{Z1}}}{\left(1 + \frac{s}{\omega_{p1}}\right) x \left(1 + \frac{s}{\omega_{p2}}\right) x \left(1 + \frac{s}{\omega_{p3}}\right)} \]  \hspace{1cm} (68)

9.2.1.2.8 Input Capacitance

Set the nominal input voltage ripple (\( \Delta V_{IN-PP} \)) by solving for the required capacitance (\( C_{IN} \)):

Buck

\[ C_{IN} = \frac{I_{LED} x (1 - D) x D}{\Delta V_{IN-PP} x f_{SW}} \]  \hspace{1cm} (69)

Boost

\[ C_{IN} = \frac{\Delta i_{L-PP}}{8 x \Delta V_{IN-PP} x f_{SW}} \]  \hspace{1cm} (70)

Buck-Boost

\[ C_{IN} = \frac{I_{LED} x D}{\Delta V_{IN-PP} x f_{SW}} \]  \hspace{1cm} (71)

Use \( D_{MAX} \) to set the worst case input voltage ripple, when solving for \( C_{IN} \) in a buck-boost regulator and \( D_{MID} = 0.5 \) when solving for \( C_{IN} \) in a buck regulator.

The minimum allowable RMS input current rating (\( I_{CIN-RMS} \)) can be approximated:

Buck

\[ I_{CIN-RMS} = I_{LED} x \sqrt{D_{MID} x (1 - D_{MID})} \]  \hspace{1cm} (72)

Boost

\[ I_{CIN-RMS} = \frac{\Delta i_{L-PP}}{\sqrt{12}} \]  \hspace{1cm} (73)

Buck-Boost

\[ I_{CIN-RMS} = I_{LED} x \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \]  \hspace{1cm} (74)

9.2.1.2.9 N-channel FET

The N-channel FET voltage rating should be at least 15% higher than the maximum N-channel FET drain-to-source voltage (\( V_{T-MAX} \)):

Buck

\[ V_{T-MAX} = V_{IN-MAX} \]  \hspace{1cm} (75)

Boost
Typical Applications (continued)

\[ V_{T-\text{MAX}} = V_O \]  \hspace{1cm} (76)

Buck-Boost

\[ V_{T-\text{MAX}} = V_{\text{IN-MAX}} + V_O \]  \hspace{1cm} (77)

The current rating should be at least 10% higher than the maximum average N-channel FET current (\(I_{T-MAX}\)):

Buck

\[ I_{T-MAX} = D_{MAX} \times I_{LED} \]  \hspace{1cm} (78)

Boost and Buck-Boost

\[ I_{T-MAX} = \frac{D_{MAX}}{1 - D_{MAX}} \times I_{LEC} \]  \hspace{1cm} (79)

Approximate the nominal RMS transistor current (\(I_{T-RMS}\)):

Buck

\[ I_{T-RMS} = I_{LED} \times \sqrt{D} \]  \hspace{1cm} (80)

9.2.1.2.9.1 Boost and Buck-Boost

\[ I_{T-RMS} = \frac{I_{LED}}{D} \times \sqrt{D} \]  \hspace{1cm} (81)

Given an N-channel FET with on-resistance (\(R_{DS-ON}\)), solve for the nominal power dissipation (\(P_T\)):

\[ P_T = I_{T-RMS}^2 \times R_{DS-ON} \]  \hspace{1cm} (82)

9.2.1.2.10 Diode

The Schottky diode voltage rating should be at least 15% higher than the maximum blocking voltage (\(V_{RD-MAX}\)):

Buck

\[ V_{RD-MAX} = V_{IN-MAX} \]  \hspace{1cm} (83)

Boost

\[ V_{RD-MAX} = V_O \]  \hspace{1cm} (84)

Buck-Boost

\[ V_{RD-MAX} = V_{IN-MAX} + V_O \]  \hspace{1cm} (85)

The current rating should be at least 10% higher than the maximum average diode current (\(I_{D-MAX}\)):

Buck

\[ I_{D-MAX} = (1 - D_{MIN}) \times I_{LED} \]  \hspace{1cm} (86)

Boost and Buck-Boost

\[ I_{D-MAX} = I_{LED} \]  \hspace{1cm} (87)

Replace \(D_{MAX}\) with \(D\) in the \(I_{D-MAX}\) equation to solve for the average diode current (\(I_D\)). Given a diode with forward voltage (\(V_{FD}\)), solve for the nominal power dissipation (\(P_D\)):

\[ P_D = I_D \times V_{FD} \]  \hspace{1cm} (88)
Typical Applications (continued)

9.2.1.2.11 Output OVLO

For boost and buck-boost regulators, output OVLO is programmed with the turn-off threshold voltage ($V_{\text{TURN-OFF}}$) and the desired hysteresis ($V_{\text{HYSO}}$). To set $V_{\text{HYSO}}$, solve for $R_{\text{OV2}}$:

$$R_{\text{OV2}} = \frac{V_{\text{HYSO}}}{23 \mu A}$$

(89)

To set $V_{\text{TURN-OFF}}$, solve for $R_{\text{OV1}}$:

Boost

$$R_{\text{OV1}} = \frac{1.24V \times R_{\text{OV2}}}{V_{\text{TURN-OFF}} - 1.24V}$$

(90)

Buck-Boost

$$R_{\text{OV1}} = \frac{1.24V \times R_{\text{OV2}}}{V_{\text{TURN-OFF}} - 620 \text{ mV}}$$

(91)

A small filter capacitor ($C_{\text{OVP}} = 47 \text{ pF}$) should be added from the OVP pin to ground to reduce coupled switching noise.

9.2.1.2.12 Input UVLO

For all topologies, input UVLO is programmed with the turn-on threshold voltage ($V_{\text{TURN-ON}}$) and the desired hysteresis ($V_{\text{HYS}}$).

**Method 1:** If no PWM dimming is required, a two resistor network can be used. To set $V_{\text{HYS}}$, solve for $R_{\text{UV2}}$:

$$R_{\text{UV2}} = \frac{V_{\text{HYS}}}{23 \mu A}$$

(92)

To set $V_{\text{TURN-ON}}$, solve for $R_{\text{UV1}}$:

$$R_{\text{UV1}} = \frac{1.24V \times R_{\text{UV2}}}{V_{\text{TURN-ON}} - 1.24V}$$

(93)

**Method 2:** If PWM dimming is required, a three resistor network is suggested. To set $V_{\text{TURN-ON}}$, assume $R_{\text{UV2}} = 10 \text{ k\Omega}$ and solve for $R_{\text{UV1}}$ as in Method 1. To set $V_{\text{HYS}}$, solve for $R_{\text{UVH}}$:

$$R_{\text{UVH}} = \frac{R_{\text{UV1}} \times (V_{\text{HYS}} - 23 \mu A \times R_{\text{UV2}})}{23 \mu A \times (R_{\text{UV1}} + R_{\text{UV2}})}$$

(94)

9.2.1.2.13 PWM Dimming Method

PWM dimming can be performed several ways:

**Method 1:** Connect the dimming MOSFET ($Q_3$) with the drain to the nDIM pin and the source to AGND. Apply an external PWM signal to the gate of $Q_{\text{DIM}}$. A pulldown resistor may be necessary to properly turn off $Q_3$.

**Method 2:** Connect the anode of a Schottky diode to the nDIM pin. Apply an external inverted PWM signal to the cathode of the same diode.

The DDRV pin should be connected to the gate of the dimFET with or without level-shifting circuitry as described in the **PWM Dimming** section. The dimFET should be rated to handle the average LED current and the nominal output voltage.

9.2.1.2.14 Analog Dimming Method

Analog dimming can be performed several ways:

**Method 1:** Place a potentiometer in series with the $R_{\text{CSH}}$ resistor to dim the LED current from the nominal $I_{\text{LED}}$ to near zero.
Typical Applications (continued)

Method 2: Connect a controlled current source as detailed in the Analog Dimming section to the CSH pin. Increasing the current sourced into the CSH node decreases the LEDs from the nominal $I_{LED}$ to zero current in the same manner as the thermal foldback circuit.
Typical Applications (continued)

9.2.2 LM3421 Buck-Boost Application

Figure 36. LM3421 Buck-Boost Application

9.2.2.1 Design Requirements

\[ N = 6 \]
\[ V_{\text{LED}} = 3.5 \text{ V} \]
\[ r_{\text{LED}} = 325 \text{ m} \Omega \]
\[ V_{\text{IN}} = 24 \text{ V} \]
\[ V_{\text{IN-MIN}} = 10 \text{ V} \]
\[ V_{\text{IN-MAX}} = 70 \text{ V} \]
\[ f_{\text{SW}} = 500 \text{ kHz} \]
\[ V_{\text{SNS}} = 100 \text{ mV} \]
\[ I_{\text{LED}} = 1 \text{ A} \]
\[ \Delta I_{\text{L-PP}} = 700 \text{ mA} \]
\[ \Delta I_{\text{LED-PP}} = 12 \text{ mA} \]
\[ \Delta V_{\text{IN-PP}} = 100 \text{ mV} \]
Typical Applications (continued)

\( I_{\text{Lim}} = 6 \, \text{A} \)
\( V_{\text{TURN-ON}} = 10 \, \text{V} \)
\( V_{\text{HYS}} = 3 \, \text{V} \)
\( V_{\text{TURN-OFF}} = 40 \, \text{V} \)
\( V_{\text{HYSO}} = 10 \, \text{V} \)

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Operating Point

Solve for \( V_O \) and \( r_D \):

\[
V_O = N x V_{\text{LED}} = 6 \times 3.5V = 21V
\]

\[
r_D = N x r_{\text{LED}} = 6 \times 325 \, \text{m}\Omega = 1.95\Omega
\]

Solve for \( D \), \( D' \), \( D_{\text{MAX}} \), and \( D_{\text{MIN}} \):

\[
D = \frac{V_O}{V_O + V_{\text{IN}}} = \frac{21V}{21V + 24V} = 0.467
\]

\[
D' = 1 - D = 1 - 0.467 = 0.533
\]

\[
D_{\text{MIN}} = \frac{V_O}{V_O + V_{\text{IN-MAX}}} = \frac{21V}{21V + 70V} = 0.231
\]

\[
D_{\text{MAX}} = \frac{V_O}{V_O + V_{\text{IN-MIN}}} = \frac{21V}{21V + 10V} = 0.677
\]

9.2.2.2 Switching Frequency

Assume \( C_T = 1 \, \text{nF} \) and solve for \( R_T \):

\[
R_T = \frac{f_{\text{SW}} \times C_T}{25} = \frac{25}{500 \, \text{kHz} \times 1 \, \text{nF}} = 50 \, \text{k}\Omega
\]

The closest standard resistor is 49.9 k\Ω; therefore, \( f_{\text{SW}} \) is:

\[
f_{\text{SW}} = \frac{25}{R_T \times C_T} = \frac{25}{49.9 \, \text{k}\Omega \times 1 \, \text{nF}} = 501 \, \text{kHz}
\]

The chosen component from step 2 is:

\( C_T = 1 \, \text{nF} \)

\( R_T = 49.9 \, \text{k}\Omega \)

9.2.2.3 Average LED Current

Solve for \( R_{\text{SNS}} \):

\[
R_{\text{SNS}} = \frac{V_{\text{SNS}}}{I_{\text{LED}}} = \frac{100 \, \text{mV}}{1A} = 0.1\Omega
\]

Assume \( R_{\text{CSH}} = 12.4 \, \text{k}\Omega \) and solve for \( R_{\text{HSP}} \):

\[
R_{\text{HSP}} = \frac{I_{\text{LED}} \times R_{\text{CSH}} \times R_{\text{SNS}}}{1.24V} = \frac{1A \times 12.4 \, \text{k}\Omega \times 0.1\Omega}{1.24V} = 1.0 \, \text{k}\Omega
\]
Typical Applications (continued)

The closest standard resistor for $R_{\text{SNS}}$ is actually 0.1 $\Omega$ and for $R_{\text{HSP}}$ is actually 1 k$\Omega$; therefore, $I_{\text{LED}}$ is:

$$I_{\text{LED}} = \frac{1.24V \times R_{\text{HSP}}}{R_{\text{SNS}} \times R_{\text{CSH}}} = \frac{1.24V \times 1.0 \text{ k}\Omega}{0.1\Omega \times 12.4 \text{ k}\Omega} = 1.0\text{A}$$

(106)

The chosen components from step 3 are:

$$R_{\text{SNS}} = 0.1\Omega$$
$$R_{\text{CSH}} = 12.4 \text{ k}\Omega$$
$$R_{\text{HSP}} = R_{\text{HSN}} = 1\text{k}\Omega$$

(107)

9.2.2.2.4 Inductor Ripple Current

Solve for $L_1$:

$$L_1 = \frac{V_{\text{IN}} \times D}{\Delta I_{\text{L-PP}} \times f_{\text{SW}}} = \frac{24V \times 0.467}{700 \text{ mA} \times 501 \text{ kHz}} = 32 \mu\text{H}$$

(108)

The closest standard inductor is 33 $\mu\text{H}$; therefore, $\Delta I_{\text{L-PP}}$ is:

$$\Delta I_{\text{L-PP}} = \frac{V_{\text{IN}} \times D}{L_1 \times f_{\text{SW}}} = \frac{24V \times 0.467}{33 \mu\text{H} \times 501 \text{ kHz}} = 678 \text{ mA}$$

(109)

Determine minimum allowable RMS current rating:

$$I_{\text{L-RMS}} = \frac{I_{\text{LED}} \times D}{\sqrt{1 + \frac{1}{12} \times \left(\frac{\Delta I_{\text{L-PP}} \times D}{I_{\text{LED}}}\right)^2}}$$

$$I_{\text{L-RMS}} = \frac{1\text{A}}{0.533} \times \sqrt{1 + \frac{1}{12} \times \left(\frac{678 \text{ mA} \times 0.533}{1\text{A}}\right)^2} = 1.89\text{A}$$

(110)

The chosen component from step 4 is:

$$L_1 = 33 \mu\text{H}$$

(111)

9.2.2.2.5 Output Capacitance

Solve for $C_{O}$:

$$C_{O} = \frac{I_{\text{LED}} \times D}{r_{D} \times \Delta I_{\text{LED-PP}} \times f_{\text{SW}}}$$

$$C_{O} = \frac{1\text{A} \times 0.467}{1.95\Omega \times 12 \text{ mA} \times 501 \text{ kHz}} = 39.8 \mu\text{F}$$

(112)

The closest capacitance totals 40 $\mu\text{F}$; therefore, $\Delta I_{\text{LED-PP}}$ is:

$$\Delta I_{\text{LED-PP}} = \frac{I_{\text{LED}} \times D}{r_{D} \times C_{D} \times f_{\text{SW}}}$$

$$\Delta I_{\text{LED-PP}} = \frac{1\text{A} \times 0.467}{1.95\Omega \times 40 \mu\text{F} \times 501 \text{ kHz}} = 12 \text{ mA}$$

(113)

Determine minimum allowable RMS current rating:
Typical Applications (continued)

\[ I_{\text{CO-RMS}} = I_{\text{LED}} \times \sqrt{\frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \]  

(114)

The chosen components from step 5 are:

\[ C_O = 4 \times 10 \mu F \]

(115)

9.2.2.2.6 Peak Current Limit

Solve for \( R_{\text{LIM}} \):

\[ R_{\text{LIM}} = \frac{245 \text{ mV}}{I_{\text{LIM}}} = \frac{245 \text{ mV}}{6A} = 0.041\Omega \]

(116)

The closest standard resistor is 0.04 \( \Omega \); therefore, \( I_{\text{LIM}} \) is:

\[ I_{\text{LIM}} = \frac{245 \text{ mV}}{R_{\text{LIM}}} = \frac{245 \text{ mV}}{0.04\Omega} = 6.13A \]

(117)

The chosen component from step 6 is:

\[ R_{\text{LIM}} = 0.04\Omega \]

(118)

9.2.2.2.7 Loop Compensation

\( \omega_{P1} \) is approximated:

\[ \omega_{P1} = \frac{1 + D}{r_D \times C_O} = \frac{1.467}{1.95\Omega \times 40 \mu F} = 19k \frac{\text{rad}}{\text{sec}} \]

(119)

\( \omega_{Z1} \) is approximated:

\[ \omega_{Z1} = \frac{r_D \times D^2}{D \times L1} = \frac{1.95\Omega \times 0.533^2}{0.467 \times 33\mu H} = 36k \frac{\text{rad}}{\text{sec}} \]

(120)

\( T_{U0} \) is approximated:

\[ T_{U0} = \frac{D' \times 620V}{(1 + D) \times I_{\text{LED}} \times R_{\text{LIM}}} = \frac{0.533 \times 620V}{1.467 \times 1A \times 0.04\Omega} = 5630 \]

(121)

To ensure stability, calculate \( \omega_{P2} \):

\[ \omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} = \frac{\omega_{P1}}{5 \times 5630} = \frac{19k}{5 \times 5630} = 0.675 \frac{\text{rad}}{\text{sec}} \]

(122)

Solve for \( C_{\text{CMP}} \):

\[ C_{\text{CMP}} = \frac{1}{\omega_{P2} \times 5 \times 10^6 \Omega} = \frac{1}{0.675 \text{ rad} \times 5 \times 10^6 \Omega} = 0.3 \mu F \]

(123)

To attenuate switching noise, calculate \( \omega_{P3} \):

\[ \omega_{P3} = (\max \omega_{P1}, \omega_{Z1}) \times 10 = \omega_{Z1} \times 10 \]

\[ \omega_{P3} = 36k \frac{\text{rad}}{\text{sec}} \times 10 = 360k \frac{\text{rad}}{\text{sec}} \]

(124)

Assume \( R_{FS} = 10 \Omega \) and solve for \( C_{FS} \):
Typical Applications (continued)

\[ C_{FS} = \frac{1}{10 \Omega \times \omega_{p3}} = \frac{1}{10 \Omega \times 360 \frac{\text{rad}}{\text{sec}}} = 0.28 \mu F \]  

The chosen components from step 7 are:

- \( C_{\text{COMP}} = 0.33 \mu F \)
- \( R_{FS} = 10 \Omega \)
- \( C_{FS} = 0.27 \mu F \)

9.2.2.8 Input Capacitance

Solve for the minimum \( C_{IN} \):

\[ C_{IN} = \frac{I_{\text{LED}} \times D}{\Delta V_{IN-PP} \times f_{SW}} = \frac{1A \times 0.467}{100 \text{ mV} \times 504 \text{ kHz}} = 9.27 \mu F \]  

To minimize power supply interaction a 200% larger capacitance of approximately 20 \( \mu F \) is used, therefore the actual \( \Delta V_{IN-PP} \) is much lower. Because high voltage ceramic capacitor selection is limited, four 4.7-\( \mu F \) X7R capacitors are chosen.

Determine minimum allowable RMS current rating:

\[ I_{IN-RMS} = I_{\text{LED}} \times \sqrt{\frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \]  

The chosen components from step 8 are:

- \( C_{IN} = 4 \times 4.7 \mu F \)

9.2.2.9 N-channel FET

Determine minimum Q1 voltage rating and current rating:

\[ V_{T-\text{MAX}} = V_{IN-\text{MAX}} + V_O = 70V + 21V = 91V \]  

\[ I_{T-\text{MAX}} = \frac{0.677}{1 - 0.677} \times 1A = 2.1A \]  

A 100-V N-channel FET is chosen with a current rating of 32 A due to the low \( R_{DS-\text{ON}} = 50 \text{ m\Omega} \). Determine \( I_{T-RMS} \) and \( P_T \):

\[ I_{T-RMS} = \frac{I_{\text{LED}}}{D} \times \sqrt{D} = \frac{1A}{0.533} \times \sqrt{0.467} = 1.28A \]  

\[ P_T = I_{T-RMS}^2 \times R_{DS-\text{ON}} = 1.28A^2 \times 50 \text{ m\Omega} = 82 \text{ mW} \]  

The chosen component from step 9 is:

- Q1 \( \rightarrow \) 32A, 100V, DPAK

9.2.2.10 Diode

Determine minimum D1 voltage rating and current rating:
Typical Applications (continued)

\[ V_{RD-MAX} = V_{IN-MAX} + V_D = 70V + 21V = 91V \]  \hspace{1cm} (135)

\[ I_{D-MAX} = I_{LED} = 1A \]  \hspace{1cm} (136)

A 100-V diode is chosen with a current rating of 12 A and \( V_{DF} = 600 \text{ mV} \). Determine \( P_D \):

\[ P_D = I_D \times V_{FD} = 1A \times 600 \text{ mV} = 600 \text{ mW} \]  \hspace{1cm} (137)

The chosen component from step 10 is:

\[ \text{D1 } \rightarrow 12A, \text{ 100V, DPAK} \]  \hspace{1cm} (138)

9.2.2.2.11 Input UVLO

Solve for \( R_{UV2} \):

\[ R_{UV2} = \frac{V_{HYS}}{23 \mu A} = \frac{3V}{23 \mu A} = 130 \text{ k}\Omega \]  \hspace{1cm} (139)

The closest standard resistor is 130 k\( \Omega \); therefore, \( V_{HYS} \) is:

\[ V_{HYS} = R_{UV2} \times 23 \mu A = 130 \text{ k}\Omega \times 23 \mu A = 2.99V \]  \hspace{1cm} (140)

Solve for \( R_{UV1} \):

\[ R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} = \frac{1.24V \times 130 \text{ k}\Omega}{10V - 1.24V} = 18.4 \text{ k}\Omega \]  \hspace{1cm} (141)

The closest standard resistor is 18.2 k\( \Omega \), making \( V_{TURN-ON} \):

\[ V_{TURN-ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}} \]

\[ V_{TURN-ON} = \frac{1.24V \times (18.2 \text{ k}\Omega + 130 \text{ k}\Omega)}{18.2 \text{ k}\Omega} = 10.1V \]  \hspace{1cm} (142)

The chosen components from step 11 are:

\[ \begin{align*}
R_{UV1} &= 18.2 \text{ k}\Omega \\
R_{UV2} &= 130 \text{ k}\Omega
\end{align*} \]  \hspace{1cm} (143)

9.2.2.2.12 Output OVLO

Solve for \( R_{OV2} \):

\[ R_{OV2} = \frac{V_{HYSO}}{23 \mu A} = \frac{10V}{23 \mu A} = 435 \text{ k}\Omega \]  \hspace{1cm} (144)

The closest standard resistor is 432 k\( \Omega \); therefore, \( V_{HYSO} \) is:

\[ V_{HYSO} = R_{OV2} \times 23 \mu A = 432 \text{ k}\Omega \times 23 \mu A = 9.94V \]  \hspace{1cm} (145)

Solve for \( R_{OV1} \):

\[ R_{OV1} = \frac{1.24V \times R_{OV2}}{V_{TURN-OFF} - 0.62V} = \frac{1.24V \times 432 \text{ k}\Omega}{40V - 0.62V} = 13.6 \text{ k}\Omega \]  \hspace{1cm} (146)

The closest standard resistor is 13.7 k\( \Omega \), making \( V_{TURN-OFF} \):
Typical Applications (continued)

\[
V_{\text{TURN-OFF}} = \frac{1.24V \times (0.5 \times R_{\text{OV1}} + R_{\text{OV2}})}{R_{\text{OV1}}}
\]

\[
V_{\text{TURN-OFF}} = \frac{1.24V \times (0.5 \times 13.7 \, \text{k}\Omega + 432 \, \text{k}\Omega)}{13.7 \, \text{k}\Omega} = 39.7V
\]

The chosen components from step 12 are:

\[
\begin{align*}
R_{\text{OV1}} &= 13.7 \, \text{k}\Omega \\
R_{\text{OV2}} &= 432 \, \text{k}\Omega
\end{align*}
\]

Table 2. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LM3421</td>
<td>Buck-boost controller</td>
<td>TI</td>
<td>LM3421MH</td>
</tr>
<tr>
<td>1</td>
<td>C_{GYP}</td>
<td>2.2-µF X7R 10% 16V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
</tr>
<tr>
<td>1</td>
<td>C_{CMP}</td>
<td>0.33-µF X7R 10% 25V</td>
<td>MURATA</td>
<td>GRM21BR71E334KA01L</td>
</tr>
<tr>
<td>1</td>
<td>C_{FS}</td>
<td>0.27-µF X7R 10% 25V</td>
<td>MURATA</td>
<td>GRM21BR71E274KA01L</td>
</tr>
<tr>
<td>4</td>
<td>C_{IN}</td>
<td>4.7-µF X7R 10% 100V</td>
<td>TDK</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>4</td>
<td>C_{D}</td>
<td>10-µF X7R 10% 50V</td>
<td>TDK</td>
<td>C4532X7R1H106K</td>
</tr>
<tr>
<td>1</td>
<td>C_{OV}</td>
<td>47-pF COG/NPO 5% 50V</td>
<td>AVX</td>
<td>0805A470JAT2A</td>
</tr>
<tr>
<td>1</td>
<td>C_{T}</td>
<td>1000-pF COG/NPO 5% 50V</td>
<td>MURATA</td>
<td>GRM2165C1H102JA01D</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>Schottky 100 V 12 A</td>
<td>VISHAY</td>
<td>12CWQ10FP2BF</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>33 µH 20% 6.3 A</td>
<td>COILCRAFT</td>
<td>MSS1278-333MLB</td>
</tr>
<tr>
<td>1</td>
<td>Q1</td>
<td>NMOS 100 V 32 A</td>
<td>FAIRCHILD</td>
<td>FDD3682</td>
</tr>
<tr>
<td>1</td>
<td>Q2</td>
<td>PNP 150 V 600 mA</td>
<td>FAIRCHILD</td>
<td>MMBT5401</td>
</tr>
<tr>
<td>1</td>
<td>R_{CSH}</td>
<td>12.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080512K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{FS}</td>
<td>10 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW080510R0FKEA</td>
</tr>
<tr>
<td>2</td>
<td>R_{HSP}, R_{HSN}</td>
<td>1 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{UM}</td>
<td>0.04 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R0400FEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{OV1}</td>
<td>13.7 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080513K7FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{OV2}</td>
<td>432 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW0805432KFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{SNS}</td>
<td>0.1 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R1000FEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{T}</td>
<td>49.9 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805489KFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{UV1}</td>
<td>18.2 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080518K2FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{UV2}</td>
<td>130 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805130KFKEA</td>
</tr>
</tbody>
</table>
9.2.2.3 Application Curve

\[ V_{\text{OUT}} = 21 \text{ V} \]

Figure 37. Sample Buck-Boost Efficiency vs Input Voltage.
9.2.3 LM3421 BOOST Application

![Diagram of LM3421 BOOST Application](image)

Figure 38. LM3421 BOOST Application

9.2.3.1 Design Requirements

- Input: 8 V to 28 V
- Output: 9 LEDs at 1 A
- PWM Dimming up to 30kHz
- Switching Frequency: 700-kHz
### Detailed Design Procedure

#### Table 3. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LM3421</td>
<td>Boost controller</td>
<td>TI</td>
<td>LM3421MH</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;BYP&lt;/sub&gt;</td>
<td>2.2-µF X7R 10% 16 V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;CMP&lt;/sub&gt;</td>
<td>0.1-µF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E104KA01L</td>
</tr>
<tr>
<td>0</td>
<td>C&lt;sub&gt;FS&lt;/sub&gt;</td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>4.7-µF X7R 10% 100 V</td>
<td>TDK</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>4</td>
<td>C&lt;sub&gt;O&lt;/sub&gt;</td>
<td>10-µF X7R 10% 50 V</td>
<td>TDK</td>
<td>C4532X7R1H106K</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;OV&lt;/sub&gt;</td>
<td>47-pF COG/NPO 5% 50 V</td>
<td>AVX</td>
<td>0805SA470JAT2A</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;T&lt;/sub&gt;</td>
<td>1000-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H102JA01D</td>
</tr>
<tr>
<td>2</td>
<td>D1, D2</td>
<td>Schottky 60 V 5 A</td>
<td>COMCHIP</td>
<td>CDBC560-G</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>33-µH 20% 6.3 A</td>
<td>COILCRAFT</td>
<td>MSS1278-333MLB</td>
</tr>
<tr>
<td>2</td>
<td>Q1, Q2</td>
<td>NMOS 60 V 8 A</td>
<td>VISHAY</td>
<td>SI4436DY</td>
</tr>
<tr>
<td>1</td>
<td>Q3</td>
<td>NMOS 60 V 115 mA</td>
<td>ON-SEMI</td>
<td>2N7002ET1G</td>
</tr>
<tr>
<td>2</td>
<td>R&lt;sub&gt;CSH&lt;/sub&gt;, R&lt;sub&gt;OV1&lt;/sub&gt;</td>
<td>12.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080512K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;FS&lt;/sub&gt;</td>
<td>0 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW08050000Z0EA</td>
</tr>
<tr>
<td>2</td>
<td>R&lt;sub&gt;HSP&lt;/sub&gt;, R&lt;sub&gt;HSN&lt;/sub&gt;</td>
<td>1 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K00FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;LM&lt;/sub&gt;</td>
<td>0.06 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R0600FEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;OV2&lt;/sub&gt;</td>
<td>499 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;NS&lt;/sub&gt;</td>
<td>0.1 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R1000FEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;UV2&lt;/sub&gt;</td>
<td>10 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080510K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;T&lt;/sub&gt;</td>
<td>35.7 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080535K7FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;UV1&lt;/sub&gt;</td>
<td>1.82 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K82FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;UVH&lt;/sub&gt;</td>
<td>17.8 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080517K8FKEA</td>
</tr>
</tbody>
</table>
9.2.4 LM3421 Buck-Boost Application

### Design Requirements

- **Input:** 10 V to 30 V
- **Output:** 4 LEDs at 2 A
- **PWM Dimming:** up to 10 kHz
- **Analog Dimming**
- **Switching Frequency:** 600-kHz
## 9.2.4.2 Detailed Design Procedure

Table 4. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LM3421</td>
<td>Buck-boost controller</td>
<td>Ti</td>
<td>LM3421MH</td>
</tr>
<tr>
<td>1</td>
<td>C_B</td>
<td>100-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H101JA01D</td>
</tr>
<tr>
<td>1</td>
<td>C_BYP</td>
<td>2.2-µF X7R 10% 16 V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
</tr>
<tr>
<td>3</td>
<td>C_CMP, C_REF, C_SS</td>
<td>1-µF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E105KA01L</td>
</tr>
<tr>
<td>1</td>
<td>C_F</td>
<td>0.1-µF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E104KA01L</td>
</tr>
<tr>
<td>0</td>
<td>C_FS</td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>C_IN</td>
<td>6.8-µF X7R 10% 50 V</td>
<td>TDK</td>
<td>CS750X7R1H685K</td>
</tr>
<tr>
<td>4</td>
<td>C_O</td>
<td>10-µF X7R 10% 50 V</td>
<td>TDK</td>
<td>C4532X7R1H106K</td>
</tr>
<tr>
<td>1</td>
<td>C_UV</td>
<td>47-pF COG/NPO 5% 50 V</td>
<td>AVX</td>
<td>08055A470JAT2A</td>
</tr>
<tr>
<td>1</td>
<td>C_T</td>
<td>1000-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H102JA01D</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>Schottky 100 V 12 A</td>
<td>VISHAY</td>
<td>12CQ10FNPBF</td>
</tr>
<tr>
<td>1</td>
<td>D2</td>
<td>Zener 10 V 500 mA</td>
<td>ON-SEMI</td>
<td>BZ84C10LT1G</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>22 µH 20% 7.2 A</td>
<td>COILCRAFT</td>
<td>MSS1278-223MLB</td>
</tr>
<tr>
<td>2</td>
<td>Q1, Q2</td>
<td>NMOS 60 V 8 A</td>
<td>VISHAY</td>
<td>SI4436DY</td>
</tr>
<tr>
<td>1</td>
<td>Q3</td>
<td>NMOS 60 V 260 mA</td>
<td>ON-SEMI</td>
<td>2N7002ET1G</td>
</tr>
<tr>
<td>1</td>
<td>Q4</td>
<td>PNP 40 V 200 mA</td>
<td>FAIRCHILD</td>
<td>MBT5087</td>
</tr>
<tr>
<td>1</td>
<td>Q5</td>
<td>PNP 150 V 600 mA</td>
<td>FAIRCHILD</td>
<td>MBT5401</td>
</tr>
<tr>
<td>1</td>
<td>Q6</td>
<td>NPN 300 V 600 mA</td>
<td>FAIRCHILD</td>
<td>MBTA42</td>
</tr>
<tr>
<td>1</td>
<td>Q7</td>
<td>NPN 40 V 200 mA</td>
<td>FAIRCHILD</td>
<td>MBT6428</td>
</tr>
<tr>
<td>1</td>
<td>R_CSH</td>
<td>12.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080512K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_C</td>
<td>10 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080510R0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_FS</td>
<td>0 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW0805000020EA</td>
</tr>
<tr>
<td>1</td>
<td>R_UV2</td>
<td>10 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080510K0FKEA</td>
</tr>
<tr>
<td>2</td>
<td>R_HSP, R_HSN</td>
<td>1 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K00FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_UIM</td>
<td>0.04 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R0400FEA</td>
</tr>
<tr>
<td>1</td>
<td>R_UV1</td>
<td>18.2 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080518K2FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_UV2</td>
<td>499 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_POT</td>
<td>1-MΩ potentiometer</td>
<td>BOURNS</td>
<td>3352P-1-105</td>
</tr>
<tr>
<td>1</td>
<td>R_PU</td>
<td>4.99 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080517K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_SER</td>
<td>499 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW0805499RFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_INS</td>
<td>0.05 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R0500FEA</td>
</tr>
<tr>
<td>1</td>
<td>R_T</td>
<td>41.2 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K2FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_UV1</td>
<td>1.43 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K43FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_UVH</td>
<td>17.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080517K4FKEA</td>
</tr>
</tbody>
</table>
9.2.5 LM3423 Boost Application

**Figure 40. LM3423 Boost Application**

### 9.2.5.1 Design Requirements

- **Input:** 18 V to 38 V
- **Output:** 12 LEDs at 700 mA
- **High-Side PWM Dimming:** up to 30 kHz
- **Dimming:** Analog
- **Zero Current Shutdown**
- **Switching Frequency:** 700-kHz
### 9.2.5.2 Detailed Design Procedure

#### Table 5. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LM3423</td>
<td>Boost controller</td>
<td>TI</td>
<td>LM3423MH</td>
</tr>
<tr>
<td>1</td>
<td>C_{BP}</td>
<td>2.2-µF X7R 10% 16 V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
</tr>
<tr>
<td>1</td>
<td>C_{CM}</td>
<td>1-µF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E105KA01L</td>
</tr>
<tr>
<td>4</td>
<td>C_{IN}</td>
<td>4.7-µF X7R 10% 100 V</td>
<td>TDK</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>4</td>
<td>C_{O}</td>
<td>10-µF X7R 10% 50 V</td>
<td>TDK</td>
<td>C4532X7R1H106K</td>
</tr>
<tr>
<td>1</td>
<td>C_{OV}</td>
<td>47-pF COG/NPO 5% 50 V</td>
<td>AVX</td>
<td>08055A470JAT2A</td>
</tr>
<tr>
<td>1</td>
<td>C_{T}</td>
<td>1000-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H102JA01D</td>
</tr>
<tr>
<td>2</td>
<td>D1, D2</td>
<td>Schottky 60 V 5 A</td>
<td>COMCHIP</td>
<td>CDBC560-G</td>
</tr>
<tr>
<td>1</td>
<td>D3</td>
<td>Zener 10 V 500 mA</td>
<td>ON-SEMI</td>
<td>BZX84C10LT1G</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>47 µH 20% 5.3 A</td>
<td>COILCRAFT</td>
<td>MSS1278-473MLB</td>
</tr>
<tr>
<td>1</td>
<td>Q1</td>
<td>NMOS 60 V 8 A</td>
<td>VISHAY</td>
<td>Si4436DY</td>
</tr>
<tr>
<td>1</td>
<td>Q2</td>
<td>PMOS 70 V 5.7 A</td>
<td>ZETEX</td>
<td>ZXMP7A17K</td>
</tr>
<tr>
<td>1</td>
<td>Q3</td>
<td>NMOS 60 V 260 mA</td>
<td>ON-SEMI</td>
<td>2N7002ET1G</td>
</tr>
<tr>
<td>1</td>
<td>Q4, Q5 (dual pack)</td>
<td>Dual PNP 40 V 200 mA</td>
<td>FAIRCHILD</td>
<td>FFB3906</td>
</tr>
<tr>
<td>1</td>
<td>Q6</td>
<td>NPN 300 V 600 mA</td>
<td>FAIRCHILD</td>
<td>MMBTA42</td>
</tr>
<tr>
<td>1</td>
<td>Q7</td>
<td>NPN 40 V 200 mA</td>
<td>FAIRCHILD</td>
<td>MMBT3904</td>
</tr>
<tr>
<td>1</td>
<td>R_{ADJ}</td>
<td>100-kΩ potentiometer</td>
<td>BOURNS</td>
<td>3352P-1-104</td>
</tr>
<tr>
<td>2</td>
<td>R_{BIAS2}</td>
<td>17.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080517K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{CMH}, R_{OV1}</td>
<td>12.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080512K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{FS}</td>
<td>10 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080510R0FKEA</td>
</tr>
<tr>
<td>3</td>
<td>R_{NSP}, R_{HSN}, R_{MAX}</td>
<td>1 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080510K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{ULM}</td>
<td>0.06 Ω 1% 1W</td>
<td>VISHAY</td>
<td>WSL2512R0600FEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{OV2}</td>
<td>499 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{SNS}</td>
<td>0.15 Ω 1% 1W</td>
<td>VISHAY</td>
<td>WSL2512R1500FEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{T}</td>
<td>35.7 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080535K7FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{UV1}</td>
<td>1.43 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K43FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{UV2}</td>
<td>10 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080510K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_{UVH}</td>
<td>16.9 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080516K9FKEA</td>
</tr>
</tbody>
</table>
9.2.6 LM3421 Buck-Boost Application

**Figure 41. LM3421 Buck-Boost Application**

9.2.6.1 Design Requirements

- Input: 10 V to 70 V
- Output: 6 LEDs at 500 mA
- PWM Dimming up to 10 kHz
- Slow Fade Out
- MOSFET $R_{DS-ON}$ Sensing
- 700-kHz Switching Frequency
### 9.2.6.2 Detailed Design Procedure

#### Table 6. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LM3421</td>
<td>Buck-boost controller</td>
<td>TI</td>
<td>LM3421MH</td>
</tr>
<tr>
<td>1</td>
<td>C_B</td>
<td>100-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H101JA01D</td>
</tr>
<tr>
<td>1</td>
<td>C_BYP</td>
<td>2.2-μF X7R 10% 16 V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
</tr>
<tr>
<td>1</td>
<td>C_CMP</td>
<td>1-μF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E105KA01L</td>
</tr>
<tr>
<td>1</td>
<td>C_F</td>
<td>0.1-μF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E104KA01L</td>
</tr>
<tr>
<td>0</td>
<td>C_FS</td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>C_IN</td>
<td>4.7-μF X7R 10% 100 V</td>
<td>TDK</td>
<td>CS750X7R2A475K</td>
</tr>
<tr>
<td>4</td>
<td>C_D</td>
<td>10-μF X7R 10% 50 V</td>
<td>TDK</td>
<td>C4532X7R1H106K</td>
</tr>
<tr>
<td>1</td>
<td>C_OV</td>
<td>47-pF COG/NPO 5% 50 V</td>
<td>AVX</td>
<td>08055A470JAT2A</td>
</tr>
<tr>
<td>1</td>
<td>C_T</td>
<td>1000-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H102JA01D</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>Schottky 100 V 12 A</td>
<td>VISHAY</td>
<td>12CWQ10FNPBF</td>
</tr>
<tr>
<td>1</td>
<td>D2</td>
<td>Zener 10 V 500 mA</td>
<td>ON-SEMI</td>
<td>BZX84C10LT1G</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>68 μH 20% 4.3 A</td>
<td>COILCRAFT</td>
<td>MSS1278-683MLB</td>
</tr>
<tr>
<td>2</td>
<td>Q1, Q2</td>
<td>NMOS 100 V 32 A</td>
<td>FAIRCHILD</td>
<td>FDD3682</td>
</tr>
<tr>
<td>1</td>
<td>Q3</td>
<td>NMOS 60 V 260 mA</td>
<td>ON-SEMI</td>
<td>2N7002ET1G</td>
</tr>
<tr>
<td>2</td>
<td>Q4, Q8</td>
<td>PNP 40 V 200 mA</td>
<td>FAIRCHILD</td>
<td>MMBT5087</td>
</tr>
<tr>
<td>1</td>
<td>Q5</td>
<td>PNP 150 V 600 mA</td>
<td>FAIRCHILD</td>
<td>MMBT5401</td>
</tr>
<tr>
<td>1</td>
<td>Q6</td>
<td>NPN 300 V 600 mA</td>
<td>FAIRCHILD</td>
<td>MMBTA42</td>
</tr>
<tr>
<td>2</td>
<td>Q7, Q9</td>
<td>NPN 40 V 200 mA</td>
<td>FAIRCHILD</td>
<td>MMBT6428</td>
</tr>
<tr>
<td>1</td>
<td>R_CSH</td>
<td>12.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080512K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_FS</td>
<td>0 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW08050000Z0EA</td>
</tr>
<tr>
<td>1</td>
<td>R_UV2</td>
<td>10 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080510K0FKEA</td>
</tr>
<tr>
<td>2</td>
<td>R_HS, R_HSN</td>
<td>1 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K00FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_OV1</td>
<td>15.8 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080515K8FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_OV2</td>
<td>499 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_PU</td>
<td>4.99 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_SER</td>
<td>499 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_SNS</td>
<td>0.2 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R2000FEA</td>
</tr>
<tr>
<td>1</td>
<td>R_T</td>
<td>35.7 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080535K7FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_UV1</td>
<td>1.43 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K43FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R_UVH</td>
<td>17.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080517K4FKEA</td>
</tr>
</tbody>
</table>
9.2.7 LM3423 Buck Application

15V – 50V

Figure 42. LM3423 Buck Application

9.2.7.1 Design Requirements

- Input: 15 V to 50 V
- Output: 3 LEDs at 1.25 A
- PWM Dimming up to 50 kHz
- LED Status Indicator
- Zero Current Shutdown
- 700-kHz Switching Frequency
### 9.2.7.2 Detailed Design Procedure

#### Table 7. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LM3423</td>
<td>Buck controller</td>
<td>TI</td>
<td>LM3423MH</td>
</tr>
<tr>
<td>1</td>
<td>C\textsubscript{BYP}</td>
<td>2.2 μF X7R 10% 16 V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
</tr>
<tr>
<td>2</td>
<td>C\textsubscript{CMP}, C\textsubscript{DIM}</td>
<td>0.1 μF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E104KA01L</td>
</tr>
<tr>
<td>0</td>
<td>C\textsubscript{FS}</td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>C\textsubscript{IN}</td>
<td>4.7 μF X7R 10% 100 V</td>
<td>TDK</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>0</td>
<td>C\textsubscript{O}</td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>C\textsubscript{OV}</td>
<td>47-pF COG/NPO 5% 50 V</td>
<td>AVX</td>
<td>08055A470JAT2A</td>
</tr>
<tr>
<td>1</td>
<td>C\textsubscript{T}</td>
<td>1000-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H102JA01D</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>Schottky 100 V 12 A</td>
<td>VISHAY</td>
<td>12CWQ10FNPBF</td>
</tr>
<tr>
<td>1</td>
<td>D2</td>
<td>Zener 10 V 500 mA</td>
<td>ON-SEMI</td>
<td>BZX84C10LT1G</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>22 μH 20% 7.3 A</td>
<td>COILCRAFT</td>
<td>MSS1278-223MLB</td>
</tr>
<tr>
<td>1</td>
<td>Q1</td>
<td>NMOS 60 V 8 A</td>
<td>VISHAY</td>
<td>SI4436DY</td>
</tr>
<tr>
<td>1</td>
<td>Q2</td>
<td>PMOS 30 V 6.2 A</td>
<td>VISHAY</td>
<td>SI3483DV</td>
</tr>
<tr>
<td>1</td>
<td>Q3</td>
<td>NMOS 60 V 115 mA</td>
<td>ON-SEMI</td>
<td>2N7002ET1G</td>
</tr>
<tr>
<td>1</td>
<td>Q4</td>
<td>PNP 150 V 600 mA</td>
<td>FAIRCHILD</td>
<td>MMBT5401</td>
</tr>
<tr>
<td>1</td>
<td>R\textsubscript{CSH}</td>
<td>12.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080512K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R\textsubscript{FS}</td>
<td>0 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW08050000ZEA</td>
</tr>
<tr>
<td>2</td>
<td>R\textsubscript{HSP}, R\textsubscript{HSN}</td>
<td>1 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K00FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R\textsubscript{IM}</td>
<td>0.04 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R0400FEA</td>
</tr>
<tr>
<td>1</td>
<td>R\textsubscript{OV1}</td>
<td>21.5 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080521K5FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R\textsubscript{OV2}</td>
<td>499 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFEA</td>
</tr>
<tr>
<td>3</td>
<td>R\textsubscript{PU}, R\textsubscript{PU2}, R\textsubscript{UV2}</td>
<td>100 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805100KFEA</td>
</tr>
<tr>
<td>1</td>
<td>R\textsubscript{T}</td>
<td>35.7 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080535K7FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R\textsubscript{SNS}</td>
<td>0.08 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R0800FEA</td>
</tr>
<tr>
<td>1</td>
<td>R\textsubscript{UV1}</td>
<td>11.5 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080511K5FKEA</td>
</tr>
</tbody>
</table>
9.2.8 LM3423 Buck-Boost Application

9.2.8.1 Design Requirements

- Input: 15 V to 60 V
- Output: 8 LEDs at 2.5 A
- Fault Input Disconnect
- Zero Current Shutdown
- 500-kHz Switching Frequency
## 9.2.8.2 Detailed Design Procedure

### Table 8. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LM3423</td>
<td>Buck-boost controller</td>
<td>TI</td>
<td>LM3423MH</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;byp&lt;/sub&gt;</td>
<td>2.2-µF X7R 10% 16 V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;cmp&lt;/sub&gt;</td>
<td>0.33-µF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E334KA01L</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;fs&lt;/sub&gt;</td>
<td>0.1-µF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E104KA01L</td>
</tr>
<tr>
<td>4</td>
<td>C&lt;sub&gt;in&lt;/sub&gt;</td>
<td>4.7-µF X7R 10% 100 V</td>
<td>TDK</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>4</td>
<td>C&lt;sub&gt;o&lt;/sub&gt;</td>
<td>10-µF X7R 10% 50 V</td>
<td>TDK</td>
<td>C4532X7R1H106K</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;ov&lt;/sub&gt;</td>
<td>47-pF COG/NPO 5% 50 V</td>
<td>AVX</td>
<td>08055A470JAT2A</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;t&lt;/sub&gt;</td>
<td>1000-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H102JA01D</td>
</tr>
<tr>
<td>1</td>
<td>C&lt;sub&gt;timer&lt;/sub&gt;</td>
<td>220-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H221JA01D</td>
</tr>
<tr>
<td>1</td>
<td>D&lt;sub&gt;1&lt;/sub&gt;</td>
<td>Schottky 100 V 12 A</td>
<td>VISHAY</td>
<td>12CWQ10FNPBF</td>
</tr>
<tr>
<td>1</td>
<td>D&lt;sub&gt;2&lt;/sub&gt;</td>
<td>Zener 10 V 500 mA</td>
<td>ON-SEMI</td>
<td>BZX84C10LT1G</td>
</tr>
<tr>
<td>1</td>
<td>L&lt;sub&gt;1&lt;/sub&gt;</td>
<td>22 µH 20% 7.2 A</td>
<td>COILCRAFT</td>
<td>MSS1278-223MLB</td>
</tr>
<tr>
<td>1</td>
<td>Q&lt;sub&gt;1&lt;/sub&gt;</td>
<td>NMOS 100 V 32 A</td>
<td>FAIRCHILD</td>
<td>FDD3682</td>
</tr>
<tr>
<td>1</td>
<td>Q&lt;sub&gt;2&lt;/sub&gt;</td>
<td>PMOS 70 V 5.7 A</td>
<td>ZETEX</td>
<td>ZXMP7A17K</td>
</tr>
<tr>
<td>1</td>
<td>Q&lt;sub&gt;5&lt;/sub&gt;</td>
<td>PNP 150 V 600 mA</td>
<td>FAIRCHILD</td>
<td>MBT5401</td>
</tr>
<tr>
<td>2</td>
<td>R&lt;sub&gt;CSH, ROV1&lt;/sub&gt;</td>
<td>12.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080512K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;FS&lt;/sub&gt;</td>
<td>10 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW080510R0FKEA</td>
</tr>
<tr>
<td>2</td>
<td>R&lt;sub&gt;FLT, RPU2&lt;/sub&gt;</td>
<td>100 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805100KFKEA</td>
</tr>
<tr>
<td>2</td>
<td>R&lt;sub&gt;HSP, RHSN&lt;/sub&gt;</td>
<td>1 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K00FKEA</td>
</tr>
<tr>
<td>2</td>
<td>R&lt;sub&gt;LIM, RSN&lt;/sub&gt;</td>
<td>0.04 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R0400FEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;OV1&lt;/sub&gt;</td>
<td>15.8 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080515K8FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;OV2&lt;/sub&gt;</td>
<td>499 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;T&lt;/sub&gt;</td>
<td>49.9 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499K9FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;UV1&lt;/sub&gt;</td>
<td>13.7 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080513K7FKEA</td>
</tr>
<tr>
<td>1</td>
<td>R&lt;sub&gt;UV2&lt;/sub&gt;</td>
<td>150 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805150KFKEA</td>
</tr>
</tbody>
</table>
9.2.9 LM3421 SEPIC Application

9V – 36V

Figure 44. LM3421 SEPIC Application

9.2.9.1 Design Procedure

- Input: 9 V to 36 V
- Output: 5 LEDs at 750 mA
- PWM Dimming up to 30 kHz
- 500-kHz Switching Frequency
### Detailed Design Procedure

**Table 9. Bill of Materials**

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>LM3421</td>
<td>SEPIC controller</td>
<td>TI</td>
<td>LM3421MH</td>
</tr>
<tr>
<td>1</td>
<td>C35P</td>
<td>2.2-µF X7R 10% 16 V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
</tr>
<tr>
<td>1</td>
<td>C35MP</td>
<td>0.47-µF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E474KA01L</td>
</tr>
<tr>
<td>0</td>
<td>CFS</td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>CIN</td>
<td>4.7-µF X7R 10% 100 V</td>
<td>TDK</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>4</td>
<td>CO</td>
<td>10-µF X7R 10% 50 V</td>
<td>TDK</td>
<td>C4532X7R1H106K</td>
</tr>
<tr>
<td>1</td>
<td>CSEP</td>
<td>1-µF X7R 10% 100 V</td>
<td>TDK</td>
<td>C4532X7R2A105K</td>
</tr>
<tr>
<td>1</td>
<td>COV</td>
<td>47-pF COG/NPO 5% 50 V</td>
<td>AVX</td>
<td>08055A470JAT2A</td>
</tr>
<tr>
<td>1</td>
<td>CT</td>
<td>1000-pF COG/NPO 5% 50 V</td>
<td>MURATA</td>
<td>GRM2165C1H102JA01D</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>Schottky 60 V 5 A</td>
<td>COMCHIP</td>
<td>CDDBC560-G</td>
</tr>
<tr>
<td>2</td>
<td>L1, L2</td>
<td>68 µH 20% 4.3 A</td>
<td>COILCRAFT</td>
<td>DO3340P-683</td>
</tr>
<tr>
<td>2</td>
<td>Q1, Q2</td>
<td>NMOS 60 V 8 A</td>
<td>VISHAY</td>
<td>Si4436DY</td>
</tr>
<tr>
<td>1</td>
<td>Q3</td>
<td>NMOS 60 V 115 mA</td>
<td>ON-SEMI</td>
<td>2N7002ET1G</td>
</tr>
<tr>
<td>1</td>
<td>RCSH</td>
<td>12.4 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080512K4FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RFS</td>
<td>0 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW08050000OZEA</td>
</tr>
<tr>
<td>2</td>
<td>RHP, RHN</td>
<td>750 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW0805750RFKEA</td>
</tr>
<tr>
<td>1</td>
<td>RLIM</td>
<td>0.04 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R0400FEA</td>
</tr>
<tr>
<td>1</td>
<td>ROV1</td>
<td>15.8 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080515K8FKEA</td>
</tr>
<tr>
<td>1</td>
<td>ROV2</td>
<td>499 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
</tr>
<tr>
<td>2</td>
<td>REF1, REF2</td>
<td>49.9 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080549K9FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RNS</td>
<td>0.1 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL2512R1000FEA</td>
</tr>
<tr>
<td>1</td>
<td>RT</td>
<td>49.9 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080549K9FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RUV1</td>
<td>1.62 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW08051K62FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RUV2</td>
<td>10 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080510K0FKEA</td>
</tr>
<tr>
<td>1</td>
<td>RUVH</td>
<td>16.9 kΩ 1%</td>
<td>VISHAY</td>
<td>CRCW080516K9FKEA</td>
</tr>
</tbody>
</table>
10 Power Supply Recommendations

10.1 General Recommendations
The device is designed to operate from an input voltage supply range from 4.5 V to 75 V. This input supply should be well regulated. If the input supply is located more than a few inches from the EVM or PCB, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10.2 Input Supply Current Limit
It is important to set the output current limit of your input supply to an appropriate value to avoid delays in your converter analysis and optimization. If not set high enough, current limit can be tripped during start-up or when your converter output power is increased, causing a foldback or shutdown condition. It is a common oversight when powering up a converter for the first time.

11 Layout

11.1 Layout Guidelines
- The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines allows maximum noise rejection and minimal generation of EMI within the circuit.
- Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. The main path for discontinuous current in the LM34xx-Q1 buck regulator contains the input capacitor (CIN), the recirculating diode (D1), the N-channel MOSFET (Q1), and the sense resistor (RLIM). In the LM34xx-Q1 boost regulator, the discontinuous current flows through the output capacitor (CO), D1, Q1, and RLIM. In the buck-boost regulator, both loops are discontinuous and should be carefully layed out. These loops should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.
- The RT, COMP, CSH, IS, HSP and HSN pins are all high-impedance inputs which couple external noise easily; therefore, the loops containing these nodes should be minimized whenever possible.
- In some applications the LED or LED array can be far away (several inches or more) from the controller or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.
11.2 Layout Example

Note critical paths and component placement:

- Minimize power loop containing discontinuous currents
- Minimize signal current loops (components close to IC)
- Ground plane under IC for signal routing helps minimize noise coupling

---

Figure 45. LM3421 Boost Layout Guideline
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer
TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>LM3421-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>LM3423</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>LM3423-Q1</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** Ti's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** Ti's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

**SLYZ2022 — Ti Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421MH/NOPB</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>92</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>LM3421MH</td>
<td></td>
</tr>
<tr>
<td>LM3421MHX/NOPB</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>LM3421MH</td>
<td></td>
</tr>
<tr>
<td>LM3423MH/NOPB</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>73</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>LM3423MH</td>
<td></td>
</tr>
<tr>
<td>LM3423MHX/NOPB</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>LM3423MH</td>
<td></td>
</tr>
</tbody>
</table>

### Notes:

1. The marketing status values are defined as follows:
   - **ACTIVE**: Product device recommended for new designs.
   - **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
   - **OBSOLETE**: TI has discontinued the production of the device.

2. **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
   - **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
   - **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

3. **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. **Important Information and Disclaimer**: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM3421, LM3423:

- Automotive: LM3421-Q1, LM3423-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
TAPE AND REEL INFORMATION

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421MHX/NOPB</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.95</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>LM3423MHX/NOPB</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.95</td>
<td>7.1</td>
<td>1.6</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
**TAPE AND REEL BOX DIMENSIONS**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421MHX/NOPB</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>16</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LM3423MHX/NOPB</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>20</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
5. Features may not be present.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.

11. Board assembly site may have different recommendations for stencil design.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated