1 Features
- LM3421Q0/LM3423Q0 are Automotive Grade Products That are AEC-Q100 Grade 0 Qualified
- LM3421Q1/LM3423Q1 are Automotive Grade Products That are AEC-Q100 Grade 1 Qualified
- \( V_{\text{IN}} \) Range From 4.5 V to 75 V
- High-Side Adjustable Current Sense
- 2-\( \Omega \), 1-A Peak MOSFET Gate Driver
- Input Undervoltage and Output Overvoltage Protection
- PWM and Analog Dimming
- Cycle-by-Cycle Current Limit
- Programmable Switching Frequency
- Zero Current Shutdown and Thermal Shutdown
- LED Output Status Flag (LM3423/23Q1/23Q0 Only)
- Fault Status Flag and Timer (LM3423/23Q1/23Q0 Only)

2 Applications
- LED Drivers: Buck, Boost, Buck-Boost, and SEPIC
- Indoor and Outdoor Area SSL
- Automotive
- General Illumination
- Constant-Current Regulators

3 Description
The LM3421 and LM3423 family of devices are versatile high voltage N-channel MOSFET controllers for LED drivers. They can be easily configured in buck, boost, buck-boost and SEPIC topologies. This flexibility, along with an input voltage rating of 75 V, makes the LM3421 and LM3423 devices ideal for illuminating LEDs in a large family of applications.

Adjustable high-side current sense voltage allows for tight regulation of the LED current with the highest efficiency possible. The LM3421 and LM3423 devices use predictive off-time (PRO) control, which is a combination of peak current-mode control and a predictive off-timer. This method of control eases the design of loop compensation while providing inherent input voltage feed-forward compensation.

The LM3421 and LM3423 devices include a high-voltage start-up regulator that operates over a wide input range of 4.5 V to 75 V. The internal PWM controller is designed for adjustable switching frequencies of up to 2 MHz, thus enabling compact solutions.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421</td>
<td>HTSSOP (16)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
<tr>
<td>LM3421-Q1</td>
<td>HTSSOP (20)</td>
<td>6.50 mm × 4.40 mm</td>
</tr>
<tr>
<td>LM3423</td>
<td>HTSSOP (20)</td>
<td>6.50 mm × 4.40 mm</td>
</tr>
<tr>
<td>LM3423-Q1</td>
<td>HTSSOP (20)</td>
<td>6.50 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2013) to Revision F Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1

Changes from Revision D (May 2013) to Revision E Page

• Changed layout of National Data Sheet to TI format ................................................................. 62
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_IN</td>
<td>I</td>
<td>Input voltage</td>
<td>Bypass with 100-nF capacitor to AGND as close to the device as possible in the printed-circuit-board layout.</td>
</tr>
<tr>
<td>EN</td>
<td>I</td>
<td>Enable</td>
<td>Connect to AGND for zero current shutdown or apply &gt; 2.4 V to enable device.</td>
</tr>
<tr>
<td>COMP</td>
<td>I</td>
<td>Compensation</td>
<td>Connect a capacitor to AGND to set the compensation.</td>
</tr>
<tr>
<td>CSH</td>
<td>I</td>
<td>Current sense high</td>
<td>Connect a resistor to AGND to set the signal current. For analog dimming, connect a controlled current source or a potentiometer to AGND as detailed in the Analog Dimming section.</td>
</tr>
<tr>
<td>RCT</td>
<td>I</td>
<td>Resistor capacitor timing</td>
<td>External RC network sets the predictive off-time and thus the switching frequency.</td>
</tr>
<tr>
<td>AGND</td>
<td>GND</td>
<td>Analog ground</td>
<td>Connect to PGND through the DAP copper pad to provide ground return for CSH, COMP, RCT, and TIMR.</td>
</tr>
<tr>
<td>OVP</td>
<td>I</td>
<td>Overvoltage protection</td>
<td>Connect to a resistor divider from V_IN to program overvoltage lockout (OVLO). Turnoff threshold is 1.24 V and hysteresis for turnon is provided by 23-µA current source.</td>
</tr>
<tr>
<td>nDIM</td>
<td>I</td>
<td>Dimming input / undervoltage protection</td>
<td>Connect a PWM signal for dimming as detailed in the PWM Dimming section and/or a resistor divider from V_IN to program undervoltage lockout (UVLO). Turnon threshold is 1.24 V and hysteresis for turnon is provided by a 23-µA current source.</td>
</tr>
<tr>
<td>FLT</td>
<td>I</td>
<td>Fault flag</td>
<td>Connect to pullup resistor from V_IN and N-channel MOSFET open-drain output is high when a fault condition is latched by the timer.</td>
</tr>
<tr>
<td>TIMR</td>
<td>I</td>
<td>Fault timer</td>
<td>Connect a capacitor to AGND to set the time delay before a sensed fault condition is latched.</td>
</tr>
<tr>
<td>LRDY</td>
<td>O</td>
<td>LED ready flag</td>
<td>Connect to pullup resistor from V_IN and N-channel MOSFET open-drain output pulls down when the LED current is not in regulation.</td>
</tr>
<tr>
<td>DPOL</td>
<td>I</td>
<td>Dim polarity</td>
<td>Connect to AGND if dimming with a series P-channel MOSFET or leave open when dimming with series N-channel MOSFET.</td>
</tr>
<tr>
<td>DDRV</td>
<td>O</td>
<td>Dim gate drive output</td>
<td>Connect to the gate of the dimming MOSFET.</td>
</tr>
<tr>
<td>PGND</td>
<td>GND</td>
<td>Power ground</td>
<td>Connect to AGND through the DAP copper pad to provide ground return for GATE and DDRV.</td>
</tr>
<tr>
<td>GATE</td>
<td>O</td>
<td>Main gate drive output</td>
<td>Connect to the gate of the main switching MOSFET.</td>
</tr>
<tr>
<td>V_CC</td>
<td>I</td>
<td>Internal regulator output</td>
<td>Bypass with 2.2-µF to 3.3-µF ceramic capacitor to PGND.</td>
</tr>
</tbody>
</table>
Pin Functions (continued)

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>IS</td>
<td>17</td>
<td>13</td>
<td>Main switch current sense</td>
</tr>
<tr>
<td>RPD</td>
<td>18</td>
<td>14</td>
<td>Resistor Pulldown</td>
</tr>
<tr>
<td>HSP</td>
<td>19</td>
<td>15</td>
<td>LED current sense positive</td>
</tr>
<tr>
<td>HSN</td>
<td>20</td>
<td>16</td>
<td>LED current sense negative</td>
</tr>
<tr>
<td>DAP</td>
<td>DAP (21)</td>
<td>DAP (17)</td>
<td>GND</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{IN}}, \text{EN}, \text{RPD}, \text{nDIM} )</td>
<td>(-0.3)</td>
<td>76</td>
</tr>
<tr>
<td></td>
<td>(-1) continuous</td>
<td>mA</td>
</tr>
<tr>
<td>( OVP, \text{HSP}, \text{HSN}, \text{LRDY}, \text{FLT}, \text{DPOL} )</td>
<td>(-0.3)</td>
<td>76</td>
</tr>
<tr>
<td></td>
<td>(-100) continuous</td>
<td>( \mu )A</td>
</tr>
<tr>
<td>( \text{RCT} )</td>
<td>(-0.3)</td>
<td>76</td>
</tr>
<tr>
<td></td>
<td>(-1) continuous</td>
<td>5 continuous</td>
</tr>
<tr>
<td>( \text{IS} )</td>
<td>(-0.3)</td>
<td>76</td>
</tr>
<tr>
<td></td>
<td>(-2) for 100 ns</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>(-1) continuous</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{\text{CC}} )</td>
<td>(-0.3)</td>
<td>8</td>
</tr>
<tr>
<td>( \text{TIMR} )</td>
<td>(-0.3)</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>(-100) continuous</td>
<td>100 continuous</td>
</tr>
<tr>
<td>( \text{COMP}, \text{CSH} )</td>
<td>(-0.3)</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>(-200) continuous</td>
<td>200 continuous</td>
</tr>
<tr>
<td>( \text{GATE}, \text{DDRVD} )</td>
<td>(-0.3)</td>
<td>( V_{\text{CC}} )</td>
</tr>
<tr>
<td></td>
<td>(-2.5) for 100 ns</td>
<td>( V_{\text{CC}}+2.5) for 100 ns</td>
</tr>
<tr>
<td></td>
<td>(-1) continuous</td>
<td>1 continuous</td>
</tr>
<tr>
<td>( \text{PGND} )</td>
<td>(-0.3)</td>
<td>0.3</td>
</tr>
<tr>
<td></td>
<td>(-2.5) for 100 ns</td>
<td>2.5 for 100 ns</td>
</tr>
<tr>
<td>Continuous power dissipation</td>
<td>Internally Limited</td>
<td></td>
</tr>
<tr>
<td>Maximum junction temperature</td>
<td>Internally Limited</td>
<td></td>
</tr>
<tr>
<td>Maximum lead temperature (solder and reflow) (^{(3)})</td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>(-65)</td>
<td>150</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

\(^{(3)}\) Refer to http://www.ti.com/packaging for more detailed information and mounting techniques.
6.2 ESD Ratings: LM3421, LM3423

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>VALUE (V)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3421, LM3423</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{(ESD)} ) Electrostatic discharge</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(^{(2)})</td>
<td>±500</td>
<td>V</td>
</tr>
<tr>
<td>LM3421-Q1, LM3423-Q1, LM3421-Q0, LM3423-Q0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{(ESD)} ) Electrostatic discharge</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Human body model (HBM), per AEC Q100-002(^{(3)})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM), per AEC Q100-011, All Pins</td>
<td>±750</td>
<td>V</td>
</tr>
<tr>
<td>Pin 4</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
\(^{(3)}\) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating junction temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>LM3421, LM3421Q1, LM3423, LM3423Q1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM3421Q0, LM3423Q0</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Input voltage ( V_{IN} )</td>
<td>4.5</td>
<td>75</td>
<td>V</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>( R_{\theta JA} ) Junction-to-ambient thermal resistance</th>
<th>( R_{\theta JC(top)} ) Junction-to-case (top) thermal resistance</th>
<th>( R_{\theta JB} ) Junction-to-board thermal resistance</th>
<th>( \psi_{JT} ) Junction-to-top characterization parameter</th>
<th>( \psi_{JB} ) Junction-to-board characterization parameter</th>
<th>( R_{\theta JC(bot)} ) Junction-to-case (bottom) thermal resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>38.9 ( ^{\circ} \mathrm{C/W} )</td>
<td>23.1 ( ^{\circ} \mathrm{C/W} )</td>
<td>16.8 ( ^{\circ} \mathrm{C/W} )</td>
<td>0.6 ( ^{\circ} \mathrm{C/W} )</td>
<td>16.6 ( ^{\circ} \mathrm{C/W} )</td>
<td>1.7 ( ^{\circ} \mathrm{C/W} )</td>
</tr>
<tr>
<td></td>
<td>36.7 ( ^{\circ} \mathrm{C/W} )</td>
<td>21.5 ( ^{\circ} \mathrm{C/W} )</td>
<td>18 ( ^{\circ} \mathrm{C/W} )</td>
<td>0.5 ( ^{\circ} \mathrm{C/W} )</td>
<td>17.8 ( ^{\circ} \mathrm{C/W} )</td>
<td>1.9 ( ^{\circ} \mathrm{C/W} )</td>
</tr>
<tr>
<td></td>
<td><strong>PWP (HTSSOP)</strong></td>
<td><strong>PWP (HTSSOP)</strong></td>
<td><strong>PWP (HTSSOP)</strong></td>
<td><strong>PWP (HTSSOP)</strong></td>
<td><strong>PWP (HTSSOP)</strong></td>
<td><strong>PWP (HTSSOP)</strong></td>
</tr>
<tr>
<td></td>
<td>16 PINS</td>
<td>20 PINS</td>
<td>16 PINS</td>
<td>20 PINS</td>
<td>16 PINS</td>
<td>20 PINS</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
6.5 Electrical Characteristics

MIN and MAX limits apply for $T_J = -40^\circ$C to 150$^\circ$C for LM3421Q0/LM3423Q0, $T_J = -40^\circ$C to 125$^\circ$C for all others, unless otherwise specified. Specifications that differ between the two operating ranges will be identified in the Temp Range column as Q0 for $T_J = -40^\circ$C to 150$^\circ$C and as Q1 for $T_J = -40^\circ$C to 125$^\circ$C. If no temperature range is indicated then the specification holds for both Q1 and Q0. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ$C, and are provided for reference purposes only. Unless otherwise stated the following condition applies: $V_{IN} = 14$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TEMP RANGE</th>
<th>MIN(1)</th>
<th>TYP(2)</th>
<th>MAX(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>START-UP REGULATOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CCREG}$ $V_{CC}$ Regulation</td>
<td>$I_{CC} = 0$ mA</td>
<td>6.3</td>
<td>6.9</td>
<td>7.35</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{CLIM}$ $V_{CC}$ Current Limit</td>
<td>$V_{CC} = 0$ V</td>
<td>20</td>
<td>25</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_Q$ Quiescent Current</td>
<td>$EN = 3$ V, Static</td>
<td>Q1</td>
<td>2</td>
<td>3</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$EN = 0$ V</td>
<td>Q0</td>
<td>2</td>
<td>3.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{SD}$ Shutdown Current</td>
<td></td>
<td>0.1</td>
<td>1</td>
<td></td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>VCC SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV}$ $V_{CC}$ UVLO Threshold</td>
<td>$V_{CC}$ Increasing</td>
<td>4.17</td>
<td>4.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{CC}$ Decreasing</td>
<td>3.7</td>
<td>4.08</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.1</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN THRESHOLDS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$EN_{ST}$ EN Start-up Threshold</td>
<td>EN Increasing</td>
<td>Q1</td>
<td>1.75</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN Decreasing</td>
<td>Q0</td>
<td>1.75</td>
<td>2.75</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$EN_{STHYS}$ EN Start-up Hysteresis</td>
<td>EN Increasing</td>
<td>0.8</td>
<td>1.63</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EN Decreasing</td>
<td>0.1</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{EN}$ EN Pulldown Resistance</td>
<td>EN = 1 V</td>
<td>Q1</td>
<td>0.45</td>
<td>0.82</td>
<td>1.3</td>
<td>$M\Omega$</td>
</tr>
<tr>
<td></td>
<td>Q0</td>
<td>0.45</td>
<td>0.82</td>
<td>1.8</td>
<td>$M\Omega$</td>
<td></td>
</tr>
<tr>
<td>CSH THRESHOLDS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CSH High Fault</td>
<td></td>
<td>1.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CSH Low Condition on LRDY Pin (LM3423)</td>
<td>CSH increasing</td>
<td>1</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OV THRESHOLDS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$OVP_{CB}$ OVP OVLO Threshold</td>
<td>OVP Increasing</td>
<td>1.185</td>
<td>1.24</td>
<td>1.285</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$OVP_{HYS}$ OVP Hysteresis Source Current</td>
<td>OVP Active (high)</td>
<td>Q1</td>
<td>20</td>
<td>23</td>
<td>25</td>
<td>$\mu$A</td>
</tr>
<tr>
<td></td>
<td>Q0</td>
<td>20</td>
<td>23</td>
<td>26</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>DPOL THRESHOLDS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$DPOL_{THRES}$ DPOL Logic Threshold</td>
<td>DPOL Increasing</td>
<td>2</td>
<td>2.3</td>
<td>2.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$R_{DPOL}$ DPOL Pullup Resistance</td>
<td></td>
<td>500</td>
<td>1200</td>
<td>$k\Omega$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FAULT TIMER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FLTTH}$ Fault Threshold</td>
<td></td>
<td>Q1</td>
<td>1.185</td>
<td>1.24</td>
<td>1.285</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Q0</td>
<td>1.185</td>
<td>1.24</td>
<td>1.29</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{FLT}$ Fault Pin Source Current</td>
<td>Q1</td>
<td>10</td>
<td>11.5</td>
<td>13</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Q0</td>
<td>10</td>
<td>11.5</td>
<td>13.5</td>
<td>$\mu$A</td>
<td></td>
</tr>
<tr>
<td>ERROR AMPLIFIER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{REF}$ CSH Reference Voltage</td>
<td>With Respect to AGND</td>
<td>1.21</td>
<td>1.235</td>
<td>1.26</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Error Amplifier Input Bias Current</td>
<td>MIN, MAX $= T_J = 25^\circ$C</td>
<td>$-0.6$</td>
<td>0</td>
<td>0.6</td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>

(1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

(2) Typical numbers are at 25$^\circ$C and represent the most likely norm.
Electrical Characteristics (continued)

MIN and MAX limits apply for $T_J = -40°C$ to 150°C for LM3421Q0/LM3423Q0, $T_J = -40°C$ to 125°C for all others, unless otherwise specified. Specifications that differ between the two operating ranges will be identified in the Temp Range column as Q0 for $T_J = -40°C$ to 150°C and as Q1 for $T_J = -40°C$ to 125°C. If no temperature range is indicated then the specification holds for both Q1 and Q0. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only. Unless otherwise stated the following condition applies: $V_{IN} = 14$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TEMP RANGE</th>
<th>MIN(1)</th>
<th>TYP(2)</th>
<th>MAX(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP Sink / Source Current</td>
<td>Q1</td>
<td>22</td>
<td>30</td>
<td>35</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Q0</td>
<td>22</td>
<td>30</td>
<td>36</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Transconductance</td>
<td>(3)</td>
<td>±125</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Linear Input Range</td>
<td>(3)</td>
<td>±125</td>
<td>mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transconductance Bandwidth</td>
<td>-6dB Unloaded Response</td>
<td>0.5</td>
<td>1</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**OFF TIMER**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Q1</th>
<th>Q0</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum OFF-time</td>
<td>$V_{IN} = 14$ V through 1 kΩ</td>
<td>35</td>
<td>35</td>
<td>ns</td>
</tr>
<tr>
<td>$R_{RCT}$</td>
<td>RCT Reset Pulldown Resistance</td>
<td>36</td>
<td>120</td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{RCT}$</td>
<td>$V_{IN}/25$ Reference Voltage</td>
<td>540</td>
<td>565</td>
<td>585</td>
</tr>
<tr>
<td>$f$</td>
<td>Continuous Conduction Switching Frequency</td>
<td>2.2 nF &gt; $C_T &gt; 470$ pF</td>
<td>$25/(C_T R_T)$</td>
<td>Hz</td>
</tr>
</tbody>
</table>

**PWM COMPARATOR**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Q1</th>
<th>Q0</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP to PWM Offset</td>
<td></td>
<td>700</td>
<td>800</td>
<td>900</td>
</tr>
</tbody>
</table>

**CURRENT LIMIT (IS)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Q1</th>
<th>Q0</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{LIM}$</td>
<td>Current Limit Threshold</td>
<td>215</td>
<td>245</td>
<td>275</td>
</tr>
<tr>
<td>$I_{LIM}$ Delay to Output</td>
<td></td>
<td>35</td>
<td>35</td>
<td>ns</td>
</tr>
<tr>
<td>Leading Edge Blanking Time</td>
<td></td>
<td>115</td>
<td>210</td>
<td>325</td>
</tr>
</tbody>
</table>

**HIGH SIDE TRANSCONDUCTANCE AMPLIFIER**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Q1</th>
<th>Q0</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Bias Current</td>
<td></td>
<td>11.5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Transconductance</td>
<td></td>
<td>20</td>
<td>119</td>
<td>mA/V</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td></td>
<td>−1.5</td>
<td>0</td>
<td>1.5</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td></td>
<td>−7</td>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td>Transconductance Bandwidth</td>
<td>$I_{CSH} = 100$ µA(3), $T_J = 25°C$</td>
<td>250</td>
<td>500</td>
<td>kHz</td>
</tr>
</tbody>
</table>

**GATE DRIVER (GATE)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>GATE = High</th>
<th>GATE = Low</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{SRC(GATE)}$</td>
<td>GATE Sourcing Resistance</td>
<td>2</td>
<td>6</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{SINK(GATE)}$</td>
<td>GATE Sinking Resistance</td>
<td>1.3</td>
<td>4.5</td>
<td>Ω</td>
</tr>
</tbody>
</table>

**DIM DRIVER (DIM, DDRV)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>DIM = High</th>
<th>DIM = Low</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$nDIM_{VTH}$</td>
<td>nDIM / UVLO Threshold</td>
<td>1.185</td>
<td>1.24</td>
<td>1.285</td>
</tr>
<tr>
<td>$nDIM_{HYS}$</td>
<td>nDIM Hysteresis Current</td>
<td>20</td>
<td>23</td>
<td>25</td>
</tr>
<tr>
<td>$R_{SRC(DDRV)}$</td>
<td>DDRV Sourcing Resistance</td>
<td>13.5</td>
<td>30</td>
<td>Ω</td>
</tr>
<tr>
<td>$R_{SINK(DDRV)}$</td>
<td>DDRV Sinking Resistance</td>
<td>3.5</td>
<td>10</td>
<td>Ω</td>
</tr>
</tbody>
</table>

**PULLDOWN N-CHANNEL MOSFETS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Q1</th>
<th>Q0</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{RPD}$</td>
<td>RPD Pulldown Resistance</td>
<td>145</td>
<td>300</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>145</td>
<td>350</td>
<td>Ω</td>
</tr>
</tbody>
</table>

(3) These electrical parameters are specified by design, and are not verified by test.

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Electrical Characteristics (continued)

MIN and MAX limits apply for $T_J = -40^\circ C$ to 150$^\circ C$ for LM3421Q0/LM3423Q0, $T_J = -40^\circ C$ to 125$^\circ C$ for all others, unless otherwise specified. Specifications that differ between the two operating ranges will be identified in the Temp Range column as Q0 for $T_J = -40^\circ C$ to 150$^\circ C$ and as Q1 for $T_J = -40^\circ C$ to 125$^\circ C$. If no temperature range is indicated then the specification holds for both Q1 and Q0. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ C$, and are provided for reference purposes only. Unless otherwise stated the following condition applies: $V_{IN} = 14\, V$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TEMP RANGE</th>
<th>MIN$^{(1)}$</th>
<th>TYP$^{(2)}$</th>
<th>MAX$^{(1)}$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{FLT}$</td>
<td>FLT Pulldown Resistance</td>
<td>Q1</td>
<td>145</td>
<td>300</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0</td>
<td>145</td>
<td>350</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$R_{LRDY}$</td>
<td>LRDY Pulldown Resistance</td>
<td>Q1</td>
<td>135</td>
<td>300</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0</td>
<td>135</td>
<td>350</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

THERMAL SHUTDOWN

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TEMP RANGE</th>
<th>MIN$^{(1)}$</th>
<th>MAX$^{(1)}$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{SD}$</td>
<td>Thermal Shutdown Threshold</td>
<td>Q1</td>
<td>165</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0</td>
<td>210</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{HY}$</td>
<td>Thermal Shutdown Hysteresis</td>
<td>Q1</td>
<td>25</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Q0</td>
<td>25</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Minimum and Maximum limits applicable for $T_J = -40^\circ C$ to 150$^\circ C$ for LM3421Q0/LM3423Q0, $T_J = -40^\circ C$ to 125$^\circ C$ for all others, unless otherwise specified.

(2) Typical values represent the most likely parametric norm at $T_J = 25^\circ C$.

(3) If no temperature range is indicated then the specification holds for both Q1 and Q0.
6.6 Typical Characteristics

\[ T_A = 25^\circ C \text{ and } V_{IN} = 14 \text{ V unless otherwise specified} \]

**Figure 1. Boost Efficiency vs. Input Voltage**

\[ V_O = 32 \text{V (9 LEDs)} \]

**Figure 2. Buck-Boost Efficiency vs. Input Voltage**

\[ V_O = 21 \text{V (6 LEDs)} \]

**Figure 3. Boost LED Current vs. Input Voltage**

\[ V_O = 21 \text{V (6 LEDs)} \]

**Figure 4. Buck-Boost LED Current vs. Input Voltage**

\[ V_O = 32 \text{V (9 LEDs)} \]

**Figure 5. Analog Dimming**

\[ V_O = 21 \text{V (6 LEDs); } V_{IN} = 24 \text{ V} \]

**Figure 6. PWM Dimming**

\[ V_O = 32 \text{V (9 LEDs); } V_{IN} = 24 \text{ V} \]
Typical Characteristics (continued)

\( T_A = 25°C \) and \( V_{\text{IN}} = 14 \text{ V} \) unless otherwise specified

**Figure 7.** \( V_{\text{CSH}} \) vs Junction Temperature

**Figure 8.** \( V_{\text{CC}} \) vs Junction Temperature

**Figure 9.** \( V_{\text{RCT}} \) vs Junction Temperature

**Figure 10.** \( V_{\text{LIM}} \) vs Junction Temperature

**Figure 11.** \( t_{\text{ON-MIN}} \) vs Junction Temperature
7 Detailed Description

7.1 Overview

The LM34xx-Q1 are N-channel MOSFET (NFET) controllers for buck, boost and buck-boost current regulators which are ideal for driving LED loads. The controller has wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency. The LM34xx-Q1 uses a Predictive Off-time (PRO) control architecture that allows the regulator to be operated using minimal external control loop compensation, while providing an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current and the output enable/disable function with external dimming FET driver allows for fast PWM dimming of the LED load. When designing, the maximum attainable LED current is not internally limited because the LM34xx-Q1 is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the LM34xx-Q1 to easily provide constant currents up to 5A. This controller contains all the features necessary to implement a high-efficiency versatile LED driver.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 Current Regulators

Current regulators can be designed to accomplish three basic functions: buck, boost, and buck-boost. All three topologies in their most basic form contain a main switching MOSFET, a recirculating diode, an inductor and capacitors. The LM34xx-Q1 is designed to drive a ground referenced NFET which is perfect for a standard boost regulator. Buck and buck-boost regulators, on the other hand, usually have a high-side switch. When driving an LED load, a ground referenced load is often not necessary, therefore a ground referenced switch can be used to drive a floating load instead. The LM34xx-Q1 can then be used to drive all three basic topologies as shown in the Basic Topology Schematics section. Other topologies such as the SEPIC and flyback converter (both derivatives of the buck-boost) can be implemented as well.

Looking at the buck-boost design, the basic operation of a current regulator can be analyzed. During the time that the NFET (Q1) is turned on (t_{ON}), the input voltage source stores energy in the inductor (L1) while the output capacitor (C_O) provides energy to the LED load. When Q1 is turned off (t_{OFF}), the re-circulating diode (D1) becomes forward biased and L1 provides energy to both C_O and the LED load. Figure 12 shows the inductor current (i_L(t)) waveform for a regulator operating in CCM.

The average output LED current (I_{LED}) is proportional to the average inductor current (i_L), therefore if i_L is tightly controlled, I_{LED} will be well regulated. As the system changes input voltage or output voltage, the ideal duty cycle (D) is varied to regulate i_L and ultimately I_{LED}. For any current regulator, D is a function of the conversion ratio:

**Buck**

\[
D = \frac{V_O}{V_{IN}} \quad (1)
\]

**Boost**

\[
D = \frac{V_O - V_{IN}}{V_O} \quad (2)
\]

**Buck-boost**

\[
D = \frac{V_O}{V_O + V_{IN}} \quad (3)
\]

7.3.2 Predictive Off-Time (PRO) Control

PRO control is used by the LM34xx-Q1 to control I_{LED}. It is a combination of average peak current control and a one-shot off-time that varies with input voltage. The LM34xx-Q1 uses peak current control to regulate the average LED current through an array of HBLEDs. This method of control uses a series resistor in the LED path to sense LED current and can use either a series resistor in the MOSFET path or the MOSFET R_{DS-ON} for both cycle-by-cycle current limit and input voltage feed forward. D is indirectly controlled by changes in both t_{OFF} and t_{ON}, which vary depending on the operating point.
Feature Description (continued)

Even though the off-time control is quasi-hysteretic, the input voltage proportionality in the off-timer creates an essentially constant switching frequency over the entire operating range for boost and buck-boost topologies. The buck topology can be designed to give constant ripple over either input voltage or output voltage, however switching frequency is only constant at a specific operating point.

This type of control minimizes the control loop compensation necessary in many switching regulators, simplifying the design process. The averaging mechanism in the peak detection control loop provides extremely accurate LED current regulation over the entire operating range.

PRO control was designed to mitigate “current mode instability” (also called “sub-harmonic oscillation”) found in standard peak current mode control when operating near or above 50% duty cycles. When using standard peak current mode control with a fixed switching frequency, this condition is present, regardless of the topology. However, using a constant off-time approach, current mode instability cannot occur, enabling easier design and control.

Predictive off-time advantages:
- There is no current mode instability at any duty cycle.
- Higher duty cycles / voltage transformation ratios are possible, especially in the boost regulator.

The only disadvantage is that synchronization to an external reference frequency is generally not available.

7.3.3 Average LED Current

The LM3421/23 uses an external current sense resistor (RSNS) placed in series with the LED load to convert the LED current (ILED) into a voltage (VSNS) as shown in Figure 13. The HSP and HSN pins are the inputs to the high-side sense amplifier which are forced to be equal potential (VHSP=VHSN) through negative feedback. Because of this, the VSNS voltage is forced across RHSP to generate the signal current (ICSH) which flows out of the CSH pin and through the RCSH resistor. The error amplifier will regulate the CSH pin to 1.24 V, therefore ICSH can be calculated using Equation 4.

\[
I_{CSH} = \frac{V_{SNS}}{R_{HSP}}
\] (4)

This means VSNS will be regulated as follows:

\[
V_{SNS} = 1.24V \times \frac{R_{HSP}}{R_{CSH}}
\] (5)

ILED can then be calculated using Equation 6.
Feature Description (continued)

\[ I_{LED} = \frac{V_{SNS}}{R_{SNS}} = \frac{1.24V}{R_{SNS}} \times \frac{R_{HSP}}{R_{CSH}} \]  

(6)

The selection of the three resistors (\(R_{SNS}\), \(R_{CSH}\), and \(R_{HSP}\)) is not arbitrary. For matching and noise performance, the suggested signal current \(I_{CSH}\) is approximately 100 µA. This current does not flow in the LEDs and will not affect either the off-state LED current or the regulated LED current. \(I_{CSH}\) can be above or below this value, but the high-side amplifier offset characteristics may be affected slightly. In addition, to minimize the effect of the high-side amplifier voltage offset on LED current accuracy, the minimum \(V_{SNS}\) is suggested to be 50 mV. Finally, a resistor (\(R_{HSN} = R_{HSP}\)) should be placed in series with the HSN pin to cancel out the effects of the input bias current (approximately 10 µA) of both inputs of the high-side sense amplifier.

The sense resistor (\(R_{SNS}\)) can be placed anywhere in the series string of LEDs as long as the voltage at the HSN and HSP pins (\(V_{HSP}\) and \(V_{HSN}\)) satisfies the following conditions:

\[ V_{HSP} < 76V \]
\[ V_{HSN} > 3.5V \]  

(7)

Typically, for a buck-boost configuration, \(R_{SNS}\) is placed at the bottom of the string (LED-) which allows for greater flexibility of input and output voltage. However, if there is substantial input voltage ripple allowed, it can help to place \(R_{SNS}\) at the top of the string (LED+) which limits the output voltage of the string to:

\[ V_O = 76V - V_{IN} \]  

(8)

The CSH pin can also be used as a low-side current sense input regulated to 1.24 V. The high-side sense amplifier is disabled if HSP and HSN are tied to AGND (or \(V_{HSN} > V_{HSP}\)).

7.3.4 Analog Dimming

The CSH pin can be used to analog dim the LED current by adjusting the current sense voltage (\(V_{SNS}\)). There are several different methods to adjust \(V_{SNS}\) using the CSH pin:

1. External variable resistance: Adjust a potentiometer placed in series with \(R_{CSH}\) to vary \(V_{SNS}\).
2. External variable current source: Source current (0 µA to \(I_{CSH}\)) into the CSH pin to adjust \(V_{SNS}\).

![Variabile Current Source](https://www.ti.com/lit/ds/symlink/lm3421-q1.pdf)

**Figure 14. Analog Dimming Circuitry**

In general, analog dimming applications require a lower switching frequency to minimize the effect of the leading edge blanking circuit. As the LED current is reduced, the output voltage and the duty cycle decreases. Eventually, the minimum on-time is reached. The lower the switching frequency, the wider the linear dimming range. Figure 14 shows how both CSH methods are physically implemented.

Method 1 uses an external potentiometer in the CSH path which is a simple addition to the existing circuitry. However, the LEDs cannot dim completely because there is always some resistance causing signal current to flow. This method is also susceptible to noise coupling at the CSH pin because the potentiometer increases the size of the signal current loop.
Feature Description (continued)

Method 2 provides a complete dimming range and better noise performance, though it is more complex. It consists of a PNP current mirror and a bias network consisting of an NPN, 2 resistors and a potentiometer (R_{ADJ}), where R_{ADJ} controls the amount of current sourced into the CSH pin. A higher resistance value will source more current into the CSH pin causing less regulated signal current through R_{HSP}, effectively dimming the LEDs. V_{REF} should be a precise external voltage reference, while Q7 and Q8 should be a dual pair PNP for best matching and performance. The additional current (I_{ADD}) sourced into the CSH pin can be calculated using Equation 9.

\[
I_{ADD} = \frac{R_{ADJ} \times V_{REF}}{R_{ADJ} + R_{MAX}} - V_{BE-Q6} - \frac{R_{BIAS}}{R_{BIAS}}
\]

The corresponding I_{LED} for a specific I_{ADD} is:

\[
I_{LED} = (I_{CSH} - I_{ADD}) \times \left(\frac{R_{HSP}}{R_{SNS}}\right)
\]

7.3.5 Current Sense and Current Limit

The LM34xx-Q1 achieves peak current mode control using a comparator that monitors the main MOSFET (Q1) transistor current, comparing it with the COMP pin voltage as shown in Figure 15. Further, it incorporates a cycle-by-cycle overcurrent protection function. Current limit is accomplished by a redundant internal current sense comparator. If the voltage at the current sense comparator input (IS) exceeds 245 mV (typical), the on cycle is immediately terminated. The IS input pin has an internal N-channel MOSFET which pulls it down at the conclusion of every cycle. The discharge device remains on an additional 210 ns (typical) after the beginning of a new cycle to blank the leading edge spike on the current sense signal. The leading edge blanking (LEB) determines the minimum achievable on-time (t_{ON-MIN}).

![Figure 15. Current Sense / Current Limit Circuitry](image)

There are two possible methods to sense the transistor current. The R_{DS-ON} of the main power MOSFET can be used as the current sense resistance because the IS pin was designed to withstand the high voltages present on the drain when the MOSFET is in the off state. Alternatively, a sense resistor located in the source of the MOSFET may be used for current sensing; however, TI suggests a low inductance (ESL) type. The cycle-by-cycle current limit (I_{LIM}) can be calculated using either method as the limiting resistance (R_{LIM}):

\[
I_{LIM} = \frac{245 \text{ mV}}{R_{LIM}}
\]
Feature Description (continued)

7.3.6 Overcurrent Protection

The LM34xx-Q1 devices have a secondary method of overcurrent protection. Switching action is disabled whenever the current in the LEDs is more than 30% above the regulation set point. The dimming MOSFET switch driver (DDRV) is not disabled however as this would immediately remove the fault condition and cause oscillatory behavior.

7.3.7 Zero Current Shutdown

The LM34xx-Q1 devices implement zero current shutdown through the EN and RPD pins. When pulled low, the EN pin places the devices into near-zero current state, where only the leakage currents will be observed at the pins (typical 0.1 µA). The applications circuits frequently have resistor dividers to set UVLO, OVLO, or other similar functions. The RPD pin is an open-drain N-channel MOSFET that is enabled only when the device is enabled. Tying the bottom of all resistor dividers to the RPD pin as shown in Figure 16 allows them to float during shutdown, thus removing their current paths and providing true application-wide zero current shutdown.

![Zero Current Shutdown Circuit](image)

Figure 16. Zero Current Shutdown Circuit

7.3.8 Control Loop Compensation

The LM34xx-Q1 control loop is modeled like any current mode controller. Using a first order approximation, the uncompensated loop can be modeled as a single pole created by the output capacitor and, in the boost and buck-boost topologies, a right half plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance. There is also a high-frequency pole in the model; however, it is near the switching frequency and plays no part in the compensation design process. Therefore, it will be neglected. Because ceramic capacitance is recommended for use with LED drivers, due to long lifetimes and high ripple current rating, the ESR of the output capacitor can also be neglected in the loop analysis. Finally, there is a DC gain of the uncompensated loop which is dependent on internal controller gains and the external sensing network.

A buck-boost regulator will be used as an example case.

Use Equation 12 to calculate the uncompensated loop gain for a buck-boost regulator.

\[
T_u = T_{uo} \times \frac{1 - \frac{S}{\omega_{z1}}}{1 + \frac{S}{\omega_{p1}}} \tag{12}
\]

Where the uncompensated DC loop gain of the system is calculated using Equation 13.

\[
T_{uo} = \frac{D' \times 500V \times R_{CSN} \times R_{OVS}}{(1+D) \times I_{LED} \times R_{LM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LM}} \tag{13}
\]

And the output pole \((\omega_{p1})\) is approximated using Equation 14.

\[
\omega_{p1} = \frac{1+D}{r_D \times C_D} \tag{14}
\]
Feature Description (continued)

And the right half plane zero \( (\omega_{Z_1}) \) is:

\[
\omega_{Z_1} = \frac{r_D x D}{D x L_1}
\]

Figure 17. Uncompensated Loop Gain Frequency Response

Figure 17 shows the uncompensated loop gain in a worst-case scenario when the RHP zero is below the output pole. This occurs at high duty cycles when the regulator is trying to boost the output voltage significantly. The RHP zero adds 20dB/decade of gain while losing 45°/decade of phase, which places the crossover frequency (when the gain is zero dB) extremely high because the gain only starts falling again due to the high-frequency pole (not shown in Figure 17). The phase will be below \(-180^\circ\) at the crossover frequency, which means there is no phase margin \((180^\circ + \text{phase at crossover frequency})\) causing system instability. Even if the output pole is below the RHP zero, the phase will still reach \(-180^\circ\) before the crossover frequency in most cases yielding instability.

Figure 18. Compensation Circuitry
Feature Description (continued)

To mitigate this problem, a compensator should be designed to give adequate phase margin (above 45°) at the crossover frequency. A simple compensator using a single capacitor at the COMP pin (C\text{CMP}) will add a dominant pole to the system, which will ensure adequate phase margin if placed low enough. At high duty cycles (as shown in Figure 17), the RHP zero places extreme limits on the achievable bandwidth with this type of compensation. However, because an LED driver is essentially free of output transients (except catastrophic failures open or short), the dominant pole approach, even with reduced bandwidth, is usually the best approach. The dominant compensation pole (ω\text{P2}) is determined by C\text{CMP} and the output resistance (R\text{O}) of the error amplifier (typically 5 MΩ) as demonstrated in Equation 16.

\[
\omega_{\text{P2}} = \frac{1}{5 \times 10^6 \times C_{\text{CMP}}}
\]

It may also be necessary to add one final pole at least one decade above the crossover frequency to attenuate switching noise and, in some cases, provide better gain margin. This pole can be placed across R\text{SNS} to filter the ESL of the sense resistor at the same time. Figure 18 shows how the compensation is physically implemented in the system.

The high-frequency pole (ω\text{P3}) can be calculated using Equation 17.

\[
\omega_{\text{P3}} = \frac{1}{R_{\text{FS}} \times C_{\text{FS}}}
\]

The total system transfer function becomes:

\[
T = T_{\text{U0}} \times \left( \frac{1 - S}{\omega_{\text{P2}}} \right) \times \left( \frac{1}{1 + S/\omega_{\text{P1}}} \right) \times \left( \frac{1}{1 + S/\omega_{\text{P3}}} \right)
\]

The resulting compensated loop gain frequency response shown in Figure 19 indicates that the system has adequate phase margin (above 45°) if the dominant compensation pole is placed low enough, ensuring stability.

7.3.9 Start-Up Regulator

The LM34xx-Q1 includes a high voltage, low dropout bias regulator. When power is applied, the regulator is enabled and sources current into an external capacitor (C\text{BYP}) connected to the V\text{CC} pin. The recommended bypass capacitance for the V\text{CC} regulator is 2.2 µF to 3.3 µF. The output of the V\text{CC} regulator is monitored by an internal UVLO circuit that protects the device from attempting to operate with insufficient supply voltage and the supply is also internally current limited. Figure 20 shows the typical start-up waveforms for the LM34xx-Q1.
Feature Description (continued)

![Start-Up Waveforms](image.png)

**Figure 20. Start-Up Waveforms**

First, C\textsubscript{BYP} is charged to be above \( V_{CC} \) UVLO threshold (approximately 4.2 V). The \( C_{VCC} \) charging time \( t_{VCC} \) can be estimated using Equation 19.

\[
t_{VCC} = \frac{4.2V}{25 \text{ mA}} \times C_{BYP} = 168\Omega \times C_{BYP}
\]

(19)

\( C_{CMP} \) is then charged to 0.9 V over the charging time \( t_{CMP} \), which can be estimated using Equation 20.

\[
t_{CMP} = \frac{0.9V}{25 \mu A} \times C_{CMP} = 36k\Omega \times C_{CMP}
\]

(20)

Once \( C_{CMP} = 0.9 \text{ V} \), the part starts switching to charge \( C_{O} \) until the LED current is in regulation. The \( C_{O} \) charging time \( t_{CO} \) can be roughly estimated using Equation 21.

\[
t_{CO} = C_{O} \times \frac{V_{O}}{I_{LED}}
\]

(21)

The system start-up time \( t_{SU} \) is defined using Equation 22.

\[
t_{SU} = t_{VCC} + t_{CMP} + t_{CO}
\]

(22)

In some configurations, the start-up waveform will overshoot the steady state COMP pin voltage. In this case, the LED current and output voltage will overshoot also, which can trip the overvoltage or protection, causing a race condition. The easiest way to prevent this is to use a larger compensation capacitor \( C_{CMP} \), thereby slowing down the control loop.

### 7.3.10 Overvoltage Lockout (OVLO)

The LM34xx-Q1 can be configured to detect an output (or input) overvoltage condition through the OVP pin. The pin features a precision 1.24-V threshold with 23 µA (typical) of hysteresis current as shown in Figure 21. When the OVLO threshold is exceeded, the GATE pin is immediately pulled low and a 23-µA current source provides hysteresis to the lower threshold of the OVLO hysteretic band.

If the LEDs are referenced to a potential other than ground (floating), as in the buck-boost and buck configuration, the output voltage \( V_{O} \) should be sensed and translated to ground by using a single PNP as shown in Figure 22.

The overvoltage turnoff threshold \( V_{TURN-OFF} \) is defined:

**Ground Referenced**

\[
V_{TURN-OFF} = 1.24V \times \left( \frac{R_{OV1} + R_{OV2}}{R_{OV1}} \right)
\]

(23)

**Floating**

\[
V_{TURN-OFF} = 1.24V \times \left( 0.5 \times \frac{R_{OV1} + R_{OV2}}{R_{OV1}} \right)
\]

(24)
Feature Description (continued)

In the ground referenced configuration, the voltage across $R_{OV2}$ is $V_O - 1.24$ V whereas in the floating configuration it is $V_O - 620$ mV where $620$ mV approximates $V_{BE}$ of the PNP.

The overvoltage hysteresis ($V_{HYSO}$) is defined using Equation 25.

$$V_{HYSO} = 23 \mu A \times R_{OV2}$$  
(25)

![Figure 21. Overvoltage Protection Circuitry](image1)

![Figure 22. Floating Output OVP Circuitry](image2)

The OVLO feature can cause some interesting results if the OVLO trip-point is set too close to $V_O$. At turnon, the converter has a modest amount of voltage overshoot before the control loop gains control of $I_{LED}$. If the overshoot exceeds the OVLO threshold, the controller shuts down, opening the dimming MOSFET. This isolates the LED load from the converter and the output capacitance. The voltage will then discharge very slowly through the HSP and HSN pins until $V_O$ drops below the lower threshold, where the process repeats. This looks like the LEDs are blinking at around 2 Hz. This mode can be escaped if the input voltage is reduced.

7.3.11 Input Undervoltage Lockout (UVLO)

The nDIM pin is a dual-function input that features an accurate 1.24-V threshold with programmable hysteresis as shown in Figure 23. This pin functions as both the PWM dimming input for the LEDs and as a $V_{IN}$ UVLO. When the pin voltage rises and exceeds the 1.24-V threshold, 23 $\mu A$ (typical) of current is driven out of the nDIM pin into the resistor divider providing programmable hysteresis.
Feature Description (continued)

When using the nDIM pin for UVLO and PWM dimming concurrently, the UVLO circuit can have an extra series resistor to set the hysteresis. This allows the standard resistor divider to have smaller resistor values minimizing PWM delays due to a pulldown MOSFET at the nDIM pin (see PWM Dimming section). In general, at least 3 V of hysteresis is preferable when PWM dimming, if operating near the UVLO threshold.

The turnon threshold ($V_{\text{TURN-ON}}$) is defined using Equation 26.

$$V_{\text{TURN-ON}} = 1.24V \times \frac{R_{\text{UV1}} + R_{\text{UV2}}}{R_{\text{UV1}}}$$  \hspace{1cm} (26)

The hysteresis ($V_{\text{HYS}}$) is defined as follows:

7.3.11.1 UVLO Only

$$V_{\text{HYS}} = 23 \mu A \times R_{\text{UV2}}$$  \hspace{1cm} (27)

7.3.11.2 PWM Dimming and UVLO

$$V_{\text{HYS}} = 23 \mu A \times \frac{R_{\text{UV2}} x (R_{\text{UV1}} + R_{\text{UV2}})}{R_{\text{UV1}}}$$  \hspace{1cm} (28)

When zero current shutdown and UVLO are implemented together, the EN pin can be used to escape UVLO. The nDIM pin will pull up to $V_{\text{IN}}$ when EN is pulled low; therefore, if $V_{\text{IN}}$ is within the UVLO hysteretic window when EN is pulled high again, the controller will start-up even though $V_{\text{TURN-ON}}$ is not exceeded.

7.3.12 PWM Dimming

The active low nDIM pin can be driven with a PWM signal which controls the main NFET and the dimming FET (dimFET). The brightness of the LEDs can be varied by modulating the duty cycle of this signal. LED brightness is approximately proportional to the PWM signal duty cycle, (that is, 30% duty cycle equals approximately 30% LED brightness). This function can be ignored if PWM dimming is not required by using nDIM solely as a $V_{\text{IN}}$ UVLO input as described in Input Undervoltage Lockout (UVLO) or by tying it directly to $V_{\text{CC}}$ or $V_{\text{IN}}$. 

Figure 23. UVLO Circuit
Feature Description (continued)

**Figure 24. PWM Dimming Circuit**

Figure 24 shows how the PWM signal is applied to nDIM:

1. Connect the dimming MOSFET \( Q_{\text{DIM}} \) with the drain to the nDIM pin and the source to AGND. Apply an external logic-level PWM signal to the gate of \( Q_{\text{DIM}} \).

2. Connect the anode of a Schottky diode \( D_{\text{DIM}} \) to the nDIM pin. Apply an inverted external logic-level PWM signal to the cathode of the same diode.

The DDRV pin is a PWM output that follows the nDIM PWM input signal. When the nDIM pin rises, the DDRV pin rises and the PWM latch reset signal is removed allowing the main MOSFET Q1 to turn on at the beginning of the next clock set pulse. In boost and buck-boost topologies, the DDRV pin is used to control a N-channel MOSFET placed in series with the LED load, while it would control a P-channel MOSFET in parallel with the load for a buck topology.

The series dimFET will open the LED load, when nDIM is low, effectively speeding up the rise and fall times of the LED current. Without any dimFET, the rise and fall times are limited by the inductor slew rate and dimming frequencies above 1 kHz are impractical. Using the series dimFET, dimming frequencies up to 30 kHz are achievable. With a parallel dimFET (buck topology), even higher dimming frequencies are achievable.

When using the PWM functionality in a boost regulator, the PWM signal can drive a ground referenced FET. However, with buck-boost and buck topologies, level shifting circuitry is necessary to translate the PWM dim signal to the floating dimFET as shown in Figure 25 and Figure 26. If high side dimming is necessary in a boost regulator using the LM3423, level shifting can be added providing the polarity inverting DPOL pin is pulled low (see LM3423 Only: DPOL, FLT, TIMR, and LRDY section) as shown in Figure 27.

When using a series dimFET to PWM dim the LED current, more output capacitance is always better. A general rule of thumb is to use a minimum of 40 µF when PWM dimming. For most applications, this will provide adequate energy storage at the output when the dimFET turns off and opens the LED load. Then when the dimFET is turned back on, the capacitance helps source current into the load, improving the LED current rise time.

A minimum on-time must be maintained in order for PWM dimming to operate in the linear region of its transfer function. Because the controller is disabled during dimming, the PWM pulse must be long enough such that the energy intercepted from the input is greater than or equal to the energy being put into the LEDs. For boost and buck-boost regulators, the minimum dimming pulse length in seconds \( t_{\text{PULSE}} \) is:

\[
 t_{\text{PULSE}} = \frac{2 \times I_{\text{LED}} \times V_{\text{O}} \times L1}{V_{\text{IN}}^2}
\]  

(29)

Even maintaining a dimming pulse greater than \( t_{\text{PULSE}} \), preserving linearity at low dimming duty cycles is difficult.
Feature Description (continued)

The second helpful modification is to remove the $C_{FS}$ capacitor and $R_{FS}$ resistor, eliminating the high-frequency compensation pole. This should not affect stability, but it will speed up the response of the CSH pin, specifically at the rising edge of the LED current when PWM dimming, thus improving the achievable linearity at low dimming duty cycles.

![Figure 25. Buck-boost Level-Shifted PWM Circuit](image1)

![Figure 26. Buck Level-Shifted PWM Circuit](image2)

![Figure 27. Boost Level-Shifted PWM Circuit](image3)
Feature Description (continued)

7.3.13 LM3423 Only: DPOL, FLT, TIMR, and LRDY

The LM3423 has four additional pins: DPOL, FLT, TIMR, and LRDY. The DPOL pin is simply used to invert the DDRV polarity. If DPOL is left open, then it is internally pulled high and the polarity is correct for driving a series N-channel dimFET. If DPOL is pulled low then the polarity is correct for using a series P-channel dimFET in high-side dimming applications. For a parallel P-channel dimFET, as used in the buck topology, leave DPOL open for proper polarity.

Among the LM3423’s other additional pins are TIMR and FLT which can be used in conjunction with an input disconnect MOSFET switch as shown in Figure 28 to protect the module from various fault conditions.

A fault is detected and an 11.5 µA (typical) current is sourced from the TIMR pin whenever any of the following conditions exist:
1. LED current is above regulation by more than 30%.
2. OVLO has engaged.
3. Thermal shutdown has engaged.

An external capacitor \( (C_{\text{TMR}}) \) from TIMR to AGND programs the fault filter time as follows:

\[
C_{\text{TMR}} = \frac{t_{\text{FLT}} \times 11.5 \mu A}{1.24 V}
\]  

(30)

When the voltage on the TIMR pin reaches 1.24 V, the device is latched off and the N-channel MOSFET open-drain FLT pin transitions to a high impedance state. The TIMR pin will be immediately pulled to ground (reset) if the fault condition is removed at any point during the filter period. Otherwise, if the timer expires, the fault will remain latched until one of three things occurs:
1. The EN pin is pulled low long enough for the \( V_{\text{CC}} \) pin to drop below 4.1 V (approximately 200 ms).
2. The TIMR pin is pulled to ground.
3. A complete power cycle occurs.

When using the EN and OVP pins in conjunction with the RPD pulldown pin, a race condition exists when exiting the disabled (EN low) state. When disabled, the OVP pin is pulled up to the output voltage because the RPD pulldown is disabled, and this will appear to be a real OVLO condition. The timer pin will immediately rise and latch the controller to the fault state. To protect against this behavior, a minimum timer capacitor \( (C_{\text{TMR}} = 220 \text{ pF}) \) should be used. If fault latching is not required, short the TMR pin to AGND, which will disable the FLT flag function.

The LM3423 also includes an LED Ready (LRDY) flag to notify the system that the LEDs are in proper regulation. The N-channel MOSFET open-drain LRDY pin is pulled low whenever any of the following conditions are met:
1. \( V_{\text{CC}} \) UVLO has engaged.
2. LED current is below regulation by more than 20%.
3. LED current is above regulation by more than 30%.
4. Overvoltage protection has engaged
5. Thermal shutdown has engaged.
6. A fault has latched the device off.

The LRDY pin is pulled low during start-up of the device and remains low until the LED current is in regulation.
Feature Description (continued)

Figure 28. Fault Detection and LED Status Circuit
8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Inductor

The inductor (L1) is the main energy storage device in a switching regulator. Depending on the topology, energy is stored in the inductor and transferred to the load in different ways (as an example, buck-boost operation is detailed in the Current Regulators section). The size of the inductor, the voltage across it, and the length of the switching subinterval (\(t_{ON}\) or \(t_{OFF}\)) determines the inductor current ripple (\(\Delta i_{L-PP}\)). In the design process, \(L1\) is chosen to provide a desired \(\Delta i_{L-PP}\). For a buck regulator the inductor has a direct connection to the load, which is good for a current regulator. This requires little to no output capacitance therefore \(\Delta i_{L-PP}\) is basically equal to the LED ripple current \(\Delta i_{LED-PP}\). However, for boost and buck-boost regulators, there is always an output capacitor which reduces \(\Delta i_{LED-PP}\); therefore, the inductor ripple can be larger than in the buck regulator case where output capacitance is minimal or completely absent.

In general, \(\Delta i_{LED-PP}\) is recommended by manufacturers to be less than 40% of the average LED current (\(I_{LED}\)). Therefore, for the buck regulator with no output capacitance, \(\Delta i_{L-PP}\) should also be less than 40% of \(I_{LED}\). For the boost and buck-boost topologies, \(\Delta i_{L-PP}\) can be much higher depending on the output capacitance value. However, \(\Delta i_{L-PP}\) is suggested to be less than 100% of the average inductor current (\(I_L\)) to limit the RMS inductor current.

\(L1\) is also suggested to have an RMS current rating at least 25% higher than the calculated minimum allowable RMS inductor current (\(I_{L-RMS}\)).

8.1.2 LED Dynamic Resistance

When the load is a string of LEDs, the output load resistance is the LED string dynamic resistance plus \(R_{SNS}\). LEDs are PN junction diodes, and their dynamic resistance shifts as their forward current changes. Dividing the forward voltage of a single LED (\(V_{LED}\)) by the forward current (\(I_{LED}\)) leads to an incorrect calculation of the dynamic resistance of a single LED (\(r_{LED}\)). The result can be 5 to 10 times higher than the true \(r_{LED}\) value.

![Figure 29. Dynamic Resistance](image)

Obtaining \(r_{LED}\) is accomplished by referring to the manufacturer’s LED I-V characteristic. It can be calculated as the slope at the nominal operating point as shown in Figure 29. For any application with more than 2 series LEDs, \(R_{SNS}\) can be neglected allowing \(r_D\) to be approximated as the number of LEDs multiplied by \(r_{LED}\).
Application Information (continued)

8.1.3 Output Capacitor

For boost and buck-boost regulators, the output capacitor (C\textsubscript{O}) provides energy to the load when the recirculating diode (D\textsubscript{1}) is reverse biased during the first switching subinterval. An output capacitor in a buck topology will simply reduce the LED current ripple (\Delta i_{LED-PP}) below the inductor current ripple (\Delta i_{L-PP}). In all cases, C\textsubscript{O} is sized to provide a desired \Delta i_{LED-PP}. As mentioned in the Inductor section, \Delta i_{LED-PP} is recommended by manufacturers to be less than 40% of the average LED current (i_{LED}).

C\textsubscript{O} should be carefully chosen to account for derating due to temperature and operating voltage. It must also have the necessary RMS current rating. Ceramic capacitors are the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

8.1.4 Input Capacitors

The input capacitance (C\textsubscript{IN}) provides energy during the discontinuous portions of the switching period. For buck and buck-boost regulators, C\textsubscript{IN} provides energy during t\textsubscript{ON} and during t\textsubscript{OFF}, the input voltage source charges up C\textsubscript{IN} with the average input current (I\textsubscript{IN}). For boost regulators, C\textsubscript{IN} only needs to provide the ripple current due to the direct connection to the inductor. C\textsubscript{IN} is selected given the maximum input voltage ripple (\Delta v_{IN-PP}) which can be tolerated. \Delta v_{IN-PP} is suggested to be less than 10% of the input voltage (V\textsubscript{IN}).

An input capacitance at least 100% greater than the calculated C\textsubscript{IN} value is recommended to account for derating due to temperature and operating voltage. When PWM dimming, even more capacitance can be helpful to minimize the large current draw from the input voltage source during the rising transition of the LED current waveform.

The chosen input capacitors must also have the necessary RMS current rating. Ceramic capacitors are again the best choice due to their high ripple current rating, long lifetime, and good temperature performance. An X7R dielectric rating is suggested.

For most applications, TI recommends bypassing the V\textsubscript{IN} pin with an 0.1 µF ceramic capacitor placed as close as possible to the pin. In situations where the bulk input capacitance may be far from the LM34xx-Q1 device, a 10-Ω series resistor can be placed between the bulk input capacitance and the bypass capacitor, creating a 150-kHz filter to eliminate undesired high-frequency noise.

8.1.5 Main MOSFET / Dimming MOSFET

The LM34xx-Q1 requires an external NFET (Q1) as the main power MOSFET for the switching regulator. TI recommends Q1 have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node. In practice, all switching regulators have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. TI recommends the current rating be at least 10% higher than the average transistor current. The power rating is then verified by calculating the power loss given the RMS transistor current and the NFET on-resistance (R\textsubscript{DS-ON}).

When PWM dimming, the LM34xx-Q1 requires another MOSFET (Q2) placed in series (or parallel for a buck regulator) with the LED load. This MOSFET should have a voltage rating greater than the output voltage (V\textsubscript{O}) and a current rating at least 10% higher than the nominal LED current (i_{LED}). The power rating is simply R\textsubscript{DS-ON} multiplied by i_{LED}, assuming 100% dimming duty cycle (continuous operation) will occur.

In general, the NFETs should be chosen to minimize total gate charge (Q\textsubscript{g}) when f\textsubscript{SW} is high and minimize R\textsubscript{DS-ON} otherwise. This will minimize the dominant power losses in the system. Frequently, higher current NFETs in larger packages are chosen for better thermal performance.

8.1.6 Re-Circulating Diode

A recirculating diode (D\textsubscript{1}) is required to carry the inductor current during t\textsubscript{OFF}. The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, TI recommends D1 have a voltage rating at least 15% higher than the maximum transistor voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current. The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage from the I-V curve on the product data sheet and multiplying by the average diode current. In general, higher current diodes have a lower forward voltage and come in better performing packages minimizing both power losses and temperature rise.
Application Information (continued)

8.1.7 Boost Inrush Current

When configured as a boost converter, there is a phantom power path comprised of the inductor, the output diode, and the output capacitor. This path will cause two things to happen when power is applied. First, there will be a very large inrush of current to charge the output capacitor. Second, the energy stored in the inductor during this inrush will end up in the output capacitor, charging it to a higher potential than the input voltage.

Depending on the state of the EN pin, the output capacitor would be discharged by:

1. EN < 1.3 V: no discharge path (leakage only).
2. EN > 1.3 V, the OVP divider resistor path, if present, and 10 µA into each of the HSP & HSN pins.

In applications using the OVP divider and with EN > 1.3 V, the output capacitor voltage can charge higher than V_{TURN-OFF}. In this situation, the FLT pin (LM3423 only) is open and the PWM dimming MOSFET is turned off. This condition (the system appearing disabled) can persist for an undesirably long time. Possible solutions to this condition are:

- Add an inrush diode from V_{IN} to the output as shown in Figure 30.
- Add an NTC thermistor in series with the input to prevent the inrush from overcharging the output capacitor too high.
- Use a current limited source supply.
- Raise the OVP threshold.

![Figure 30. Boost Topology with Inrush Diode](image)

8.1.8 Switching Frequency

An external resistor (R_T) connected between the RCT pin and the switch node (where D1, Q1, and L1 connect), in combination with a capacitor (C_T) between the RCT and AGND pins, sets the off-time (t_{OFF}) as shown in Figure 31. For boost and buck-boost topologies, the V_{IN} proportionality ensures a virtually constant switching frequency (f_{SW}).

For a buck topology, R_T and C_T are also used to set t_{OFF}, however the V_{IN} proportionality will not ensure a constant switching frequency. Instead, constant ripple operation can be achieved. Changing the connection of R_T in Figure 31 from V_{SW} to V_{IN} will provide a constant ripple over varying V_{IN}. Adding a PNP transistor as shown in Figure 32 will provide constant ripple over varying V_{O}.

The switching frequency is defined:

**Buck (Constant Ripple vs. V_{IN})**

\[
f_{SW} = \frac{25 \times (V_{IN} \cdot V_O)}{R_T \times C_T \times V_{IN}}
\]

\[\text{(31)}\]

**Buck (Constant Ripple vs. V_{O})**

\[
f_{SW} = \frac{25 \times (V_{IN} \times V_O^2 - V_O^2)}{R_T \times C_T \times V_{IN}^2}
\]

\[\text{(32)}\]

Boost and Buck-boost
Application Information (continued)

\[
 f_{SW} = \frac{25}{R_T \times C_T}
\]

(33)

For all topologies, the \( C_T \) capacitor is recommended to be 1 nF and should be located very close to the LM34xx-Q1.

---

**Figure 31. Off-timer Circuitry for Boost and Buck-boost Regulators**

**Figure 32. Off-timer Circuitry for Buck Regulators**
8.2 Typical Applications

8.2.1 Basic Topology Schematics

Figure 33. Boost Regulator ($V_{IN} < V_{O}$)
Typical Applications (continued)

Figure 34. Buck Regulator (V_{IN} > V_{O})
Typical Applications (continued)

Figure 35. Buck-Boost Regulator
Typical Applications (continued)

8.2.1.1 Design Requirements

Number of series LEDs: N
Single LED forward voltage: \( V_{\text{LED}} \)
Single LED dynamic resistance: \( r_{\text{LED}} \)
Nominal input voltage: \( V_{\text{IN}} \)
Input voltage range: \( V_{\text{IN-MAX}}, V_{\text{IN-MIN}} \)
Switching frequency: \( f_{\text{SW}} \)
Current sense voltage: \( V_{\text{SNS}} \)
Average LED current: \( I_{\text{LED}} \)
Inductor current ripple: \( \Delta i_{\text{L-PP}} \)
LED current ripple: \( \Delta i_{\text{LED-PP}} \)
Peak current limit: \( I_{\text{LIM}} \)
Input voltage ripple: \( \Delta V_{\text{IN-PP}} \)
Output OVLO characteristics: \( V_{\text{TURN-OFF}}, V_{\text{HYSO}} \)
Input UVLO characteristics: \( V_{\text{TURN-ON}}, V_{\text{HYS}} \)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Operating Point

Given the number of series LEDs (N), the forward voltage (\( V_{\text{LED}} \)) and dynamic resistance (\( r_{\text{LED}} \)) for a single LED, solve for the nominal output voltage (\( V_{O} \)) and the nominal LED string dynamic resistance (\( r_{D} \)):

\[
V_{O} = N \times V_{\text{LED}}
\]
\[
r_{D} = N \times r_{\text{LED}}
\]

Solve for the ideal nominal duty cycle (D):

Buck:
\[
D = \frac{V_{O}}{V_{\text{IN}}}
\]

Boost:
\[
D = \frac{V_{O} - V_{\text{IN}}}{V_{O}}
\]

Buck-Boost:
\[
D = \frac{V_{O}}{V_{O} + V_{\text{IN}}}
\]

Using the same equations, find the minimum duty cycle (\( D_{\text{MIN}} \)) using maximum input voltage (\( V_{\text{IN-MAX}} \)) and the maximum duty cycle (\( D_{\text{MAX}} \)) using the minimum input voltage (\( V_{\text{IN-MIN}} \)). Also, remember that \( D' = 1 - D \).

8.2.1.2.2 Switching Frequency

Set the switching frequency (\( f_{\text{SW}} \)) by assuming a \( C_{T} \) value of 1 nF and solving for \( R_{T} \):

Buck (Constant Ripple vs. \( V_{\text{IN}} \)
Typical Applications (continued)

\[ R_T = \frac{25 \times (V_{IN} - V_O)}{f_{SW} \times C_T \times V_{IN}} \]  
(39)

Buck (Constant Ripple vs. \( V_O \))

\[ R_T = \frac{25 \times (V_{IN} \times V_O - V_O^2)}{f_{SW} \times C_T \times V_{IN}^2} \]  
(40)

Boost and Buck-Boost

\[ R_T = \frac{25}{f_{SW} \times C_T} \]  
(41)

8.2.1.2.3 Average LED Current

For all topologies, set the average LED current (\( I_{LED} \)) knowing the desired current sense voltage (\( V_{SNS} \)) and solving for \( R_{SNS} \):

\[ R_{SNS} = \frac{V_{SNS}}{I_{LED}} \]  
(42)

If the calculated \( R_{SNS} \) is too far from a desired standard value, then \( V_{SNS} \) will have to be adjusted to obtain a standard value.

Setup the suggested signal current of 100 µA by assuming \( R_{CSH} = 12.4 \, k\Omega \) and solving for \( R_{HSP} \):

\[ R_{HSP} = \frac{I_{LED} \times R_{CSH} \times R_{SNS}}{1.24V} \]  
(43)

If the calculated \( R_{HSP} \) is too far from a desired standard value, then \( R_{CSH} \) can be adjusted to obtain a standard value.

8.2.1.2.4 Inductor Ripple Current

Set the nominal inductor ripple current (\( \Delta i_{L-PP} \)) by solving for the appropriate inductor (\( L_1 \)):

Buck

\[ L_1 = \frac{(V_{IN} - V_O) \times D}{\Delta i_{L-PP} \times f_{SW}} \]  
(44)

Boost and Buck-Boost

\[ L_1 = \frac{V_{IN} \times D}{\Delta i_{L-PP} \times f_{SW}} \]  
(45)

To set the worst case inductor ripple current, use \( V_{IN-MAX} \) and \( D_{MIN} \) when solving for \( L_1 \).

The minimum allowable inductor RMS current rating (\( I_{L-RMS} \)) can be calculated as:

Buck

\[ I_{L-RMS} = I_{LED} \times \sqrt{1 + \frac{1}{12} \times \left( \frac{\Delta i_{L-PP}}{I_{LED}} \right)^2} \]  
(46)

Boost and Buck-Boost

\[ I_{L-RMS} = \frac{I_{LED}}{D'} \times \sqrt{1 + \frac{1}{12} \times \left( \frac{\Delta i_{L-PP} \times D'}{I_{LED}} \right)^2} \]  
(47)
Typical Applications (continued)

8.2.1.2.5 LED Ripple Current

Set the nominal LED ripple current ($\Delta i_{LED-PP}$), by solving for the output capacitance ($C_O$):

Buck

$$C_O = \frac{\Delta i_{LED-PP}}{8 \times f_{SW} \times f_D \times \Delta i_{LED-PP}}$$  \hspace{1cm} (48)

Boost and Buck-boost

$$C_O = \frac{i_{LED} \times D}{f_D \times \Delta i_{LED-PP} \times f_{SW}}$$  \hspace{1cm} (49)

To set the worst case LED ripple current, use $D_{MAX}$ when solving for $C_O$. Remember, when PWM dimming, TI recommends using a minimum of 40 µF of output capacitance to improve performance.

The minimum allowable RMS output capacitor current rating ($I_{CO-RMS}$) can be approximated:

Buck

$$I_{CO-RMS} = \frac{\Delta i_{LED-PP}}{\sqrt{12}}$$  \hspace{1cm} (50)

Boost and Buck-boost

$$I_{CO-RMS} = i_{LED} \times \sqrt{\frac{D_{MAX}}{1-D_{MAX}}}$$  \hspace{1cm} (51)

8.2.1.2.6 Peak Current Limit

Set the peak current limit ($I_{LIM}$) by solving for the transistor path sense resistor ($R_{LIM}$):

$$R_{LIM} = \frac{245 \text{ mV}}{I_{LIM}}$$  \hspace{1cm} (52)

8.2.1.2.7 Loop Compensation

Using a simple first order peak current mode control model, neglecting any output capacitor ESR dynamics, the necessary loop compensation can be determined.

First, the uncompensated loop gain ($T_U$) of the regulator can be approximated:

Buck

$$T_U = T_{U0} \times \left( \frac{1}{1 + \frac{S}{\omega_{p1}}} \right)$$  \hspace{1cm} (53)

Boost and Buck-boost

$$T_U = T_{U0} \times \left( \frac{1 - \frac{S}{\omega_{Z1}}}{1 + \frac{S}{\omega_{p1}}} \right)$$  \hspace{1cm} (54)

Where the pole ($\omega_{p1}$) is approximated:

Buck

$$\omega_{p1} = \frac{1}{r_D \times C_O}$$  \hspace{1cm} (55)
Typical Applications (continued)

Boost

\[ \omega_{p1} = \frac{2}{r_D \times C_O} \]  

(56)

Buck-Boost

\[ \omega_{p1} = \frac{1+D}{r_D \times C_O} \]  

(57)

And the RHP zero \((\omega_{z1})\) is approximated:

Boost

\[ \omega_{z1} = \frac{r_D \times D^2}{L1} \]  

(58)

Buck-Boost

\[ \omega_{z1} = \frac{r_D \times D^2}{D \times L1} \]  

(59)

And the uncompensated DC loop gain \((T_{U0})\) is approximated:

Buck

\[ T_{U0} = \frac{500V \times R_{CSH} \times R_{SNS}}{R_{HSP} \times R_{LIM}} = \frac{620V}{I_{LED} \times R_{LIM}} \]  

(60)

Boost

\[ T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{2 \times R_{HSP} \times R_{LIM}} = \frac{D' \times 310V}{I_{LED} \times R_{LIM}} \]  

(61)

Buck-Boost

\[ T_{U0} = \frac{D' \times 500V \times R_{CSH} \times R_{SNS}}{(1+D) \times R_{HSP} \times R_{LIM}} = \frac{D' \times 620V}{(1+D) \times I_{LED} \times R_{LIM}} \]  

(62)

For all topologies, the primary method of compensation is to place a low frequency dominant pole \((\omega_{p2})\), which will ensure that there is ample phase margin at the crossover frequency. This is accomplished by placing a capacitor \((C_{CMP})\) from the COMP pin to AGND, which is calculated according to the lower value of the pole and the RHP zero of the system (shown as a minimizing function):

\[ \omega_{p2} = \min(\omega_{p1}, \omega_{z1}) \]  

(63)

\[ C_{CMP} = \frac{1}{\omega_{p2} \times 5 \times 10^6} \]  

(64)

If analog dimming is used, \(C_{CMP}\) should be approximately 4× larger to maintain stability as the LEDs are dimmed to zero.

A high-frequency compensation pole \((\omega_{p3})\) can be used to attenuate switching noise and provide better gain margin. Assuming \(R_{FS} = 10 \, \Omega\), \(C_{FS}\) is calculated according to the higher value of the pole and the RHP zero of the system (shown as a maximizing function):

\[ \omega_{p3} = \max(\omega_{p1}, \omega_{z1}) \times 10 \]  

(65)

\[ C_{FS} = \frac{1}{10 \times \omega_{p3}} \]  

(66)

The total system loop gain \((T)\) can then be written as:
Typical Applications (continued)

Buck
\[ T = T_0 \cdot \frac{1}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right) \cdot \left(1 + \frac{s}{\omega_{p3}}\right)} \]  
(67)

Boost and Buck-Boost
\[ T = T_0 \cdot \frac{1 - \frac{s}{\omega_{Z1}}}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right) \cdot \left(1 + \frac{s}{\omega_{p3}}\right)} \]  
(68)

8.2.1.2.8 Input Capacitance

Set the nominal input voltage ripple (\(\Delta V_{IN-PP}\)) by solving for the required capacitance (\(C_{IN}\)):

Buck
\[ C_{IN} = \frac{I_{LED} \times (1 - D) \times D}{\Delta V_{IN-PP} \times f_{SW}} \]  
(69)

Boost
\[ C_{IN} = \frac{\Delta i_{L-PP}}{8 \times \Delta V_{IN-PP} \times f_{SW}} \]  
(70)

Buck-Boost
\[ C_{IN} = \frac{I_{LED} \times D}{\Delta V_{IN-PP} \times f_{SW}} \]  
(71)

Use \(D_{MAX}\) to set the worst case input voltage ripple, when solving for \(C_{IN}\) in a buck-boost regulator and \(D_{MID} = 0.5\) when solving for \(C_{IN}\) in a buck regulator.

The minimum allowable RMS input current rating (\(I_{CIN-RMS}\)) can be approximated:

Buck
\[ I_{CIN-RMS} = I_{LED} \times \sqrt{D_{MID} \times (1 - D_{MID})} \]  
(72)

Boost
\[ I_{CIN-RMS} = \frac{\Delta i_{L-PP}}{\sqrt{12}} \]  
(73)

Buck-Boost
\[ I_{CIN-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \]  
(74)

8.2.1.2.9 NFET

The NFET voltage rating should be at least 15% higher than the maximum NFET drain-to-source voltage (\(V_{T-MAX}\)):

Buck
\[ V_{T-MAX} = V_{IN-MAX} \]  
(75)

Boost
Typical Applications (continued)

\[ V_{T-\text{MAX}} = V_O \]  

(76)

Buck-Boost

\[ V_{T-\text{MAX}} = V_{\text{IN-MAX}} + V_O \]  

(77)

The current rating should be at least 10% higher than the maximum average NFET current \((I_{T-\text{MAX}})\):

Buck

\[ I_{T-\text{MAX}} = D_{\text{MAX}} \times I_{\text{LED}} \]  

(78)

Boost and Buck-Boost

\[ D_{\text{MAX}} \]

\[ I_{T-\text{MAX}} = \frac{1 - D_{\text{MAX}}}{} \times I_{\text{LED}} \]  

(79)

Approximate the nominal RMS transistor current \((I_{T-\text{RMS}})\):

Buck

\[ I_{T-\text{RMS}} = I_{\text{LED}} \times \sqrt{D} \]  

(80)

\subsection{8.2.1.2.9.1 Boost and Buck-Boost}

\[ I_{T-\text{RMS}} = I_{\text{LED}} \times \sqrt{D} \]  

(81)

Given an NFET with on-resistance \((R_{DS-\text{ON}})\), solve for the nominal power dissipation \((P_T)\):

\[ P_T = I_{T-\text{RMS}}^2 \times R_{DS-\text{ON}} \]  

(82)

\subsection{8.2.1.2.10 Diode}

The Schottky diode voltage rating should be at least 15% higher than the maximum blocking voltage \((V_{RD-\text{MAX}})\):

Buck

\[ V_{RD-\text{MAX}} = V_{\text{IN-MAX}} \]  

(83)

Boost

\[ V_{RD-\text{MAX}} = V_O \]  

(84)

Buck-Boost

\[ V_{RD-\text{MAX}} = V_{\text{IN-MAX}} + V_O \]  

(85)

The current rating should be at least 10% higher than the maximum average diode current \((I_{D-\text{MAX}})\):

Buck

\[ I_{D-\text{MAX}} = (1 - D_{\text{MIN}}) \times I_{\text{LED}} \]  

(86)

Boost and Buck-Boost

\[ I_{D-\text{MAX}} = I_{\text{LED}} \]  

(87)

Replace \(D_{\text{MAX}}\) with \(D\) in the \(I_{D-\text{MAX}}\) equation to solve for the average diode current \((I_D)\). Given a diode with forward voltage \((V_{FD})\), solve for the nominal power dissipation \((P_D)\):

\[ P_D = I_D \times V_{FD} \]  

(88)
Typical Applications (continued)

8.2.1.2.11 Output OVLO
For boost and buck-boost regulators, output OVLO is programmed with the turn-off threshold voltage \( V_{\text{TURN-OFF}} \) and the desired hysteresis \( V_{\text{HYS}} \). To set \( V_{\text{HYS}} \), solve for \( R_{\text{OV2}} \):

\[
R_{\text{OV2}} = \frac{V_{\text{HYS}}}{23 \, \mu A}
\]  \( \quad (89) \)

To set \( V_{\text{TURN-OFF}} \), solve for \( R_{\text{OV1}} \):

Boost

\[
R_{\text{OV1}} = \frac{1.24V \times R_{\text{OV2}}}{V_{\text{TURN-OFF}} - 1.24V}
\]  \( \quad (90) \)

Buck-Boost

\[
R_{\text{OV1}} = \frac{1.24V \times R_{\text{OV2}}}{V_{\text{TURN-OFF}} - 620 \, \text{mV}}
\]  \( \quad (91) \)

A small filter capacitor \( (C_{\text{OVP}} = 47 \, \text{pF}) \) should be added from the OVP pin to ground to reduce coupled switching noise.

8.2.1.2.12 Input UVLO
For all topologies, input UVLO is programmed with the turn-on threshold voltage \( V_{\text{TURN-ON}} \) and the desired hysteresis \( V_{\text{HYS}} \).

**Method 1:** If no PWM dimming is required, a two resistor network can be used. To set \( V_{\text{HYS}} \), solve for \( R_{\text{UV2}} \):

\[
R_{\text{UV2}} = \frac{V_{\text{HYS}}}{23 \, \mu A}
\]  \( \quad (92) \)

To set \( V_{\text{TURN-ON}} \), solve for \( R_{\text{UV1}} \):

\[
R_{\text{UV1}} = \frac{1.24V \times R_{\text{UV2}}}{V_{\text{TURN-ON}} - 1.24V}
\]  \( \quad (93) \)

**Method 2:** If PWM dimming is required, a three resistor network is suggested. To set \( V_{\text{TURN-ON}} \), assume \( R_{\text{UV2}} = 10 \, \text{k} \Omega \) and solve for \( R_{\text{UV1}} \) as in Method 1. To set \( V_{\text{HYS}} \), solve for \( R_{\text{UVH}} \):

\[
R_{\text{UVH}} = \frac{R_{\text{UV1}} \times (V_{\text{HYS}} - 23 \, \mu A \times R_{\text{UV2}})}{23 \, \mu A \times (R_{\text{UV1}} + R_{\text{UV2}})}
\]  \( \quad (94) \)

8.2.1.2.13 PWM Dimming Method

PWM dimming can be performed several ways:

**Method 1:** Connect the dimming MOSFET \( (Q_3) \) with the drain to the nDIM pin and the source to AGND. Apply an external PWM signal to the gate of \( Q_{\text{DIM}} \). A pulldown resistor may be necessary to properly turn off \( Q_3 \).

**Method 2:** Connect the anode of a Schottky diode to the nDIM pin. Apply an external inverted PWM signal to the cathode of the same diode.

The DDRV pin should be connected to the gate of the dimFET with or without level-shifting circuitry as described in the **PWM Dimming** section. The dimFET should be rated to handle the average LED current and the nominal output voltage.

8.2.1.2.14 Analog Dimming Method

Analog dimming can be performed several ways:

**Method 1:** Place a potentiometer in series with the \( R_{\text{CSH}} \) resistor to dim the LED current from the nominal \( I_{\text{LED}} \) to near zero.
Typical Applications (continued)

**Method 2:** Connect a controlled current source as detailed in the *Analog Dimming* section to the CSH pin. Increasing the current sourced into the CSH node will decrease the LEDs from the nominal $I_{\text{LED}}$ to zero current in the same manner as the thermal foldback circuit.
Typical Applications (continued)

8.2.2 LM3421 Buck-Boost Application

8.2.2.1 Design Requirements

N = 6

\( V_{\text{LED}} = 3.5 \text{ V} \)

\( r_{\text{LED}} = 325 \text{ m}\Omega \)

\( V_{\text{IN}} = 24 \text{ V} \)

\( V_{\text{IN-MIN}} = 10 \text{ V} \)

\( V_{\text{IN-MAX}} = 70 \text{ V} \)

\( f_{\text{SW}} = 500 \text{ kHz} \)

\( V_{\text{SNS}} = 100 \text{ mV} \)

\( I_{\text{LED}} = 1 \text{ A} \)

\( \Delta I_{\text{L-PP}} = 700 \text{ mA} \)

\( \Delta I_{\text{LED-PP}} = 12 \text{ mA} \)

\( \Delta V_{\text{IN-PP}} = 100 \text{ mV} \)
Typical Applications (continued)

\[ I_{\text{LIM}} = 6 \, \text{A} \]
\[ V_{\text{TURN-ON}} = 10 \, \text{V} \]
\[ V_{\text{HYS}} = 3 \, \text{V} \]
\[ V_{\text{TURN-OFF}} = 40 \, \text{V} \]
\[ V_{\text{HYSO}} = 10 \, \text{V} \]

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Operating Point

Solve for \( V_O \) and \( r_D \):
\[ V_O = \frac{6 \times 3.5 \, \text{V}}{21 \, \text{V}} = 21 \, \text{V} \]  
\[ r_D = \frac{6 \times 325 \, \text{m\Omega}}{1.95 \, \text{\Omega}} = 1.95 \, \text{\Omega} \]  

Solve for \( D \), \( D' \), \( D_{\text{MAX}} \), and \( D_{\text{MIN}} \):
\[ D = \frac{21 \, \text{V}}{V_O + V_{\text{IN}}} = \frac{21 \, \text{V}}{21 \, \text{V} + 24 \, \text{V}} = 0.467 \]  
\[ D' = 1 - D = 1 - 0.467 = 0.533 \]  
\[ D_{\text{MIN}} = \frac{21 \, \text{V}}{V_O + V_{\text{IN-MAX}}} = \frac{21 \, \text{V}}{21 \, \text{V} + 70 \, \text{V}} = 0.231 \]  
\[ D_{\text{MAX}} = \frac{21 \, \text{V}}{V_O + V_{\text{IN-MIN}}} = \frac{21 \, \text{V}}{21 \, \text{V} + 10 \, \text{V}} = 0.677 \]

8.2.2.2 Switching Frequency

Assume \( C_T = 1 \, \text{nF} \) and solve for \( R_T \):
\[ R_T = \frac{25}{f_{\text{SW}} \times C_T} = \frac{25}{500 \, \text{kHz} \times 1 \, \text{nF}} = 50 \, \text{k\Omega} \]  

The closest standard resistor is 49.9 k\Omega; therefore, \( f_{\text{SW}} \) is:
\[ f_{\text{SW}} = \frac{25}{R_T \times C_T} = \frac{25}{49.9 \, \text{k\Omega} \times 1 \, \text{nF}} = 501 \, \text{kHz} \]

The chosen component from step 2 is:
\[ C_T = 1 \, \text{nF} \]
\[ R_T = 49.9 \, \text{k\Omega} \]

8.2.2.3 Average LED Current

Solve for \( R_{\text{SNS}} \):
\[ R_{\text{SNS}} = \frac{V_{\text{SNS}}}{I_{\text{LED}}} = \frac{100 \, \text{mV}}{1 \, \text{A}} = 0.1 \, \text{\Omega} \]  

Assume \( R_{\text{CSH}} = 12.4 \, \text{k\Omega} \) and solve for \( R_{\text{HSP}} \):
\[ R_{\text{HSP}} = \frac{I_{\text{LED}} \times R_{\text{CSH}} \times R_{\text{SNS}}}{1.24 \, \text{V}} = \frac{1 \, \text{A} \times 12.4 \, \text{k\Omega} \times 0.1 \, \text{\Omega}}{1.24 \, \text{V}} = 1.0 \, \text{k\Omega} \]
Typical Applications (continued)

The closest standard resistor for $R_{SNS}$ is actually 0.1 $\Omega$ and for $R_{HSP}$ is actually 1 k$\Omega$; therefore, $I_{LED}$ is:

$$I_{LED} = \frac{1.24 \times R_{HSP}}{R_{SNS} \times R_{CSH}} = \frac{1.24 \times 1 \text{ k}$\Omega$}{0.1 \Omega \times 12.4 \text{ k}$\Omega$} = 1.0\text{A}$$  \hspace{1cm} (106)

The chosen components from step 3 are:
- $R_{SNS} = 0.1 \Omega$
- $R_{CSH} = 12.4 \text{ k}$\Omega$
- $R_{HSP} = R_{HSN} = 1 \text{k}$\Omega$

\hspace{1cm} (107)

8.2.2.2.4 Inductor Ripple Current

Solve for $L_1$:

$$L_1 = \frac{V_{in} \times D}{\Delta i_{L-PP} \times f_{SW}} = \frac{24\text{V} \times 0.467}{700 \text{mA} \times 501 \text{kHz}} = 32 \mu\text{H}$$  \hspace{1cm} (108)

The closest standard inductor is 33 $\mu$H; therefore, $\Delta i_{L-PP}$ is:

$$\Delta i_{L-PP} = \frac{V_{in} \times D}{L_1 \times f_{SW}} = \frac{24\text{V} \times 0.467}{33 \mu\text{H} \times 501 \text{kHz}} = 678 \text{mA}$$  \hspace{1cm} (109)

Determine minimum allowable RMS current rating:

$$I_{L-RMS} = I_{LED} \times \sqrt{1 + \frac{1}{12} \left( \frac{\Delta i_{L-PP} \times D}{I_{LED}} \right)^2}$$

$$I_{L-RMS} = 1\text{A} \times 0.533 \times \sqrt{1 + \frac{1}{12} \left( \frac{678 \text{mA} \times 0.533}{1\text{A}} \right)^2} = 1.89\text{A}$$  \hspace{1cm} (110)

The chosen component from step 4 is:

$$L_1 = 33 \mu\text{H}$$  \hspace{1cm} (111)

8.2.2.2.5 Output Capacitance

Solve for $C_O$:

$$C_O = \frac{I_{LED} \times D}{r_D \times \Delta i_{LED-PP} \times f_{SW}}$$

$$C_O = \frac{1\text{A} \times 0.467}{1.95\text{$\Omega$} \times 12 \text{mA} \times 501 \text{kHz}} = 39.8 \mu\text{F}$$  \hspace{1cm} (112)

The closest capacitance totals 40 $\mu$F; therefore, $\Delta i_{LED-PP}$ is:

$$\Delta i_{LED-PP} = \frac{I_{LED} \times D}{r_D \times C_O \times f_{SW}}$$

$$\Delta i_{LED-PP} = \frac{1\text{A} \times 0.467}{1.95\text{$\Omega$} \times 40 \mu\text{F} \times 501 \text{kHz}} = 12 \text{mA}$$  \hspace{1cm} (113)

Determine minimum allowable RMS current rating:
Typical Applications (continued)

\[ I_{CO-RMS} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \]

The chosen components from step 5 are:

\[ C_O = 4 \times 10 \, \mu F \]

8.2.2.6 Peak Current Limit

Solve for \( R_{LIM} \):

\[ R_{LIM} = \frac{245 \text{ mV}}{I_{LIM}} = \frac{245 \text{ mV}}{6A} = 0.041\Omega \]

The closest standard resistor is 0.04 \( \Omega \); therefore, \( I_{LIM} \) is:

\[ I_{LIM} = \frac{245 \text{ mV}}{R_{LIM}} = \frac{245 \text{ mV}}{0.04\Omega} = 6.13A \]

The chosen component from step 6 is:

\[ R_{LIM} = 0.04\Omega \]

8.2.2.7 Loop Compensation

\( \omega_{P1} \) is approximated:

\[ \omega_{P1} = \frac{1 + D}{r_D \times C_O} = \frac{1.467}{1.95\Omega \times 40 \, \mu F} = 19\text{ rad} \/ \text{sec} \]

\( \omega_{Z1} \) is approximated:

\[ \omega_{Z1} = \frac{r_D \times D^2}{D \times L1} = \frac{1.95\Omega \times 0.533^2}{0.467 \times 33\mu H} = 36\text{ rad} \/ \text{sec} \]

\( T_{U0} \) is approximated:

\[ T_{U0} = \frac{D' \times 620V}{(1 + D) \times I_{LED} \times R_{LIM}} = \frac{0.533 \times 620V}{1.467 \times 1A \times 0.04\Omega} = 5630 \]

To ensure stability, calculate \( \omega_{P2} \):

\[ \omega_{P2} = \frac{\min(\omega_{P1}, \omega_{Z1})}{5 \times T_{U0}} = \frac{\omega_{P1}}{5 \times 5630} = \frac{19\text{ rad}}{5 \times 5630} = 0.675\text{ rad} \/ \text{sec} \]

Solve for \( C_{CMP} \):

\[ C_{CMP} = \frac{1}{\omega_{P2} \times 5 \times 10^6\Omega} = \frac{1}{0.675\text{ rad} \/ \text{sec} \times 5 \times 10^6\Omega} = 0.3\mu F \]

To attenuate switching noise, calculate \( \omega_{P3} \):

\[ \omega_{P3} = (\max(\omega_{P1}, \omega_{Z1}) \times 10 = \omega_{Z1} \times 10 \]

\[ \omega_{P3} = 36\text{ rad} \/ \text{sec} \times 10 = 360\text{ rad} \/ \text{sec} \]

Assume \( R_{FS} = 10 \, \Omega \) and solve for \( C_{FS} \):
Typical Applications (continued)

\[ C_{FS} = \frac{1}{10\Omega \times \omega_p^3} = \frac{1}{10\Omega \times 360\text{k}\text{rad/sec}} = 0.28 \mu F \]  

The chosen components from step 7 are:

\[
\begin{align*}
C_{\text{CMP}} &= 0.33 \mu F \\
R_{FS} &= 10 \Omega \\
C_{FS} &= 0.27 \mu F
\end{align*}
\]  

(125)

### 8.2.2.8 Input Capacitance

Solve for the minimum \( C_{IN} \):

\[ C_{IN} = \frac{I_{LED} \times D}{\Delta V_{IN-PP} \times f_{SW}} = \frac{1A \times 0.467}{100 \text{mV} \times 504 \text{kHz}} = 9.27 \mu F \]  

(127)

To minimize power supply interaction a 200% larger capacitance of approximately 20 µF is used, therefore the actual \( \Delta V_{IN-PP} \) is much lower. Because high voltage ceramic capacitor selection is limited, four 4.7-µF X7R capacitors are chosen.

Determine minimum allowable RMS current rating:

\[ I_{IN-RMS} = I_{LED} \times \sqrt{\frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}}} = 1A \times \sqrt{\frac{0.677}{1 - 0.677}} = 1.45A \]  

(128)

The chosen components from step 8 are:

\[ C_{IN} = 4 \times 4.7 \mu F \]  

(129)

### 8.2.2.9 NFET

Determine minimum Q1 voltage rating and current rating:

\[ V_{T-MAX} = V_{IN-MAX} + V_O = 70V + 21V = 91V \]  

(130)

\[ I_{T-MAX} = \frac{0.677}{1 - 0.677} \times 1A = 2.1A \]  

(131)

A 100-V NFET is chosen with a current rating of 32 A due to the low \( R_{DS-ON} = 50 \Omega \). Determine \( I_{T-RMS} \) and \( P_T \):

\[ I_{T-RMS} = \frac{I_{LED}}{D} \times \sqrt{D} = \frac{1A}{0.533} \times \sqrt{0.467} = 1.28A \]  

(132)

\[ P_T = I_{T-RMS}^2 \times R_{DS-ON} = 1.28A^2 \times 50 \Omega = 82 \text{mW} \]  

(133)

The chosen component from step 9 is:

\[ Q1 \rightarrow 32A, 100V, \text{DPAK} \]  

(134)

### 8.2.2.10 Diode

Determine minimum D1 voltage rating and current rating:

\[ V_{RD-MAX} = V_{IN-MAX} + V_O = 70V + 21V = 91V \]  

(135)
Typical Applications (continued)

\[ I_{D-\text{MAX}} = I_{\text{LED}} = 1A \]  \hspace{1cm} (136)

A 100-V diode is chosen with a current rating of 12 A and \( V_{DF} = 600 \) mV. Determine \( P_D \):

\[ P_D = I_d \times V_{FD} = 1A \times 600 \text{ mV} = 600 \text{ mW} \]  \hspace{1cm} (137)

The chosen component from step 10 is:

\[ \text{D1} \rightarrow 12A, 100V, \text{ DPAK} \]  \hspace{1cm} (138)

8.2.2.2.11 Input UVLO

Solve for \( R_{UV2} \):

\[ R_{UV2} = \frac{V_{\text{HY5}}} {23 \mu A} = \frac{3V} {23 \mu A} = 130 \text{ k}\Omega \]  \hspace{1cm} (139)

The closest standard resistor is 130 k\( \Omega \); therefore, \( V_{\text{HY5}} \) is:

\[ V_{\text{HY5}} = R_{UV2} \times 23 \mu A = 130 \text{ k}\Omega \times 23 \mu A = 2.99V \]  \hspace{1cm} (140)

Solve for \( R_{UV1} \):

\[ R_{UV1} = \frac{1.24V \times R_{UV2}} {V_{\text{TURN-ON}} - 1.24V} = \frac{1.24V \times 130k\Omega} {10V - 1.24V} = 18.4k\Omega \]  \hspace{1cm} (141)

The closest standard resistor is 18.2 k\( \Omega \), making \( V_{\text{TURN-ON}} \):

\[ V_{\text{TURN-ON}} = \frac{1.24V \times (R_{UV1} + R_{UV2})} {R_{UV1}} \]  \hspace{1cm} (142)

\[ V_{\text{TURN-ON}} = \frac{1.24V \times (18.2k\Omega + 130k\Omega)} {18.2k\Omega} = 10.1V \]

The chosen components from step 11 are:

\[ R_{UV1} = 18.2k\Omega \]
\[ R_{UV2} = 130k\Omega \]  \hspace{1cm} (143)

8.2.2.2.12 Output OVLO

Solve for \( R_{OV2} \):

\[ R_{OV2} = \frac{V_{\text{HYSO}}} {23 \mu A} = \frac{10V} {23 \mu A} = 435k\Omega \]  \hspace{1cm} (144)

The closest standard resistor is 432 k\( \Omega \); therefore, \( V_{\text{HYSO}} \) is:

\[ V_{\text{HYSO}} = R_{OV2} \times 23 \mu A = 432k\Omega \times 23 \mu A = 9.94V \]  \hspace{1cm} (145)

Solve for \( R_{OV1} \):

\[ R_{OV1} = \frac{1.24V \times R_{OV2}} {V_{\text{TURN-OFF}} - 0.62V} = \frac{1.24V \times 432k\Omega} {40V - 0.62V} = 13.6k\Omega \]  \hspace{1cm} (146)

The closest standard resistor is 13.7 k\( \Omega \), making \( V_{\text{TURN-OFF}} \):

\[ \text{--- END OF PAGE ---} \]
Typical Applications (continued)

\[
V_{\text{TURN-OFF}} = \frac{1.24V \times (0.5 \times R_{OV1} + R_{OV2})}{R_{OV1}}
\]

\[
V_{\text{TURN-OFF}} = \frac{1.24V \times (0.5 \times 13.7 \, k\Omega + 432 \, k\Omega)}{13.7 \, k\Omega} = 39.7V
\]

(147)

The chosen components from step 12 are:

\[
R_{OV1} = 13.7 \, k\Omega \\
R_{OV2} = 432 \, k\Omega
\]

(148)

Table 1. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
</tr>
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<tbody>
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<tr>
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<td>CRCW080510RFKEA</td>
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8.2.2.3 Application Curve

Figure 37. Sample Buck-Boost Efficiency vs Input Voltage. \( V_o = 21 \) V
8.2.3 LM3421 BOOST Application

Figure 38. LM3421 BOOST Application

8.2.3.1 Design Requirements
- Input: 8 V to 28 V
- Output: 9 LEDs at 1 A
- PWM Dimming up to 30kHz
- 700-kHz Switching Frequency
### 8.2.3.2 Detailed Design Procedure

#### Table 2. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
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<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
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<td>C_{FS}</td>
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<tr>
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8.2.4  LM3421 Buck-Boost Application

8.2.4.1  Design Requirements

- Input: 10 V to 30 V
- Output: 4 LEDs at 2 A
- PWM Dimming up to 10 kHz
- Analog Dimming
- 600-kHz Switching Frequency
### 8.2.4.2 Detailed Design Procedure

#### Table 3. Bill of Materials

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<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
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<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
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<td>BOURNS</td>
<td>3352P-1-105</td>
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<td>R&lt;sub&gt;&lt;i&gt;PU&lt;/i&gt;&lt;/sub&gt;</td>
<td>4.99 kΩ 1%</td>
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<td>CRCW0805499KFKEA</td>
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<tr>
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<td>R&lt;sub&gt;&lt;i&gt;SER&lt;/i&gt;&lt;/sub&gt;</td>
<td>499 Ω 1%</td>
<td>VISHAY</td>
<td>CRCW0805499KFKEA</td>
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<tr>
<td>1</td>
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<td>0.05 Ω 1% 1 W</td>
<td>VISHAY</td>
<td>WSL251R0500FEA</td>
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<tr>
<td>1</td>
<td>R&lt;sub&gt;&lt;i&gt;7&lt;/i&gt;&lt;/sub&gt;</td>
<td>41.2 kΩ 1%</td>
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<tr>
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<td>CRCW08051K43FKEA</td>
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<td>R&lt;sub&gt;&lt;i&gt;UVH&lt;/i&gt;&lt;/sub&gt;</td>
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<td>CRCW080517K4FKEA</td>
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8.2.5 LM3423 Boost Application

**Figure 40. LM3423 Boost Application**

### 8.2.5.1 Design Requirements

- Input: 18 V to 38 V
- Output: 12 LEDs at 700 mA
- High Side PWM Dimming up to 30 kHz
- Analog Dimming
- Zero Current Shutdown
- 700-kHz Switching Frequency
### 8.2.5.2 Detailed Design Procedure

#### Table 4. Bill of Materials

<table>
<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
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<td>MURATA</td>
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<tr>
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<td>C&lt;sub&gt;FS&lt;/sub&gt;</td>
<td>0.1-µF X7R 10% 25 V</td>
<td>MURATA</td>
<td>GRM21BR71E104KA01L</td>
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<tr>
<td>4</td>
<td>C&lt;sub&gt;N&lt;/sub&gt;</td>
<td>4.7-µF X7R 10% 100 V</td>
<td>TDK</td>
<td>C5750X7R2A475K</td>
</tr>
<tr>
<td>4</td>
<td>C&lt;sub&gt;O&lt;/sub&gt;</td>
<td>10-µF X7R 10% 50 V</td>
<td>TDK</td>
<td>C4532X7R1H106K</td>
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<tr>
<td>1</td>
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<tr>
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<tr>
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<td>COMCHIP</td>
<td>CDBC560-G</td>
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<tr>
<td>1</td>
<td>D3</td>
<td>Zener 10 V 500 mA</td>
<td>ON-SEMI</td>
<td>BZX84C10LT1G</td>
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<tr>
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<td>L1</td>
<td>47 µH 20% 5.3 A</td>
<td>COILCRAFT</td>
<td>MSS1278-473MLB</td>
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<td>Si4436DY</td>
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<td>Q4, Q5 (dual pack)</td>
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<tr>
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<tr>
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8.2.6 LM3421 Buck-Boost Application

8.2.6.1 Design Requirements

- Input: 10 V to 70 V
- Output: 6 LEDs at 500 mA
- PWM Dimming up to 10 kHz
- Slow Fade Out
- MOSFET $R_{DS-ON}$ Sensing
- 700-kHz Switching Frequency
### 8.2.6.2 Detailed Design Procedure

#### Table 5. Bill of Materials

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<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
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<tr>
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<td>2.2-µF X7R 10% 16 V</td>
<td>MURATA</td>
<td>GRM21BR71C225KA12L</td>
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<tr>
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<tr>
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<td>17.4 kΩ 1%</td>
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8.2.7 LM3423 Buck Application

15V – 50V V\text{IN}

---

8.2.7.1 Design Requirements

- Input: 15 V to 50 V
- Output: 3 LEDs at 1.25 A
- PWM Dimming up to 50 kHz
- LED Status Indicator
- Zero Current Shutdown
- 700-kHz Switching Frequency
## 8.2.7.2 Detailed Design Procedure

### Table 6. Bill of Materials

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<thead>
<tr>
<th>QTY</th>
<th>PART ID</th>
<th>PART VALUE</th>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
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8.2.8 LM3423 Buck-Boost Application

8.2.8.1 Design Requirements

- Input: 15 V to 60 V
- Output: 8 LEDs at 2.5 A
- Fault Input Disconnect
- Zero Current Shutdown
- 500-kHz Switching Frequency
### 8.2.8.2 Detailed Design Procedure

#### Table 7. Bill of Materials

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<tr>
<th>QTY</th>
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8.2.9 LM3421 SEPIC Application

8.2.9.1 Design Procedure

- Input: 9 V to 36 V
- Output: 5 LEDs at 750 mA
- PWM Dimming up to 30 kHz
- 500-kHz Switching Frequency
### 8.2.9.2 Detailed Design Procedure

**Table 8. Bill of Materials**

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<th>MANUFACTURER</th>
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9 Power Supply Recommendations

9.1 General Recommendations

The device is designed to operate from an input voltage supply range from 4.5 V to 75 V. This input supply should be well regulated. If the input supply is located more than a few inches from the EVM or PCB, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

9.2 Input Supply Current Limit

It is important to set the output current limit of your input supply to an appropriate value to avoid delays in your converter analysis and optimization. If not set high enough, current limit can be tripped during start-up or when your converter output power is increased, causing a foldback or shutdown condition. It is a common oversight when powering up a converter for the first time.

10 Layout

10.1 Layout Guidelines

The performance of any switching regulator depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines will maximize noise rejection and minimize the generation of EMI within the circuit.

Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. The main path for discontinuous current in the LM34xx-Q1 buck regulator contains the input capacitor (C\textsubscript{IN}), the recirculating diode (D\textsubscript{1}), the N-channel MOSFET (Q\textsubscript{1}), and the sense resistor (R\textsubscript{LIM}). In the LM34xx-Q1 boost regulator, the discontinuous current flows through the output capacitor (C\textsubscript{O}), D\textsubscript{1}, Q\textsubscript{1}, and R\textsubscript{LIM}. In the buck-boost regulator, both loops are discontinuous and should be carefully layed out. These loops should be kept as small as possible and the connections between all the components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L\textsubscript{1}, D\textsubscript{1} and Q\textsubscript{1} connect) should be just large enough to connect the components. To minimize excessive heating, large copper pours can be placed adjacent to the short current path of the switch node.

The RT, COMP, CSH, IS, HSP and HSN pins are all high-impedance inputs which couple external noise easily; therefore, the loops containing these nodes should be minimized whenever possible.

In some applications the LED or LED array can be far away (several inches or more) from the LM34xx-Q1, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the regulator, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.
10.2 Layout Example

Note critical paths and component placement:

- Minimize power loop containing discontinuous currents
- Minimize signal current loops (components close to IC)

- Ground plane under IC for signal routing helps minimize noise coupling

Figure 45. LM3421 Boost Layout Guideline
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
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</table>

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ2022 — *Ti Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# Packaging Information

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<th>Package Type</th>
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<th>Package Qty</th>
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<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
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(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LM3421, LM3421-Q1, LM3423, LM3423-Q1:**

- **Catalog:** LM3421, LM3423
- **Automotive:** LM3421-Q1, LM3423-Q1

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

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<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

**Legend:**
- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

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*Some of the images and diagrams are not visible due to the text-based format.*
**DEVICE**

| Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|-----------------|------|------|-------------|------------|-------------
| LM3421MHX/NOPB                | HTSSOP           | 16   | 2500 | 367.0       | 367.0      | 35.0        |
| LM3421Q0MHX/NOPB              | HTSSOP           | 16   | 2500 | 367.0       | 367.0      | 35.0        |
| LM3421Q1MHX/NOPB              | HTSSOP           | 16   | 2500 | 367.0       | 367.0      | 35.0        |
| LM3423MHX/NOPB                | HTSSOP           | 20   | 2500 | 367.0       | 367.0      | 35.0        |
| LM3423Q0MHX/NOPB              | HTSSOP           | 20   | 2500 | 367.0       | 367.0      | 35.0        |
| LM3423Q1MHX/NOPB              | HTSSOP           | 20   | 2500 | 367.0       | 367.0      | 35.0        |

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
5. Features may not be present.

PowerPAD is a trademark of Texas Instruments.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

9. Size of metal pad may vary due to creepage requirement.
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

NOTES: (continued)
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