LM3475 Hysteretic PFET Buck Controller

1 Features
- Easy-to-Use Control Methodology
- 0.8 V to V_{IN} Adjustable Output Range
- High Efficiency (90% Typical)
- ±0.9% (±1.5% Over Temperature) Feedback Voltage
- 100% Duty Cycle Capable
- Maximum Operating Frequency up to 2 MHz
- Internal Soft-Start
- Enable Pin

2 Applications
- TFT Monitor
- Auto PC
- Vehicle Security
- Navigation Systems
- Notebook Standby Supply
- Battery Powered Portable Applications
- Distributed Power Systems

3 Description
The LM3475 is a hysteretic P-FET buck controller designed to support a wide range of high efficiency applications in a very small SOT-23-5 package. The hysteretic control scheme has several advantages, including simple system design with no external compensation, stable operation with a wide range of components, and extremely fast transient response. Hysteretic control also provides high efficiency operation, even at light loads. The PFET architecture allows for low component count as well as 100% duty cycle and ultra-low dropout operation.

Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3475</td>
<td>SOT-23 (5)</td>
<td>1.60 mm × 2.90 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

\(V_{IN} = 5\text{V}\)

\(V_{OUT} = 2.5\text{V} / 2\text{A}\)
Table of Contents

1 Features ................................................................. 1
2 Applications .......................................................... 1
3 Description ............................................................ 1
4 Revision History .................................................... 2
5 Pin Configuration and Functions .............................. 3
6 Specifications ......................................................... 4
   6.1 Absolute Maximum Ratings ......................... 4
   6.2 ESD Ratings ................................................ 4
   6.3 Recommended Operating Ratings .................. 4
   6.4 Thermal Information .................................... 4
   6.5 Electrical Characteristics .............................. 5
   6.6 Typical Characteristics .................................. 6
7 Detailed Description .............................................. 8
   7.1 Overview .................................................... 8
   7.2 Functional Block Diagram .............................. 8
   7.3 Feature Description ...................................... 8
8 Application and Implementation ............................. 10
   8.1 Application Information ............................... 11
   8.2 Typical Application .................................... 11
9 Power Supply Recommendations ............................. 16
10 Layout ................................................................. 16
   10.1 Layout Guidelines ...................................... 16
   10.2 Layout Example ......................................... 17
11 Device and Documentation Support ....................... 18
   11.1 Device Support .......................................... 18
   11.2 Community Resources ............................... 18
   11.3 Trademarks ................................................ 18
   11.4 Electrostatic Discharge Caution .................... 18
   11.5 Glossary ................................................... 18
12 Mechanical, Packaging, and Orderable Information .... 18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ................................................................. 1

Changes from Revision A (March 2013) to Revision B Page

• Changed layout of National Data Sheet to TI format. ........................................................................................................... 1
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB</td>
<td>1</td>
<td>I</td>
<td>Feedback input. Connect to a resistor divider between the output and GND.</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>G</td>
<td>Ground.</td>
<td></td>
</tr>
<tr>
<td>EN</td>
<td>3</td>
<td>O</td>
<td>Enable. Pull this pin above 1.5 V (typical) for normal operation. When EN is low, the device enters shutdown mode.</td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>4</td>
<td>P</td>
<td>Power supply input.</td>
<td></td>
</tr>
<tr>
<td>PGATE</td>
<td>5</td>
<td>O</td>
<td>Gate drive output for the external PFET.</td>
<td></td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;In&lt;/sub&gt;</td>
<td>−0.3</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>PGATE</td>
<td>−0.3</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>FB</td>
<td>−0.3</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>EN</td>
<td>−0.3</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>Power dissipation (3)</td>
<td></td>
<td>440</td>
<td>mW</td>
</tr>
<tr>
<td>Lead temperature</td>
<td>Vapor phase (60 s)</td>
<td>215</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Infrared (15 s)</td>
<td>220</td>
<td>°C</td>
</tr>
<tr>
<td>T&lt;sub&gt;stg&lt;/sub&gt; Storage temperature</td>
<td>−65</td>
<td>1150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J_MAX</sub>, the junction-to-ambient thermal resistance, θ<sub>JA</sub> and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is calculated using: P<sub>D_MAX</sub> = (T<sub>J_MAX</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. The maximum power dissipation of 0.44 W is determined using T<sub>A</sub> = 25°C, θ<sub>JA</sub> = 225°C/W, and T<sub>J_MAX</sub> = 125°C.

6.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;(ESD)&lt;/sub&gt;</td>
<td>Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>2.7</td>
<td>10</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>T&lt;sub&gt;J&lt;/sub&gt; Operating junction temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>LM3475</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&lt;sub&gt;JA&lt;/sub&gt; Junction-to-ambient thermal resistance</td>
<td>164.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>R&lt;sub&gt;JC(top)&lt;/sub&gt; Junction-to-case (top) thermal resistance</td>
<td>115.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>R&lt;sub&gt;JB&lt;/sub&gt; Junction-to-board thermal resistance</td>
<td>27.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JT&lt;/sub&gt; Junction-to-top characterization parameter</td>
<td>12.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JB&lt;/sub&gt; Junction-to-board characterization parameter</td>
<td>26.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>R&lt;sub&gt;JC(bot)&lt;/sub&gt; Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics

Typical limits are for $T_J = 25^\circ C$, unless otherwise specified, $V_{IN} = EN = 5.0 \text{ V}$. Maximum and minimum specification limits are specified by design, test, or statistical analysis.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_Q$</td>
<td>Quiescent current</td>
<td></td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$EN = V_{IN}$ (PGATE Open)</td>
<td></td>
<td>260</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ C$</td>
<td>170</td>
<td></td>
<td>320</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ C$ to $+125^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FB}$</td>
<td>Feedback voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ C$</td>
<td>0.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = -40^\circ C$ to $+125^\circ C$</td>
<td></td>
<td>0.788</td>
<td>0.812</td>
<td></td>
</tr>
<tr>
<td>$% \Delta V_{FB}/\Delta V_{IN}$</td>
<td>Feedback voltage line regulation</td>
<td>2.7 V $&lt; V_{IN} &lt; 10$ V</td>
<td>0.01</td>
<td>0.1</td>
<td>%/V</td>
</tr>
<tr>
<td>$V_{HYST}$</td>
<td>Comparator hysteresis</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$2.7$ V $&lt; V_{IN} &lt; 10$ V</td>
<td>21</td>
<td>28</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$-40^\circ C$ to $+125^\circ C$</td>
<td>21</td>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>FB bias current</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ C$</td>
<td>50</td>
<td></td>
<td>600</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$-40^\circ C$ to $+125^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{TH_{EN}}$</td>
<td>Enable threshold voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Increasing $T_J = 25^\circ C$</td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$-40^\circ C$ to $+125^\circ C$</td>
<td>1.2</td>
<td>1.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{EN}$</td>
<td>Enable leakage current</td>
<td></td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$EN = 10$ V</td>
<td>0.025</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$-40^\circ C$ to $+125^\circ C$</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{PGATE}$</td>
<td>Driver resistance</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>$I_{SOURCE} = 100$ mA</td>
<td>2.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{sink} = 100$ mA</td>
<td>1.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{PGATE}$</td>
<td>Driver output current</td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>$V_{PGATE} = 3.5$ V</td>
<td>0.475</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$C_{PGATE} = 1$ nF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{PGATE} = 3.5$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$C_{PGATE} = 1$ nF</td>
<td>1.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{SS}$</td>
<td>Soft-start time</td>
<td></td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>$2.7$ V $&lt; V_{IN} &lt; 10$ V (EN Rising)</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{ONMIN}$</td>
<td>Minimum on-time</td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>PGATE Open</td>
<td>180</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{LVD}$</td>
<td>Undervoltage detection</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Measured at the FB Pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = 25^\circ C$</td>
<td>0.56</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$-40^\circ C$ to $+125^\circ C$</td>
<td>0.487</td>
<td>0.613</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.6 Typical Characteristics

Unless specified otherwise, all curves taken at $V_{IN} = 5$ V, $V_{OUT} = 2.5$ V, $L = 10 \mu$H, $C_{OUT} = 100 \mu$F, ESR = 100 mΩ, and $T_A = 25^\circ$C.
Typical Characteristics (continued)

Unless specified otherwise, all curves taken at \( V_{\text{IN}} = 5 \, \text{V} \), \( V_{\text{OUT}} = 2.5 \, \text{V} \), \( L = 10 \, \mu\text{H} \), \( C_{\text{OUT}} = 100 \, \mu\text{F} \), \( \text{ESR} = 100 \, \text{mΩ} \), and \( T_A = 25^\circ\text{C} \).

Figure 7. Start Up

Figure 8. Output Ripple Voltage
7 Detailed Description

7.1 Overview
The LM3475 is a buck (step-down) DC-DC controller that uses a hysteretic control architecture, which results in Pulse Frequency Modulated (PFM) regulation. The hysteretic control scheme does not utilize an internal oscillator. Switching frequency depends on external components and operating conditions. Operating frequency decreases at light loads, resulting in excellent efficiency compared to PWM architectures. Because switching is directly controlled by the output conditions, hysteretic control provides exceptional load transient response.

7.2 Functional Block Diagram

7.3 Feature Description
7.3.1 Hysteretic Control Circuit
The LM3475 uses a comparator-based voltage control loop. The voltage on the feedback pin is compared to a 0.8V reference with 21mV of hysteresis. When the FB input to the comparator falls below the reference voltage, the output of the comparator goes low. This results in the driver output, PGATE, pulling the gate of the PFET low and turning on the PFET.

With the PFET on, the input supply charges \( C_{OUT} \) and supplies current to the load through the PFET and the inductor. Current through the inductor ramps up linearly, and the output voltage increases. As the FB voltage reaches the upper threshold (reference voltage plus hysteresis) the output of the comparator goes high, and the PGATE turns the PFET off. When the PFET turns off, the catch diode turns on, and the current through the inductor ramps down. As the output voltage falls below the reference voltage, the cycle repeats. The resulting output, inductor current, and switch node waveforms are shown in Figure 9.
Feature Description (continued)

7.3.2 Soft-Start
The LM3475 includes an internal soft-start function to protect components from excessive inrush current and output voltage overshoot. As $V_{IN}$ rises above 2.7 V (typical), the internal bias circuitry becomes active. When EN goes high, the device enters soft-start. During soft-start, the reference voltage is ramped up to the nominal value of 0.8 V in approximately 4ms. Duty cycle and output voltage will increase as the reference voltage is ramped up.

7.3.3 Under Voltage Detection
When the output voltage falls below 70% (typical) of the normal voltage, as measured at the FB pin, the device turns off PFET and restarts a new soft-start cycle. In short circuit, the PFET is always on, and the converter is effectively a resistor divider from input to output to ground. Whether the part restarts depends on the power path resistance and the short circuit resistance. This feature should not be considered as overcurrent protection or output short circuit protection.

7.3.4 PGATE
During switching, the PGATE pin swings from $V_{IN}$ (off) to ground (on). As input voltage increases, the time it takes to slew the gate of the PFET on and off also increases. Also, as the PFET gate voltage approaches $V_{IN}$, the PGATE current driving capability decreases. This can cause a significant additional delay in turning the switch off when using a PFET with a low threshold voltage. These two effects will increase power dissipation and reduce efficiency. Therefore, a PFET with relatively high threshold voltage and low gate capacitance is recommended.

7.3.5 Minimum On or Off Time
To ensure accurate comparator switching, the LM3475 imposes a blanking time after each comparator state change. This blanking time is 180 ns typically. Immediately after the comparator goes high or low, it will be held in that state for the duration of the blanking time. This helps keep the hysteretic comparator from improperly responding to switching noise spikes (See Reducing Switching Noise) and ESL spikes (See Output Capacitor Selection) at the output.

At very low or very high duty cycle operation, maximum frequency will be limited by the blanking time. The maximum operating frequency can be determined by the following equations:

$$F_{MAX} = D / t_{on_{min}}$$
$$F_{MAX} = (1-D) / t_{off_{min}}$$

where

Figure 9. Hysteretic Waveforms
Feature Description (continued)

- D is the duty cycle, defined as $V_{OUT}/V_{IN}$, and $t_{on_{min}}$
- $t_{off_{min}}$ is the sum of the blanking time, the propagation delay time, and the PFET delay time (see Figure 9)  \(2\)

7.3.6 Enable Pin (EN)

The LM3475 provides a shutdown function via the EN pin to disable the device. The device is active when the EN pin is pulled above 1.5 V (typ) and in shutdown mode when EN is below 1.135 V (typ). In shutdown mode, total quiescent current is less than 10 µA. The EN pin can be directly connected to $V_{IN}$ for always-on operation.

7.4 Device Functional Modes

The LM3475 operates in discontinuous conduction mode at light load current and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the inductor starts at zero and ramps up to the peak, then ramps down to zero. The next cycle starts when the FB voltage reaches the reference voltage. Until then, the inductor current remains zero. Operating frequency is low, as are switching losses. In continuous conduction mode, current always flows through the inductor and never ramps down to zero.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The LM3475 employs a hysteretic control architecture; which provides excellent load transient response and efficiency even at light loads, as compared to its PWM architectures. No external compensation is required which results in a simple design and low component count. A typical schematic is described in the next section.

8.2 Typical Application

8.2.1 Design Requirements
To properly size the components for the application, the designer needs the following parameters: input voltage range, output voltage, output current range, and required switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior. Although hysteretic control is a simple control scheme, the operating frequency and other performance characteristics depend on external conditions and components. If the inductance, output capacitance, ESR, VIN, or Cff is changed, there will be a change in the operating frequency and possibly output ripple. Therefore, care must be taken to select components which will provide the desired operating range.

8.2.2 Detailed Design Procedure

Table 1. Bill of Materials

<table>
<thead>
<tr>
<th>DESIGNATOR</th>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>VENDOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{IN} )</td>
<td>10 ( \mu )F, 16 V, X5R</td>
<td>EMK325BJ106MN</td>
<td>TAIYO YUDEN</td>
</tr>
<tr>
<td>( C_{OUT} )</td>
<td>100 ( \mu )F, 6 V, Ta</td>
<td>TPSY107M006R0100</td>
<td>AVX</td>
</tr>
<tr>
<td>( C_{FF} )</td>
<td>1 ( n )F, 25 V, X7R</td>
<td>VJ1206Y102KXXA</td>
<td>Vishay</td>
</tr>
<tr>
<td>D1</td>
<td>Schottky, 20 V, 2 A</td>
<td>CMSH2-20L</td>
<td>Central Semiconductor</td>
</tr>
<tr>
<td>L1</td>
<td>10 ( \mu )H, 3.1 A</td>
<td>CDRH103R100</td>
<td>Sumida</td>
</tr>
<tr>
<td>Q1</td>
<td>30 ( \mu )V, 2.5 A</td>
<td>Si2343</td>
<td>Vishay</td>
</tr>
<tr>
<td>( R_{FB2} )</td>
<td>1 k( \Omega ), 0805, 1%</td>
<td>CRW08051001F</td>
<td>Vishay</td>
</tr>
<tr>
<td>( R_{FB1} )</td>
<td>2.15 k( \Omega ), 0805, 1%</td>
<td>CRCW08052151F</td>
<td>Vishay</td>
</tr>
</tbody>
</table>
8.2.2.1 Setting Output Voltage

The output voltage is programmed using a resistor divider between \( V_{\text{OUT}} \) and GND as shown in Figure 11. The feedback resistors can be calculated as follows:

\[
V_{\text{OUT}} = \frac{R_1 + R_2}{R_2} \times V_{\text{FB}}
\]

where
- \( V_{\text{FB}} \) is 0.8 V typically

The feedback resistor ratio, \( \alpha = \frac{R_1 + R_2}{R_2} \), will also be used below to calculate output ripple and operating frequency.

\[ V_{\text{OUT}} = \frac{R_1 + R_2}{R_2} \times V_{\text{FB}} \]

8.2.2.2 Setting Operating Frequency and Output Ripple

Although hysteretic control is a simple control scheme, the operating frequency and other performance characteristics depend on external conditions and components. If the inductance, output capacitance, ESR, \( V_{\text{IN}} \), or \( C_{\text{ff}} \) is changed, there will be a change in the operating frequency and possibly output ripple. Therefore, care must be taken to select components which will provide the desired operating range. The best approach is to determine what operating frequency is desirable in the application and then begin with the selection of the inductor and output capacitor ESR. The design process usually involves a few iterations to select appropriate standard values that will result in the desired frequency and ripple.

Without the feedforward capacitor (\( C_{\text{ff}} \)), the operating frequency (\( F \)) can be approximately calculated using the formula:

\[
F = \frac{R_1 + R_2}{R_2} \times \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times \text{ESR}}{(V_{\text{HYST}} \times \alpha \times L) + (V_{\text{IN}} \times \text{delay} \times \text{ESR})}
\]

where
- Delay is the sum of the LM3475 propagation delay time and the PFET delay time
- The propagation delay is 90ns typically

Minimum output ripple voltage can be determined using the following equation:

\[
V_{\text{OUT,PP}} = \frac{V_{\text{HYST}} (R_1 + R_2)}{R_2}
\]
8.2.2.3 Using a Feed-forward Capacitor

The operating frequency and output ripple voltage can also be significantly influenced using a speed up capacitor, \( C_{ff} \), as shown in Figure 11. \( C_{ff} \) is connected in parallel with the high side feedback resistor, \( R_1 \). The output ripple causes a current to be sourced or sunk through this capacitor. This current is essentially a square wave. Since the input to the feedback pin (FB) is a high impedance node, the bulk of the current flows through \( R_2 \). This superimposes a square wave ripple voltage on the FB node. The end result is a reduction in output ripple and an increase in operating frequency. When adding \( C_{ff} \), calculate the formula above with \( \alpha = 1 \). The value of \( C_{ff} \) depends on the desired operating frequency and the value of \( R_2 \). A good starting point is 1nF ceramic at 100kHz decreasing linearly with increased operating frequency. Also note that as the output voltage is programmed below 1.6V, the effect of \( C_{ff} \) will decrease significantly.

8.2.2.4 Inductor Selection

The most important parameters for the inductor are the inductance and the current rating. The LM3475 operates over a wide frequency range and can use a wide range of inductance values. Minimum inductance can be calculated using the following equation:

\[
L = \frac{V_{IN} - V_{SD} - V_{OUT}}{\Delta I} \times \frac{D}{F}
\]

where
- \( D \) is the duty cycle, defined as \( V_{OUT}/V_{IN} \)
- \( \Delta I \) is the allowable inductor ripple current

Maximum allowable inductor ripple current should be calculated as a function of output current (\( I_{OUT} \)) as shown below:

\[
\Delta I_{max} = I_{OUT} \times 0.3
\]

The inductor must also be rated to handle the peak current (\( I_{PK} \)) and RMS current given by:

\[
I_{PK} = (I_{OUT} + \Delta I/2) \times 1.1
\]

\[
I_{RMS} = \sqrt{I_{OUT}^2 + \Delta I^2/3}
\]

The inductance value and the resulting ripple is one of the key parameters controlling operating frequency.

8.2.2.5 Output Capacitor Selection

Once the desired operating frequency and inductance value are selected, ESR must be selected based on Equation 4. This process may involve a few iterations to select standard ESR and inductance values.

In general, the ESR of the output capacitor and the inductor ripple current create the output ripple of the regulator. However, the comparator hysteresis sets the first order value of this ripple. Therefore, as ESR and ripple current vary, operating frequency must also vary to keep the output ripple voltage regulated. The hysteretic control topology is well suited to using ceramic output capacitors. However, ceramic capacitors have a very low ESR, resulting in a 90° phase shift of the output voltage ripple. This results in low operating frequency and increased output ripple. To fix this problem a low value resistor could be added in series with the ceramic output capacitor. Although counter intuitive, this combination of a ceramic capacitor and external series resistance provide highly accurate control over the output voltage ripple. Another method is to add an external ramp at the FB pin as shown in Figure 12. By proper selection of \( R_1 \) and \( C_2 \), the FB pin sees faster voltage change than the output ripple can cause. As a result, the switching frequency is higher while the output ripple becomes lower. The switching frequency is approximately:

\[
F = \frac{V_{IN}}{2\pi \times R_1 \times C_2 \times V_{HYS}}
\]

Other types of capacitor, such as Sanyo POSCAP, OS-CON, and Nichicon ‘NA’ series are also recommended and may be used without additional series resistance. For all practical purposes, any type of output capacitor may be used with proper circuit verification.
Capacitors with high ESL (equivalent series inductance) values should not be used. As shown in Figure 9, the output ripple voltage contains a small step at both the high and low peaks. This step is caused by and is directly proportional to the output capacitor’s ESL. A large ESL, such as in an electrolytic capacitor, can create a step large enough to cause abnormal switching behavior.

**8.2.2.6 Input Capacitor Selection**

A bypass capacitor is required between VIN and ground. It must be placed near the source of the external PFET. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on. The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manufacturer’s recommended voltage de-rating. RMS current and power dissipation (PD) can be calculated with the equations below:

\[
I_{\text{RMS,CIN}} = \frac{I_{\text{OUT}}}{V_{\text{IN}}} \sqrt{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}
\]

(10)

**8.2.2.7 Diode Selection**

The catch diode provides the current path to the load during the PFET off time. Therefore, the current rating of the diode must be higher than the average current through the diode, which be calculated as shown:

\[
I_{\text{D,AVE}} = I_{\text{OUT}} \times (1 - D)
\]

(11)

The peak voltage across the catch diode is approximately equal to the input voltage. Therefore, the diode’s peak reverse voltage rating should be greater than 1.3 times the input voltage.

A Schottky diode is recommended, since a low forward voltage drop will improve efficiency.

For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

**8.2.2.8 P-Channel MOSFET Selection**

The PFET switch should be selected based on the maximum Drain-Source voltage (VDS), Drain current rating (ID), maximum Gate-Source voltage (VGS), on resistance (RDSON), and Gate capacitance. The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The VDS must be selected to provide some margin beyond the sum of the input voltage and Vd.

Since the current flowing through the PFET is equal to the current through the inductor, ID must be rated higher than the maximum IPK. During switching, PGATE swings the PFET’s gate from VIN to ground. Therefore, A PFET must be selected with a maximum VGS larger than VIN. To insure that the PFET turns on completely and quickly, refer to the PGATE section.

![Figure 12. External Ramp](image-url)
The power loss in the PFET consists of switching losses and conducting losses. Although switching losses are difficult to precisely calculate, the equation below can be used to estimate total power dissipation. Increasing $R_{DSON}$ will increase power losses and degrade efficiency. Note that switching losses will also increase with lower gate threshold voltages.

$$ PD_{\text{switch}} = R_{DSON} \times (I_{OUT})^2 \times D + F \times I_{OUT} \times V_{IN} \times (t_{on} + t_{off})/2 $$

where

- $t_{on} = \text{FET turn on time}$
- $t_{off} = \text{FET turn off time}$
- A value of 10ns to 50ns is typical for $t_{on}$ and $t_{off}$

Note that the $R_{DSON}$ has a positive temperature coefficient. At 100°C, the $R_{DSON}$ may be as much as 150% higher than the value at 25°C.

The Gate capacitance of the PFET has a direct impact on both PFET transition time and the power dissipation in the LM3475. Most of the power dissipated in the LM3475 is used to drive the PFET switch. This power can be calculated as follows:

The amount of average gate driver current required during switching ($I_G$) is:

$$ I_G = Q_g \times F $$

And the total power dissipated in the device is:

$$ I_qu \times V_{IN} + I_G \times V_{IN} $$

where

- $I_q$ is typically 260µA as shown in Electrical Characteristics

As gate capacitance increases, operating frequency may need to be reduced, or additional heat sinking may be required to lower the power dissipation in the device.

In general, keeping the gate capacitance below 2000 pF is recommended to keep transition times (switching losses), and power losses low.

### 8.2.2.9 Reducing Switching Noise

Although the LM3475 employs internal noise suppression circuitry, external noise may continue to be excessive. There are several methods available to reduce noise and EMI.

MOSFETs are very fast switching devices. The fast increase in PFET current coupled with parasitic trace inductance can create unwanted noise spikes at both the switch node and at $V_{IN}$. Switching noise will increase with load current and input voltage. This noise can also propagate through the ground plane, sometimes causing unpredictable device performance. Slowing the rise and fall times of the PFET can be very effective in reducing this noise. Referring to Figure 13, the PFET can be slowed down by placing a small (1-Ω to 10-Ω) resistor in series with PGATE. However, this resistor will increase the switching losses in the PFET and will lower efficiency. Therefore it should be kept as small as possible and only used when necessary. Another method to reduce switching noise (other than good PCB layout, see Layout) is to use a small RC filter or snubber. The snubber should be placed in parallel with the catch diode, connected close to the drain of the PFET, as shown in Figure 13. Again, the snubber should be kept as small as possible to limit its impact on system efficiency. A typical range is a 10-Ω to 100-Ω resistor and a 470-pF to 2.2-nF ceramic capacitor.

![Figure 13. PGATE Resistor and Snubber](image-url)
8.2.3 Application Curves

![Figure 14. Load Transient Response with External Ramp](image)

![Figure 15. Load Transient Response](image)

9 Power Supply Recommendations

The LM3475 controller is designed to operate from various DC power supplies. VIN input should be protected from reversal voltage and voltage dump over 16 volts. The impedance of the input supply rail should be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

10 Layout

10.1 Layout Guidelines

PC board layout is very important in all switching regulator designs. Poor layout can cause EMI problems, excess switching noise and poor operation.

As shown in Figure 16, place the ground of the input capacitor as close as possible to the anode of the diode. This path also carries a large AC current. The switch node, the node connecting the diode cathode, inductor, and PFET drain, should be kept as small as possible. This node is one of the main sources for radiated EMI.

The feedback pin is a high impedance node and is therefore sensitive to noise. Be sure to keep all feedback traces away from the inductor and the switch node, which are sources of noise. Also, the resistor divider should be placed close to the FB pin. The gate pin of the external PFET should be located close to the PGATE pin.

TI also recommends using a large, continuous ground plane, particularly in higher current applications.
10.2 Layout Example

Figure 16. Layout Example (2:1 Scale)
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI’s publication of information regarding third-party products or services does not constitute an endorsement regarding the suitability of such products or services or a warranty, representation or endorsement of such products or services, either alone or in combination with any TI product or service.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

**TI E2E™ Online Community**  *TI’s Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI’s Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3475MF/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>S6SB</td>
<td>Samples</td>
</tr>
<tr>
<td>LM3475MFX/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>S6SB</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
In no event shall TI’s liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3475MF/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LM3475MFX/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>Device</td>
<td>Package Type</td>
<td>Package Drawing</td>
<td>Pins</td>
<td>SPQ</td>
<td>Length (mm)</td>
<td>Width (mm)</td>
<td>Height (mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>----------------</td>
<td>--------------</td>
<td>-----------------</td>
<td>------</td>
<td>------</td>
<td>-------------</td>
<td>------------</td>
<td>-------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM3475MF/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LM3475MFX/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and/or implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designers represent that, with respect to their applications, Designers have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designers agree that prior to using or distributing any applications that include TI products, Designers will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY TECHNOLOGY, INTELLECTUAL PROPERTY RIGHT OR ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.