**1 Features**
- Drives up to 2 Strings of 10 Series LEDs
- Wide 2.3-V to 5.5-V Input Voltage Range
- Up to 87% Efficient
- 8-bit \( \text{i}^2\text{C} \)-Compatible Programmable Exponential or Linear Brightness Control
- PWM Brightness Control for CABC Operation
- Independent Current Control per String
- True Shutdown Isolation for LEDs
- Internal Soft-Start Limits Inrush Current
- Adaptive Headroom
- Programmable 16-V/24-V/32-V/40-V Overvoltage Protection
- Selectable Boost Frequency of 500 kHz or 1 MHz with Optionally Additional Offset
- Low Profile 12-Pin DSBGA Package
- Solution Size 32 mm²

**2 Applications**
- Smart-Phone LCD Backlighting
- LCD and Keypad Lighting

**3 Description**
The LM3630A is a current-mode boost converter which supplies the power and controls the current in up to two strings of 10 LEDs per string. Programming is done over an \( \text{i}^2\text{C} \)-compatible interface. The maximum LED current is adjustable from 5 mA to 28.5 mA. At any given maximum LED current the LED brightness is further adjusted with 256 exponential or linear dimming steps. Additionally, pulsed width modulation (PWM) brightness control can be enabled allowing for LED current adjustment by a logic level PWM signal.

The boost switching frequency is programmable at 500 kHz for low switching loss performance or 1 MHz to allow the use of tiny low-profile inductors. A setting for a 10% offset of these frequencies is available. Overvoltage protection is programmable at 16 V, 24 V, 32 V, or 40 V to accommodate a wide variety of LED configurations and Schottky diode/output capacitor combinations.

The device operates over a 2.3-V to 5.5-V operating voltage range and –40°C to +85°C ambient temperature range. The LM3630A is available in an ultra-small 12-bump DSBGA package.

**Device Information**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (MAX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3630A</td>
<td>DSBGA (12)</td>
<td>1.94 mm × 1.42 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## Changes from Revision A (January 2014) to Revision B

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Added Device Information and Pin Configuration and Functions sections, ESD Rating table, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information sections</td>
<td>1</td>
</tr>
</tbody>
</table>

## Changes from Original (April 2013) to Revision A

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed equation in note 2 of Electrical Char table</td>
<td>5</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

**YFQ Package 12-Pin DSBGA Top View**

- **A1 SDA** Input/Output: Serial data connection for I²C-compatible interface
- **A2 SCL** Input: Serial clock connection for I²C-compatible interface
- **A3 SW** PWR: Inductor connection, diode anode connection, and drain connection for internal NFET. Connect the inductor and diode as close as possible to SW to reduce inductance and capacitive coupling to nearby traces.
- **B1 HWEN** Input: Logic high hardware enable
- **B2 INTN** Output: Interrupt output for fault status change. Open drain active low signal.
- **B3 GND** GND: Ground
- **C1 PWM** Input: External PWM brightness control input
- **C2 SEL** Input: Selects I²C-compatible address. Ground selects 7-bit address 36h. $V_{IN}$ selects address 38h.
- **C3 IN** Input: Input voltage connection. Connect a 2.3-V to 5.5-V supply to IN and bypass to GND with a 2.2-µF or greater ceramic capacitor.
- **D1 OVP** Input: Output voltage sense connection for overvoltage sensing. Connect OVP to the positive terminal of the output capacitor.
- **D2 ILED2** Input: Input terminal to internal current sink 2.
- **D3 ILED1** Input: Input terminal to internal current sink 1.

**YFQ Package 12-Pin DSBGA Bottom View**

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>SDA</td>
<td>Input/Output</td>
<td>Serial data connection for I²C-compatible interface</td>
</tr>
<tr>
<td>A2</td>
<td>SCL</td>
<td>Input</td>
<td>Serial clock connection for I²C-compatible interface</td>
</tr>
<tr>
<td>A3</td>
<td>SW</td>
<td>PWR</td>
<td>Inductor connection, diode anode connection, and drain connection for internal NFET. Connect the inductor and diode as close as possible to SW to reduce inductance and capacitive coupling to nearby traces.</td>
</tr>
<tr>
<td>B1</td>
<td>HWEN</td>
<td>Input</td>
<td>Logic high hardware enable</td>
</tr>
<tr>
<td>B2</td>
<td>INTN</td>
<td>Output</td>
<td>Interrupt output for fault status change. Open drain active low signal.</td>
</tr>
<tr>
<td>B3</td>
<td>GND</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>C1</td>
<td>PWM</td>
<td>Input</td>
<td>External PWM brightness control input</td>
</tr>
<tr>
<td>C2</td>
<td>SEL</td>
<td>Input</td>
<td>Selects I²C-compatible address. Ground selects 7-bit address 36h. $V_{IN}$ selects address 38h.</td>
</tr>
<tr>
<td>C3</td>
<td>IN</td>
<td>Input</td>
<td>Input voltage connection. Connect a 2.3-V to 5.5-V supply to IN and bypass to GND with a 2.2-µF or greater ceramic capacitor.</td>
</tr>
<tr>
<td>D1</td>
<td>OVP</td>
<td>Input</td>
<td>Output voltage sense connection for overvoltage sensing. Connect OVP to the positive terminal of the output capacitor.</td>
</tr>
<tr>
<td>D2</td>
<td>ILED2</td>
<td>Input</td>
<td>Input terminal to internal current sink 2.</td>
</tr>
<tr>
<td>D3</td>
<td>ILED1</td>
<td>Input</td>
<td>Input terminal to internal current sink 1.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>−0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>−0.3</td>
<td>45</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the potential at the GND pin.

(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J = 140°C$ (typical) and disengages at $T_J = 125°C$ (typical).

(4) For detailed soldering specifications and information, refer to Texas Instruments Application Note 1112: DSBGA Wafer Level Chip Scale Package (SNVA009).

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.3</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>−40</td>
<td>85</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC$^{(1)}$</th>
<th>LM3630A</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$</td>
<td>78.1</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics

Typical limits are for \( T_A = 25°C \); minimum and maximum limits apply over the full operating ambient temperature range \((-40°C \leq T_A \leq 85°C)\); \( V_{IN} = 3.6 \text{ V} \), unless otherwise specified.\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>ILED1, ILED2</td>
<td>Output current regulation</td>
<td>2.5 V ≤ ( V_{IN} ) ≤ 5.5 V, full-scale current = 20 mA</td>
<td>19</td>
<td>20</td>
<td>21</td>
</tr>
<tr>
<td>( I_{MATCH} )</td>
<td>ILED1 to ILED2 current matching (^{(2)})</td>
<td>ILED1 on A</td>
<td>ILED2 on B</td>
<td>( -1% )</td>
<td>0.5%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 2.5 \text{ V} \leq ( V_{IN} ) \leq 5.5 \text{ V}, ; I_{LED} = 10 \text{ mA}, ; T_A = 25°C )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 0°C \leq T_A \leq 70°C )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{REG_{CS}} )</td>
<td>Regulated current sink headroom voltage</td>
<td>( I_{LED} = 5 \text{ mA} )</td>
<td>250</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_{HR} )</td>
<td>Current sink minimum headroom voltage</td>
<td>( I_{LED} = 95% ) of nominal, ( I_{LED} = 20 \text{ mA} )</td>
<td>160</td>
<td>240</td>
<td></td>
</tr>
<tr>
<td>( R_{DSON} )</td>
<td>NMOS switch on resistance</td>
<td>( I_{SW} = 100 \text{ mA} )</td>
<td>0.25</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>( I_{CL} )</td>
<td>NMOS switch current limit</td>
<td>2.5 V ≤ ( V_{IN} ) ≤ 5.5 V</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( V_{OVP} )</td>
<td>Output overvoltage protection</td>
<td>ON threshold, 2.3 V ≤ ( V_{IN} ) ≤ 5.5 V</td>
<td>( 24\text{-V option} )</td>
<td>23</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ON threshold, 2.3 V ≤ ( V_{IN} ) ≤ 5.5 V</td>
<td>( 40\text{-V option} )</td>
<td>39</td>
<td>41</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysteresis</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>( f_{SW} )</td>
<td>Switching frequency</td>
<td>2.5 V ≤ ( V_{IN} ) ≤ 5.5 V</td>
<td>( 560\text{-kHz shift} = 1 )</td>
<td>538</td>
<td>560</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 500\text{-kHz shift} = 0 )</td>
<td>481</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 1.12\text{-MHz shift} = 1 )</td>
<td>1077</td>
<td>1120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 1\text{-MHz shift} = 0 )</td>
<td>962</td>
<td>1000</td>
</tr>
<tr>
<td>( D_{MAX} )</td>
<td>Maximum duty cycle</td>
<td></td>
<td></td>
<td></td>
<td>94%</td>
</tr>
<tr>
<td>( I_Q )</td>
<td>Quiescent current into device, not switching</td>
<td>( V_{IN} = 3.6 \text{ V} )</td>
<td>( I_{LED1} = I_{LED2} = 20 \text{ mA}, ) feedback disabled.</td>
<td>350</td>
<td></td>
</tr>
<tr>
<td>( I_{SHDN} )</td>
<td>Shutdown current</td>
<td>2.3 V ≤ ( V_{IN} ) ≤ 5.5 V</td>
<td>HWEN = ( V_{IN} ), ( \text{I}^2\text{C} ) shutdown</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>HWEN = GND</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>( I_{LED_{MIN}} )</td>
<td>Minimum LED current in ILED1 or ILED2</td>
<td>Full-scale current = 20 mA, BRT = 0x01, Exponential mapping mode</td>
<td></td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>( T_{SD} )</td>
<td>Thermal shutdown</td>
<td></td>
<td></td>
<td>140</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td></td>
<td></td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>( I_{WAIT} )</td>
<td>Initialization timing</td>
<td>Time period to wait from the assertion of HWEN or after software reset, before an ( \text{I}^2\text{C} ) transaction will be ACK'ed. During this time period an ( \text{I}^2\text{C} ) transaction will be NAK'ed</td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Minimum and maximum limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: \( V_{IN} = 3.6 \text{ V} \) and \( T_A = 25°C \).

\(^{(2)}\) LED current sink matching between LED1 and LED2 is given by taking the difference between \( I_{LED1} \) and \( I_{LED2} \) and dividing by the sum of \( I_{LED1} \) and \( I_{LED2} \). The formula is \((I_{LED1} - I_{LED2})/(I_{LED1} + I_{LED2})\) at \( I_{LED} = 10 \text{ mA} \). \( I_{LED1} \) is driven by Bank A and \( I_{LED2} \) is driven by Bank B.
Electrical Characteristics (continued)

Typical limits are for $T_A = 25^\circ C$; minimum and maximum limits apply over the full operating ambient temperature range ($-40^\circ C \leq T_A \leq 85^\circ C$); $V_{IN} = 3.6 \text{ V}$, unless otherwise specified.\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOGIC INPUTS (PWM, HWEN, SEL, SCL, SDA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input logic low</td>
<td>2.3 V $\leq$ $V_{IN}$ $\leq$ 5.5 V</td>
<td>0</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input logic high</td>
<td>2.3 V $\leq$ $V_{IN}$ $\leq$ 5.5 V</td>
<td>1.2</td>
<td>$V_{IN}$</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output logic low (SDA, INTN)</td>
<td>2.3 V $\leq$ $V_{IN}$ $\leq$ 5.5 V</td>
<td>400</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$f_{PWM}$</td>
<td>PWM input frequency</td>
<td>2.3 V $\leq$ $V_{IN}$ $\leq$ 5.5 V</td>
<td>10</td>
<td>80</td>
<td>kHz</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input capacitance</td>
<td>SDA</td>
<td>4.5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SCL</td>
<td>5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6.6 \text{I^2C-Compatible Timing Requirements (SCL, SDA)}

See\(^{(1)}\).

| $t_1$ | SCL (clock period) | 2.5 |      | μs   |
| $t_2$ | Data in setup time to SCL high | 100 |      |      |
| $t_3$ | Data in setup time to SCL low | 0 |      | ns   |
| $t_4$ | SDA low setup time to SCL low (start) | 100 |      |      |
| $t_5$ | SDA high hold time to SCL high (stop) | 100 |      |      |

\(^{(1)}\) SCL and SDA must be glitch-free in order for proper brightness to be realized.
6.7 Typical Characteristics

$T_A = 25^\circ C$, $I_{LED}$ full-scale = 20 mA, unless specified otherwise.

**Figure 1. Boost and LED Efficiency**

$V_{IN} = 2.5\, V$
Frequency = 500 kHz

**Figure 2. Boost and LED Efficiency**

$V_{IN} = 2.7\, V$
Frequency = 500 kHz

**Figure 3. Boost and LED Efficiency**

$V_{IN} = 3.6\, V$
Frequency = 500 kHz

**Figure 4. Boost and LED Efficiency**

$V_{IN} = 4.2\, V$
Frequency = 500 kHz

**Figure 5. Boost and LED Efficiency**

$V_{IN} = 5.5\, V$
Frequency = 500 kHz

**Figure 6. Boost and LED Efficiency**

$V_{IN} = 2.5\, V$
Frequency = 500 kHz
Typical Characteristics (continued)

\( T_A = 25^\circ C, \ V_{\text{LED}} \text{ full-scale} = 20 \ mA, \) unless specified otherwise.

- **Figure 7. Boost and LED Efficiency**
  - \( V_{\text{IN}} = 2.7 \ V \)
  - Frequency = 500 kHz
  - 2p6s
  - \( L = 10 \ \mu\text{H} \)

- **Figure 8. Boost and LED Efficiency**
  - \( V_{\text{IN}} = 3.6 \ V \)
  - Frequency = 500 kHz
  - 2p6s
  - \( L = 10 \ \mu\text{H} \)

- **Figure 9. Boost and LED Efficiency**
  - \( V_{\text{IN}} = 4.2 \ V \)
  - Frequency = 500 kHz
  - 2p6s
  - \( L = 10 \ \mu\text{H} \)

- **Figure 10. Boost and LED Efficiency**
  - \( V_{\text{IN}} = 5.5 \ V \)
  - Frequency = 500 kHz
  - 2p6s
  - \( L = 10 \ \mu\text{H} \)

- **Figure 11. Boost and LED Efficiency**
  - \( V_{\text{IN}} = 2.5 \ V \)
  - Frequency = 500 kHz
  - 1p10s
  - \( L = 22 \ \mu\text{H} \)

- **Figure 12. Boost and LED Efficiency**
  - \( V_{\text{IN}} = 2.7 \ V \)
  - Frequency = 500 kHz
  - 1p10s
  - \( L = 22 \ \mu\text{H} \)
Typical Characteristics (continued)

\[ T_A = 25^\circ C, \ I_{\text{LED}} \ \text{full-scale} = 20 \ mA, \ \text{unless specified otherwise.} \]

\[ V_{\text{IN}} = 3.6 \ V \quad 1\text{p10s} \quad L = 22 \ \mu H \]
\[ V_{\text{IN}} = 4.2 \ V \quad 1\text{p10s} \quad L = 22 \ \mu H \]
\[ V_{\text{IN}} = 5.5 \ V \quad 1\text{p10s} \quad L = 22 \ \mu H \]
\[ V_{\text{IN}} = 2.5 \ V \quad 1\text{p10s} \quad L = 10 \ \mu H \]

Figure 13. Boost and LED Efficiency

Figure 14. Boost and LED Efficiency

Figure 15. Boost and LED Efficiency

Figure 16. Boost and LED Efficiency

Figure 17. Boost and LED Efficiency

Figure 18. Boost and LED Efficiency
Typical Characteristics (continued)

$T_A = 25^\circ C$, $I_{LED}$ full-scale $= 20$ mA, unless specified otherwise.

![Figure 19. Boost and LED Efficiency](image1)

$V_{IN} = 4.2$ V
Frequency $= 500$ kHz

$V_{IN} = 5.5$ V
Frequency $= 500$ kHz

![Figure 20. Boost and LED Efficiency](image2)

$V_{IN} = 2.5$ V
Frequency $= 1$ MHz

$V_{IN} = 2.7$ V
Frequency $= 1$ MHz

![Figure 21. Boost and LED Efficiency](image3)

$V_{IN} = 3.6$ V
Frequency $= 1$ MHz

$V_{IN} = 4.2$ V
Frequency $= 1$ MHz

![Figure 22. Boost and LED Efficiency](image4)

![Figure 23. Boost and LED Efficiency](image5)

![Figure 24. Boost and LED Efficiency](image6)
Typical Characteristics (continued)

\( T_A = 25^\circ \text{C}, \ I_{\text{LED}} \ \text{full-scale} = 20 \ \text{mA}, \) unless specified otherwise.

\[
\begin{array}{c|c|c|c|c|c}
\hline
\text{V}_{\text{IN}} & \text{Frequency} & \text{LED} & L & \text{Efficiency} \% & \text{Brightness} \% \\
5.5 \text{ V} & 1 \ \text{MHz} & 2p10s & 10 \ \mu\text{H} & 90 & 50 \\
2.7 \text{ V} & 500 \ \text{kHz} & 2p10s & 10 \ \mu\text{H} & 80 & 60 \\
3.6 \text{ V} & 500 \ \text{kHz} & 2p10s & 10 \ \mu\text{H} & 70 & 70 \\
4.2 \text{ V} & 500 \ \text{kHz} & 2p10s & 10 \ \mu\text{H} & 60 & 80 \\
5.5 \text{ V} & 500 \ \text{kHz} & 2p10s & 10 \ \mu\text{H} & 50 & 90 \\
\hline
\end{array}
\]

Figure 25. Boost and LED Efficiency

Figure 26. Boost and LED Efficiency

Figure 27. Boost and LED Efficiency

Figure 28. Boost and LED Efficiency

Figure 29. Boost and LED Efficiency

Figure 30. \( I_{\text{IN}} \) Across \( V_{\text{IN}} \)
Typical Characteristics (continued)

$T_A = 25^\circ C$, $I_{LED}$ full-scale = 20 mA, unless specified otherwise.

---

**Figure 31. $P_{WR_IN}$ Across $V_{IN}$**

$I_{LED}$ Full Scale = 28.5 mA
Frequency = 500 kHz
2p6s  L = 10 µH

---

**Figure 32. $V_{OUT}$ Across $V_{IN}$**

$I_{LED}$ Full Scale = 28.5 mA
Frequency = 500 kHz
2p6s  L = 10 µH

---

**Figure 33. $I_{OUT}$ Across $V_{IN}$**

$I_{LED}$ Full Scale = 28.5 mA
Frequency = 500 kHz
2p6s  L = 10 µH

---

**Figure 34. $P_{WR_OUT}$ Across $V_{IN}$**

$I_{LED}$ Full Scale = 28.5 mA
Frequency = 500 kHz
2p6s  L = 10 µH

---

**Figure 35. $I_{LED}$ Across $V_{IN}$**

$I_{LED}$ Full Scale = 28.5 mA
Frequency = 500 kHz
2p6s  L = 10 µH

---

**Figure 36. $I_{INDUCTOR}$ Across $V_{IN}$**

$I_{LED}$ Full Scale = 28.5 mA
Frequency = 500 kHz
2p6s  L = 10 µH
Typical Characteristics (continued)

\[ T_A = 25^\circ C, \quad I_{\text{LED}} \text{ full-scale} = 20 \text{ mA}, \quad \text{unless specified otherwise.} \]

\[ I_{\text{LED}} \text{ Full Scale} = 28.5 \text{ mA} \]

- LED1 on DACA
- LED2 on DACB
- Frequency = 500 kHz
- \( L = 10 \mu \text{H} \)

**Figure 37. I_IN Across V_IN**

**Figure 38. PWR_IN Across V_IN**

**Figure 39. V_OUT Across V_IN**

**Figure 40. I_OUT Across V_IN**

**Figure 41. PWR_OUT Across V_IN**

**Figure 42. I_LED Across V_IN**
Typical Characteristics (continued)

\( T_A = 25^\circ C, \ I_{LED} \) full-scale = 20 mA, unless specified otherwise.

\[\begin{array}{|c|c|c|}
\hline
\text{2.7V} & \text{LED1 DACA} & \text{2p6s, L=10uH, Freq=500kHz} \\
\text{3.05V} & \text{LED2 DACB} & \\
\text{3.6V} & \text{I_{Inductor} vs VIN} & \\
\text{4.2V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\text{5.5V} & \text{LED1 on DACA} & \\
\hline
\end{array}\]

\[\begin{array}{|c|c|c|}
\hline
\text{2.7V} & \text{LED1 & 2 on DACA} & \text{2p10s, L=10uH, Freq=1MHz} \\
\text{3.05V} & \text{PWR_IN vs VIN} & \\
\text{3.6V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\text{4.2V} & \text{LED1 and LED2 on DACA} & \\
\text{5.5V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\hline
\end{array}\]

\[\begin{array}{|c|c|c|}
\hline
\text{2.7V} & \text{VOUT vs VIN} & \text{LED1 & 2 on DACA} \\
\text{3.05V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\text{3.6V} & \text{LED1 and LED2 on DACA} & \\
\text{4.2V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\text{5.5V} & \text{LED1 and LED2 on DACA} & \\
\hline
\end{array}\]

\[\begin{array}{|c|c|c|}
\hline
\text{2.7V} & \text{I_{Inductor} vs VIN} & \text{LED1 DACA} \\
\text{3.05V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\text{3.6V} & \text{LED2 on DACB} & \\
\text{4.2V} & \text{Frequency = 1 MHz} & \\
\text{5.5V} & \text{2p10s, L = 10 µH} & \\
\hline
\end{array}\]

\[\begin{array}{|c|c|c|}
\hline
\text{2.7V} & \text{PWR_OUT vs VIN} & \text{LED1 & 2 on DACA} \\
\text{3.05V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\text{3.6V} & \text{LED1 and LED2 on DACA} & \\
\text{4.2V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\text{5.5V} & \text{LED1 and LED2 on DACA} & \\
\hline
\end{array}\]

\[\begin{array}{|c|c|c|}
\hline
\text{2.7V} & \text{I_{Inductor} vs VIN} & \text{LED1 DACA} \\
\text{3.05V} & \text{I_{LED} Full Scale = 28.5 mA} & \\
\text{3.6V} & \text{LED2 DACB} & \\
\text{4.2V} & \text{Frequency = 500 kHz} & \\
\text{5.5V} & \text{2p6s} & \\
\hline
\end{array}\]

Figure 43. \( I_{Inductor} \) Across \( V_{IN} \)

Figure 44. \( I_{IN} \) Across \( V_{IN} \)

Figure 45. PWR_IN Across \( V_{IN} \)

Figure 46. VOUT Across \( V_{IN} \)

Figure 47. IOUT Across \( V_{IN} \)

Figure 48. PWR_OUT Across \( V_{IN} \)
Typical Characteristics (continued)

**T_A = 25°C, I_{LED} full-scale = 20 mA, unless specified otherwise.**

- **Figure 49. I_{LED} Across V_{IN}**
  - I_{LED} Full Scale = 28.5 mA
  - LED1 and LED2 on DACA
  - Frequency = 1 MHz
  - L = 10 µH

- **Figure 50. I_{INDUCTOR} Across V_{IN}**
  - I_{LED} Full Scale = 28.5 mA
  - LED1 and LED2 on DACA
  - Frequency = 1 MHz
  - L = 10 µH

- **Figure 51. I_{IN} Across V_{IN}**
  - I_{LED} Full Scale = 28.5 mA
  - LED1 on DACA
  - LED2 on DACB
  - Frequency = 1 MHz
  - L = 10 µH

- **Figure 52. PWR_IN Across V_{IN}**
  - I_{LED} Full Scale = 28.5 mA
  - LED1 on DACA
  - LED2 on DACB
  - Frequency = 1 MHz
  - L = 10 µH

- **Figure 53. V_{OUT} Across V_{IN}**
  - I_{LED} Full Scale = 28.5 mA
  - LED1 on DACA
  - LED2 on DACB
  - Frequency = 1 MHz
  - L = 10 µH

- **Figure 54. I_{OUT} Across V_{IN}**
  - I_{LED} Full Scale = 28.5 mA
  - LED1 on DACA
  - LED2 on DACB
  - Frequency = 1 MHz
  - L = 10 µH
Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $I_{LED}$ full-scale = 20 mA, unless specified otherwise.

**Figure 55. PWR_OUT Across $V_{IN}$**

- $I_{LED}$ Full Scale = 28.5 mA
- LED1 on DACA
- 2p10s
- Frequency = 1 MHz
- LED2 on DACB
- $L = 10 \mu\text{H}$

**Figure 56. $I_{LED}$ Across $V_{IN}$**

- $I_{LED}$ Full Scale = 28.5 mA
- LED1 on DACA
- 2p10s
- Frequency = 1 MHz
- LED2 on DACB
- $L = 10 \mu\text{H}$

**Figure 57. $I_{INDUCTOR}$ Across $V_{IN}$**

- $I_{LED}$ Full Scale = 28.5 mA
- LED1 on DACA
- 2p10s
- Frequency = 1 MHz
- LED2 on DACB
- $L = 10 \mu\text{H}$

**Figure 58. $I_{IN}$ Across $V_{IN}$**

- $I_{LED}$ Full Scale = 28.5 mA
- LED1 and LED2 on DACA
- Frequency = 500 kHz
- 2p6s
- $L = 22 \mu\text{H}$

**Figure 59. PWR_IN Across $V_{IN}$**

- $I_{LED}$ Full Scale = 28.5 mA
- LED1 and LED2 on DACA
- Frequency = 500 kHz
- 2p6s
- $L = 22 \mu\text{H}$

**Figure 60. VOUT Across $V_{IN}$**

- $I_{LED}$ Full Scale = 28.5 mA
- LED1 and LED2 on DACA
- Frequency = 500 kHz
- 2p6s
- $L = 22 \mu\text{H}$
Typical Characteristics (continued)

\( T_A = 25^\circ C, \) \( I_{LED} \) full-scale = 20 mA, unless specified otherwise.

- **Figure 61.** \( I_{OUT} \) Across \( V_{IN} \)
- **Figure 62.** \( PWR_{OUT} \) Across \( V_{IN} \)
- **Figure 63.** \( I_{LED} \) Across \( V_{IN} \)
- **Figure 64.** \( I_{INDUCTOR} \) Across \( V_{IN} \)
- **Figure 65.** \( I_{IN} \) Across \( V_{IN} \)
- **Figure 66.** \( PWR_{IN} \) Across \( V_{IN} \)

**Typical Characteristics**

- **Figure 61.** \( I_{OUT} \) Across \( V_{IN} \)
  - Full Scale: 28.5 mA
  - Frequency: 500 kHz
  - Components: LED1 and LED2 on DACA
  - L = 22 \( \mu \)H

- **Figure 62.** \( PWR_{OUT} \) Across \( V_{IN} \)
  - Full Scale: 28.5 mA
  - Frequency: 500 kHz
  - Components: LED1 and LED2 on DACA
  - L = 22 \( \mu \)H

- **Figure 63.** \( I_{LED} \) Across \( V_{IN} \)
  - Full Scale: 28.5 mA
  - Frequency: 500 kHz
  - Components: LED1 and LED2 on DACA
  - L = 22 \( \mu \)H

- **Figure 64.** \( I_{INDUCTOR} \) Across \( V_{IN} \)
  - Full Scale: 28.5 mA
  - Frequency: 500 kHz
  - Components: LED1 and LED2 on DACA
  - L = 22 \( \mu \)H

- **Figure 65.** \( I_{IN} \) Across \( V_{IN} \)
  - Full Scale: 28.5 mA
  - Frequency: 500 kHz
  - Components: LED1 on DACA, LED2 on DACB
  - L = 22 \( \mu \)H

- **Figure 66.** \( PWR_{IN} \) Across \( V_{IN} \)
  - Full Scale: 28.5 mA
  - Frequency: 500 kHz
  - Components: LED1 on DACA, LED2 on DACB
  - L = 22 \( \mu \)H
**Typical Characteristics (continued)**

\( T_A = 25^\circ C, \) \( I_{LED} \) full-scale = 20 mA, unless specified otherwise.

### Figure 67. \( V_{OUT} \) Across \( V_{IN} \)

- \( I_{LED} \) Full Scale = 28.5 mA
- LED1 on DACA
- LED2 on DACB
- Frequency = 500 kHz
- \( L = 22 \mu H \)

### Figure 68. \( I_{OUT} \) Across \( V_{IN} \)

- \( I_{LED} \) Full Scale = 28.5 mA
- LED1 on DACA
- LED2 on DACB
- Frequency = 500 kHz
- \( L = 22 \mu H \)

### Figure 69. \( PWR\_OUT \) Across \( V_{IN} \)

- \( I_{LED} \) Full Scale = 28.5 mA
- LED1 on DACA
- LED2 on DACB
- Frequency = 500 kHz
- \( L = 22 \mu H \)

### Figure 70. \( I_{LED} \) Across \( V_{IN} \)

- \( I_{LED} \) Full Scale = 28.5 mA
- LED1 on DACA
- LED2 on DACB
- Frequency = 500 kHz
- \( L = 22 \mu H \)

### Figure 71. \( I_{INDUCTOR} \) Across \( V_{IN} \)

- \( I_{LED} \) Full Scale = 28.5 mA
- LED1 on DACA
- LED2 on DACB
- Frequency = 500 kHz
- \( L = 22 \mu H \)
7 Detailed Description

7.1 Overview
The LM3630A provides the power for two high-voltage LED strings (up to 40 V at 28.5 mA each). The two high-voltage LED strings are powered from an integrated asynchronous boost converter. The device is programmable over an I²C-compatible interface. Additional features include a PWM input for content adjustable brightness control, programmable switching frequency, and programmable overvoltage protection (OVP).

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Operation

7.3.1.1 Control Bank Mapping
Control of the LM3630A device current sinks is not done directly, but through the programming of Control Banks. The current sinks are then assigned to the programmed Control Bank (see Figure 72). Both current sinks can be assigned to Control Bank A or LED1 can use Control Bank A while LED2 uses Control Bank B. Assigning LED1 to Control Bank A and LED2 to Control Bank B allows for better LED current matching. Assigning each current sink to different control banks allows for each current sink to be programmed with a different current or have the PWM input control a specific current sink.
Feature Description (continued)

![Control Diagram](image)

**Figure 72. Control Diagram**

### Table 1. Bank Configuration Examples: Register Values

<table>
<thead>
<tr>
<th>REGISTERS TO PROGRAM</th>
<th>ILED1 on A, ILED2 ON B WITH PWM DIMMING(1)</th>
<th>ILED1 AND ILED2 ON A WITH PWM DIMMING</th>
<th>ILED1 ON A WITH PWM</th>
<th>ILED2 ON B NO PWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>1EH linear or 06h exp</td>
<td>15h linear or 05h exp</td>
<td>1EH linear or 06h exp</td>
<td></td>
</tr>
<tr>
<td>Configuration</td>
<td>1Bh</td>
<td>09h</td>
<td>19h</td>
<td></td>
</tr>
<tr>
<td>Brightness A</td>
<td>used for A</td>
<td>used for both</td>
<td>used for A</td>
<td></td>
</tr>
<tr>
<td>Brightness B</td>
<td>used for B</td>
<td>not used</td>
<td>used for B</td>
<td>(A and B do not have to be equal)</td>
</tr>
</tbody>
</table>

(1) LED current matching is specified using this configuration.

#### 7.3.1.2 PWM Input Polarity

The PWM Input can be set for active high (default) or active low polarity. With active low polarity the LED current is a function of the negative duty cycle at PWM.

#### 7.3.1.3 HWEN Input

HWEN is the global hardware enable to the LM3630A. HWEN must be pulled high to enable the device. HWEN is a high-impedance input so it cannot be left floating. When HWEN is pulled low the LM3630A is placed in shutdown and all the registers are reset to their default state.

#### 7.3.1.4 SEL Input

SEL is the select pin for the serial bus device address. When this pin is connected to ground, the seven-bit device address is 36H. When this pin is tied to the VIN power rail, the device address is 38H.

#### 7.3.1.5 INTN Output

The INTN pin is an open-drain active-low output signal which indicates detected faults. The signal asserts low when either OCP, OVP, or TSD is detected by the LED driver. The Interrupt Enable register must be set to connect these faults to the INTN pin.

#### 7.3.1.6 Boost Converter

The high-voltage boost converter provides power for the two current sinks (ILED1 and ILED2). The boost circuit operates using a 10-μH to 22-μH inductor and a 1-μF output capacitor. The selectable 500-kHz or 1-MHz switching frequency allows for the use of small external components and provides for high boost converter efficiency. Both LED1 and LED2 feature an adaptive voltage regulation scheme where the feedback point (LED1 or LED2) is regulated to a minimum of 300 mV. When there are different voltage requirements in both high-voltage LED strings, because of different programmed voltages or string mismatch, the LM3630A regulates the feedback point of the highest voltage string to 300 mV and drop the excess voltage of the lower voltage string across the lower strings current sink.
7.3.1.7 Boost Switching Frequency Select

The LM3630A’s boost converter can have a 500-kHz or 1-MHz switching frequency. For a 500-kHz switching frequency the inductor value must be between 10 μH and 22 μH. For the 1-MHz switching frequency the inductor can be between 10 μH and 22 μH. Additionally, there is a Frequency Shift bit which offsets the frequency approximately 10%. For the 500 kHz setting, shift = 0. The boost frequency is shifted to 560 kHz when Shift = 1. For the 1-MHz setting, Shift = 0. The boost frequency is shifted to 1120 kHz when shift = 1.

7.3.1.8 Adaptive Headroom

Reference Figure 73 and Figure 74 for the following description.

The adaptive headroom circuit controls the boost output voltage to provide the minimal headroom voltage necessary for the current sinks to provide the specified ILED current. The headroom voltage is fed back to the Error Amplifier to dynamically adjust the Boost output voltage. The error amplifier’s reference voltage is adjusted as the brightness level is changed, because the currents sinks require less headroom at lower ILED currents than at higher ILED currents. Note that the VHR Min block dynamically selects the LED string that requires the higher boost voltage to maintain the ILED current; this string has the lower headroom voltage. In Figure 74 this is LED string 2. The headroom voltage on LED string 1 is higher, but this is due to LED string 2 have an overall higher forward voltage than LED string 1. LED strings that have closely matched forward voltages have closely matched headroom voltages and better overall efficiency.

In a single string LED configuration the Feedback enable must be enabled for only that string (LED1 or LED2). The adaptive headroom circuit is control by that single string. In a two string LED configuration the Feedback enable must be enabled for both strings (LED1 and LED2). The VHR Min block then dynamically selects the LED string to control the adaptive headroom circuit.
7.3.1.9 Current Sinks

LED1 and LED2 control the current up to a 40-V LED string voltage. Each current sink has 5-bit full-scale current programmability and 8-bit brightness control. Either current sink has its current set through a dedicated brightness register and can additionally be controlled via the PWM input.
7.3.1.10 **Current String Biasing**
Each current string can be powered from the LM3630A device’s boost or from an external source. When powered from an external source the feedback input for either current sink can be disabled in the Configuration Register so it no longer controls the boost output voltage.

7.3.1.11 **Full-Scale LED Current**
The LM3630A device’s full-scale current is programmable with 32 different full-scale levels. The full-scale current is the LED current in the control bank when the brightness code is at max code (0xFF). The 5-bit full-scale current vs code is given by Equation 1:

\[
I_{\text{LED,FULLSCALE}} = 5 \text{ mA} + \text{Code} \times 0.75 \text{ mA}
\]  
(1)

With a maximum full-scale current of 28.5 mA.

7.3.1.12 **Brightness Register**
Each control bank has its own 8-bit brightness register. The brightness register code and the full-scale current setting determine the LED current depending on the programmed mapping mode.

7.3.1.13 **Exponential Mapping**
In exponential mapping mode the brightness code to backlight current transfer function is given by Equation 2:

\[
I_{\text{LED}} = I_{\text{LED,FULLSCALE}} \times 0.85 \left(44 - \frac{\text{Code} + 1}{5.8181818}\right) \times D_{\text{PWM}}
\]

where
- \(I_{\text{LED,FULLSCALE}}\) is the full-scale LED current setting
- Code is the backlight code in the brightness register
- DPWM is the PWM input duty cycle

Figure 75 and Figure 76 show the approximate backlight code to LED current response using exponential mapping mode. Figure 75 shows the response with a linear Y axis, and Figure 76 shows the response with a logarithmic Y axis. In exponential mapping mode the current ramp (either up or down) appears to the human eye as a more uniform transition then the linear ramp. This is due to the logarithmic response of the eye.

![Figure 75. Exponential Mapping Mode (Linear Scale)](image1)

![Figure 76. Exponential Mapping Mode (Log Scale)](image2)
7.3.1.14  Linear Mapping

In linear mapping mode the brightness code to backlight current has a linear relationship and follows Equation 3:

\[ I_{LED} = \frac{I_{LED\_FULLSCALE}}{255} \times \text{Code} \times D_{PWM} \]

where

- \( I_{LED\_FULLSCALE} \) is the full scale LED current setting
- \( \text{Code} \) is the backlight code in the brightness register
- \( D_{PWM} \) is the PWM input duty cycle

Equation 3

Figure 77 shows the backlight code-to-LED current response using linear-mapping mode. The Configuration Register must be set to enable linear mapping.

Figure 77. Linear Mapping Mode

7.3.2  Test Features

The LM3630A contains an LED open, an LED short, and overvoltage manufacturing fault detection. This fault detection is designed to be used during the manufacturing process only and not normal operation. These faults do not set the INTN pin.

7.3.2.1  Open LED String (LED1 And LED2)

An open LED string is detected when the voltage at the input to either LED1 or LED2 has fallen below 200 mV, and the boost output voltage has hit the OVP threshold. This test assumes that the LED string that is being detected for an open is being powered from the boost output (Feedback Enabled). For an LED string not connected to the boost output, and connected to another voltage source, the boost output would not trigger the OVP flag. In this case an open LED string would not be detected.

7.3.2.2  Shorted LED String

The LM3630A features an LED short fault flag indicating if either of the LED strings have experienced a short. There are two methods that can trigger a short in the LED strings:

1. An LED current sink with feedback enabled, and the difference between OVP input and the LED current sink input voltage goes below 1 V.
2. An LED current sink is configured with feedback disabled (not powered from the boost output) and the difference between \( V_{IN} \) and the LED current sink input voltage goes below 1 V.

7.3.2.3  Overvoltage Protection (Manufacturing Fault Detection and Shutdown)

The LM3630A provides an overvoltage Protection (OVP) mechanism specifically for manufacturing test where a display may not be connected to the device. The OVP threshold on the LM3630A has 4 different programmable options (16 V, 24 V, 32 V, and 40 V). The manufacturing protection is enabled in the Fault Status register bit 0. When enabled, this feature causes the boost converter to shutdown anytime the selected OVP threshold is exceeded. The OVP fault bit in the Fault Status register is set to one. The boost converter does not resume operation until the LM3630A is reset with either a write to the Software Reset bit in the Software Reset register or a cycling of the HWEN pin. The reset clears the fault.
7.3.3 Fault Flags/Protection Features
The Interrupt Status register contains the status of the protection circuits of the LM3630A. The corresponding bits are set to one if an OVP, OCP, or TSD event occurs. These faults do set the INTN pin when the corresponding bit is set in the Interrupt Enable register.

7.3.3.1 Overvoltage Protection (Inductive Boost Operation)
The overvoltage protection threshold (OVP) on the LM3630A has 4 different programmable options (16 V, 24 V, 32 V, and 40 V). OVP protects the device and associated circuitry from high voltages in the event the feedback enabled LED string becomes open. During normal operation, the LM3630A device’s inductive boost converter boosts the output up so as to maintain at least 300 mV at the active current sink inputs. When a high-voltage LED string becomes open the feedback mechanism is broken, and the boost converter inadvertently over boosts the output. When the output voltage reaches the OVP threshold the boost converter stops switching, thus allowing the output node to discharge. When the output discharges to \(V_{OVP} - 1\ V\) the boost converter begins switching again. The OVP sense is at the OVP pin, so this pin must be connected directly to the inductive boost output capacitor’s positive terminal.

For current sinks that have feedback disabled the over voltage sense mechanism is not in place to protect from potential over-voltage conditions. In this situation the application must ensure that the voltage at LED1 or LED2 doesn’t exceed 40 V.

The default setting for OVP is set at 24 V. For applications that require higher than 24 V at the boost output the OVP threshold has to be programmed to a higher level at power up.

7.3.3.2 Current Limit
The switch current limit for the LM3630A device’s inductive boost is set at 1 A. When the current through the NFET switch hits this over current protection threshold (OCP) the device turns the NFET off and the energy of the inductor is discharged into the output capacitor. Switching is then resumed at the next cycle. The current limit protection circuitry can operate continuously each switch cycle. The result is that during high output power conditions the device can continuously run in current limit. Under these conditions the device inductive boost converter stops regulating the headroom voltage across the high voltage current sinks. This results in a drop in the LED current.

7.3.3.3 Thermal Shutdown
The LM3630A contains thermal shutdown protection. In the event the die temperature reaches 140°C, the boost power supply and current sinks shut down until the die temperature drops to typically 125°C.

7.3.4 Initialization Timing
7.3.4.1 Initialization Timing With HWEN Tied to \(V_{IN}\)
If the HWEN input is tied to \(V_{IN}\), then the \(t_{WAIT}\) time starts when \(V_{IN}\) crosses 2.5 V as shown in Figure 78. The initial I\(^2\)C transaction can occur after the \(t_{WAIT}\) time expires. Any I\(^2\)C transaction during the \(t_{WAIT}\) period are NAK\'ed.

![Figure 78. Initialization Timing With HWEN Is Tied to \(V_{IN}\)](image-url)
7.3.4.2 Initialization Timing With HWEN Driven by GPIO

If the HWEN input is driven by a GPIO then the $t_{\text{WAIT}}$ time starts when HWEW crosses 1.2 V as shown in Figure 79. The initial I²C transaction can occur after the $t_{\text{WAIT}}$ time expires. Any I²C transaction during the $t_{\text{WAIT}}$ period are NAK'ed.

![Figure 79. Initialization Timing With HWEN Driven by a GPIO](image)

7.3.4.3 Initialization After Software Reset

The time between the I²C transaction that issues the software reset, and the subsequent I²C transaction (that is, to configure the LM3630A) must be at greater or equal to the $t_{\text{WAIT}}$ period of 1 ms. Any I²C transaction during the $t_{\text{WAIT}}$ period are NAK'ed.

7.4 Device Functional Modes

7.4.1 LED Current Ramping

7.4.1.1 Start-Up/Shutdown Ramp

The LED current turn on time from 0 to the initial LED current set-point is programmable. Similarly, the LED current shutdown time to 0 is programmable. Both the startup and shutdown times are independently programmable with 8 different levels. The start-up times are independently programmable from the shutdown times, but not independently programmable for each Control Bank. For example, programming a start-up or shutdown time, programs the same ramp time for each control bank. The start-up time is used when the device is first enabled to a non-zero brightness value. The shutdown time is used when the brightness value is programmed to zero. If HWEN is used to disable the device, the action is immediate and the Shutdown time is not used. The zero code does take a small amount of time which is approximately 0.5 ms.

<table>
<thead>
<tr>
<th>CODE</th>
<th>START-UP TIME</th>
<th>SHUTDOWN TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>4 ms</td>
<td>0</td>
</tr>
<tr>
<td>001</td>
<td>261 ms</td>
<td>261 ms</td>
</tr>
<tr>
<td>010</td>
<td>522 ms</td>
<td>522 ms</td>
</tr>
<tr>
<td>011</td>
<td>1.045 s</td>
<td>1.045 s</td>
</tr>
<tr>
<td>100</td>
<td>2.091 s</td>
<td>2.091 s</td>
</tr>
<tr>
<td>101</td>
<td>4.182 s</td>
<td>4.182 s</td>
</tr>
<tr>
<td>110</td>
<td>8.364 s</td>
<td>8.364 s</td>
</tr>
<tr>
<td>111</td>
<td>16.73 s</td>
<td>16.73 s</td>
</tr>
</tbody>
</table>

7.4.1.2 Run-Time Ramp

Current ramping from one brightness level to the next is programmable. There are 8 different ramp up times and 8 different ramp down times. The ramp up time is independently programmable from the ramp down time, but not independently programmable for each Control Bank. For example, programming a ramp up time or a ramp down time programs the same ramp time for each control bank. The run time ramps are used whenever the device is enabled with a non-zero brightness value and a new non-zero brightness value is written.
Table 3. LED Current Run Ramp Times

<table>
<thead>
<tr>
<th>CODE</th>
<th>RAMP-UP TIME</th>
<th>RAMP-DOWN TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>001</td>
<td>261 ms</td>
<td>261 ms</td>
</tr>
<tr>
<td>010</td>
<td>522 ms</td>
<td>522 ms</td>
</tr>
<tr>
<td>011</td>
<td>1.045 s</td>
<td>1.045 s</td>
</tr>
<tr>
<td>100</td>
<td>2.091 s</td>
<td>2.091 s</td>
</tr>
<tr>
<td>101</td>
<td>4.182 s</td>
<td>4.182 s</td>
</tr>
<tr>
<td>110</td>
<td>8.364 s</td>
<td>8.364 s</td>
</tr>
<tr>
<td>111</td>
<td>16.73 s</td>
<td>16.73 s</td>
</tr>
</tbody>
</table>

7.4.2 PWM Operation

![PWM Sampler Diagram](image)

Figure 80. PWM Sampler

![Hysteresis Block Diagram](image)

Figure 81. Hysteresis Block (Details)
7.4.2.1 PWM Input

The PWM input can be assigned to any control bank. When assigned to a control bank, the programmed current in the control bank also becomes a function of the duty cycle at the PWM input. The PWM input is sampled by a digital circuit which outputs a brightness code that is equivalent to the PWM input duty cycle. The resultant brightness value is a combination of the maximum current setting, the brightness registers, and the equivalent PWM brightness code.

7.4.2.2 PWM Input Frequency

The specified input frequency of the PWM signal is 10 kHz to 80 kHz. The recommended frequency is 30 kHz or greater. The PWM input sampler operates beyond those frequency limits. Performance changes based on the input frequency used. Using frequencies outside the specified range is not recommended. Lower PWM input frequency increases the likelihood that the output of the sampler may change and that a single brightness step may be visible on the screen. This may be visible at low brightness because the step change is large relative to the output level.

7.4.2.3 Recommended Settings

For best performance of the PWM sampler it is recommended to have a PWM input frequency of at least 30 kHz. The Filter Strength (register 50h) must be set to 03h. The Hysteresis 1 bit must be set in register 05h to 1 when setting the maximum current for bank A. For example if max current is 20 mA, register 05h is set to 14h, change that to 94h for 1 bit hysteresis and a smooth min-to-max brightness transition.

7.4.2.4 Adjustments to PWM Sampler

The digital sampler has controls for hysteresis and minimum output brightness which allow the optimization of sampler output. The default hysteresis mode of the PWM sampler requires detecting a two code change in the input to increase brightness. Reducing the hysteresis to change on 1 code allows a smoother brightness transition when the brightness control is swept across the screen in a system. The filter strength bits affect the speed of the output transitions from the PWM sampler. A lower bound to the brightness is enabled by default which limits the minimum output of the PWM sampler to an equivalent code of 6 when the LEDs are turned on. A detected code of 1 is forced to off. A minimum 2% PWM input duty cycle is recommended. Input duty cycles of 1% or less causes delayed off-to-on transitions.

7.4.2.4.1 Filter Strength, Register 50h Bits [1:0]

- Filter Strength controls the amount of sampling cycles that are fed back to the PWM input sampler. A filter strength of 00b allows the output of the PWM sampler to change on every Sample Period. A filter strength of 01b allows the output of the PWM sampler to change every two Sample Periods. A filter strength of 10b allows the output of the PWM sampler to change every four Sample Periods. A filter strength of 11b allows the output of the PWM sampler to change every eight Sample Periods.
- The effect of setting this value to 11b forces the output of the PWM sampler to change less frequently then lower values. The benefit is this reduces the appearance of flicker because the output is slower to change.
The negative is that the output is slower to change.

7.4.2.4.2 Hysteresis 1 Bit, Register 05h, Bit 7

- The default setting for the LM3630A has Bit 7 of register 05h is 0b. This requires the detection of a PWM input change that is at least 3 equivalent codes higher than the present code. If this bit is set to 1b, the hysteresis is turned off and the PWM sampler output is allowed to change by 2 code.
- Setting this bit to 1b turns off the 2 code requirement for the PWM sampler output to change. The benefit is that the output change is smoother. The negative is that there may be some PWM input value where the output could change by one code and it might appear as flicker.

7.4.2.4.3 Lower Bound Disable, Register 05h, Bit 6

- The default setting for the LM3630A has Bit 6 of register 05h is 0b. This turns on the lower bound where the minimum output value of the PWM sampler is an equivalent code of 6. If the PWM sampler detects an equivalent code of 0 or 1, the output is 0, and the LEDs are off. If the PWM sampler detects an equivalent code of 2 through 6, a current equal to code 6 is output. Detection of any higher code outputs that code conforming to the rules of hysteresis above.
- Setting Bit 6 of register 05h to 1b can be used to allow the output to be below an equivalent code 6. The output of the PWM sampler matches the input pulse width conforming to the rules of Hysteresis and equivalent codes 1, 2, 3, 4, and 5 are also allowed. The benefit is the output is allowed to go dimmer than in the default mode. The negative is at the low codes of 1 and 2, the LEDs may not turn on or the LEDs may appear to flicker.
- Disabling the Lower Bound (05h Bit 6 = 1b) allows the minimum duty cycle to be detected at 0.35% PWM input duty cycle. At 30-kHz PWM input frequency, the minimum pulse width required to turn on the LEDs is $0.39\% \times 33 \mu\text{s} = 129 \text{ ns}$. There is no specified tolerance to this value.

7.4.2.5 Minimum $T_{ON}$ Pulse Width

The minimum $T_{ON}$ pulse width required to produce a non-zero output is dependent upon the LM3630A settings. The default setting of the LM3630A requires a minimum of 0.78% duty cycle for the output to be turned on. Because the lower bound feature is enabled, a value of 0.78% (equivalent brightness code 2) up to 2.35% (equivalent brightness code 6) all produce an output equivalent to brightness code 6. At 30-kHz PWM input frequency, the minimum pulse width required to turn on the LEDs is $0.78\% \times 33 \mu\text{s} = 260 \text{ ns}$.

Because of the hysteresis on the PWM input, this pulse width may not be sufficient to turn on the LEDs. It is recommended that a minimum pulse width of 2% be used. $2\% \times 33 \mu\text{s} = 660 \text{ ns}$ at 30 kHz input frequency.

Disabling the lower bound as described allows a smaller minimum pulse width.
7.5 Programming

7.5.1 I²C-Compatible Interface

7.5.1.1 Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

![Data Validity Diagram](image)

A pullup resistor between the VIO line of the controller and SDA must be greater than \([ (V_{IO} - V_{OL}) / 3 \text{ mA} ]\) to meet the \(V_{OL}\) requirement on SDA. Using a larger pullup resistor results in lower switching current with slower edges, while using a smaller pullup results in higher switching currents with faster edges.

7.5.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition.

![Start and Stop Conditions](image)

During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

7.5.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3630A pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3630A generates an acknowledge after each byte is received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3630A address is 36h. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.
Programming (continued)

The following tables summarize LM3630A I²C-compatible register usage and show default register bit values after reset, as programmed by the factory. The following sub-sections provide additional details on the use of individual registers. Register bits which are blank in the following tables are considered undefined. Undefined bits should be ignored on reads and written as zero.

### Slave Address [0x36h for SEL = 0, 0x38h for SEL = 1]

<table>
<thead>
<tr>
<th>REGISTER NAME</th>
<th>ADDRESS</th>
<th>TYPE</th>
<th>DEFAULT RESET VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>0x00</td>
<td>R/W</td>
<td>0xC0</td>
</tr>
<tr>
<td>Configuration</td>
<td>0x01</td>
<td>R/W</td>
<td>0x18</td>
</tr>
<tr>
<td>Boost Control</td>
<td>0x02</td>
<td>R/W</td>
<td>0x38</td>
</tr>
<tr>
<td>Brightness A</td>
<td>0x03</td>
<td>R/W</td>
<td>0x00</td>
</tr>
<tr>
<td>Brightness B</td>
<td>0x04</td>
<td>R/W</td>
<td>0x00</td>
</tr>
<tr>
<td>Current A</td>
<td>0x05</td>
<td>R/W</td>
<td>0x1F</td>
</tr>
<tr>
<td>Current B</td>
<td>0x06</td>
<td>R/W</td>
<td>0x1F</td>
</tr>
<tr>
<td>On/Off Ramp</td>
<td>0x07</td>
<td>R/W</td>
<td>0x00</td>
</tr>
<tr>
<td>Run Ramp</td>
<td>0x08</td>
<td>R/W</td>
<td>0x00</td>
</tr>
<tr>
<td>Interrupt Status</td>
<td>0x09</td>
<td>R/W</td>
<td>0x00</td>
</tr>
<tr>
<td>Interrupt Enable</td>
<td>0x0A</td>
<td>R/W</td>
<td>0x00</td>
</tr>
<tr>
<td>Fault Status</td>
<td>0x0B</td>
<td>R/W</td>
<td>0x00</td>
</tr>
<tr>
<td>Software Reset</td>
<td>0x0F</td>
<td>R/W</td>
<td>0x00</td>
</tr>
<tr>
<td>PWM Out Low</td>
<td>0x12</td>
<td>Read</td>
<td>0x00</td>
</tr>
<tr>
<td>PWM Out High</td>
<td>0x13</td>
<td>Read</td>
<td>0x00</td>
</tr>
<tr>
<td>Revision</td>
<td>0x1F</td>
<td>Read</td>
<td>0x02</td>
</tr>
<tr>
<td>Filter Strength</td>
<td>0x50</td>
<td>R/W</td>
<td>0x00</td>
</tr>
</tbody>
</table>

### Figure 85. I²C-Compatible Chip Address (0x36), SEL = 0

### Figure 86. I²C-Compatible Chip Address (0x38), SEL = 1

### 7.6 Register Maps

#### 7.6.1 LM3630A I²C Register Map

This table summarizes LM3630A I²C-compatible register usage and shows default register bit values after reset, as programmed by the factory. The following sub-sections provide additional details on the use of individual registers. Register bits which are blank in the following tables are considered undefined. Undefined bits should be ignored on reads and written as zero.
### 7.6.2 Register Descriptions

#### Table 4. Control (Offset = 0x00, Default = 0xC0)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>Name</th>
<th>Bit</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SLEEP_CMD</td>
<td>7</td>
<td>R/W</td>
<td>The device is put into sleep mode when set to ‘1’.</td>
</tr>
<tr>
<td></td>
<td>SLEEP_STATUS</td>
<td>6</td>
<td>Read</td>
<td>Reflects the sleep mode status. A ‘1’ indicates the part is in sleep mode. Used to determine when part has entered or exited sleep mode after writing the SLEEP_CMD bit.</td>
</tr>
<tr>
<td>5</td>
<td>LINEAR_A</td>
<td>4</td>
<td>R/W</td>
<td>Enables the linear output mode for Bank A when set to ‘1’.</td>
</tr>
<tr>
<td></td>
<td>LINEAR_B</td>
<td>3</td>
<td>R/W</td>
<td>Enables the linear output mode for Bank B when set to ‘1’.</td>
</tr>
<tr>
<td>2</td>
<td>LED_EN_A</td>
<td>2</td>
<td>R/W</td>
<td>Enables the LED A output</td>
</tr>
<tr>
<td></td>
<td>LED_EN_B</td>
<td>1</td>
<td>R/W</td>
<td>Enables the LED B output</td>
</tr>
<tr>
<td>0</td>
<td>LED2_ON_A</td>
<td>0</td>
<td>R/W</td>
<td>Connect the LED2 output to Bank A Control</td>
</tr>
</tbody>
</table>

#### Table 5. Configuration (Offset = 0x01, Default = 0x18)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>Name</th>
<th>Bit</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>FB_EN_B</td>
<td>7</td>
<td>Read</td>
<td>Enable Feedback on Bank B</td>
</tr>
<tr>
<td></td>
<td>FB_EN_A</td>
<td>6</td>
<td>Read</td>
<td>Enable Feedback on Bank A</td>
</tr>
<tr>
<td>5</td>
<td>PWM_LOW</td>
<td>5</td>
<td>Read</td>
<td>Sets the PWM to active low</td>
</tr>
<tr>
<td></td>
<td>PWM_EN_B</td>
<td>4</td>
<td>R/W</td>
<td>Enables the PWM for Bank B</td>
</tr>
<tr>
<td></td>
<td>PWM_EN_A</td>
<td>3</td>
<td>R/W</td>
<td>Enables the PWM for Bank A</td>
</tr>
</tbody>
</table>

#### Table 6. Boost Control (Offset = 0x02, Default = 0x38)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>Name</th>
<th>Bit</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>BOOST_OVP[1]</td>
<td>6:5</td>
<td>R/W</td>
<td>Selects the voltage limit for over-voltage protection: 00 = 16 V 01 = 24 V 10 = 32 V 11 = 40 V</td>
</tr>
<tr>
<td></td>
<td>BOOST_OVP[0]</td>
<td>4:3</td>
<td>R/W</td>
<td>Selects the current limit for over-current protection: 00 = 600 mA 01 = 800 mA 10 = 1 A 11 = 1.2 A</td>
</tr>
<tr>
<td>2</td>
<td>SLOW_START</td>
<td>2</td>
<td>R/W</td>
<td>Slows the boost output transition</td>
</tr>
<tr>
<td></td>
<td>SHIFT</td>
<td>1</td>
<td>R/W</td>
<td>Enables the alternate oscillator frequencies: For FMODE = 0: SHIFT = 0F = 500 kHz; SHIFT 1F = 560 kHz For FMODE = 1: SHIFT = 0F = 1 MHz; SHIFT 1F = 1120 MHz</td>
</tr>
</tbody>
</table>
### Table 6. Boost Control (Offset = 0x02, Default = 0x38) (continued)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FMODE</td>
<td>0</td>
<td>R/W</td>
<td>Selects the boost frequency: 0 = 500 kHz, 1 = 1MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 7. Brightness A (Offset = 0x03, Default = 0x00) (1)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
</tr>
<tr>
<td>Access</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>Description</td>
<td>A[7:0]</td>
<td>R/W</td>
<td>Sets the 8-bit brightness value for outputs connected to Bank A. Minimum brightness setting is code 04h.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) These registers are not updated if the device is in Sleep Mode (Control: SLEEP_STATUS = 1).

### Table 8. Brightness B (Offset = 0x04, Default = 0x00) (1)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
<td>7:0</td>
</tr>
<tr>
<td>Access</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>Description</td>
<td>B[7:0]</td>
<td>R/W</td>
<td>Sets the 8-bit brightness value for outputs connected to Bank B. Minimum brightness setting is code 04h.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) These registers are not updated if the device is in Sleep Mode (Control: SLEEP_STATUS = 1).

### Table 9. Current A (Offset = 0x05, Default 0x1F)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
<td>7</td>
<td>6</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>Access</td>
<td>R/W</td>
<td>R/W</td>
<td>Description</td>
<td>Hysteresis</td>
<td>Lower Bound</td>
<td>A[4:0]</td>
<td>R/W</td>
<td>Sets the 5-bit full-scale current for outputs connected to Bank A.</td>
</tr>
<tr>
<td>Description</td>
<td>Determines the hysteresis of the PWM Sampler. Clearing this bit, the PWM sampler changes its output upon detecting at least 3 equivalent code changes on the PWM input. Setting this bit, the PWM sampler changes its output upon detecting 2 equivalent code changes on the PWM input.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Determines the lower bound of the PWM Sampler. Clearing this bit, the PWM sampler outputs code 6 when it detects equivalent codes 2 thru 6; and code 0 when it detects equivalent codes 0 thru 1. Setting this bit, the PWM sampler can output codes below 6, based upon the Hysteresis setting and equivalent code sampled from the input PWM.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 10. Current B (Offset = 0x06, Default = 0x1F)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
<td>7</td>
<td>6</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
<td>R/W</td>
</tr>
<tr>
<td>Access</td>
<td>R/W</td>
<td>R/W</td>
<td>Description</td>
<td>B[4:0]</td>
<td>R/W</td>
<td>Sets the 5-bit full-scale current for outputs connected to Bank B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Description</td>
<td>Sets the 5-bit full-scale current for outputs connected to Bank B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 11. On/Off Ramp (Offset = 0x07, Default 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

**Name** | **Bit** | **Access** | **Description**
--- | --- | --- | ---
T_START | 7 | Read | Ramp time for startup events.
T_SHUT | 6 | Read | Ramp time for shutdown events.

**Code** | **Start-Up Time** | **Shutdown Time**
--- | --- | ---
000 | 4 ms | 0 ms
001 | 261 ms | 261 ms
010 | 522 ms | 522 ms
011 | 1.045 s | 1.045 s
100 | 2.091 s | 2.091 s
101 | 4.182 s | 4.182 s
110 | 8.364 s | 8.364 s
111 | 16.73 s | 16.73 s

*Code 0 results in approximately 0.5 ms ramp time.

Table 12. Run Ramp (Offset = 0x08, Default = 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

**Name** | **Bit** | **Access** | **Description**
--- | --- | --- | ---
T_UP | 7 | Read | Time for ramp-up events
T_DOWN | 6 | Read | Time for ramp-down events

**Code** | **Ramp-Up Time** | **Ramp-down Time**
--- | --- | ---
000 | 0 ms | 0 ms
001 | 261 ms | 261 ms
010 | 522 ms | 522 ms
011 | 1.045 s | 1.045 s
100 | 2.091 s | 2.091 s
101 | 4.182 s | 4.182 s
110 | 8.364 s | 8.364 s
111 | 16.73 s | 16.73 s

*Code 0 results in approximately 0.5 ms ramp time.
Table 13. Interrupt Status (Offset = 0x09, Default = 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
</tr>
<tr>
<td>OCP</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OCP</td>
<td>2</td>
<td>R/W</td>
<td>An overcurrent condition occurred.</td>
</tr>
<tr>
<td>OVP</td>
<td>1</td>
<td>R/W</td>
<td>An overvoltage condition occurred.</td>
</tr>
<tr>
<td>TSD</td>
<td>0</td>
<td>R/W</td>
<td>A thermal shutdown event occurred.</td>
</tr>
</tbody>
</table>

The interrupt status register is cleared upon a read of the register. If the condition that caused the interrupt is still present, then the bit is set to one again and another interrupt is signaled on the INTN output pin. The interrupt status register is not cleared if the device is in sleep mode (Control: SLEEP_STATUS = 1). To disconnect the interrupt condition from the INTN pin during sleep mode, disable the fault connection in the Interrupt Enable register. An interrupt condition sets the status bit and causes an event on the INTN pin only if the corresponding bit in the Interrupt Enable register is one and the Global Enable bit is also one.

Table 14. Interrupt Enable (Offset = 0x0A, Default = 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
</tr>
<tr>
<td>OCP</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GLOBAL</td>
<td>7</td>
<td>R/W</td>
<td>Set to ‘1’ to enable interrupts to drive the INTN pin.</td>
</tr>
<tr>
<td>OCP</td>
<td>2</td>
<td>R/W</td>
<td>Set to ‘1’ to enable the over-current condition interrupt.</td>
</tr>
<tr>
<td>OVP</td>
<td>1</td>
<td>R/W</td>
<td>Set to ‘1’ to enable the over-voltage condition interrupt.</td>
</tr>
<tr>
<td>TSD</td>
<td>0</td>
<td>R/W</td>
<td>Set to ‘1’ to enable the thermal shutdown interrupt.</td>
</tr>
</tbody>
</table>

Table 15. Fault Status (Offset = 0x0B, Default = 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
</tr>
<tr>
<td>OPEN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPEN</td>
<td>7</td>
<td>Read</td>
<td>.</td>
</tr>
<tr>
<td>OVP F_EN</td>
<td>0</td>
<td>R/W</td>
<td>Set to ‘1’ to enable OVP manufacturing test.</td>
</tr>
<tr>
<td>OVP_FAULT</td>
<td>1</td>
<td>R/W</td>
<td>An OVP occurred in manufacturing test.</td>
</tr>
<tr>
<td>SHORT_EN</td>
<td>2</td>
<td>R/W</td>
<td>Set to ‘1’ to enable short test.</td>
</tr>
<tr>
<td>LED1_SHORT</td>
<td>3</td>
<td>R/W</td>
<td>A short was detected on LED string 1.</td>
</tr>
<tr>
<td>LED2_SHORT</td>
<td>4</td>
<td>R/W</td>
<td>A short was detected on LED string 2.</td>
</tr>
<tr>
<td>OVP_FAULT</td>
<td>1</td>
<td>R/W</td>
<td>An OVP occurred in manufacturing test.</td>
</tr>
<tr>
<td>OVP_F_EN</td>
<td>0</td>
<td>R/W</td>
<td>Set to ‘1’ to enable OVP manufacturing test.</td>
</tr>
</tbody>
</table>

An open circuit was detected on one of the LED strings.
### Table 16. Software Reset (Offset = 0x0F, Default = 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Access</td>
<td>Read</td>
<td>Read</td>
<td>Read</td>
<td>Read</td>
<td>Read</td>
<td>Read</td>
<td>Read</td>
<td>Read</td>
</tr>
<tr>
<td>Description</td>
<td>SW_RESET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Set to ‘1’ to reset the device. This is a full reset which clears the registers, executes a power-on reset, and reads the EPROM configuration.

### Table 17. PWM_OUT Low (Offset = 0x12, Default 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>PWM_OUT[7:0]</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The value of the PWM detector. Maximum value is 256 or 100h. If PWM_OUT[7:0] is non-zero PWM_OUT[8] is zero.

### Table 18. PWM_OUT High (Offset = 0x13, Default 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>PWM_OUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit</td>
<td>[7:0]</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 19. Revision (Offset = 0x1F, Default = 0x02)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Access</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Description</td>
<td>REV[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 20. Filter Strength (Offset = 0x50, Default = 0x00)

<table>
<thead>
<tr>
<th>Register Bits</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>FLTR_STR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit</td>
<td>[1:0]</td>
<td>R/W</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Description</td>
<td>FLTR_STR[1:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Product Folder Links: **LM3630A**
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The LM3630A is a dual-channel backlight driver. The device has 5-bit full-scale current programmability (5 mA to 30 mA) and for every full-scale current there is 8 bits of LED current adjustment from 0 to \( I_{\text{FULL\_SCALE}} \). Both current sinks can be independently controlled via two separate full-scale current registers and two separate 8-bit brightness registers, or can be made to track together via a single brightness register.

8.2 Typical Application

Figure 87. LM3630A Typical Application

8.2.1 Design Requirements
For typical white LED applications, use the parameters listed in Table 21.

Table 21. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum input voltage</td>
<td>2.3 V</td>
</tr>
<tr>
<td>Minimum output voltage</td>
<td>( V_{IN} )</td>
</tr>
<tr>
<td>Output current</td>
<td>28.5 mA per channel</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>500 kHz or 1 MHz</td>
</tr>
</tbody>
</table>
8.2.2 Detailed Design Procedure

8.2.2.1 Inductor Selection

The LM3630A is designed to work with a 10-µH to 22-µH inductor. When selecting the inductor, ensure that the saturation rating for the inductor is high enough to accommodate the peak inductor current. Equation 4 calculates the peak inductor current based upon LED current, V_{IN}, V_{OUT}, and efficiency.

\[ I_{PEAK} = \frac{I_{LED} \times V_{OUT}}{\eta \times V_{IN}} + \Delta I_L \]  

(4)

where:

\[ \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \]  

(5)

When choosing L, the inductance value must also be large enough so that the peak inductor current is kept below the LM3630A device’s switch current limit. This forces a lower limit on L given by Equation 6.

\[ L > \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times V_{OUT} \times \left( I_{SW_{MAX}} - \frac{I_{LED_{MAX}} \times V_{OUT}}{\eta \times V_{IN}} \right)} \]  

(6)

\( I_{SW_{MAX}} \) is given in Electrical Characteristics, efficiency (\( \eta \)) is shown in the Typical Characteristics, and \( f_{SW} \) is typically 500 kHz or 1 MHz.

### Table 22. Inductors

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>PART NUMBER</th>
<th>VALUE</th>
<th>SIZE</th>
<th>CURRENT RATING</th>
<th>DC RESISTANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDK</td>
<td>VLF4014ST-100M1R0</td>
<td>10 µH</td>
<td>3.8 mm × 3.6 mm × 1.4 mm</td>
<td>1A</td>
<td>0.22 Ω</td>
</tr>
<tr>
<td>TDK</td>
<td>VLF302512MT-220M</td>
<td>22 µH</td>
<td>3 mm × 2.5 mm × 1.2 mm</td>
<td>0.43A</td>
<td>0.583 Ω</td>
</tr>
</tbody>
</table>

8.2.2.2 Maximum Power Output

The LM3630A device's maximum output power is governed by two factors: the peak current limit (\( I_{CL} = 1.2 \) A maximum), and the maximum output voltage (\( V_{OVP} = 40 \) V minimum). When the application causes either of these limits to be reached, it is possible that the proper current regulation and matching between LED current strings may not be met.

In the case of a peak current limited situation, when the peak of the inductor current hits the LM3630A device's current limit the NFET switch turns off for the remainder of the switching period. If this happens, each switching cycle the LM3630A begins to regulate the peak of the inductor current instead of the headroom across the current sinks. This can result in the dropout of the feedback-enabled current sinks and the current dropping below its programmed level.

The peak current in a boost converter is dependent on the value of the inductor, total LED current (\( I_{OUT} \)), the output voltage (\( V_{OUT} \)) (which is the highest voltage LED string + 0.3 V regulated headroom voltage), the input voltage \( V_{IN} \), and the efficiency (Output Power/Input Power). Additionally, the peak current is different depending on whether the inductor current is continuous during the entire switching period (CCM) or discontinuous (DCM) where it goes to 0 before the switching period ends.

For CCM the peak inductor current is given by:

\[ I_{PEAK} = \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \eta} + \left[ \frac{V_{IN}}{2 \times f_{SW} \times L} \times \left( 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \right) \right] \]  

(7)

For DCM the peak inductor current is given by:

\[ I_{PEAK} = \frac{2 \times I_{OUT}}{f_{SW} \times L \times \eta} \times \left[ V_{OUT} - V_{IN} \times \eta \right] \]  

(8)

To determine which mode the circuit is operating in (CCM or DCM), a calculation must be done to test whether the inductor current ripple is less than the anticipated input current (\( I_{IN} \)). If \( \Delta I_L < I_{IN} \), the device operates in CCM. If \( \Delta I_L > I_{IN} \) then the device is operating in DCM.
Typically at currents high enough to reach the LM3630A device’s peak current limit, the device is operating in CCM.

**Application Curves** show the output current and output voltage derating for a 10-µH and a 22-µH inductor, at switch frequencies of 500 kHz and 1 MHz. A 10-µH inductor is typically a smaller device with lower on resistance, but the peak currents are higher. A 22-µH inductor provides for lower peak currents, but to match the DC resistance of a 10 µH requires a larger-sized device.

### 8.2.3 Application Curves

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Inductor Value</th>
<th>Figure</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 kHz</td>
<td>10 µH</td>
<td>88</td>
</tr>
<tr>
<td>1 MHz</td>
<td>10 µH</td>
<td>89</td>
</tr>
<tr>
<td>500 kHz</td>
<td>22 µH</td>
<td>90</td>
</tr>
<tr>
<td>1 MHz</td>
<td>22 µH</td>
<td>91</td>
</tr>
</tbody>
</table>
8.3 Initialization Setup

8.3.1 Recommended Initialization Sequence

The recommended initialization sequence for the device registers is as follows:

1. Set Filter Strength register (offset = 50h) to 03h.
2. Set Configuration register (offset = 01h) to enable the PWM and the feedback for Bank A; for example, writing 09h to the Configuration register, enables PWM and feedback for Bank A. Note the Bank B PWM and feedback need to be configured if Bank B is used, otherwise disable the Bank B feedback by clearing bit 4 and disable the Bank B PWM by clearing bit 1.
3. Configure the Boost Control register (offset = 02h) to select the OVP, OCP and FMODE. For example, writing 78h to the Boost Control register sets OVP to 40 V, OCP to 1.2 A and FMODE to 500 kHz.
4. Set the full scale LED current for Bank A and Bank B (if used), by writing to the Current A (offset = 05h), and Current B (offset = 06) registers. For example, writing 14h to the Current A register selects a full scale LED current of 20 mA for Bank A.
5. Set the PWM Sampler Hysteresis to 2 codes by setting Bit 7 of the Current A register. Set the PWM Sampler Lower Bound code to 6 by clearing Bit 6 of the Current A register. Note these settings apply to both Bank A and Bank B. If only Bank B is used, these setting are still necessary when PWM is enabled.
6. Select the current control and enable or disable the LED Bank A and/or B by writing to Control register (offset = 00h). For example, writing 14h to the Control register select linear current control and enables Bank A.
7. Set the LED brightness by writing to Brightness A (offset = 03h) and Brightness B (Offset = 04h) registers. For example, writing FFh to Brightness A sets the LED current to 20 mA, with the Current A register set to 14h, and the PWM input is high.

9 Power Supply Recommendations

The LM3630A operates from a 2.3-V to 5.5-V input voltage. The boost switching frequency is programmable at 500 kHz for low switching loss performance or 1 MHz to allow the use of tiny low-profile inductors. This input supply must be well regulated and provide the peak current required by the LED configuration and inductor selected.
10 Layout

10.1 Layout Guidelines

The LM3630A contains an inductive boost converter which detects a high switched voltage (up to 40 V) at the SW pin, and a step current (up to 900 mA) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OVP pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 92 highlights these two noise generating components.

Figure 92. LM3630A Boost Converter Showing Pulsed Voltage At SW (High Dv/Dt) and Current Through Schottky and C\textsubscript{OUT} (High Di/Dt)

The following lists the main (layout sensitive) areas of the LM3630A in order of decreasing importance:

- Output Capacitor
  - Schottky Cathode to C\textsubscript{OUT}+
  - C\textsubscript{OUT}− to GND
- Schottky Diode
  - SW Pin to Schottky Anode
  - Schottky Cathode to C\textsubscript{OUT}+
- Inductor
  - SW Node PCB capacitance to other traces
- Input Capacitor
  - C\textsubscript{IN}+ to IN pin
  - C\textsubscript{IN}− to GND
Layout Guidelines (continued)

10.1.1 Output Capacitor Placement

The output capacitor is in the path of the inductor current discharge path. As a result \( C_{OUT} \) detects a high current step from 0 to \( I_{PEAK} \) each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through \( C_{OUT} \) and back into the LM3630A GND pin will contribute to voltage spikes \( (V_{SPIKE} = L_p \times dI/dt) \) at SW and OUT which can potentially overvoltage the SW pin, or feed through to GND. To avoid this, \( C_{OUT+} \) must be connected as close as possible to the Cathode of the Schottky diode and \( C_{OUT-} \) must be connected as close as possible to the device GND bump. The best placement for \( C_{OUT} \) is on the same layer as the LM3630A so as to avoid any vias that can add excessive series inductance (see Figure 94).

10.1.2 Schottky Diode Placement

The Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode detects a high current step from 0 to \( I_{PEAK} \) each time the switch turns off and the diode turns on. Any inductance in series with the diode will cause a voltage spike \( (V_{SPIKE} = L_p \times dI/dt) \) at SW and OUT which can potentially overvoltage the SW pin, or feed through to \( V_{OUT} \) and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to \( C_{OUT+} \) will reduce the inductance \( (L_p) \) and minimize these voltage spikes (see Figure 94).

10.1.3 Inductor Placement

The node where the inductor connects to the LM3630A SW bump has 2 issues. First, a large switched voltage (0 to \( V_{OUT} + V_{F, SCHOTTKY} \)) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW bump. Any resistance in this path can cause large voltage drops that will negatively affect efficiency.

To reduce the capacitively coupled signal from SW into nearby traces, the SW bump to inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, the other traces need to be routed away from SW and not directly beneath. This is especially true for high impedance nodes that are more susceptible to capacitive coupling such as (SCL, SDA, HWEN, PWM, and possibly ASL1 and ALS2). A GND plane placed directly below SW will dramatically reduce the capacitive coupling from SW into nearby traces.

To limit the trace resistance of the VBATT to inductor connection and from the inductor to SW connection, use short, wide traces (see Figure 94).

10.1.4 Input Capacitor Selection and Placement

The input bypass capacitor filters the inductor current ripple, and the internal MOSFET driver currents during turnon of the power switch.

The driver current requirement can range from 50 mA at 2.7 V to over 200 mA at 5.5 V with fast durations of approximately 10 ns to 20 ns. This will appear as high \( dI/dt \) current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical since any series inductance between IN and \( C_{IN+} \) or \( C_{IN-} \) and GND can create voltage spikes that could appear on the \( V_{IN} \) supply line and in the GND plane.

Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM3630A, form a series RLC circuit. If the output resistance from the source \( (R_S) \) is low enough the circuit will be underdamped and will have a resonant frequency (typically the case). Depending on the size of \( L_S \) the resonant frequency could occur below, close to, or above switching frequency of the device. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM3630A switching frequency;
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency; and
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency.
Layout Guidelines (continued)

Figure 93 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor. The circuit is re-drawn for the AC case where the \( V_{\text{IN}} \) supply is replaced with a short to GND and the LM3630A plus inductor is replaced with a current source (\( \Delta I_L \)). In Figure 93, equation 1 is the criteria for an underdamped response, equation 2 is the resonant frequency, and equation 3 is the approximated supply current ripple as a function of \( L_S \), \( R_S \), and \( C_{\text{IN}} \).

As an example, consider a 3.6-V supply with 0.1-\( \Omega \) of series resistance connected to \( C_{\text{IN}} \) through 50 nH of connecting traces. This results in an underdamped input filter circuit with a resonant frequency of 712 kHz. Since the switching frequency lies near to the resonant frequency of the input RLC network, the supply current is probably larger than the inductor current ripple. In this case using equation 2 from Figure 93 the supply current ripple can be approximated as 1.68 multiplied by the inductor current ripple. Increasing the series inductance (\( L_S \)) to 500 nH causes the resonant frequency to move to around 225 kHz and the supply current ripple to be approximately 0.25 multiplied by the inductor current ripple.

\[
1. \quad \frac{1}{L_S \times C_{\text{IN}}} > \frac{R_S^2}{4 \times L_S^2} \\
2. \quad I_{\text{RESONANT}} = \frac{1}{2\pi \sqrt{L_S \times C_{\text{IN}}}} \\
3. \quad I_{\text{SUPPLY RIPPLE}} \approx \Delta I_L \times \frac{1}{\frac{2\pi \times 500\, \text{kHz} \times C_{\text{IN}}}{R_S^2 + \left( \frac{2\pi \times 500\, \text{kHz} \times L_S}{2\pi \times 500\, \text{kHz} \times C_{\text{IN}}} \right)^2}}
\]

**Figure 93. Input RLC Network**
10.2 Layout Example

Figure 94. Typical LP3630A PCB Layout (2 x 10 Led Application)
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer
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11.2 Documentation Support

11.2.1 Related Documentation
For additional information, see the following:
Texas Instruments Application Note 1112: DSBGA Wafer Level Chip Scale Package (SNVA009).

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective
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TI E2E™ Online Community  TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration
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contact information for technical support.

11.4 Trademarks
E2E is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam
during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most
current data available for the designated devices. This data is subject to change without notice and revision of
this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3630ATME</td>
<td>ACTIVE</td>
<td>DSBGA</td>
<td>YFQ</td>
<td>12</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>D6</td>
<td></td>
</tr>
<tr>
<td>LM3630ATMX</td>
<td>ACTIVE</td>
<td>DSBGA</td>
<td>YFQ</td>
<td>12</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>D6</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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### TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3630ATME</td>
<td>DSBGA</td>
<td>YFQ</td>
<td>12</td>
<td>250</td>
<td>178.0</td>
<td>8.4</td>
<td>1.52</td>
<td>2.04</td>
<td>0.76</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
<tr>
<td>LM3630ATMX</td>
<td>DSBGA</td>
<td>YFQ</td>
<td>12</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>1.52</td>
<td>2.04</td>
<td>0.76</td>
<td>4.0</td>
<td>8.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM3630ATME</td>
<td>DSBGA</td>
<td>YFQ</td>
<td>12</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LM3630ATMX</td>
<td>DSBGA</td>
<td>YFQ</td>
<td>12</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
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