1 Features
- $T_A = 25^\circ C$. Typical Values Unless Otherwise Specified.
- 5-Pin SOT-23 Package
- Industrial Operating Range $-40^\circ C$ to $+85^\circ C$
- Single or Dual Power Supplies
- Wide Supply Voltage Range 5 V to 30 V
- Low Supply Current 300 µA
- Low Input Bias Current 7 nA
- Low Input Offset Current ±1 nA
- Low Input Offset Voltage ±2 mV
- Response Time 440 ns (50-mV Overdrive)
- Input Common-Mode Voltage 0 to $V_S - 1.5$ V

2 Applications
- A/D Converters
- Pulse, Square-Wave Generators
- Peak Detector
- Industrial Applications

3 Description
The LM397 device is a single voltage comparator with an input common mode that includes ground. The LM397 is designed to operate from a single 5-V to 30-V power supply or a split power supply. Its low supply current is virtually independent of the magnitude of the supply voltage.

The LM397 features an open-collector output stage. This allows the connection of an external resistor at the output. The output can directly interface with TTL, CMOS and other logic levels, by tying the resistor to different voltage levels (level translator).

The LM397 is available in the space-saving 5-Pin SOT-23 package and is pin-compatible to TI’s TL331, a single differential comparator.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM397</td>
<td>SOT-23 (5)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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1 Features ................................................................. 1
2 Applications .......................................................... 1
3 Description ............................................................ 1
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2015) to Revision F .................................................. 3
• Changed incorrect Pin Functions table entries. Pins 4 and 5 were swapped.

Changes from Revision D (March 2013) to Revision E .................................................. 1
• Added ESD Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.

Changes from Revision C (March 2013) to Revision D .................................................. 8
• Changed layout of National Data Sheet to TI format.
## 5 Pin Configuration and Functions

![DBV Package 5-Pin SOT-23 Top View](image)

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>NO.</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>2</td>
<td>P</td>
<td>Ground</td>
</tr>
<tr>
<td>OUTPUT</td>
<td>4</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>V.IN+</td>
<td>3</td>
<td>I</td>
<td>Noninverting Input</td>
</tr>
<tr>
<td>V.IN-</td>
<td>1</td>
<td>I</td>
<td>Inverting Input</td>
</tr>
<tr>
<td>V.S</td>
<td>5</td>
<td>P</td>
<td>Supply</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>±15</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>−0.3</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>235</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

(3) The maximum power dissipation is a function of \(T_{J(MAX)}\), \(R_{\theta JA}\). The maximum allowable power dissipation at any ambient temperature is

\[
P_D = \frac{(T_{J(MAX)} - T_A)}{R_{\theta JA}}
\]

All numbers apply for packages soldered directly onto a PCB.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>±200</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.


6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) The maximum power dissipation is a function of \(T_{J(MAX)}\), \(R_{\theta JA}\). The maximum allowable power dissipation at any ambient temperature is

\[
P_D = \frac{(T_{J(MAX)} - T_A)}{R_{\theta JA}}
\]

All numbers apply for packages soldered directly onto a PCB.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>LM397 DBV (SOT-23)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-ambient thermal resistance ((R_{\theta JA}))</td>
<td>186</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-case (top) thermal resistance ((R_{\theta JC(top)}))</td>
<td>92.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board thermal resistance ((R_{\theta JB}))</td>
<td>38.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-top characterization parameter ((\psi_{JT}))</td>
<td>5.6</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board characterization parameter ((\psi_{JB}))</td>
<td>38.4</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

(2) The maximum power dissipation is a function of \(T_{J(MAX)}\), \(R_{\theta JA}\). The maximum allowable power dissipation at any ambient temperature is

\[
P_D = \frac{(T_{J(MAX)} - T_A)}{R_{\theta JA}}
\]

All numbers apply for packages soldered directly onto a PCB.
6.5 Electrical Characteristics

Unless otherwise specified, all limits are ensured for $T_A = 25^\circ C$, $V_S = 5$ V, $V^- = 0$ V, $V_{CM} = V^+/2 = V_O$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(1)</th>
<th>TYP(2)</th>
<th>MAX(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$ Input offset voltage</td>
<td>$V_S = 5$ V to 30 V, $V_O = 1.4$ V, $V_{CM} = 0$ V</td>
<td>$T_A = 25^\circ C$</td>
<td>2</td>
<td>7</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$ Input offset current</td>
<td>$V_O = 1.4$ V, $V_{CM} = 0$ V</td>
<td>$T_A = 25^\circ C$</td>
<td>1.6</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td>250</td>
</tr>
<tr>
<td>$I_B$ Input bias current</td>
<td>$V_O = 1.4$ V, $V_{CM} = 0$ V</td>
<td>$T_A = 25^\circ C$</td>
<td>10</td>
<td>250</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td>400</td>
</tr>
<tr>
<td>$I_S$ Supply current</td>
<td>$R_L$ = open, $V_S = 5$ V</td>
<td></td>
<td>0.25</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$R_L$ = open, $V_S = 30$ V</td>
<td></td>
<td>0.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_O$ Output sink current</td>
<td>$V_{IN}^+ = 1$ V, $V_{IN}^- = 0$ V, $V_O = 1.5$ V</td>
<td></td>
<td>6</td>
<td>13</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{LEAKAGE}$ Output leakage current</td>
<td>$V_{IN}^+ = 1$ V, $V_{IN}^- = 0$ V, $V_O = 5$ V</td>
<td></td>
<td>0.1</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>$V_{IN}^+ = 1$ V, $V_{IN}^- = 0$ V, $V_O = 30$ V</td>
<td></td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{OL}$ Output voltage low</td>
<td>$I_O = -4$ mA, $V_{IN}^+ = 0$ V, $V_{IN}^- = 1$ V</td>
<td>$T_A = 25^\circ C$</td>
<td>180</td>
<td>400</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td>700</td>
</tr>
<tr>
<td>$V_{CM}$ Common-mode input voltage range</td>
<td>$V_S = 5$ V to 30 V(3)</td>
<td>$T_A = 25^\circ C$</td>
<td>0</td>
<td>$V_S - 1.5$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td>0</td>
<td>$V_S - 2$</td>
<td></td>
</tr>
<tr>
<td>$A_V$ Voltage gain</td>
<td>$V_S = 15$ V, $V_O = 1.4$ V to 11.4 V, $R_L &gt; = 15$ kΩ connected to $V_S$</td>
<td></td>
<td>120</td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td>$t_{PHL}$ Propagation delay (high to low)</td>
<td>Input overdrive = 5 mV $R_L = 5.1$ kΩ connected to 5 V, $C_L = 15$ pF</td>
<td></td>
<td>900</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Input overdrive = 50 mV $R_L = 5.1$ kΩ connected to 5 V, $C_L = 15$ pF</td>
<td></td>
<td>250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{PLH}$ Propagation delay (low to high)</td>
<td>Input Overdrive = 5 mV $R_L = 5.1$ kΩ connected to 5 V, $C_L = 15$ pF</td>
<td></td>
<td>940</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>Input overdrive = 50 mV $R_L = 5.1$ kΩ connected to 5 V, $C_L = 15$ pF</td>
<td></td>
<td>440</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) All limits are specified by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) The input common-mode voltage of either input should not be permitted to go below the negative rail by more than 0.3V. The upper end of the common-mode voltage range is $V_S - 1.5$ V at $25^\circ C$. 

Copyright © 2001–2016, Texas Instruments Incorporated
6.6 Typical Characteristics

\( T_A = 25^\circ C \). Unless otherwise specified.

- **Figure 1. Supply Current vs Supply Voltage**
- **Figure 2. Input Bias Current vs Supply Current**
- **Figure 3. Output Saturation Voltage vs Output Sink Current**
- **Figure 4. Input Offset Voltage vs Supply Voltage**
7 Detailed Description

7.1 Overview

A comparator is often used to convert an analog signal to a digital signal. The comparator compares an input voltage ($V_{IN}$) at the noninverting pin to the reference voltage ($V_{REF}$) at the inverting pin. If $V_{IN}$ is less than $V_{REF}$ the output ($V_{O}$) is low ($V_{OL}$). However, if $V_{IN}$ is greater than $V_{REF}$, the output voltage ($V_{O}$) is high ($V_{OH}$). Refer to Figure 6.

![Figure 5. Basic Comparator](https://www.ti.com/lit/ds/sos0977f/sos0977f.pdf)

![Figure 6. Basic Comparator Output](https://www.ti.com/lit/ds/sos0977f/sos0977f.pdf)

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Input Stage

The LM397 has a bipolar input stage. The input common-mode voltage range is from 0 to ($V_{S} - 1.5$ V).

7.3.2 Output Stage

The LM397 has an open-collector grounded-emitter NPN output transistor for the output stage. This requires an external pullup resistor connected between the positive supply voltage and the output. The external pullup resistor should be high enough resistance so to avoid excessive power dissipation. In addition, the pullup resistor should be low enough resistance to enable the comparator to switch with the load circuitry connected. Because it is an open-collector output stage, several comparator outputs can be connected together to create an OR’ing function output. With an open collector, the output can be used as a simple SPST switch to ground. The amount of current which the output can sink is approximately 10 mA. When the maximum current limit is reached, the output transistor will saturate and the output will rise rapidly (Figure 7).
7.4 Device Functional Modes

7.4.1 Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input is near
the input offset voltage of the comparator. This tends to occur when the voltage on the input is equal or very
close to the other input voltage. Adding hysteresis can prevent this problem. Hysteresis creates two switching
thresholds (one for the rising input voltage and the other for the falling input voltage). Hysteresis is the voltage
difference between the two switching thresholds. When both inputs are nearly equal, hysteresis causes one input
to effectively move quickly pass the other. Thus, effectively moving the input out of region that oscillation may
occur.

For an inverting configured comparator, hysteresis can be added with a three resistor network and positive
feedback. When input voltage ($V_{IN}$) at the inverting node is less than non-inverting node ($V_T$), the output is high.
The equivalent circuit for the three resistor network is $R_1$ in parallel with $R_3$ and in series with $R_2$. The lower
threshold voltage $V_{T1}$ is calculated by Equation 1:

$$V_{T1} = ((V_S R_2) / ((R_1 R_3) / (R_1 + R_3)) + R_2)$$  \hspace{1cm} (1)

When $V_{IN}$ is greater than $V_T$, the output voltage is low. The equivalent circuit for the three resistor network is $R_2$
in parallel with $R_3$ and in series with $R_1$. The upper threshold voltage $V_{T2}$ is calculated by Equation 2:

$$V_{T2} = V_S ((R_2 R_3) / (R_2 + R_3)) / (R_1 + ((R_2 R_3) / (R_2 + R_3)))$$  \hspace{1cm} (2)

The hysteresis is defined in Equation 3:

$$\Delta V_{IN} = V_{T1} - V_{T2}$$  \hspace{1cm} (3)
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
LM397 will typically be used to compare a single signal to a reference or two signals against each other.

8.2 Typical Application

8.2.1 Design Requirements
For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>0 V to $V_S - 1.5$ V</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>5 V to 30 V</td>
</tr>
<tr>
<td>Logic supply voltage ($R_{PULLUP}$ voltage)</td>
<td>5 V to 30 V</td>
</tr>
<tr>
<td>Output current ($V_{LOGIC,R_{PULLUP}}$)</td>
<td>1 µA to 20 mA</td>
</tr>
<tr>
<td>Input overdrive voltage</td>
<td>100 mV</td>
</tr>
<tr>
<td>Reference voltage</td>
<td>5.5 V</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure
When using TL331 in a general comparator application, determine the following:
- Input voltage range
- Minimum overdrive voltage
- Output and drive current
8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{CM}) must be taken into account. If temperature operation is above or below 25°C the V_{CM} can range from 0 V to V_S – 1.5 V. This limits the input voltage range to as high as V_S – 1.5 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN– and IN+ are both within the common mode range:
   (a) If IN– is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   (b) If IN– is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN– is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN– is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN– and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage. To make an accurate comparison, the overdrive voltage should be higher than the input offset voltage. Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive.

8.2.2.3 Output and Drive Current

Output current is determined by the pullup resistance (R_{PULLUP}) and V_S voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use Figure 3 to determine V_{OL} based on the output current. The output current can also affect the transient response.

8.2.3 Application Curves

![Figure 10. Response Time for Various Input Overdrives – \(t_{PHL}\)](image1)

![Figure 11. Response Time for Various Input Overdrives – \(t_{PLH}\)](image2)
9 Power Supply Recommendations

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement; see the Layout Guidelines section.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed-circuit-board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the LM397.
- To minimize supply noise, place a decoupling capacitor (0.1-μF ceramic, surface-mount capacitor) as close as possible to $V_S$ as shown in Figure 12.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the top-side ground plane between the output and inputs.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

![Comparator Board Layout](image-url)

Figure 12. Comparator Board Layout
11 Device and Documentation Support

11.1 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary
**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM397MF</td>
<td>NRND</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 85</td>
<td>C397</td>
<td></td>
</tr>
<tr>
<td>LM397MF/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>C397</td>
<td></td>
</tr>
<tr>
<td>LM397MFX/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>C397</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

![Reel Dimensions Diagram]

##### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram]

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM397MF</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LM397MF/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LM397MFX/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM397MF</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LM397MF/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LM397MFX/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: 

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
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