1 Features
- Internal High-Voltage (100 V) Start-Up Regulator
- Single Resistor Oscillator Setting
- Synchronizable
- Precision Reference Output
- Adjustable Soft Start
- Overcurrent Protection
- Direct Optocoupler Interface
- 1.5-A Peak Gate Drivers
- Thermal Shutdown

2 Applications
- Intermediate DC-DC Bus Converter
- Telecommunication Power Converters
- Industrial Power Converters
- 42-V Automotive Systems

3 Description
The LM5033 high-voltage PWM controller contains all the features necessary to implement push-pull, half-bridge, and full-bridge topologies. Applications include closed-loop voltage mode converters with a highly regulated output voltage, or open-loop DC transformers such as an Intermediate bus converter (IBC) with an efficiency greater than 95%. Two alternating gate driver outputs with a specified deadtime are provided.

The LM5033 includes a start-up regulator that operates over a wide input range from 15 V to 100 V. Additional features include: precision voltage reference output, current limit detection, remote shutdown, soft start, sync capability, and thermal shutdown. This high-speed IC has total propagation delays less than 100 ns and a 1-MHz capable oscillator.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
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</thead>
<tbody>
<tr>
<td>LM5033</td>
<td>VSSOP (10)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
<tr>
<td></td>
<td>WSON (10)</td>
<td>4.00 mm × 4.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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Table of Contents

1 Features .................................................................. 1
2 Applications ........................................................... 1
3 Description ............................................................. 1
4 Revision History ..................................................... 2
5 Pin Configuration and Functions ......................... 3
6 Specifications ......................................................... 4
   6.1 Absolute Maximum Ratings ................................. 4
   6.2 ESD Ratings ........................................................ 4
   6.3 Recommended Operating Conditions ..................... 4
   6.4 Thermal Information .............................................. 4
   6.5 Electrical Characteristics ....................................... 5
   6.6 Typical Characteristics .......................................... 6
7 Detailed Description .............................................. 8
   7.1 Overview ........................................................... 8
   7.2 Functional Block Diagram ...................................... 8
   7.3 Feature Description .............................................. 9
8 Application and Implementation ......................... 11
   8.1 Application Information ........................................ 12
   8.2 Typical Application ............................................. 12
9 Power Supply Recommendations ......................... 15
10 Layout................................................................... 15
   10.1 Layout Guidelines .............................................. 15
   10.2 Layout Example ................................................ 16
11 Device and Documentation Support ................. 17
   11.1 Documentation Support ....................................... 17
   11.2 Receiving Notification of Documentation Updates 17
   11.3 Community Resources ....................................... 17
   11.4 Trademarks ....................................................... 17
   11.5 Electrostatic Discharge Caution ......................... 17
   11.6 Glossary ........................................................... 17
12 Mechanical, Packaging, and Orderable Information .............................................................................................................. 17

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C

<table>
<thead>
<tr>
<th>Changes</th>
<th>Page</th>
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</thead>
<tbody>
<tr>
<td>• Added Device Information table, Pin Configuration and Functions section, Specifications section, ESD Ratings table, Thermal Information table, Detailed Description section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section</td>
<td>1</td>
</tr>
<tr>
<td>• Deleted Ordering Information Table; see POA at the end of the datasheet</td>
<td>1</td>
</tr>
<tr>
<td>• Changed values in the Thermal Information table to align with JEDEC standards</td>
<td>4</td>
</tr>
</tbody>
</table>

Changes from Revision A (May 2005) to Revision B

<table>
<thead>
<tr>
<th>Changes</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed layout of National Semiconductor Data Sheet to TI format ..............................................................................................................</td>
<td>1</td>
</tr>
</tbody>
</table>
## 5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP</td>
<td>3 I</td>
<td>Feedback to the inverting input of the PWM comparator, through a 3:1 divider. The output duty cycle increases as the voltage to this pin increases. Internally there is a 5-kΩ pullup resistor to 5.2 V.</td>
</tr>
<tr>
<td>CS</td>
<td>8 I</td>
<td>Current sense input for the current limit detection. If voltage to this pin exceeds 0.5 V the outputs are disabled and the soft-start (SS) pin is discharged to ground.</td>
</tr>
<tr>
<td>GND</td>
<td>—</td>
<td>Connections to external ground must be done with care for optimum performance. See Feature Description and Application and Implementation for more information.</td>
</tr>
<tr>
<td>OUT1</td>
<td>5 O</td>
<td>Alternating output gate driver, which can source and sink 1.5 A.</td>
</tr>
<tr>
<td>OUT2</td>
<td>6 O</td>
<td>Alternating output gate driver, which can source and sink 1.5 A.</td>
</tr>
<tr>
<td>REF</td>
<td>2 O</td>
<td>Sink only, requires an external pullup resistor. This can be used as a 2.5-V precision output reference for external circuitry.</td>
</tr>
<tr>
<td>RT/SYNC</td>
<td>9 I</td>
<td>Oscillator timing resistor pin and synchronization input. An external resistor to ground sets the oscillator frequency. This pin also accepts AC-coupled synchronization pulses from an external source.</td>
</tr>
<tr>
<td>SS</td>
<td>10 I</td>
<td>Soft-start pin. An internal 10-µA current source and an external capacitor set the soft-start timing. This pin can be externally pulled to below 0.5 V to disable the output drivers.</td>
</tr>
<tr>
<td>VCC</td>
<td>4 I/O</td>
<td>9.6-V output from the internal high voltage series pass regulator. An external voltage, 10 V to 15 V, can be applied to this pin to shutdown the internal regulator, reducing internal dissipation. An internal diode connects VCC to VIN.</td>
</tr>
<tr>
<td>VIN</td>
<td>1 I</td>
<td>Input to the start-up regulator. Input range from 15 V to 90 V, with transient capability to 100 V.</td>
</tr>
<tr>
<td>Exposed Pad(1)</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

(1) Only available on the WSON package.
6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN to GND</td>
<td>–0.3</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>VCC to GND</td>
<td>–0.3</td>
<td>16</td>
<td>V</td>
</tr>
<tr>
<td>RT/SYNC to GND</td>
<td>–0.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>COMP, CS, and SS to GND</td>
<td>–0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Power dissipation (2)</td>
<td>Internally Limited</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum junction temperature, T&lt;sub&gt;J(max)&lt;/sub&gt;</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature, T&lt;sub&gt;stg&lt;/sub&gt;</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum allowable power dissipation is a function of the maximum allowed junction temperature (T<sub>J(max)</sub>), the ambient temperature (T<sub>A</sub>), and the junction-to-ambient thermal resistance (θ<sub>JA</sub>). The maximum allowable power dissipation can be calculated from PD = (T<sub>J(max)</sub> – T<sub>A</sub>) / θ<sub>JA</sub>. Excessive power dissipation causes the thermal shutdown to activate.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>15</td>
<td>99</td>
<td>V</td>
</tr>
<tr>
<td>T&lt;sub&gt;J&lt;/sub&gt;</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>LM5033</th>
</tr>
</thead>
<tbody>
<tr>
<td>DGS (VSSOP)</td>
<td>DPR (WSON)</td>
</tr>
<tr>
<td>10 PINS</td>
<td>10 PINS</td>
</tr>
<tr>
<td>R&lt;sub&gt;UA&lt;/sub&gt;</td>
<td>Junction-to-ambient thermal resistance</td>
</tr>
<tr>
<td>R&lt;sub&gt;UC(top)&lt;/sub&gt;</td>
<td>Junction-to-case (top) thermal resistance</td>
</tr>
<tr>
<td>R&lt;sub&gt;UB&lt;/sub&gt;</td>
<td>Junction-to-board thermal resistance</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JT&lt;/sub&gt;</td>
<td>Junction-to-top characterization parameter</td>
</tr>
<tr>
<td>Ψ&lt;sub&gt;JB&lt;/sub&gt;</td>
<td>Junction-to-board characterization parameter</td>
</tr>
<tr>
<td>R&lt;sub&gt;UC(bot)&lt;/sub&gt;</td>
<td>Junction-to-case (bottom) thermal resistance</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Electrical Characteristics

\( V_{IN} = 48 \, \text{V}, \quad V_{CC} = 10 \, \text{V} \) (applied externally), and \( R_T = 26.7 \, \text{k\Omega} \). Typical limits are given for \( T_J = 25^\circ \text{C} \), Minimum and Maximum limits apply over \( T_J = -40^\circ \text{C} \) to \( 125^\circ \text{C} \) (unless otherwise noted).\textsuperscript{(1)(2)}

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CCReg} )</td>
<td>VCC voltage</td>
<td>9.2</td>
<td>9.6</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>( I_{CC(OUT)} )</td>
<td>OUT1 and OUT2 disabled, extended supply to VCC disconnected</td>
<td>20</td>
<td>34</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_N )</td>
<td>Startup regulator current into VIN</td>
<td>150</td>
<td>500</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( UVT )</td>
<td>VCC undervoltage threshold (increasing VCC)</td>
<td>( V_{CCReg} - 300 , \text{mV} )</td>
<td>( V_{CCReg} - 100 , \text{mV} )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{CC(IN)} )</td>
<td>Supply current from external source to VCC</td>
<td>( V_{SS} = 0 , \text{V} )</td>
<td>SS is open, output load = 1800 pF</td>
<td>7</td>
<td>mA</td>
</tr>
<tr>
<td>( V_{REF} )</td>
<td>Output voltage</td>
<td>2.44</td>
<td>2.5</td>
<td>2.56</td>
<td>V</td>
</tr>
<tr>
<td>( CS )</td>
<td>Threshold voltage</td>
<td>0.45</td>
<td>0.5</td>
<td>0.55</td>
<td>V</td>
</tr>
<tr>
<td>( V_{SYNC} )</td>
<td>Sync threshold</td>
<td>3.2</td>
<td>3.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( F_s1 )</td>
<td>Internal frequency</td>
<td>( R_T = 26.7 , \text{k\Omega} )</td>
<td>175</td>
<td>200</td>
<td>225</td>
</tr>
<tr>
<td>( F_s2 )</td>
<td>Internal frequency</td>
<td>( R_T = 8.2 , \text{k\Omega} )</td>
<td>600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PWM} )</td>
<td>Gain from COMP to PWM comparator</td>
<td>0.34</td>
<td></td>
<td></td>
<td>V/V</td>
</tr>
</tbody>
</table>

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI’s Average Outgoing Quality Level (AOQL).

(2) Typical specifications represent the most likely parametric norm at 25°C operation.
6.6 Typical Characteristics

**Figure 1.** $V_{CC}$ vs $V_{IN}$

$V_{CC}$ not externally powered

**Figure 2.** $V_{CC}$ vs $I_{CC}$

$V_{IN} = 48$ V

**Figure 3.** Oscillator Frequency vs $R_T$

$R_T = 26.7$ k$\Omega$

**Figure 4.** Oscillator Frequency vs Temperature

**Figure 5.** Soft-Start Current vs Temperature

**Figure 6.** Dead Time vs Temperature

VCC not externally powered

$|V_{CC}|$ not externally powered
Typical Characteristics (continued)

**Figure 7. Output Duty Cycle vs COMP Voltage**

**Figure 8. V_{REF} vs I_{REF}**

**Figure 9. I_{CC} vs V_{CC}**

**Figure 10. I_{IN} vs V_{IN}**
7 Detailed Description

7.1 Overview
The LM5033 high-voltage PWM controller contains all of the features necessary to implement push-pull and bridge topologies, using voltage-mode control in a small 10-pin package. Features include a start-up regulator, precision 2.5-V reference output, current limit detection, alternating gate drivers, sync capability, thermal shutdown, soft start, and remote shutdown. This high-speed IC has total propagation delays less than 100 ns. These features simplify the design of an open-loop DC-DC converter, or a voltage controlled closed-loop converter.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 High Voltage Start-Up Regulator (VIN and VCC)

The LM5033 contains an internal high-voltage start-up regulator. The input pin (VIN) can be connected directly to line voltages as high as 90 V for normal operation, and can withstand transients to 100 V. The regulator output at VCC, 9.6 V (typical), is internally current limited to 20 mA (minimum). Upon power up, the capacitor at VCC charges up, providing a time delay while internal circuits stabilize. When $V_{CC}$ reaches the upper threshold of the undervoltage sensor (typically 9.5 V), the undervoltage sensor resets, enabling the output drivers, although the PWM duty cycle is initially at zero. As the soft-start capacitor charges up, the output duty cycle increases until regulated by the PWM control loop. The value of the VCC capacitor which affects the start-up delay depends on the total system design and its start-up characteristics. TI recommends the VCC capacitor to be from 0.1 µF to 50 µF.

The lower threshold of the undervoltage sensor is typically at 6.8 V. If $V_{CC}$ falls below this value the outputs are disabled and the soft-start capacitor is discharged. When $V_{CC}$ increases above the upper threshold the outputs are enabled, and the soft-start sequence repeats.

The internal power dissipation of the LM5033 can be reduced by powering VCC from an external supply. Typically this is done by means of an auxiliary transformer winding which is diode connected to the VCC pin to provide 10 V to 15 V as the controller completes the start-up sequence. The externally applied VCC voltage causes the internal regulator to shut off. The undervoltage sensor circuit still functions in this mode, requiring that the external VCC capacitor be sized so that $V_{CC}$ never falls below 6.8 V. The required current into the VCC pin from the external source is shown in Figure 9.

If a fault condition occurs such that the external supply to VCC fails, external current draw from the VCC pin must be limited to not exceed the current limit of the regulator, or the maximum power dissipation of the IC. An external start-up or other bias rail can be used instead of the internal start-up regulator by connecting the VCC and the VIN pins together and feeding the external bias voltage, 10 V to 15 V, into that node.

7.3.2 Reference (REF)

The REF pin provides a reference voltage of 2.5 V ± 2.4%. The pin is internally connected to an NMOS FET drain at the output of the buffer amplifier, allowing it to sink, but not source current. An external pullup resistor is required. Current into the pin must be limited to less than 20 mA to maintain regulation (see Figure 8).

During start-up if the pullup voltage is present before the reference amplifier establishes regulation, the voltage on REF must not exceed 5.5 V. If this reference is not used the REF pin can float or be connected to ground.

7.3.3 PWM Comparator (COMP), Duty Cycle and Deadtime

The PWM comparator compares an internal ramp signal, 0 V to 0.65 V, with the loop-error voltage derived from the COMP pin. The COMP voltage is typically set by an external error amplifier through an optocoupler for closed-loop applications. Internally, the voltage at the COMP pin passes through two level shifting diodes, and a gain reducing, 3:1 resistor divider. The output of the PWM comparator provides the pulse width information to the output drivers (OUT1 and OUT2). This comparator is optimized for speed to achieve minimum discernable duty cycles. The output duty cycle is 0% for $V_{COMP} < 1.5$ V, and maximum for $V_{COMP} > 3.5$ V (see Figure 7). The maximum duty cycle for each output is limited to less than 50% due to the forced deadtime. The typical deadtime from the falling edge of one gate driver output to the rising edge of the other gate driver output is 135 ns, and does not vary with frequency. The maximum duty cycle for each output can be calculated with Equation 1.

$$DC = \frac{(0.5 \times t_s) - t_d}{t_s}$$

where
- $t_s$ is the period of each output
- $t_d$ is the deadtime

For example, if the oscillator frequency is 200 kHz, each output cycles at 100 kHz, and $t_s = 10$ µs. Using the nominal deadtime of 135 ns, the maximum duty cycle at this frequency is 48.65%. Using the minimum deadtime of 85 ns, the maximum duty cycle increases to 49.15%.
Feature Description (continued)

When the SS pin is pulled down, internally or externally, the COMP pin voltage is pulled down with it, with a difference of 0.5 V. When SS voltage increases the COMP voltage is allowed to increase, pulled up by an internal 5.2-V supply through a 5-kΩ resistor.

In an open-loop application, such as an intermediate bus converter, COMP can be left open resulting in maximum duty cycle at the output drivers.

7.3.4 Current Sense (CS)

The current sense circuit is intended to protect the power converter when an abnormal primary current is sensed by initiating a low duty cycle hiccup mode. When the threshold, 0.5 V, at CS is exceeded the outputs are disabled, and the soft-start capacitor is internally discharged. When the soft-start capacitor is fully discharged and the voltage at the CS pin is below 0.5 V, the outputs are re-enabled allowing the soft-start capacitor voltage and the output duty cycle to increase.

The external current sensing circuit must include an RC filter placed near the IC to prevent false triggering of the current sense comparator due to transients or noise. An internal MOSFET discharges the external filter capacitor at the conclusion of each PWM cycle to improve dynamic performance. The discharge time is equal to the deadtime between OUT1 and OUT2 at maximum duty cycle. Additionally, CS is pulled low when V_{CC} is below the undervoltage threshold or when an overtemperature condition occurs.

7.3.5 Oscillator, Sync Capability (RT/SYNC)

The LM5033 oscillator frequency is set by a single external resistor (R_{T}) connected between RT/SYNC and ground. The value of the required R_{T} resistor is calculated with Equation 2.

\[ R_T = \frac{1 - 172 \times 10^{-6}}{182 \times 10^{-12}} \]

where

• \( F_{osc} \) is the desired oscillator frequency

The outputs (OUT1 and OUT2) alternate at half the oscillator frequency. The voltage at the RT/SYNC pin is internally regulated to a nominal 2 V. The R_{T} resistor must be placed as close as possible to the IC, and connected directly to the pins (RT/SYNC and GND).

The LM5033 can be synchronized to an external clock by applying a narrow pulse to RT/SYNC. The external clock must be a higher frequency than the free running frequency set by the R_{T} resistor, and the pulse width must be from 15 ns to 150 ns. The clock signal must be coupled into the RT/SYNC pin through a 100-pF capacitor. When the synchronizing pulse transitions low-to-high, the voltage at RT/SYNC must exceed 3.8 V from its nominal 2-V DC level. During the clock signal low time the voltage at RT/SYNC is clamped at 2 V by an internal regulator. The R_{T} resistor is always required, whether the oscillator is free running or externally synchronized.

7.3.6 Soft Start (SS)

The soft-start feature allows the converter to gradually reach a steady state operating point, thereby reducing start-up stresses and current surges. Upon turnon, after the undervoltage sensor resets at VCC, an internal 10-µA current source charges an external capacitor at SS to generate a ramping voltage, 0 V to 5 V, which allows the voltage on the COMP pin to increase gradually. As the COMP voltage increases the output duty cycle increases from zero to the value required for regulation. Internally, the SS pin is pulled low when a current fault is detected at CS, the VCC voltage is below the lower threshold of the under-voltage sensor, or when a thermal shutdown occurs. Additionally, the SS pin can be pulled low by an external device.

In the event of a current fault, the soft-start capacitor is discharged by an internal pulldown device (see Current Sense (CS)). The falling voltage at SS pulls down the COMP pin, ensuring a minimum output duty cycle when the outputs are re-enabled. Then he soft-start capacitor begins to ramp up, allowing the COMP voltage to increase. As the COMP voltage increases, the output duty cycle increases from zero to the value required for regulation. However, if the fault condition is still present the above sequence repeats until the fault is removed.
Feature Description (continued)

If the VCC voltage falls below the lower undervoltage sensor threshold, typically 6.8 V, the outputs are disabled, and the soft-start capacitor is discharged. The falling voltage at SS pulls down the COMP pin, thereby ensuring minimum output duty cycle when the outputs are re-enabled. After the VCC voltage increases above the upper threshold, typically 9.5 V, the outputs are enabled, and the soft-start capacitor begins to ramp up, allowing the COMP pin voltage to increase. The output duty cycle then increases from zero to the value required for regulation.

In the event of a fault which results in an excessively high die temperature, an internal thermal shutdown circuit is provided to protect the IC. See Thermal Protection for more information.

Using an externally controlled switch, the outputs (OUT1 and OUT2) can be disabled at any time by pulling SS below 0.5 V. This pulls down the COMP pin to near ground, causing the output duty cycle to go to zero. Upon releasing SS, the soft-start capacitor ramps up, allowing the COMP pin voltage to increase. The output duty cycle then increases from zero to the value required for regulation.

7.3.7 OUT1 and OUT2

The LM5033 provides two alternating outputs, OUT1 and OUT2, each capable of sourcing and sinking 1.5-A peak current. Each toggles at one-half the internal oscillator frequency. The voltage output levels are nominally ground and V\text{CC}, minus a saturation voltage at each level which depends on the current flow.

The outputs can drive power MOSFETs directly in a push-pull application, or they can drive a high voltage gate driver (for example, LM5100) in a bridge application.

The outputs are disabled when any of the following conditions occur:
1. An overcurrent condition is detected at CS.
2. The VCC undervoltage sensor is active.
3. An overtemperature condition is detected.
4. The voltage at SS is below 0.5 V.

7.3.8 Thermal Protection

The system design must limit the LM5033 junction temperature to not exceed 125°C during normal operation. However, in the event of a fault which results in a higher die temperature, an internal thermal shutdown circuit is provided to protect the IC. When thermal shutdown is activated, typically at 165°C, the IC is forced into a low power reset state disabling the output drivers and the VCC regulator. This feature helps prevent catastrophic failures from accidental device overheating. When the die temperature drops below 150°C, typical hysteresis is 15°C, the VCC regulator is enabled and a soft-start sequence initiates.

7.4 Device Functional Modes

The LM5033 is a versatile PWM controller that can be used as a half-bridge PWM controller or as a push-pull PWM controller. The LM5033 delivers 180° out-of-phase ground-referenced PWM signals to the gates of power MOSFETs. The LM5033 can also operate in conjunction with a high-side driver, for example, LM5100, to implement in a half-bridge application.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The following information is intended to provide guidelines for implementing the LM5033. However, final selection of all external components is dependent on the configuration and operating characteristics of the complete power conversion system.

8.2 Typical Application
Figure 11 shows an example circuit for a half-bridge, 200-W, DC-DC converter built in a quarter brick format. The circuit is that of an intermediate bus converter (IBC) which operates open-loop (unregulated output), converting a nominal 48-V input to a nominal 9-V output with a 30-mΩ output impedance. The current sense transformer (T2), and the associated filter at the CS pin, provide overcurrent detection at approximately 23 A. The auxiliary winding on T1 powers VCC and the LM5100’s V+ pin (once the outputs are enabled) to reduce power dissipation within the LM5033. The LM5100 provides appropriate level shifting for Q1. Synchronous rectifiers Q3 and Q4 minimize conduction losses in the output stage. Dual comparators U2 and U3 provide undervoltage and overvoltage sensing at VIN. The undervoltage sense levels are 37 V increasing, and 33 V decreasing. The overvoltage sense levels are 63 V increasing, and 61.5 V decreasing. The circuit can be shut down by taking the ON/OFF input below 0.8 V. An external synchronizing frequency can be applied to the SYNC input. Measured efficiency and output characteristics for this circuit are shown in Figure 14 and Figure 15.

Figure 11. Intermediate Bus Converter
40-V to 60-V Input; 7.5-V to 11.3-V, 20-A Output
Typical Application (continued)

8.2.1 Design Requirements

Table 1 lists the input parameters for this design example.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
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<tr>
<td>Input voltage, $V_{IN}$</td>
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<td>48</td>
<td>60</td>
<td>V</td>
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<tr>
<td>Output voltage, $V_{OUT}$</td>
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<td>9</td>
<td>11.3</td>
<td>V</td>
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<td>Output current, $I_{OUT}$</td>
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<td>A</td>
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<td>Output current limit, $I_{LIMIT}$</td>
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<td></td>
<td></td>
<td>A</td>
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<tr>
<td>Load regulation</td>
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<td></td>
<td></td>
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<tr>
<td>Oscillator frequency</td>
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<tr>
<td>Switching frequency</td>
<td>157</td>
<td></td>
<td></td>
<td>kHz</td>
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</table>

8.2.2 Detailed Design Procedure

8.2.2.1 $V_{IN}$

The voltage applied at $V_{IN}$, normally the same as that applied to the primary of the main transformer, can be from 15 V to 90 V, with transient capability to 100 V. The current into $V_{IN}$ depends not only on $V_{IN}$, but also on the load on the output driver pins, any load on $V_{CC}$, and whether or not an external voltage is applied to $V_{CC}$. If $V_{IN}$ is close to the absolute maximum rating of the LM5033, TI recommends the circuit of Figure 12 be used to filter transients which may occur at the input supply.

![Figure 12. Input Transient Protection](image)

If $V_{CC}$ is not powered externally, requiring all internal bias currents for the LM5033, and output driver currents, to be supplied at $V_{IN}$ and through the internal regulator, the required input current ($I_{IN}$) is shown in Figure 10.

If $V_{CC}$ is powered externally, $I_{IN}$ increases with $V_{IN}$ as shown in Figure 9 until the external voltage is applied to $V_{CC}$. In most applications, this occurs once the outputs are enabled and load current begins to flow. The current into $V_{IN}$ then drops to a nominal 150 µA; SS is either open or grounded.

8.2.2.2 $V_{CC}$

The capacitor at the $V_{CC}$ pin provides not only noise filtering and stability, but also a necessary time delay during start-up. The time delay allows the internal circuitry of the LM5033, and associated external circuitry, to stabilize before $V_{CC}$ reaches its final value, at which time the outputs are enabled and the soft-start sequence begins. Any external circuitry connected to the REF output and SS must be designed to stabilize during the time delay.

The current limit of the $V_{CC}$ regulator, and the external capacitor, determine the $V_{CC}$ turnon time delay. Typically, a 1-µF capacitor provides approximately 300 µs of delay, with larger capacitors providing proportionately longer delays. Experimentation with the final design may be necessary to determine the minimum value for the $V_{CC}$ capacitor.
8.2.2.3 Soft Start (SS)
The capacitor at SS determines the time required for the output duty cycle to increase from zero to the final value for regulation. The minimum acceptable time is dependent on the response of the feedback loops to the COMP pin, as well as the characteristics of the magnetic components. If the soft-start time is too quick, the system output could significantly overshoot its intended voltage before the loop is able to establish regulation, possibly adversely affecting the load. Experimentation with the final design is usually necessary to determine the minimum value for the SS capacitor.

8.2.2.4 Current Sense (CS)
This pin typically receives an input representative of the primary current from the current sense elements of the external circuitry. The peak amplitude at this pin must be less than 0.5 V for normal operation. Filtering at this pin must be sufficient to prevent false triggering of the current sense comparator, but not significantly delay detection of an overcurrent condition. The filter’s capacitor at CS must not be larger than 2200 pF.

8.2.2.5 Oscillator, Sync Input (RT/SYNC)
The internal oscillator frequency is generally selected in conjunction with the system magnetic components, and any other aspects of the system which may be affected by the frequency. The $R_T$ resistor at RT/SYNC sets the frequency according to Equation 2. Each output (OUT1 and OUT2) switches at half the oscillator frequency. If the required frequency value is critical in a particular application, the tolerance of the external resistor, and the frequency tolerance indicated in Electrical Characteristics, must be taken into account when selecting the resistor.

If the LM5033 is to be synchronized to an external clock, that signal must be coupled into RT/SYNC through a 100-pF capacitor. The $R_T$ resistor is still required in this case, and it must be selected to set the internal oscillator to a frequency lower than the external synchronizing frequency. The amplitude of the external pulses must take RT/SYNC above 3.8 V on the low-to-high transition but no higher than 5.5 V. The clock pulse width must be from 15 ns to 150 ns.

8.2.2.6 Deadtime Adjustment
TI recommends the circuits in Figure 13 if the application requires a change in the minimum deadtime between the outputs. Suggested values for the resistor and capacitor at each output are 500 $\Omega$, and 100 pF, respectively for a nominal 50-ns change. The diodes can be 1N4148, or similar.

![Figure 13. Deadtime Adjustment](image-url)
8.2.3 Application Curves

![Efficiency vs Output Current](image1)

![VOUT vs Load Current and VIN](image2)

**Figure 14. Efficiency vs Output Current**

**Figure 15. VOUT vs Load Current and VIN**

9 Power Supply Recommendations

The VCC pin requires a local decoupling capacitor that is connected to GND. This capacitor ensures stability of the internal regulator from the VIN pin. The decoupling capacitor also provides the current pulses to drive the gates of the external MOSFETs through the driver output (OUT1 and OUT2) pins. The decoupling capacitor must be placed close to the VCC and GND pins, and must be tracked directly to the pins.

10 Layout

10.1 Layout Guidelines

The LM5033 current sense and PWM comparators are very fast, and as such responds to short-duration noise pulses. Layout considerations are critical for the current sense filter. The components at COMP, CS, RT/SYNC, and SS pins must be placed as close as possible to the IC, thereby minimizing noise pickup in the printed-circuit tracks.

If a current sense transformer is used both leads of the transformer secondary must be routed to the sense filter components, and to the IC pins. The ground side of the transformer must be connected through a dedicated printed-circuit track to GND of the IC rather than through the ground plane.

If the current sense circuit employs a sense resistor in the drive transistor sources, a low-inductance resistor must be used. In this case all the noise-sensitive low-power grounds must be connected in common near the IC, and then a single connection made to the power ground (sense resistor ground point).

The outputs of the LM5033, or of the high-voltage gate driver (if used), must have short, direct paths to the power MOSFETs to minimize the effects of inductance in the PCB traces.

If the internal dissipation of the LM5033 and any of the power devices produces high junction temperatures during normal operation, good use of the PCB ground plane can help considerably to dissipate heat. The exposed pad on the bottom of the 10-pin WSON package can be soldered to the ground plane on the PCB, and the ground plane must extend out from beneath the IC to help dissipate the heat. The exposed pad is internally connected to the IC substrate.

Additionally, the use of wide PCB traces where possible can help conduct heat away from the IC. Judicious positioning of the PCB within the end product, along with use of any available air flow (forced or natural convection) can help reduce the junction temperatures.
10.2 Layout Example

Figure 16. Layout Recommendation
11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation
For related documentation see the following:

AN-1187 Leadless Leadframe Package (LLP) (SNOA401)

11.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community  TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support  TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 —  Ti Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## Packaging Information

<table>
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<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

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*All dimensions are nominal*

---

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

---

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

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### TAPE AND REEL BOX DIMENSIONS

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*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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