1 Features

- **AEC-Q100 Qualified:**
  - Device Temperature Grade 1: −40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- **Wide VIN Input Range** From 1.5 V to 42 V When \( \text{VOUT} \geq 5 \text{V} \) (65-V Absolute Maximum)
- **Low Shutdown Current** (\( \text{I}_{\text{Q}} \leq 5 \mu\text{A} \))
- **Low Standby Current** (\( \text{I}_{\text{Q}} \leq 15 \mu\text{A} \))
- **Four Programmable Output Voltage Options and Two Selectable Configurations**
  - 6.8 V, 7.5 V, 8.5 V, or 10.5 V
  - Start-Stop or E-Call Configurations
- **Adjustable Switching Frequency** From 220 kHz to 2.3 MHz
- **Automatic Wake-Up and Standby Mode Transition**
- **Optional Clock Synchronization**
- **Boost Status Indicator**
- **1.5-A Peak MOSFET Gate Driver**
- **Adjustable Cycle-by-Cycle Current Limit**
- **Thermal Shutdown**
- **16-Pin WQFN With Watettable Flanks**
- **Create a Custom Design Using the LM5150-Q1 With the WEBENCH® Power Designer**

2 Applications

- Automotive Start-Stop System
- Automotive Emergency Call System
- Battery-Powered Boost Converters

3 Description

The LM5150-Q1 device is a wide input range automatic boost controller. The device is suitable for use as a pre-boost converter which maintains the output voltage from a vehicle battery during automotive cranking or from a back-up battery during the loss of vehicle battery.

The LM5150-Q1 switching frequency is programmed by a resistor from 220 kHz to 2.3 MHz. Fast switching (\( \geq 2.2\text{-MHz} \)) minimizes AM band interference and allows for a small solution size and fast transient response.

The LM5150-Q1 operates in low \( \text{I}_{\text{Q}} \) standby mode when the input or output voltage is above the preset standby thresholds and automatically wakes up when the output voltage drops below the preset wake-up threshold.

The device transients in and out of the low \( \text{I}_{\text{Q}} \) standby mode to extend battery life at light load. A single resistor programs the target output regulation voltage as well as the configuration. Additional features include low shutdown current, boost status indicator, adjustable cycle-by-cycle current limit, and thermal shutdown.

### Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM5150-Q1</td>
<td>WQFN (16)</td>
<td>4.00 mm × 4.00 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.
Table of Contents

1 Features ................................................................. 1
2 Applications ......................................................... 1
3 Description ............................................................ 1
4 Revision History ...................................................... 2
5 Pin Configuration and Functions ................................. 3
6 Specifications .......................................................... 4
    6.1 Absolute Maximum Ratings ................................. 4
    6.2 ESD Ratings ..................................................... 4
    6.3 Recommended Operating Conditions ....................... 5
    6.4 Thermal Information ........................................... 5
    6.5 Electrical Characteristics ..................................... 5
    6.6 Typical Characteristics ....................................... 8
7 Detailed Description ................................................ 10
    7.1 Overview ......................................................... 10
    7.2 Functional Block Diagram ................................... 11
    7.3 Feature Description ............................................ 11
    7.4 Device Functional Modes ..................................... 17
8 Application and Implementation ............................... 21
    8.1 Application Information ...................................... 21
    8.2 Typical Application ......................................... 24
    8.3 System Examples .............................................. 31
9 Power Supply Recommendations ............................... 33
10 Layout ................................................................. 33
    10.1 Layout Guidelines ........................................... 33
    10.2 Layout Example ............................................... 34
11 Device and Documentation Support ........................... 35
    11.1 Device Support ............................................... 35
    11.2 Receiving Notification of Documentation Updates .... 35
    11.3 Community Resources ....................................... 35
    11.4 Trademarks .................................................... 35
    11.5 Electrostatic Discharge Caution .......................... 35
    11.6 Glossary ........................................................ 35
12 Mechanical, Packaging, and Orderable Information ....... 36

4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>September 2017</td>
<td>*</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO.</td>
<td>NAME</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SYNC</td>
<td>I</td>
</tr>
<tr>
<td>2</td>
<td>STATUS</td>
<td>O</td>
</tr>
<tr>
<td>3</td>
<td>EN</td>
<td>I</td>
</tr>
<tr>
<td>4</td>
<td>VOUT</td>
<td>I/P</td>
</tr>
<tr>
<td>5</td>
<td>PVCC</td>
<td>O/P</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td>—</td>
</tr>
<tr>
<td>7</td>
<td>AVCC</td>
<td>I/P</td>
</tr>
<tr>
<td>8</td>
<td>NC</td>
<td>—</td>
</tr>
<tr>
<td>9</td>
<td>LO</td>
<td>O</td>
</tr>
<tr>
<td>10</td>
<td>PGND</td>
<td>G</td>
</tr>
<tr>
<td>11</td>
<td>AGND</td>
<td>G</td>
</tr>
<tr>
<td>12</td>
<td>CS</td>
<td>I</td>
</tr>
<tr>
<td>13</td>
<td>COMP</td>
<td>O</td>
</tr>
<tr>
<td>14</td>
<td>RT</td>
<td>I</td>
</tr>
</tbody>
</table>

(1) G = GROUND, I = INPUT, O = OUTPUT, P = POWER

Copyright © 2017, Texas Instruments Incorporated

Product Folder Links: LM5150-Q1
Pin Functions (continued)

<table>
<thead>
<tr>
<th>NO.</th>
<th>NAME</th>
<th>I/O(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>VSET</td>
<td>I</td>
<td>Configuration selection and VOUT regulation target programming pin. During initial power on, a resistor between the VSET pin and AGND configures the VOUT regulation target and the configuration.</td>
</tr>
<tr>
<td>16</td>
<td>VIN</td>
<td>I</td>
<td>Boost input voltage sensing pin. Connect to the input supply of the boost converter.</td>
</tr>
<tr>
<td>—</td>
<td>EP</td>
<td>—</td>
<td>Exposed pad of the package. No internal electrical connection to silicon die. The EP is electrically connected to anchor pads. The EP must be connected to the large ground copper plain to reduce thermal resistance.</td>
</tr>
<tr>
<td>—</td>
<td>AP</td>
<td>—</td>
<td>Anchor pad of the package. No internal electrical connection to silicon die. The AP is electrically connected to the EP. The AP can be left floating or soldered to the ground copper.</td>
</tr>
</tbody>
</table>

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>PIN</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN to AGND</td>
<td>-0.3</td>
<td>65</td>
<td>V</td>
</tr>
<tr>
<td>VOUT to AGND</td>
<td>-0.3</td>
<td>65</td>
<td>V</td>
</tr>
<tr>
<td>EN to AGND</td>
<td>-0.3</td>
<td>65</td>
<td>V</td>
</tr>
<tr>
<td>RT to AGND(2)</td>
<td>-0.3</td>
<td>AVCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>SYNC to AGND</td>
<td>-0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>VSET to AGND</td>
<td>-0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>CS to AGND (DC)</td>
<td>-0.3</td>
<td>AVCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>CS to AGND (40ns transient)</td>
<td>-1.0</td>
<td>AVCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>CS to AGND (20ns transient)</td>
<td>-2.0</td>
<td>AVCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>PGND to AGND</td>
<td>-0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>LO to AGND (DC)</td>
<td>-0.3</td>
<td>PVCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>LO to AGND (40ns transient)</td>
<td>-1.0</td>
<td>PVCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>LO to AGND (20ns transient)</td>
<td>-2.0</td>
<td>PVCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>STATUS to AGND(3)</td>
<td>-0.3</td>
<td>65</td>
<td>V</td>
</tr>
<tr>
<td>COMP to AGND(2)</td>
<td>-0.3</td>
<td>AVCC+0.3</td>
<td>V</td>
</tr>
<tr>
<td>AVCC to AGND</td>
<td>-0.3</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>PVCC to AVCC</td>
<td>-0.3</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>(T_J) JunctionTemperature(4)</td>
<td>-40</td>
<td>150</td>
<td>℃</td>
</tr>
<tr>
<td>(T_{stg}) Storage Temperature</td>
<td>-55</td>
<td>150</td>
<td>℃</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The pin voltage is clamped by an internal circuit, and is not specified to have an external voltage applied.

(3) STATUS can go below ground during the STATUS low-to-high transition. The negative voltage on STATUS during this transition is clamped by an internal diode and it does not damage the device.

(4) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per AEC Q100-002(1)</td>
<td>-2000</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged device model (CDM), per AEC Q100-011 Corner pins</td>
<td>-750</td>
<td>750</td>
<td></td>
</tr>
<tr>
<td>Charged device model (CDM), per AEC Q100-011 Other pins</td>
<td>-500</td>
<td>500</td>
<td></td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise specified)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{VIN}})</td>
<td>Boost input voltage sense</td>
<td>1.5</td>
<td>42</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{VOUT}})</td>
<td>Boost output voltage sense(^{(2)})</td>
<td>5</td>
<td>42</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{EN}})</td>
<td>EN input</td>
<td>0</td>
<td>42</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{PVCC}})</td>
<td>PVCC Voltage(^{(3)})</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{SYNC}})</td>
<td>SYNC Input</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{\text{CS}})</td>
<td>Current sense Input</td>
<td>0</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(F_{\text{SW}})</td>
<td>Typical switching frequency</td>
<td>220</td>
<td>2300</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>(F_{\text{SYNC}})</td>
<td>Synchronization pulse frequency</td>
<td>220</td>
<td>2300</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>(T_{\text{J}})</td>
<td>Operating junction temperature(^{(4)})</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

(2) The device requires minimum 5V at VOUT pin to start up

(3) \(V_{\text{PVCC}}\) should be less than \(V_{\text{VOUT}} + 0.3\) V

(4) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>(\text{LM5150-Q1})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{UA}}) Junction-to-ambient thermal resistance</td>
<td>44.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{UB}}) Junction-to-board thermal resistance</td>
<td>19.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\Psi_{\text{JT}}) Junction-to-top characterization parameter</td>
<td>0.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>(\Psi_{\text{JB}}) Junction-to-board characterization parameter</td>
<td>19.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>(R_{\text{UB}}) Junction-to-case (bottom) thermal resistance</td>
<td>2</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Typical values correspond to \(T_{\text{J}} = 25°C\). Minimum and maximum limits apply over \(T_{\text{J}} = -40°C\) to 125°C. Unless otherwise stated, \(V_{\text{VOUT}} = 6.8\) V, \(R_{\text{T}} = 9.09\) kΩ

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{\text{SHUTDOWN(VOUT)}})</td>
<td>VOUT shutdown current</td>
<td>(V_{\text{VOUT}} = 12) V, (V_{\text{EN}} = 0) V</td>
<td>5</td>
<td>12</td>
<td>µA</td>
</tr>
<tr>
<td>(I_{\text{STANDBY(VOUT)}})</td>
<td>VOUT standby current (PVCC in regulation, STATUS is low)</td>
<td>(V_{\text{VOUT}} = 12) V, (V_{\text{EN}} = 3.3) V, (R_{\text{SET}} = 90.9) kΩ</td>
<td>15</td>
<td>25</td>
<td>µA</td>
</tr>
<tr>
<td>(I_{\text{WAKEUP(VOUT)}})</td>
<td>VOUT operating current (exclude current into RT resistor)</td>
<td>(V_{\text{VOUT}} = 10.5) V, (V_{\text{EN}} = 2.5) V, non-switching, (R_{\text{T}} = 9.09) kΩ</td>
<td>1.2</td>
<td>2.0</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{\text{SHUTDOWN(VIN)}})</td>
<td>VIN shutdown current</td>
<td>(V_{\text{VIN}} = 12) V, (V_{\text{EN}} = 0) V</td>
<td>0.1</td>
<td>0.5</td>
<td>µA</td>
</tr>
<tr>
<td>(I_{\text{STANDBY(VIN)}})</td>
<td>VIN standby current</td>
<td>(V_{\text{VIN}} = 12) V, (V_{\text{EN}} = 3.3) V, (R_{\text{SET}} = 29.4) kΩ</td>
<td>0.1</td>
<td>0.5</td>
<td>µA</td>
</tr>
<tr>
<td>(I_{\text{WAKEUP(VIN)}})</td>
<td>VIN operating current</td>
<td>(V_{\text{VIN}} = 10.5) V, (V_{\text{EN}} = 2.5) V, non-switching, (R_{\text{T}} = 9.09) kΩ</td>
<td>30</td>
<td>45</td>
<td>µA</td>
</tr>
</tbody>
</table>

**VCC REGULATOR**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{VCC-REG-NOLOAD}})</td>
<td>PVCC regulation</td>
<td>(V_{\text{VOUT}} = 6.0) V, No load, wake-up mode</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
</tr>
<tr>
<td>(V_{\text{VCC-REG-FULLLOAD}})</td>
<td>PVCC regulation</td>
<td>(V_{\text{VOUT}} = 5.0) V, (I_{\text{PVCC}} = 70) mA</td>
<td>4.5</td>
<td>4.8</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{VCC-UVLO-RISING}})</td>
<td>AVCC UVLO threshold</td>
<td>AVCC rising</td>
<td>4.1</td>
<td>4.3</td>
<td>4.5</td>
</tr>
<tr>
<td>(V_{\text{VCC-UVLO-FALLING}})</td>
<td>AVCC UVLO threshold</td>
<td>AVCC falling</td>
<td>3.9</td>
<td>4.1</td>
<td>4.3</td>
</tr>
</tbody>
</table>

Copyright © 2017, Texas Instruments Incorporated

Product Folder Links: LM5150-Q1
Electrical Characteristics (continued)

Typical values correspond to $T_J = 25^\circ C$. Minimum and maximum limits apply over $T_J = -40^\circ C$ to $125^\circ C$. Unless otherwise stated, $V_{\text{VOUT}} = 6.8$ V, $R_T = 9.09$ kΩ

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{VCC-UVLO-HYS}}$</td>
<td>AVCC UVLO hysteresis</td>
<td>0.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{VCC-CL}}$</td>
<td>PVCC sourcing current limit</td>
<td>$V_{\text{PVCC}} = 0$ V, wake-up mode</td>
<td>75</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td><strong>ENABLE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{EN-RISING}}$</td>
<td>Enable threshold, EN rising</td>
<td>1.7</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{EN-FALLING}}$</td>
<td>Enable threshold, EN falling</td>
<td>1</td>
<td>1.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{EN}}$</td>
<td>EN bias current, $V_{\text{EN}} = 42$ V</td>
<td>100</td>
<td>nA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 6.8-V SETTING

| $V_{\text{VOUT-REG}}$      | VOUT regulation target            | $R_{\text{SET}} = 29.4$ kΩ or 90.9 kΩ | 6.66 | 6.80 | 6.98 | V    |
| $V_{\text{VOUT-WAKEUP}}$   | VOUT wake-up threshold             | $R_{\text{SET}} = 29.4$ kΩ or 90.9 kΩ, VOUT falling | 6.83 | 7.00 | 7.14 | V    |
| $V_{\text{VOUT-STANDBY1}}$ | VOUT standby threshold             | $R_{\text{SET}} = 90.9$ kΩ, VOUT rising | 7.02 | 7.21 | 7.35 | V    |
| $V_{\text{VOUT-STANDBY2}}$ | VOUT standby threshold             | $R_{\text{SET}} = 29.4$ kΩ, VOUT rising | 8.22 | 8.43 | 8.60 | V    |
| $V_{\text{VOUT-STATUS-OFF}}$ | VOUT standby threshold             | $R_{\text{SET}} = 29.4$ kΩ, VIN rising | 7.82 | 8.00 | 8.19 | V    |

### 7.5-V SETTING

| $V_{\text{VOUT-REG}}$      | VOUT regulation target            | $R_{\text{SET}} = 19.1$ kΩ or 71.5 kΩ | 7.37 | 7.50 | 7.67 | V    |
| $V_{\text{VOUT-WAKEUP}}$   | VOUT wake-up threshold             | $R_{\text{SET}} = 19.1$ kΩ or 71.5 kΩ, VOUT falling | 7.52 | 7.73 | 7.88 | V    |
| $V_{\text{VOUT-STANDBY1}}$ | VOUT standby threshold             | $R_{\text{SET}} = 71.5$ kΩ, VOUT rising | 7.74 | 7.95 | 8.11 | V    |
| $V_{\text{VOUT-STANDBY2}}$ | VOUT standby threshold             | $R_{\text{SET}} = 19.1$ kΩ, VOUT rising | 9.07 | 9.30 | 9.46 | V    |
| $V_{\text{VIN-STANDBY}}$   | VIN standby threshold              | $R_{\text{SET}} = 19.1$ kΩ, VIN rising | 8.50 | 8.73 | 8.93 | V    |

### 8.5-V SETTING

| $V_{\text{VOUT-REG}}$      | VOUT regulation target            | $R_{\text{SET}} = 9.53$ kΩ or 54.9 kΩ | 8.37 | 8.50 | 8.69 | V    |
| $V_{\text{VOUT-WAKEUP}}$   | VOUT wake-up threshold             | $R_{\text{SET}} = 9.53$ kΩ or 54.9 kΩ, VOUT falling | 8.52 | 8.76 | 8.93 | V    |
| $V_{\text{VOUT-STANDBY1}}$ | VOUT standby threshold             | $R_{\text{SET}} = 54.9$ kΩ, VOUT rising | 8.78 | 9.01 | 9.19 | V    |
| $V_{\text{VOUT-STANDBY2}}$ | VOUT standby threshold             | $R_{\text{SET}} = 9.53$ kΩ, VOUT rising | 10.29 | 10.54 | 10.72 | V    |
| $V_{\text{VIN-STANDBY}}$   | VIN standby threshold              | $R_{\text{SET}} = 9.53$ kΩ, VIN rising | 9.50 | 9.76 | 9.98 | V    |

### 10.5-V SETTING

| $V_{\text{VOUT-REG}}$      | VOUT regulation target            | $R_{\text{SET}} = \text{GND}$ or 41.2 kΩ | 10.31 | 10.50 | 10.75 | V    |
| $V_{\text{VOUT-WAKEUP}}$   | VOUT wake-up threshold             | $R_{\text{SET}} = \text{GND}$ or 41.2 kΩ, VOUT falling | 10.53 | 10.82 | 11.02 | V    |
| $V_{\text{VOUT-STANDBY1}}$ | VOUT standby threshold             | $R_{\text{SET}} = 41.2$ kΩ, VOUT rising | 10.84 | 11.13 | 11.33 | V    |
Electrical Characteristics (continued)

Typical values correspond to $T_J = 25°C$. Minimum and maximum limits apply over $T_J = -40°C$ to 125°C. Unless otherwise stated, $V_{VOUT} = 6.8$ V, $R_T = 9.09$ kΩ

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{VOUT STATUS-OFF}$</td>
<td>$V_{VOUT}$ status off threshold ($V_{VOUT-REG} +12%$, EC config)</td>
<td>$R_{SET} = 41.2$ kΩ, $VOUT$ rising</td>
<td>11.46</td>
<td>11.76</td>
<td>12.04</td>
</tr>
<tr>
<td>$V_{VOUT STANDBY2}$</td>
<td>$VOUT$ standby threshold ($V_{VOUT-REG} +24%$, SS config)</td>
<td>$R_{SET} = \text{GND}$, $VOUT$ rising</td>
<td>12.70</td>
<td>13.02</td>
<td>13.24</td>
</tr>
<tr>
<td>$V_{VIN STANDBY}$</td>
<td>$VIN$ standby threshold ($V_{VOUT-WAKEUP} + 1.0$ V, SS config)</td>
<td>$R_{SET} = \text{GND}$, $VIN$ rising</td>
<td>11.47</td>
<td>11.82</td>
<td>12.11</td>
</tr>
</tbody>
</table>

**RT**

$V_{RT-REG}$

RT regulation voltage

1.2 V

**CLOCK SYNCHRONIZATION**

$V_{SYNC-RISING}$

SYNC rising threshold

2.0 V

$V_{SYNC-FALLING}$

SYNC falling threshold

0.4 V

**PULSE WIDTH MODULATION AND OSCILLATOR**

$F_{SW1}$

Switching frequency

$R_T = 93.1$ kΩ

204 239 270 kHz

$F_{SW2}$

Switching frequency

$R_T = 9.09$ kΩ

2100 2300 2500 kHz

$T_{ON-MIN}$

Forced minimum on-time

SS config, $V_{COMP} = 0$ V

30 50 70 ns

$D_{MIN}$

Minimum duty cycle limit (EC config)

$R_T = 9.09$ kΩ, $F_{SYNC} = 2.0$ MHz

60 %

$F_{SW3}$

Switching frequency

$R_T = 9.09$ kΩ

2000 kHz

$D_{MAX}$

Maximum duty cycle limit

EC config, $R_T = 93.1$ kΩ

83 87 91.5 %

**CURRENT SENSE**

$V_{CSTH}$

Current limit threshold (CS-AGND)$^{(1)}$

$V_{VIN} = 5.1$ V, $V_{VOUT} = 6.8$ V at 25% DC

102 120 138 mV

$V_{VIN} = 3.4$ V, $V_{VOUT} = 6.8$ V at 50% DC

102 120 138 mV

$V_{VIN} = 1.7$ V, $V_{VOUT} = 6.8$ V at 75% DC

102 120 138 mV

**ERROR AMPLIFIER**

$Gm$

Transconductance

2 mA/V

COMP sourcing current

$V_{COMP} = 0$ V

312 μA

COMP sinking current

$V_{COMP} = 1.5$ V

120 μA

COMP clamp voltage

2.4 2.6 V

COMP to PWM offset

0.3 V

**STATUS**

Low-state voltage drop

1-mA sinking

0.1 V

STATUS rise to LO delay

5-kΩ pullup to 5 V

4 5 6 μs

**MOSFET DRIVER**

High-state voltage drop

50-mA sinking

0.075 V

Low-state voltage drop

50-mA sourcing

0.055 V

**THERMAL SHUTDOWN (TSD)**

Thermal shutdown threshold

Temperature rising

175 °C

Thermal shutdown hysteresis

15 °C

$^{(1)}$ $V_{CL}$ at the current limit comparator input is $10 \times V_{CSTH}$
6.6 Typical Characteristics

Figure 1. Peak Inductor Current vs Supply Voltage
(F_SW = 250 kHz, R_S = 8 mΩ)

Figure 2. Current Limit Threshold at CS vs Duty Cycle

Figure 3. V_PVCC vs I_PVCC (VOUT = 6 V)

Figure 4. V_PVCC vs V_VOUT (EN = 3.3 V, I_PVCC = 10 mA, VOUT Rising)

Figure 5. Frequency vs RT

Figure 6. Duty Cycle Limit in EC Configuration vs V_VIN

Figure 7. Duty Cycle Limit in EC Configuration vs V_VIN

Figure 8. Duty Cycle Limit in EC Configuration vs V_VIN
Typical Characteristics (continued)

![Figure 7. \(I_{VOUT}\) vs Temperature](image)

![Figure 8. Efficiency vs Load Current](image)

\(V_{LOAD} = 6.8\ V, F_{SW} = 440\ kHz, SS\ Configuration\)
7 Detailed Description

7.1 Overview

The LM5150-Q1 device is a wide input range automotive boost controller designed for automotive start-stop or emergency-call applications. The device can maintain the output voltage from a vehicle battery during automotive cranking or from a back-up battery during the loss of vehicle battery. The wide input range of the device covers automotive load dump transient. The control method is based upon peak current mode control.

To extend the battery life time, the LM5150-Q1 features a low $I_Q$ standby mode with automatic wake-up and standby control. The device stays in the low $I_Q$ standby mode when the boost operation is not required, and automatically enters the wake-up mode when the output voltage drops below the preset wake-up threshold. High value feedback resistors are included inside the device to minimize leakage current in the low $I_Q$ standby mode.

The LM5150-Q1 operates in one of two selectable configurations when waking up. In Start-Stop configuration (SS configuration), the device runs at a fixed switching frequency without any pulse skipping until entering into the standby mode, which helps to have a fixed EMI spectrum. In Emergency-Call configuration (EC configuration), the device will skip pulses as it automatically alternates between low $I_Q$ standby mode and wake-up mode to extend the battery life in light load conditions.

The LM5150-Q1 switching frequency is programmable from 220 kHz to 2.3 MHz. Fast switching ($\geq 2.2$-MHz) minimizes AM band interference and allows for a small solution size and fast transient response. A single resistor at the VSET pin programs the target output regulation voltage as well as the configuration. This eliminates the need for an external feedback resistor divider which enables low $I_Q$ operation. The device also features clock synchronization in the SS configuration, low quiescent current in shutdown mode, a boost status indicator, adjustable cycle-by-cycle current will limit, and thermal shutdown protection.
7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Enable (EN Pin)
When the EN pin voltage is less than 1 V, the LM5150-Q1 is in shutdown mode with all other functions disabled. To turn on the internal VCC regulator and begin start-up sequence, the EN pin voltage must be greater than 2 V. If the EN pin is controlled by user input, it is recommended to supply a voltage greater than 3 V at the EN pin. If the EN pin is not controlled by user input, connect the EN pin to the VOUT pin directly. See Device Functional Modes for more detailed information.

7.3.2 High Voltage VCC Regulator (PVCC, AVCC Pin)
The LM5150-Q1 contains an internal high voltage VCC regulator. The VCC regulator turns on when the EN pin voltage is greater than 2 V. The VCC regulator is sourced from the VOUT pin and provides 5 V (typical) bias supply for the N-channel MOSFET driver and other internal circuits.

The VCC regulator sources current into the capacitor connected to the PVCC pin with a minimum of 75-mA capability when the LM5150-Q1 is in the wake-up mode and during the device configuration period. The maximum sourcing capability is decreased to 17 mA in standby mode. The recommended PVCC capacitor is 4.7 µF to 10 µF. In normal operation, the PVCC pin voltage is either 5 V or V_{VOUT} + 0.3 V, whichever is lower.

The AVCC pin is the analog bias supply input of the LM5150-Q1. The recommended AVCC capacitor is 0.1-µF. Connect to the PVCC pin through 10-Ω resistor.
Feature Description (continued)

7.3.3 Power-On Voltage Selection (VSET Pin)

During initial power on, the VOUT regulation target and the configuration are configured by a resistor connected between the VSET and the AGND pins. The configuration starts when the EN pin voltage is greater than 2 V and the AVCC voltage crosses the AVCC UVLO threshold, and requires typically 50 µs to finish. To reset and reconfigure, EN should be toggled below 1 V or AVCC/VOUT must be fully discharged.

![Figure 9. Power-On Voltage Selection](image)

The VOUT regulation target can be programmed to 6.8 V, 7.5 V, 8.5 V, or 10.5 V with the appropriate resistor with 5% tolerance. The configuration can be selected as either SS or EC configuration. The LM5150-Q1 will not switch during the 50-µs configuration time.

<table>
<thead>
<tr>
<th>CONFIGURATION</th>
<th>CONFIGURATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT regulation target</td>
<td>6.8 V</td>
</tr>
<tr>
<td>( R_{SET} ) [Ω]</td>
<td>90.9k</td>
</tr>
</tbody>
</table>

(1) If other output regulation targets are required, contact the sales office/distributors for availability.

7.3.4 Switching Frequency (RT Pin)

The switching frequency of the LM5150-Q1 is set by a single RT resistor connected between the RT and the AGND pins. The resistor value to set the switching frequency (\( F_{SW} \)) is calculated using Equation 1.

\[
R_T = \frac{2.233 \times 10^{10}}{F_{SW \_RT \_TYPICAL}} - 619 \, \Omega
\]

(1)

The RT pin is regulated to 1.2 V by the internal RT regulator during wake-up.

7.3.5 Clock Synchronization (SYNC Pin in SS Configuration)

In SS configuration, the switching frequency of the LM5150-Q1 can be synchronized to an external clock by directly applying a pulse signal to the SYNC pin. The internal clock of the LM5150-Q1 is synchronized at the rising edge of the external clock. The device ignores the rising edge input during forced off-time.

The external synchronization pulse must be greater than the 2.4 V in the high logic state and must be less than 0.4 V in the low logic state. The duty cycle of the external synchronization pulse is not limited, but the minimum pulse width should be greater than 100 ns. Because the maximum duty cycle limit and the peak current limit threshold are affected by synchronizing the switching frequency to an external synchronization pulse, take extra care when using the clock synchronization function. See the Maximum Duty Cycle Limit, Minimum Input Supply Voltage and Current Limit (CS Pin) section for more detailed information.
If the boost converter’s minimum input supply voltage is greater than \( \frac{1}{4} \) of the VOUT regulation target \( (V_{\text{OUT-REG}}) \), the frequency of the external synchronization pulse \( (F_{\text{SYNC}}) \) should be within +15% and -15% of the typical free-running switching frequency \( (F_{\text{SW(TYPICAL)}}) \):

\[
0.85 \times F_{\text{SW RT(TYPICAL)}} \leq F_{\text{SYNC}} \leq 1.15 \times F_{\text{SW RT(TYPICAL)}}
\]  

(2)

In this range, a maximum 1:4 \( (V_{\text{SUPPLY}}:V_{\text{LOAD}}) \) step-up ratio is allowed.

A higher step-up ratio can be achieved by supplying a lower frequency synchronization pulse. 1:5 step-up ratio can be achieved by selecting \( F_{\text{SYNC}} \) within -25% and -15% of the \( F_{\text{SW RT(TYPICAL)}} \):

\[
0.75 \times F_{\text{SW RT(TYPICAL)}} \leq F_{\text{SYNC}} \leq 0.85 \times F_{\text{SW RT(TYPICAL)}}
\]

(3)

In this range, a maximum 1:5 \( (V_{\text{SUPPLY}}:V_{\text{LOAD}}) \) step-up ratio is allowed.

### 7.3.6 Current Sense, Slope Compensation, and PWM (CS Pin)

The LM5150-Q1 features low-side current sense amplifier with a gain of 10, and provides an internal slope compensation ramp to prevent sub-harmonic oscillation at high duty cycle. The device generates the slope compensation ramp using a sawtooth current source with a slope of 30 \( \mu \)A \( \times F_{\text{SW}} \) (typical). This current flows through an internal 2-k\( \Omega \) resistor and out of the CS pin. The slope compensation ramp is determined by the RT resistor and is 60 mV \( \times F_{\text{SW}} \) (typical) at the input of the current sense amplifier and 600 mV \( \times F_{\text{SW}} \) (typical) at the output of the current sense amplifier. The slope compensation ramp can be increased by adding an external slope resistor \( (R_{\text{SL}}) \) between the sense resistor \( (R_{\text{S}}) \) and the CS pin, but take extra care when using the \( R_{\text{SL}} \), because the peak current limit is affected by adding \( R_{\text{SL}} \). See Current Limit (CS Pin) for more detailed information.

According to peak current mode control theory, the slope of the compensation ramp must be greater than half of the sensed inductor current falling slope to prevent sub-harmonic oscillation at high duty cycle. Therefore, the minimum amount of slope compensation should satisfy the following inequality.

\[
0.5 \times \left( \frac{V_{\text{LOAD}} + V_{\text{F}}}{L_{\text{M}}} \right) - V_{\text{SUPPLY}} \times R_{\text{S}} \times \text{Margin} < 30 \mu \text{A} \times (2\text{k}\Omega + R_{\text{SL}}) \times F_{\text{SW}}
\]

(4)

\( V_{\text{F}} \) is a forward voltage drop of D1, the external diode. 1.2 is recommended as a margin to cover non-ideal factors.

If required, \( R_{\text{SL}} \) can be added to increase the slope of the compensation ramp from half to 82% of the slope of the sensed inductor current during the falling slope. The typical \( R_{\text{SL}} \) value is calculated using Equation 5. The maximum \( R_{\text{SL}} \) value is 1 k\( \Omega \)

\[
0.82 \times \left( \frac{V_{\text{LOAD}} + V_{\text{F}}}{L_{\text{M}}} \right) - V_{\text{SUPPLY}} \times R_{\text{S}} = 30 \mu \text{A} \times (2\text{k}\Omega + R_{\text{SL}}) \times F_{\text{SW}}
\]

(5)
The PWM comparator in Figure 10 compares the sum of sensed inductor current, slope compensation ramp and a 0.3-V (typical) internal COMP-to-PWM offset with the COMP pin voltage (V_{COMP}), and terminates the present cycle if the sum is greater than V_{COMP}.

### 7.3.7 Current Limit (CS Pin)

The LM5150-Q1 features cycle-by-cycle peak current limit without sub-harmonic oscillation at high duty cycle. If the sum of the sensed inductor current and the slope compensation ramp exceeds the current limit threshold at the current limit comparator input (V_{CL}), the current limit comparator immediately terminates the present cycle. To minimize the peak current limit variation due to changes in either the supply voltage or the output voltage, the device features a variable current limit threshold which is calculated using Equation 6.

\[
V_{CL} = 1.2 + 0.6 \times \frac{(V_{OUT} - V_{VIN})}{V_{OUT-REG}} \text{[V]}
\]  

Cycle-by-cycle peak inductor current limit (I_{PEAK-CL}) in steady state calculated as follows:

\[
I_{PEAK-CL} = \frac{V_{CL} - 10 \times 30 \mu A \times (2k\Omega + R_{SL}) \times F_{SW_RT} \times D}{10 \times R_S}
\]  

\[
D = 1 - \frac{V_{SUPPLY}}{V_{LOAD} + V_F}
\]

F_{SYNC} is included in the equation because the peak amplitude of the slope compensation varies with the frequency of the external synchronization clock. Substitute F_{SW_RT} for F_{SYNC} if clock synchronization is not used.

Boost converters have a natural pass-through path from the supply to the load through the high-side power diode (D1). Due to this path, boost converters cannot provide current limit protection when the output voltage is close to or less than the input supply voltage.

A small external RC filter (R_F, C_F) at the CS pin is required to overcome the leading edge spike of the current sense signal. Select an R_F value which is greater than 30 Ω and a C_F value which is greater than 1 nF. Due to the effect of the filter, the peak current limit is not valid when the on-time is less than 2 × R_F × C_F.

### 7.3.8 Feedback and Error Amplifier (COMP Pin)

The LM5150-Q1 includes internal feedback resistors which are set based on the VSET pin resistor selection. These feedback resistors are disconnected from the VOUT pin in the standby mode to minimize quiescent current. The feedback resistor divider is connected to an internal transconductance error amplifier which features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 3 MHz). The internal transconductance error amplifier sources current which is proportional to the difference between the feedback resistor divider voltage and the internal reference. The output of the error amplifier is connected to the COMP pin, allowing the use of a Type 2 loop compensation network.

R_{COMP}, C_{COMP} and optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. This compensation network creates a pole at very low frequency (F_{DP}), a mid-band zero (F_{Z_EA}) and a high frequency pole (F_{P_EA}). See Loop Compensation Component Selection and Maximum ESR for more detailed information.

### 7.3.9 Automatic Wake-Up and Standby

The LM5150-Q1 wakes up when V_{VOUT} drops below the VOUT wake-up threshold. The device goes into standby when V_{VOUT} rises above the VOUT standby threshold in EC or SS configuration or when V_{VIN} rises above the VIN standby threshold in SS configuration. The VOUT wake-up threshold is typically 3% higher than the VOUT regulation target. The STATUS output is released in 3 µs (with 50-kΩ pullup resistor to 5 V) after the wake-up event. The LO driver is enabled 6 µs after the STATUS output starts rising.
Figure 11. Automatic Wake-Up and Standby Control

In SS configuration, the VOUT standby threshold is typically 24% higher than the VOUT regulation target. The VIN standby threshold is typically 1 V higher than the VOUT wake-up threshold in SS configuration. To prevent chatter, the forward voltage drop of diode D1 must be less than 0.95 V. See Figure 15.

Figure 12. Automatic Wake-Up and Standby Operation in the SS Configuration (With Fast V\text{SUPPLY} Fall and Slow Switching)
In EC configuration, the VOUT standby threshold is typically 6% higher than the VOUT regulation target. Because of the minimum duty cycle limit (see Emergency-Call Configuration (EC Configuration)), the LM5150-Q1 alternates between the wake-up and the low I_Q standby modes at medium or light load. See Figure 16.

To minimize output undershoot when waking up, the LM5150-Q1 boosts the VOUT regulation target during the first 128 cycles after the wake-up event. The regulation target becomes 3% higher than the original regulation target for 64 cycles, 2% higher for the next 32 cycles and 1% higher for the final 32 cycles. The VOUT pin voltage may rise up above the VOUT standby threshold even if switching stops at the VOUT standby threshold because the energy stored in the inductor transfers to the output capacitor when switching stops. See Device Functional Modes for more information about the automatic wake-up and standby operation.
7.3.10 Boost Status Indicator (STATUS Pin)

STATUS is an open-drain output and requires a pullup resistor between 5 kΩ and 100 kΩ. The pin is pulled up after \( V_{VOUT} \) falls below the VOUT wake-up threshold, and is toggled to a low logic state when \( V_{VIN} \) rises above the VIN standby threshold in SS configuration or when \( V_{VOUT} \) rises above the VOUT status off-threshold in EC configuration. The pin is also pulled to ground when \( EN < 1 \) V and VOUT is greater than about 2 V, when AVCC < VCC-UVLO-FALLING or during thermal shutdown.

7.3.11 Maximum Duty Cycle Limit, Minimum Input Supply Voltage

When designing a boost converter, the maximum duty cycle should be reviewed at the minimum supply voltage. The minimum input supply voltage which can achieve the target output voltage is estimated from Equation 9.

\[
V_{SUPPLY(MIN)} \approx (V_{VOUT-REG} + V_F) \times (1 - D_{MAX}) \times \frac{F_{SYNC}}{F_{SW_RT}} + I_{SUPPLY(MAX)} \times R_{DCR} + I_{SUPPLY(MAX)} \times (R_{DS(ON)} + R_S) \times D_{MAX}
\]

(9)

\( I_{SUPPLY(MAX)} \) is the maximum input current. \( R_{DCR} \) is the DC resistance of the inductor. \( R_{DS(ON)} \) is the on-resistance of the MOSFET. Substitute \( F_{SW_RT} \) for \( F_{SYNC} \) if the clock synchronization is not used. The minimum input supply voltage can be decreased by supplying \( F_{SYNC} \) which is less than \( F_{SW} \).

This maximum duty cycle limit (\( D_{MAX} \)) is 87% (typical), but may fall down below 80% if the external synchronization clock frequency is higher than 0.85 \( \times \) \( F_{SW (TYPICAL)} \). Select an \( F_{SYNC} \) which is within –25% and –15% of the \( F_{SW (TYPICAL)} \) if 1:5 step-up ratio is required with clock synchronization. The minimum input supply voltage can be further decreased by supplying a lower frequency external synchronization clock. See Clock Synchronization (SYNC Pin in SS Configuration) for more information.

7.3.12 MOSFET Driver (LO Pin)

The LM5150-Q1 provides an N-channel MOSFET driver which can source or sink a peak current of 1.5 A. The driver is powered by the 5-V VCC regulator and is enabled when the EN pin voltage is greater than 2 V and the AVCC pin voltage is greater than the AVCC UVLO threshold.

7.3.13 Thermal Shutdown

Internal thermal shutdown is provided to protect the LM5150-Q1 if the junction temperature exceeds 175°C (typical). When thermal shutdown is activated, the device is forced into a low power thermal shutdown state with the MOSFET driver and the VCC regulator disabled. After the junction temperature is reduced (typical hysteresis is 15°C), the device is re-enabled.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

If the EN pin voltage is below 1 V, the LM5150-Q1 is in shutdown mode with all functions disabled except EN. In shutdown mode, the device reduces the VOUT pin current consumption to below 5.25 µA (typical) and the STATUS pin is pulled to ground. The device can be enabled by raising the EN pin above 2 V and operates in either the standby mode or the wake-up mode if \( AVCC \) is greater than the AVCC UVLO threshold.

<table>
<thead>
<tr>
<th>STATUS</th>
<th>SYNC</th>
<th>RT</th>
<th>COMP</th>
<th>EN</th>
<th>VOUT</th>
<th>PVCC/AVCC</th>
<th>LO</th>
<th>CS</th>
<th>VIN</th>
<th>VSET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grounded</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Enabled</td>
<td>I₂ ≤ 5 µA</td>
<td>Disabled</td>
<td>Grounded</td>
<td>Disabled</td>
<td>I₂ = 0.1 µA</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

7.4.2 Standby Mode

If VOUT is greater than the VOUT standby threshold or VIN is greater than the VIN standby threshold in the SS mode, the LM5150-Q1 enters into standby mode.

In standby mode, most functions are disabled, including the thermal shutdown, to minimize the current consumption. The VOUT wake-up monitor is enabled in standby mode to allow wake-up if the VOUT voltage drops below the VOUT wake-up threshold. The VCC regulator reduces the sourcing capability to 17 mA in standby mode and the AVCC UVLO comparator is disabled.

The VOUT standby threshold fulfills effectively the overvoltage protection (OVP) function.
Table 3. State of Each Pin in Standby Mode

<table>
<thead>
<tr>
<th>STATUS</th>
<th>SYNC</th>
<th>RT</th>
<th>COMP</th>
<th>EN</th>
<th>VOUT</th>
<th>PVCC/AVCC</th>
<th>LO</th>
<th>CS</th>
<th>VIN</th>
<th>VSET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Released or Grounded</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Enabled</td>
<td>I\textsubscript{O} ≤ 15 µA, VOUT wake-up monitor enabled</td>
<td>Enabled P\textsubscript{VCC} capability = 17 mA</td>
<td>Grounded</td>
<td>Disabled</td>
<td>I\textsubscript{O} = 0.1 µA</td>
<td>Disabled</td>
</tr>
</tbody>
</table>

7.4.3 Wake-Up Mode

The LM5150-Q1 wakes up from standby mode if VOUT drops below the VOUT wake-up threshold. There are two configurations when the device wakes up. One is start-stop configuration (SS configuration) and the other is emergency-call configuration (EC configuration). The configuration is selectable by the VSET resistor (see Table 1).

7.4.3.1 Start-Stop Configuration (SS Configuration)

![Figure 15. Typical Start-Stop Application](image)

The LM5150-Q1 runs at fixed switching frequency without any pulse skipping in SS configuration. The device turns on the LO driver every cycle with \( T_{ON-MIN} \) until entering into standby mode, which helps to prevent EMI spectrum shifts. Because the MOSFET turns on every cycle, the boost converter output may be above the regulation target if the required on-time is less than the \( T_{ON-MIN} \) when the boost supply voltage is close to the VOUT regulation target or the load current is very small. The output voltage will rise above the VOUT regulation target if one of the inequalities below is true.

\[
D \times \frac{1}{F_{SW}} < T_{ON-MIN} 
\]

\[
\left( \frac{V_{SUPPLY} \times T_{ON-MIN}}{2 \times L_M} \right)^2 \times \frac{F_{SW}}{(V_{LOAD} + V_F - V_{SUPPLY})} > I_{LOAD} 
\]

Figure 15. Typical Start-Stop Application

In SS configuration, the LM5150-Q1 enters into the standby mode if VOUT is greater than the VOUT standby threshold—which is 24% higher than the VOUT regulation target—or if VIN is greater than the VIN standby threshold.
7.4.3.2 Emergency-Call Configuration (EC Configuration)

The EC configuration achieves high efficiency at light/medium load by alternating between the wake-up and the low I\textsubscript{Q} standby modes. In EC configuration, the LM5150-Q1 limits the minimum duty cycle programmed by V\textsubscript{VOUT} and V\textsubscript{VIN}. The minimum duty cycle limit is calculated using Equation 12.

\[
D_{\text{MIN}} = 0.75 \times \left(1 - \frac{V_{\text{VIN}}}{V_{\text{VOUT-REG}}}\right)
\]

Due to this minimum duty cycle limit, the boost converter sources more current than required when the load current is relatively small. As a result, the output voltage increases and eventually crosses the VOUT standby threshold which is typically 6\% higher than the VOUT regulation target. The LM5150-Q1 then goes into the low I\textsubscript{Q} standby mode. The LM5150-Q1 wakes up when VOUT drops below the VOUT wake-up threshold which is typically 3\% higher than the VOUT regulation target. The device alternates between these two modes when the inequality below is true.

\[
\left(\frac{V_{\text{SUPPLY}} \times D_{\text{MIN}}}{F_{\text{SW}}}\right)^2 \times \frac{F_{\text{SW}}}{2 \times L_{\text{M}}(V_{\text{LOAD}} + V_{\text{F}} - V_{\text{SUPPLY}})} > I_{\text{LOAD}}
\]

Assuming \(V_{\text{LOAD}} = V_{\text{VOUT}} = V_{\text{VOUT-REG}}\) and \(V_{\text{SUPPLY}} = V_{\text{VIN}}\), the skip cycle operation starts when the inequality below is true.

\[
\left(\frac{V_{\text{SUPPLY}} \times 0.75}{2 \times L_{\text{M}} \times F_{\text{SW}}(V_{\text{LOAD}} + V_{\text{F}} - V_{\text{SUPPLY}})}\right)^2 > I_{\text{LOAD}}
\]

In EC configuration, the LM5150-Q1 doesn’t generate any pulse if \(V_{\text{COMP}}\) is less than the 0.3 V and the required minimum duty cycle limit is zero.

If the peak current limit is triggered before reaching the minimum duty cycle, the device terminates the LO driver output immediately.
If VOUT is greater than the VOUT status-off threshold (typically 12% higher than the VOUT regulation target), the LM5150-Q1 pulls the STATUS pin low.

In EC configuration, light load efficiency is proportional with the inductor current ripple ratio.

### Table 4: State of Each Pin in Wake-Up Mode

<table>
<thead>
<tr>
<th>STATUS</th>
<th>SYNC</th>
<th>RT</th>
<th>COMP</th>
<th>EN</th>
<th>VOUT</th>
<th>PVCC/AVCC</th>
<th>LO</th>
<th>CS</th>
<th>VIN</th>
<th>VSET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Release</td>
<td>Enabled in SS configuration</td>
<td>Enabled</td>
<td>Enabled</td>
<td>Enabled</td>
<td>Released by VOUT wake-up</td>
<td>Enabled</td>
<td>Released by VOUT wake-up</td>
<td>Pull down by VIN standby</td>
<td>Disabled</td>
<td></td>
</tr>
</tbody>
</table>

### Table 5: Start-Stop vs Emergency-Call Configuration

<table>
<thead>
<tr>
<th>CONFIGURATION</th>
<th>START-STOP</th>
<th>EMERGENCY-CALL</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT regulation options</td>
<td>6.8 V, 7.5 V, 8.5 V, 10.5 V</td>
<td></td>
</tr>
<tr>
<td>VSET resistor value [Ω]</td>
<td>29.4k, 19.1k, 9.53k, GND</td>
<td>90.9k, 71.5k, 54.9k, 41.2k</td>
</tr>
<tr>
<td>Clock Synchronization</td>
<td>Yes</td>
<td>No, SYNC should be grounded</td>
</tr>
<tr>
<td>VOUT wake-up threshold [V]</td>
<td>( V_{\text{VOUT-REG}} \times 1.03 )</td>
<td>( V_{\text{VOUT-REG}} \times 1.06 )</td>
</tr>
<tr>
<td>VOUT standby threshold [V]</td>
<td>( V_{\text{VOUT-REG}} \times 1.24 )</td>
<td>( V_{\text{VOUT-REG}} \times 1.12 )</td>
</tr>
<tr>
<td>VOUT status-off threshold [V]</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>VIN standby threshold [V]</td>
<td>( V_{\text{VOUT-REG}} \times 1.03 + 1.0 ) V</td>
<td>N/A</td>
</tr>
<tr>
<td>STATUS pin control (Open-drain with pullup resistor)</td>
<td>Released by VOUT wake-up</td>
<td>Released by VOUT wake-up</td>
</tr>
<tr>
<td></td>
<td>Pulled down by VIN standby</td>
<td>Pulled down by VOUT status-off</td>
</tr>
<tr>
<td>At heavy load when ( V_{\text{VIN}} = V_{\text{VOUT}} )</td>
<td>Pulse width modulation (PWM)</td>
<td></td>
</tr>
<tr>
<td>At light/no load when ( V_{\text{VIN}} = V_{\text{VOUT}} )</td>
<td>LO turns on at every cycle in wake-up configuration. Skip cycle operation by alternating between wake-up and standby configurations.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Minimum on-time is limited</td>
<td>Minimum duty cycle is limited</td>
</tr>
<tr>
<td>When ( V_{\text{VIN}} = V_{\text{VOUT}} ) or ( V_{\text{VIN}} \geq V_{\text{VOUT}} )</td>
<td>LO turns on at every cycle in wake-up configuration. On-time is limited by ( T_{\text{ON-MIN}} ). ( V_{\text{OUT}} ) goes out of regulation.</td>
<td>Duty cycle can drop to 0%. No pulses if ( V_{\text{COMP}} &lt; 0.3 ) V and ( D_{\text{MIN}} \leq 0% )</td>
</tr>
<tr>
<td>Maximum duty-cycle limit</td>
<td>Typically 87%</td>
<td></td>
</tr>
</tbody>
</table>
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5150-Q1 is a non-synchronous boost controller. The following design procedure can be used to select the external components for the LM5150-Q1. Alternately, the WEBENCH® software may be used to generate complete designs. The WEBENCH software uses an iterative design procedure and accesses comprehensive data bases of components when generating a design. This section presents a simplified discussion of the design process.

8.1.1 Bypass Switch / Disconnection Switch Control

The STATUS pin can be used to control an external bypass switch, which turns on when the boost is in standby mode, or to control an external disconnection switch that turns off when the boost is in standby mode. In Figure 17, a P-channel MOSFET is used to connect the boost supply input to the load directly when the boost is in standby mode. This bypass switch can be turned on slowly, but it must be turned off fast after the STATUS pin is pulled up by the wake-up event. The STATUS pin is rated to the absolute maximum 65 V.

![Figure 17. Bypass Switch Control Example](image)

In Figure 18, a P-channel MOSFET is used to disconnect the boost supply output from the battery when boost is not required. This disconnection switch can be turned off slowly, but it must be turned on fast after the STATUS pin is pulled up by the wake-up event.
8.1.2 Loop Response

The open-loop transfer function of a boost regulator is defined as the product of modulator transfer function and feedback transfer function.

The modulator transfer function of a current mode boost regulator including a power stage with an embedded current loop can be simplified as a one load pole ($F_{LP}$), one ESR zero ($F_{Z_{ESR}}$), and one Right Half Plane (RHP) zero ($F_{RHP}$) system, which can be explained as follows.

Modulator transfer function is defined as follows:

\[
\frac{\dot{V}_{LOAD}(s)}{V_{COMP}(s)} = A_M \times \left( 1+ \frac{s}{2\pi F_{Z_{ESR}}} \right) \times \left( 1- \frac{s}{2\pi F_{RHP}} \right) \left( 1+ \frac{s}{2\pi F_{LP}} \right)
\]

where

- $A_M = \frac{R_{LOAD}}{R_S \times 10} \times \frac{D'}{2}$
- $F_{LP} = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}}$ [Hz]
- $F_{Z_{ESR}} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}}$ [Hz]
- $F_{RHP} = \frac{R_{LOAD} \times (D')}{2\pi \times L_M}$ [Hz]

(15)

$R_{ESR}$ is the equivalent series resistance (ESR) of the output capacitor which is specified in the capacitor datasheet.

$R_{COMP}$, $C_{COMP}$ and $C_{HF}$ (see Figure 19) configure the error amplifier gain and phase characteristics to produce a stable voltage loop with fast response. This compensation network creates a dominant pole at low frequency ($F_{DP_{EA}}$), a mid-band zero ($F_{Z_{EA}}$), and a high frequency pole ($F_{P_{EA}}$).
Application Information (continued)

The feedback transfer function is defined as follows:

\[
\frac{\hat{V}_{\text{COMP}(s)}}{\hat{V}_{\text{LOAD}(s)}} = A_{FB} \times \frac{s}{2\pi F_{Z,EA}} \times \frac{s}{2\pi F_{Z,EA} \times s + 1} \times \frac{1}{2\pi F_{P,EA} \times s + 1} \times \frac{1}{2\pi R_{O} \times s + 1} \times \frac{1}{2\pi R_{COMP} \times s + 1} \times \frac{1}{2\pi R_{COMP} \times s + 1} \times \frac{1}{2\pi R_{COMP} \times s + 1}
\]

where

\[
A_{FB} = \frac{1.2}{V_{\text{LOAD}}} \times R_{O} \times G_{m}
\]

\[
F_{D,P,EA} = \frac{1}{2\pi R_{O} \times C_{\text{COMP}}} \quad \text{[Hz]}
\]

\[
F_{Z,EA} = \frac{1}{2\pi R_{COMP} \times C_{\text{COMP}}} \quad \text{[Hz]}
\]

\[
F_{P,EA} = \frac{1}{2\pi R_{COMP} \times \frac{C_{\text{COMP}} \times C_{HF}}{C_{COMP} + C_{HF}}} \approx \frac{1}{2\pi R_{COMP} \times C_{HF}} \quad \text{[Hz]}
\]

\[
R_{O} \approx 10 \text{ M}\Omega\) is the output resistance of the error amplifier and \(G_{m} \approx 2 \text{ mA/V}\) is the transconductance of the error amplifier.

Assuming \(F_{L,LP}\) is canceled by \(F_{Z,EA}\), \(F_{R,HP}\) is much higher than crossover frequency \((F_{\text{CROSS}})\), and \(F_{Z,ESR}\) is either canceled by \(F_{P,EA}\) or \(F_{Z,ESR}\) is much higher than \(F_{\text{CROSS}}\), the open-loop transfer function can be simplified as follows:

\[
T(s) = A_{M} \times A_{FB} \times \frac{1}{1 + \frac{s}{2\pi F_{D,P,EA}}}
\]

Because \(|T(s)| = 1\) at the crossover frequency, the crossover frequency can be simply estimated using those assumptions.

\[
F_{\text{CROSS}} \approx \sqrt{\frac{A_{M} \times A_{FB}^2 - 1}{2\pi R_{O} \times C_{\text{COMP}}} \quad \text{[Hz]}}
\]
8.2 Typical Application

The LM5150-Q1 requires a minimum number of external components to work. Figure 19 includes all optional components as an example.

Figure 19. Typical Circuit With Optional Components

8.2.1 Design Requirements

Table 6 lists the design parameters for Figure 19.

Table 6. Design Example Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Target Application</td>
<td>Start-stop</td>
</tr>
<tr>
<td>Minimum Input Supply Voltage (V_SUPPLY_MIN)</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Target Output Voltage (V_LOAD)</td>
<td>8.5 V</td>
</tr>
<tr>
<td>Maximum Load Current (I_LOAD)</td>
<td>2.94 A (≈ 25 Watt)</td>
</tr>
<tr>
<td>Switching Frequency (F_SW)</td>
<td>440 kHz</td>
</tr>
<tr>
<td>D1 Diode Forward Voltage Drop</td>
<td>0.7 V</td>
</tr>
<tr>
<td>Maximum Inductor Current Ripple Ratio (RR)</td>
<td>0.6 (≈ 60%)</td>
</tr>
<tr>
<td>Estimated Full Load Efficiency (Eff)</td>
<td>0.8 (≈ 80%)</td>
</tr>
<tr>
<td>Current Limit Margin (M_CL)</td>
<td>1.2 (≈ 120%)</td>
</tr>
<tr>
<td>F_LP over F_CROSS (K1)</td>
<td>0.15 (F_LP = 0.15 × F_CROSS)</td>
</tr>
<tr>
<td>F_Z,EA over F_LP (K2)</td>
<td>3 (F_Z,EA = 3 × F_LP)</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5150-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V\_IN), output voltage (V\_OUT), and output current (I\_OUT) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.
The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

### 8.2.2.2 $R_{\text{SET}}$ Resistor

Select the value of $R_{\text{SET}}$, referring to Table 1. 9.53 kΩ is chosen to target 8.5 V in SS configuration. In general, about 5% to approximately 10% output undershoot should be considered when selecting the VOUT regulation target.

### 8.2.2.3 $R_T$ Resistor

The value of $R_T$ for 440-kHz switching frequency is calculated as follows:

\[
R_T = \frac{2.233 \times 10^4}{440 \times 619} = 50.1 \, \text{kΩ}
\]

(19)

An standard value of 49.9 kΩ is chosen for RT.

In general, higher frequency boost converters are smaller and faster, but they also have higher switching losses and lower efficiency.

### 8.2.2.4 Inductor Selection ($L_M$)

When selecting the inductor, consider three key parameters: inductor current ripple ratio (RR), falling slope of the inductor current, and RHP zero frequency ($F_{\text{RHP}}$).

Inductor current ripple ratio is selected to have a balance between core loss and copper loss. The falling slope of the inductor current must be low enough to prevent sub-harmonic oscillation at high duty cycle (additional $R_{\text{SL}}$ resistor is required if not). Higher $F_{\text{RHP}}$ (= lower inductance) allows a higher crossover frequency and is always preferred when using a smaller value output capacitor.

The inductance value can be selected to set the inductor current ripple between 30% and 70% of the average inductor current as a good compromise between RR, $F_{\text{RHP}}$ and inductor falling slope. In this example, 60% ripple ratio (RR = 0.6) is selected as the maximum inductor current ripple ratio (the inductor current ripple ratio is the biggest when $D = 0.33$). The target inductance value is calculated as follows:

\[
L_{M(\text{TARGET})} = \frac{0.14 \times R_{\text{LOAD}}}{RR \times F_{\text{SW}}} = \frac{0.14 \times 8.5}{0.6 \times 440 \text{kΩ}} = 1.53 \, \mu\text{H}
\]

(20)

\[
L_{M(\text{GUIDE})} = \frac{\left( V_{\text{LOAD}} - V_{\text{SUPPLY(MIN)}} \right) \times V_{\text{SUPPLY(MIN)}}}{F_{\text{SW}} \times V_{\text{LOAD}} \times I_{\text{LOAD}}} = \frac{(8.5 - 2.5) \times 2.5}{440 \text{kΩ} \times 8.5 \times 2.94} = 1.36 \, \mu\text{H}
\]

(21)

If the target inductance is smaller than the value calculated using Equation 21, consider adding the slope compensation resistor ($R_{\text{SL}}$), as mentioned in the Slope Compensation Ramp ($R_{\text{SL}}$) section, or select a smaller RR and recalculate the inductance using Equation 20.

A standard value of 1.5 µH is chosen for $L_M$. The required inductor saturation current rating is estimated after selecting $R_S$ and $R_{\text{SL}}$.

### 8.2.2.5 Current Sense ($R_S$)

Based on the assumptions that 20% of current limit margin ($M_{\text{CL}} = 1.2$), 80% estimated efficiency ($\text{Eff} = 0.8$) at full load and no $R_{\text{SL}}$ populated, $R_S$ is calculated using Equation 22 and Equation 23.
\[ R_S = \frac{1.2 + 0.6 \times (V_{OUT} - V_{VIN})}{V_{OUT-REG}} - 10 \times 30 \mu A \times (2k \Omega + R_{SL}) \times \frac{F_{SW_RT}}{F_{SYNC}} \times D \]
\[ 10 \times \frac{V_{LOAD} \times I_{LOAD}}{V_{SUPPLY(MIN)} \times \text{Eff}} + \frac{1}{2} \times \frac{V_{SUPPLY(MIN)} \times D \times \frac{1}{L_M}}{F_{SYNC}} \times M_{CL} \]
\[ R_S = \frac{1.2 + 0.6 \times (8.5 - 2.5)}{8.5} - 10 \times 30 \mu \times (2k + 0) \times 1 \times \left(1 - \frac{2.5}{8.5 + 0.7}\right) \]
\[ 2.5 \times \frac{1}{1.5u} \times \frac{440k}{7m \times 1.2} = 7.12m[\Omega] \]

Substitute \( F_{SW_RT} \) for \( F_{SYNC} \) if the clock synchronization is not used.

A standard value of 7 mΩ is chosen for \( R_S \). A low-ESL resistor is recommended to minimize the error caused by the ESL.

### 8.2.2.6 Slope Compensation Ramp (\( R_{SL} \))

The minimum inductance value which can prevent sub-harmonic oscillation without \( R_{SL} \) is calculated using Equation 24. If the selected inductance value is less than the minimum inductance calculated using Equation 24, add a slope compensation resistor (\( R_{SL} \)) externally.

\[ L_{M(MIN)} = 0.5 \times \frac{V_{LOAD} + V_F - V_{SUPPLY(MIN)}}{60m \times F_{SW}} \times R_S \times \text{Margin} = 0.5 \times \frac{(8.5 + 0.7) - 2.5}{60m \times 440k} \times 7m \times 1.2 = 1.07[\mu H] \]

1.2 is the recommended margin to cover non-ideal factors.

If needed, use Equation 25 to find the \( R_{SL} \) value which matches the typical amount of slope compensation.

\[ R_{SL} = 0.82 \times \frac{V_{LOAD} + V_F - V_{SUPPLY(MIN)}}{L_M \times F_{SW} \times 30 \mu A} \times R_S - 2k[\Omega] \]

In this example, \( R_{SL} \) is not populated because the selected inductance value, 1.5 µH, is greater than the minimum required inductance from Equation 24.

After selecting \( R_S \) and \( R_{SL} \), the peak inductor current at current limit (\( I_{PEAK-CL} \)) can be calculated. Setting the inductor saturation current rating higher than the \( I_{PEAK-CL} \) is recommended.

\[ I_{PEAK-CL} = \frac{V_{CL} - 10 \times 30 \mu A \times (2k \Omega + R_{SL}) \times \frac{F_{SW_RT}}{F_{SYNC}} \times D}{10 \times R_S} + \frac{V_{SUPPLY(MIN)}}{L_M} \times T_D[A] \]
\[ 1.2 + 0.6 \times \frac{(8.5 - 2.5)}{8.5} - 10 \times 30 \mu \times 2k \times 1 \times \left(1 - \frac{2.5}{8.5 + 0.7}\right) \times \frac{2.5}{1.5u} \times 20n = 16.9[A] \]

\( T_D \) is the typical propagation delay of current limit.

### 8.2.2.7 Output Capacitor (\( C_{OUT} \))

There are a few ways to select the proper value of output capacitor (\( C_{OUT} \)). The output capacitor value can be selected based on output voltage ripple, output overshoot or undershoot due to load transient. In this example, \( C_{OUT} \) is selected based on output undershoot because the waking up performance is similar with no-load to full-load transient performance.

The output undershoot becomes smaller by increasing \( F_{CROSS} \) or by decreasing \( F_{LP} \): a smaller \( C_{OUT} \) is allowed by increasing \( F_{CROSS} \) or by decreasing \( F_{LP} \).
To increase \( F_{\text{CROSS}} \), \( F_{\text{SW}} \) and \( F_{\text{RHP}} \) must be increased because the maximum \( F_{\text{CROSS}} \) is, in general, limited at 1/10 of \( F_{\text{RHP}} \) at \( V_{\text{SUPPLY(MIN)}} \) or 1/10 of \( F_{\text{SW}} \) whichever is lower.

\( F_{\text{RHP}} \) is calculated using Equation 28.

\[
F_{\text{RHP}} = \frac{R_{\text{LOAD}} \times \left( \frac{V_{\text{SUPPLY(MIN)}}}{V_{\text{LOAD}} + V_F} \right)^2}{2\pi \times L_M} = \frac{8.5 \times \left( \frac{2.5}{8.5 + 0.7} \right)^2}{2\pi \times 1.5\mu} = 22.6\text{kHz}
\]

(28)

\( F_{\text{CROSS}} \) is selected at 1/10 of \( F_{\text{RHP}} \) or 1/10 of \( F_{\text{SW}} \) whichever is lower.

\[
\frac{F_{\text{RHP}}}{10} = 2.27\text{kHz}
\]

(29)

\[
\frac{F_{\text{SW}}}{10} = 440\text{k} = 44\text{kHz}
\]

(30)

In this example, 2.27 kHz is selected as a target \( F_{\text{CROSS}} \) and \( F_{\text{LP}} \) is selected to be 340 Hz (\( K1 = 0.15 \)).

In general, there is about 5% or less undershoot with \( F_{\text{LP}} = 0.1 \times F_{\text{CROSS}} \) (\( K1 = 0.1 \)) and 10% or less undershoot with \( F_{\text{LP}} = 0.2 \times F_{\text{CROSS}} \) (\( K1 = 0.2 \)) during 0% to 100% load transient. The recommended \( K1 \) factor range is from 0.02 to 0.2.

\( F_{\text{LP}} \) is calculated using Equation 31.

\[
F_{\text{LP}} = \frac{2}{2\pi \times R_{\text{LOAD}} \times C_{\text{OUT}}}\text{[Hz]}
\]

(31)

The minimum required output capacitance value is calculated using Equation 32.

\[
C_{\text{OUT}} = \frac{2}{2\pi \times R_{\text{LOAD}} \times F_{\text{LP}}} = \frac{2}{2\pi \times \frac{8.5}{2.94} \times 340} = 324\mu\text{F}
\]

(32)

The maximum output ripple current is calculated at the minimum input supply voltage as follows:

\[
I_{\text{RIPPLE,COUT(MAX)}} = \frac{V_{\text{LOAD}} \times I_{\text{LOAD}}}{2 \times V_{\text{SUPPLY(MIN)}}} = \frac{8.5 \times 2.94}{2 \times 2.5} = 5\text{[A]}
\]

(33)

The ripple current rating of the output capacitors must be enough to handle the output ripple current. By using multiple output capacitors, the ripple current can be split. In practice, ceramic capacitors are placed closer to the diode and the MOSFET than the bulk aluminum capacitors in order to absorb the majority of the ripple current.

In this example, three 100-\( \mu \)F capacitors are placed in parallel to ensure ripple current capability. If high-ESR capacitors are used for the output capacitor, additional 10-\( \mu \)F ceramic capacitors can be placed close to the switching components to minimize switching noise.

### 8.2.2.8 Loop Compensation Component Selection and Maximum ESR

Based on Equation 18, \( C_{\text{COMP}} \) is calculated as follows:

\[
C_{\text{COMP(over damping)}} = \sqrt{\left( A \times A_F \right)^2 - 1}\left( \frac{R_{\text{LOAD}}}{R_S \times 10} \times D' \times \frac{1.2}{V_{\text{LOAD}}} \times R_O \times G_m \right)^2 - 1
\]

\[
= \sqrt{\left( \frac{8.5}{2.94} \times \frac{2.5}{8.5 + 0.7} \times \frac{1.2}{8.5} \times 10 \times 2 \right)^2} - 1
\]

(34)

\[
C_{\text{COMP(over damping)}} = \sqrt{\left( \frac{8.5}{2 \times 10 \times 2.27} \right)^2} = 111\text{nF}
\]

(35)
By selecting $C_{\text{COMP}}$ following Equation 34, the typical phase margin is set to 90° and the loop response is overdamped. In this example, $F_{Z\_EA}$ is placed at 3 times higher frequency than $F_{LP}$ to have lower phase margin but faster settling time ($K2 = 3$, target $F_{Z\_EA}$ is 1.02 kHz). Recommended range of $F_{Z\_EA}$ is from $1 \times F_{LP}$ to $4 \times F_{LP}$ ($1 \leq K2 \leq 4$). Practical crossover frequency will vary with $K2$ with a range of $0.5 \times F_{CROSS}$ to $1.0 \times F_{CROSS}$.

\[
C_{\text{COMP}} = \frac{C_{\text{COMP(over damping)}}}{K2} = \frac{111 \text{nF}}{3} = 37 \text{nF}
\]

(36)

A standard value of 33 nF is chosen for $C_{\text{COMP}}$.

$R_{\text{COMP}}$ is selected to set the error amplifier zero at 1.02 kHz.

\[
R_{\text{COMP}} = \frac{1}{2\pi\times C_{\text{COMP}} \times F_{Z\_EA}} = \frac{1}{2\pi\times 33 \text{nF} \times 1.02 \text{kHz}} = 4.73 \text{k}\Omega
\]

(37)

A standard value of 4.64 kΩ is chosen for $R_{\text{COMP}}$.

$C_{HF}$ is usually used to create a pole at high frequency ($F_{P\_EA}$) to cancel $F_{Z\_ESR}$. By using a small ESR capacitor which can place $F_{Z\_ESR}$ greater than $10 \times F_{CROSS}$, the output capacitor ESR would not affect the loop stability. The maximum ESR which does not affect the loop response is calculated using Equation 38.

\[
R_{\text{ESR(MAX)}} = \frac{1}{2\pi\times C_{\text{COMP}} \times F_{CROSS} \times 10} = \frac{1}{2\pi\times 330 \text{uF} \times 2.27 \text{kHz}} = 23 \text{m}\Omega
\]

(38)

### 8.2.2.9 PVCC Capacitor, AVCC Capacitor, and AVCC Resistor

The PVCC capacitor supplies the peak transient current to the LO driver. The value of PVCC capacitor ($C_{PVCC}$) must be 4.7 μF or higher and must be a high-quality, low-ESR, ceramic capacitor. $C_{PVCC}$ must be placed close to the PVCC pin and the PGND pin. A value of 4.7 μF is selected for this design example. The AVCC capacitor must be placed close to the device. The recommended AVCC capacitor value is 0.1 μF. The AVCC resistor should be placed between PVCC and AVCC pins. The recommended AVCC resistor value is 10 Ω.

### 8.2.2.10 VOUT Filter ($C_{\text{VOUT}}, R_{\text{VOUT}}$)

The VOUT pin is the input of the internal VCC regulator and also is the input of the output voltage sensing. To minimize noise at the VOUT pin, a 1-μF capacitor must be placed at the VOUT pin in most cases. If multiple output capacitors are used, one of them can be placed at the VOUT pin as $C_{\text{VOUT}}$. The VOUT capacitor must be a high-quality, low-ESR, ceramic capacitor and must be placed close to the device. A resistor can be added at the VOUT pin ($R_{\text{VOUT}}$) to form a RC filter (see Figure 19). In this case, the maximum resistor value should be less than or equal to 2 Ω.

### 8.2.2.11 Input Capacitor

The input capacitors reduce the input voltage ripple. Assuming high-quality ceramic capacitors are used for the input capacitors, the maximum input voltage ripple can be calculated by using Equation 39.

\[
V_{\text{ripply(CIN)}} = \frac{V_{\text{LOAD}}}{32\times L_{M} \times C_{\text{IN}} \times F_{SW}^2} [\text{V}]
\]

(39)

The required input capacitor value is a function of the impedance of the source power supply. More input capacitors are required if the impedance of the source power supply is not low enough. In the example, three 10-μF ceramic capacitors are used.

### 8.2.2.12 MOSFET Selection

The MOSFET gate driver of the LM5150-Q1 is powered by the internal 5-V VCC regulator. The MOSFET driven by the LM5150-Q1 must have a logic-level gate threshold with its on-resistance specified at 4.5 V or lower and must be rated to handle the maximum output voltage plus any switch node ringing. The maximum gate charge is limited by the 75-mA PVCC sourcing current limit, and is calculated as follows:

\[
Q_{G1(@5V)} < \frac{75\text{mC}}{F_{SW}} [\text{C}]
\]

(40)

A leadless package is preferred for high switching-frequency designs. The MOSFET gate capacitance should be small enough so that the gate voltage is fully discharged during the off-time.
8.2.2.13 Diode Selection

A Schottky is the preferred type for D1 diode due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus any switching node ringing. Also, it must be able to handle the average output current. To prevent chatter between wake-up and standby, the forward voltage drop of the D1 diode must be less than 0.95 V at full load.

8.2.2.14 Efficiency Estimation

The total loss of the boost converter ($P_{\text{TOTAL}}$) can be expressed as the sum of the losses in the LM5150-Q1 ($P_{\text{IC}}$), MOSFET power losses ($P_{\text{Q}}$), diode power losses ($P_{\text{D}}$), inductor power losses ($P_{\text{L}}$), and the loss in the sense resistor ($P_{\text{RS}}$).

$$P_{\text{TOTAL}} = P_{\text{IC}} + P_{\text{Q}} + P_{\text{D}} + P_{\text{L}} + P_{\text{RS}} [\text{W}]$$

(41)

$P_{\text{IC}}$ can be separated into gate driving loss ($P_{\text{G}}$) and the losses caused by quiescent current ($P_{\text{IQ}}$).

$$P_{\text{IC}} = P_{\text{G}} + P_{\text{IQ}} [\text{W}]$$

(42)

Each power loss is approximately calculated as follows:

$$P_{\text{G}} = Q_{\text{G(@5V)}} \times V_{\text{OUT}} \times F_{\text{SW}} [\text{W}]$$

(43)

$$P_{\text{IQ}} = V_{\text{OUT}} \times I_{\text{OUT}} + V_{\text{IN}} \times I_{\text{VIN}} [\text{W}]$$

(44)

$I_{\text{VIN}}$ and $I_{\text{VOUT}}$ values in each mode can be found in the supply current section of the Electrical Characteristics table.

$P_{\text{Q}}$ can be separated into switching loss ($P_{\text{Q(SW)}}$) and conduction loss ($P_{\text{Q(COND)}}$).

$$P_{\text{Q}} = P_{\text{Q(SW)}} + P_{\text{Q(COND)}} [\text{W}]$$

(45)

Each power loss is approximately calculated as follows:

$$P_{\text{Q(SW)}} = 0.5 \times (V_{\text{VOUT}} + V_{\text{F}}) \times I_{\text{SUPPLY}} \times (t_{\text{R}} + t_{\text{F}}) \times F_{\text{SW}} [\text{W}]$$

(46)

$t_{\text{R}}$ and $t_{\text{F}}$ are the rise and fall times of the low-side N-channel MOSFET device. $I_{\text{SUPPLY}}$ is the input supply current of the boost converter.

$$P_{\text{Q(COND)}} = D \times I_{\text{SUPPLY}}^2 \times R_{\text{DS(ON)}} [\text{W}]$$

(47)

$R_{\text{DS(ON)}}$ is the on-resistance of the MOSFET and is specified in the MOSFET data sheet. Consider the $R_{\text{DS(ON)}}$ increase due to self-heating.

$P_{\text{D}}$ can be separated into diode conduction loss ($P_{\text{VF}}$) and reverse recovery loss ($P_{\text{RR}}$).

$$P_{\text{D}} = P_{\text{VF}} + P_{\text{RR}} [\text{W}]$$

(48)

Each power loss is approximately calculated as follows:

$$P_{\text{VF}} = (1 - D) \times V_{\text{F}} \times I_{\text{SUPPLY}} [\text{W}]$$

(49)

$$P_{\text{RR}} = V_{\text{LOAD}} \times Q_{\text{RR}} \times F_{\text{SW}} [\text{W}]$$

(50)

$Q_{\text{RR}}$ is the reverse recovery charge of the diode and is specified in the diode datasheet. Reverse recovery characteristics of the diode strongly affect efficiency, especially when the output voltage is high.

$P_{\text{L}}$ is the sum of DCR loss ($P_{\text{DCR}}$) and AC core loss ($P_{\text{AC}}$). DCR is the DC resistance of inductor which is mentioned in the inductor data sheet.

$$P_{\text{L}} = P_{\text{DCR}} + P_{\text{AC}} [\text{W}]$$

(51)

Each power loss is approximately calculated as follows:

$$P_{\text{DCR}} = I_{\text{SUPPLY}}^2 \times R_{\text{DCR}} [\text{W}]$$

(52)

$$P_{\text{AC}} = K \times \Delta I F_{\text{SW}}^\alpha [\text{W}]$$

(53)

$$\Delta I = \frac{V_{\text{SUPPLY}} \times D \times \frac{1}{F_{\text{SYNC}}}}{L_{\text{M}}}$$

(54)
$\Delta I$ is the peak-to-peak inductor current ripple. $K$, $\alpha$, and $\beta$ are core dependent factors which can be provided by the inductor manufacturer.

$P_{RS}$ is calculated as follows:

$$P_{RS} = D \times I_{SUPPLY}^2 \times R_S [W]$$

Efficiency of the power converter can be estimated as follows:

$$\text{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{P_{TOTAL} + V_{LOAD} \times I_{LOAD}} \times 100\%$$

(56)

### 8.2.3 Application Curves

- **Figure 20. Automatic Wake-Up**
- **Figure 21. Load Transient (3 A to 1.5 A, 0.1 V/DIV)**
8.3 System Examples

8.3.1 Lower Standby Threshold in SS Configuration

By connecting the VIN pin to the VOUT pin, the current limit threshold at the current limit comparator input (\(V_{CL}\)) is set to 1.2 V. In SS configuration, the VOUT standby threshold is ignored. The device goes into the standby mode when VOUT > VIN standby threshold.

![Diagram showing lower standby threshold in SS configuration](image)

Figure 22. Lower Standby Threshold in SS Configuration

8.3.2 Dithering Using Dither Enabled Device

Dithering is achieved by connecting DITH output to the RT pin through a resistor.

![Diagram showing dithering using dither enabled device](image)

Figure 23. Dithering Using Dither Enabled Device LM5141

8.3.3 Clock Synchronization With LM5140

Clock synchronization can be achieved by connecting LM5140’s SYNCOUT to SYNC.

![Diagram showing clock synchronization with LM5140](image)

Figure 24. Clock Synchronization With LM5140
**System Examples (continued)**

### 8.3.4 Dynamic Frequency Change

Switching frequency can be changed dynamically during operation by changing the RT resistor.

![Figure 25. Dynamic Frequency Change](image)

**8.3.5 Dithering Using an External Clock**

If a low-frequency clock is available, dithering can be achieved by injecting a ramp signal into RT.

![Figure 26. Dithering Using an External Clock](image)
9 Power Supply Recommendations

The LM5150-Q1 is designed to operate from a power supply or a battery whose voltage range is from 1.5 V to 42 V. The input power supply should be able to supply the maximum boost supply voltage and handle the maximum input current at 1.5 V. The impedance of the power supply and battery including cables must be low enough that an input current transient does not cause an excessive drop. Additional input ceramic capacitors may be required at the supply input of the converter.

10 Layout

10.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimize generation of unwanted EMI.

- Place Q1, D1, and Rs first.
- Place ceramic COUT and make the switching loop (COUT-D1-Q1-Rs-COUT) as small as possible.
- Leave copper area next to D1 for thermal dissipation.
- Place LM5150-Q1 close to Rs.
- Place CPVCC as close to the device as possible between PVCC and PGND.
- Connect PGND directly to the center of the sense resistor using a wide and short trace.
- Connect CS to the center of the sense resistor. Connect through vias if required. Connect filter capacitor between CS pin and exposed pad.
- Connect AGND directly to the analog ground plain and connect to RSET, RT, and CCOMP.
- Connect the exposed pad to the analog ground plain and the power ground plain through vias.
- Connect LO directly to the gate of Q1.
- Make the switching signal loop (LO-Q1-Rs-PGND-LO) as small as possible.
- Place CVOUT as close to the device as possible.
- The LM5150-Q1 has an exposed thermal pad to aid power dissipation. Adding several vias under the exposed pad helps conduct heat away from the device. Connect the vias to a large ground plane on the bottom layer.
10.2 Layout Example

Figure 27. LM5150-Q1 PCB Layout Example
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5150-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{\text{IN}}$), output voltage ($V_{\text{OUT}}$), and output current ($I_{\text{OUT}}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
EXAMPLE BOARD LAYOUT

RUM0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
NOTE: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PINS</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM5150QRUMRQ1</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>2000</td>
<td>Green</td>
<td>SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 150</td>
<td>LM5150Q</td>
<td>Samples</td>
</tr>
<tr>
<td>LM5150QRUMTQ1</td>
<td>ACTIVE</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>250</td>
<td>Green</td>
<td>SN</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 150</td>
<td>LM5150Q</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer**: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM5150QRUMQ1</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>4.3</td>
<td>4.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>LM5150QRUMTQ1</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>4.3</td>
<td>4.3</td>
<td>1.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

**Notes:**
- **A0:** Dimension designed to accommodate the component width.
- **B0:** Dimension designed to accommodate the component length.
- **K0:** Dimension designed to accommodate the component thickness.
- **W:** Overall width of the carrier tape.
- **P1:** Pitch between successive cavity centers.
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LM5150QRUMRQ1</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>2000</td>
<td>370.0</td>
<td>355.0</td>
<td>55.0</td>
</tr>
<tr>
<td>LM5150QRUMTQ1</td>
<td>WQFN</td>
<td>RUM</td>
<td>16</td>
<td>250</td>
<td>195.0</td>
<td>200.0</td>
<td>45.0</td>
</tr>
</tbody>
</table>
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated