LMC7111 Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output

Check for Samples: LMC7111

FEATURES

- Tiny 5-Pin SOT-23 Package Saves Space
- Very Wide Common Mode Input Range
- Specified at 2.7V, 5V, and 10V
- Typical Supply Current 25 μA at 5V
- 50 kHz Gain-Bandwidth at 5V
- Similar to Popular LMC6462
- Output to Within 20 mV of Supply Rail at 100k Load
- Good Capacitive Load Drive

DESCRIPTION

The LMC7111 is a micropower CMOS operational amplifier available in the space saving SOT-23 package. This makes the LMC7111 ideal for space and weight critical designs. The wide common-mode input range makes it easy to design battery monitoring circuits which sense signals above the V+ supply. The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

APPLICATIONS

- Mobile Communications
- Portable Computing
- Current Sensing for Battery Chargers
- Voltage Reference Buffering
- Sensor Interface
- Stable Bias for GaAs RF Amps

Connection Diagram

Figure 1. 8-Pin PDIP Top View

Figure 2. 5-Pin SOT-23 Top View

Figure 3. Actual Size

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings (1)/(2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SOT-23 Package</th>
<th>PDIP Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD Tolerance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage at Input/Output Pin</td>
<td>±Supply Voltage</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage (V⁺ – V⁻)</td>
<td>(V⁺) + 0.3V, (V⁻) – 0.3V</td>
<td></td>
</tr>
<tr>
<td>Current at Input Pin</td>
<td>±5 mA</td>
<td></td>
</tr>
<tr>
<td>Current at Output Pin (4)</td>
<td>±30 mA</td>
<td></td>
</tr>
<tr>
<td>Current at Power Supply Pin</td>
<td>30 mA</td>
<td></td>
</tr>
<tr>
<td>Lead Temp. (Soldering, 10 sec.)</td>
<td>260°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
<td></td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

(3) Human Body Model is 1.5 kΩ in series with 100 pF.

(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

(5) The maximum power dissipation is a function of T_J(MAX), θJA and TA. The maximum allowable power dissipation at any ambient temperature is PD = (T_J(MAX) – T_A)/θJA. All numbers apply for packages soldered directly into a PC board.

### Operating Ratings (1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>LMC7111AI</th>
<th>LMC7111BI</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction Temperature Range</td>
<td></td>
<td>−40°C to +85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.5V ≤ V⁺ ≤ 11V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance (θJA)</td>
<td>8-Pin PDIP</td>
<td>115°C/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5-Pin SOT-23</td>
<td>325°C/W</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For ensured specifications and the test conditions, see the Electrical Characteristics.

### 2.7V DC Electrical Characteristics

Unless otherwise specified, all limits specified for T_J = 25°C, V⁺ = 2.7V, V⁻ = 0V, V_CM = V_O = V/+2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (1)</th>
<th>LMC7111AI Limit(2)</th>
<th>LMC7111BI Limit(2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_OS</td>
<td>Input Offset Voltage</td>
<td>V⁺ = 2.7V</td>
<td>0.9</td>
<td>3</td>
<td>7</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>9</td>
<td>max</td>
<td></td>
</tr>
<tr>
<td>TCV_OS</td>
<td>Input Offset Voltage Average Drift</td>
<td>V⁺ = 2.7V</td>
<td>2.0</td>
<td></td>
<td></td>
<td>μV/°C</td>
</tr>
<tr>
<td>I_B</td>
<td>Input Bias Current</td>
<td>See (3)</td>
<td>0.1</td>
<td>1</td>
<td>20</td>
<td>pA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>20</td>
<td>max</td>
</tr>
<tr>
<td>I_OS</td>
<td>Input Offset Current</td>
<td>See (3)</td>
<td>0.01</td>
<td>0.5</td>
<td>0.5</td>
<td>pA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>10</td>
<td>max</td>
</tr>
<tr>
<td>R_IN</td>
<td>Input Resistance</td>
<td>&gt;10</td>
<td></td>
<td></td>
<td></td>
<td>Tera Ω</td>
</tr>
<tr>
<td>+PSRR</td>
<td>Positive Power Supply Rejection Ratio</td>
<td>2.7V ≤ V⁺ ≤ 5.0V, V⁻ = 0V, V_O = 2.5V</td>
<td>60</td>
<td>55</td>
<td>55</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>50</td>
<td>min</td>
</tr>
<tr>
<td>−PSRR</td>
<td>Negative Power Supply Rejection Ratio</td>
<td>−2.7V ≤ V⁺ ≤ −5.0V, V⁻ = 0V, V_O = 2.5V</td>
<td>60</td>
<td>55</td>
<td>55</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>50</td>
<td>min</td>
</tr>
</tbody>
</table>

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Bias Current specified by design and processing.
2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for \( T_J = 25^\circ C, \ V^+ = 2.7V, \ V^- = 0V, \ V_{CM} = V_O = V^+/2 \) and \( R_L > 1 \ M\Omega \). **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (1)</th>
<th>LMC7111AI Limit(2)</th>
<th>LMC7111BI Limit(2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CM} )</td>
<td>Input Common-Mode Voltage Range</td>
<td>( V^+ = 2.7V ) For CMRR ( \geq 50 ) dB</td>
<td>(-0.10)</td>
<td>0.0</td>
<td>0.0</td>
<td>V min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.40</td>
<td>0.40</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.8</td>
<td>2.7</td>
<td>2.7</td>
<td>V max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.25</td>
<td>2.25</td>
<td>2.25</td>
<td></td>
</tr>
<tr>
<td>( C_N )</td>
<td>Common-Mode Input Capacitance</td>
<td></td>
<td>3</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Swing</td>
<td>( V^+ = 2.7V ) ( R_L = 100 ) k( \Omega )</td>
<td>2.69</td>
<td>2.68</td>
<td>2.68</td>
<td>V min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.01</td>
<td>0.02</td>
<td>0.02</td>
<td>V max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.08</td>
<td>0.08</td>
<td>0.08</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V^+ = 2.7V ) ( R_L = 10 ) k( \Omega )</td>
<td>2.65</td>
<td>2.6</td>
<td>2.6</td>
<td>V min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.03</td>
<td>0.1</td>
<td>0.1</td>
<td>V max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Output Short Circuit Current</td>
<td>Sourcing, ( V_O = 0V )</td>
<td>7</td>
<td>1</td>
<td>1</td>
<td>mA min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, ( V_O = 2.7V )</td>
<td>7</td>
<td>1</td>
<td>1</td>
<td>mA min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td></td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Voltage Gain</td>
<td>Sourcing</td>
<td>400</td>
<td></td>
<td></td>
<td>V/mv</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>150</td>
<td></td>
<td></td>
<td>V/mv</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>( V^+ = +2.7V, \ V_O = V^+/2 )</td>
<td>20</td>
<td>45</td>
<td>50</td>
<td>( \mu )A max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>60</td>
<td>65</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits specified for \( T_J = 25^\circ C, \ V^+ = 2.7V, \ V^- = 0V, \ V_{CM} = V_O = V^+/2 \) and \( R_L > 1 \ M\Omega \). **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (1)</th>
<th>LMC7111AI Limit(2)</th>
<th>LMC7111BI Limit(2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>See (3)</td>
<td>0.015</td>
<td></td>
<td></td>
<td>V/\mu s</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
</tbody>
</table>

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, \( V^+ = 2.7V \) and \( R_L = 100 \) k\( \Omega \) connected to 1.35V. Amp excited with 1 kHz to produce \( V_O = 1 \) VPP.

3V DC Electrical Characteristics

Unless otherwise specified, all limits specified for \( T_J = 25^\circ C, \ V^+ = 3V, \ V^- = 0V, \ V_{CM} = V_O = V^+/2 \) and \( R_L > 1 \ M\Omega \). **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (1)</th>
<th>LMC7111AI Limit(2)</th>
<th>LMC7111BI Limit(2)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CM} )</td>
<td>Input Common-Mode Voltage Range</td>
<td>( V^+ = 3V ) For CMRR ( \geq 50 ) dB</td>
<td>(-0.25)</td>
<td>0.0</td>
<td>0.0</td>
<td>V min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.2</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2.8</td>
<td>2.8</td>
<td>2.8</td>
</tr>
</tbody>
</table>

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
### 3.3V DC Electrical Characteristics

Unless otherwise specified, all limits specified for \( T_J = 25^\circ C, V^+ = 3.3V, V^- = 0V, V_{CM} = V_O = V^-/2 \) and \( R_L > 1 \text{ M} \Omega \). **Boldface limits apply at the temperature extremes.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ(^{(1)})</th>
<th>LMC7111AI Limit (^{(2)})</th>
<th>LMC7111BI Limit (^{(2)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CM} )</td>
<td>Input Common-Mode Voltage Range</td>
<td>( V^+ = 3.3V ) For CMRR ( \geq 50 \text{ dB} )</td>
<td>(-0.25)</td>
<td>(-0.1)</td>
<td>(-0.1)</td>
<td>V min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 0.00)</td>
<td>( 0.00)</td>
<td>( 0.00)</td>
<td>V max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 3.5)</td>
<td>( 3.4)</td>
<td>( 3.4)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 3.2)</td>
<td>( 3.2)</td>
<td>( 3.2)</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Typical Values represent the most likely parametric norm.
\(^{(2)}\) All limits are specified by testing or statistical analysis.

### 5V DC Electrical Characteristics

Unless otherwise specified, all limits specified for \( T_J = 25^\circ C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^-/2 \) and \( R_L > 1 \text{ M} \Omega \). **Boldface limits apply at the temperature extremes.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ(^{(1)})</th>
<th>LMC7111AI Limit (^{(2)})</th>
<th>LMC7111BI Limit (^{(2)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>( V^+ = 5V )</td>
<td>( 0.9)</td>
<td>( 0.9)</td>
<td>( 0.9)</td>
<td>mV max</td>
</tr>
<tr>
<td>( TCV_{OS} )</td>
<td>Input Offset Voltage Average Drift</td>
<td></td>
<td>( 2.0)</td>
<td>( 2.0)</td>
<td>( 2.0)</td>
<td>μV/°C</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>See (^{(3)})</td>
<td>( 0.1)</td>
<td>( 1)</td>
<td>( 1)</td>
<td>pA max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 20)</td>
<td>( 20)</td>
<td>( 20)</td>
<td></td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td>See (^{(3)})</td>
<td>( 0.01)</td>
<td>( 0.5)</td>
<td>( 0.5)</td>
<td>pA max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 10)</td>
<td>( 10)</td>
<td>( 10)</td>
<td></td>
</tr>
<tr>
<td>( R_{IN} )</td>
<td>Input Resistance</td>
<td></td>
<td>( &gt;10)</td>
<td>( &gt;10)</td>
<td>( &gt;10)</td>
<td>Tera Ω</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>( 0V \leq V_{CM} \leq 5V )</td>
<td>( 85)</td>
<td>( 70)</td>
<td>( 60)</td>
<td>dB min</td>
</tr>
<tr>
<td>( +PSRR )</td>
<td>Positive Power Supply Rejection Ratio</td>
<td>( 5V \leq V^+ \leq 10V, V^- = 0V, V_O = 2.5V )</td>
<td>( 85)</td>
<td>( 70)</td>
<td>( 60)</td>
<td>dB min</td>
</tr>
<tr>
<td>( -PSRR )</td>
<td>Negative Power Supply Rejection Ratio</td>
<td>( -5V \leq V^- \leq -10V, V^+ = 0V, V_O = -2.5V )</td>
<td>( 85)</td>
<td>( 70)</td>
<td>( 60)</td>
<td>dB min</td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Input Common-Mode Voltage Range</td>
<td>( V^+ = 5V ) For CMRR ( \geq 50 \text{ dB} )</td>
<td>(-0.3)</td>
<td>(-0.20)</td>
<td>(-0.20)</td>
<td>V min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 0.00)</td>
<td>( 0.00)</td>
<td>( 0.00)</td>
<td>V max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 5.25)</td>
<td>( 5.20)</td>
<td>( 5.20)</td>
<td>V</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>( 5.00)</td>
<td>( 5.00)</td>
<td>( 5.00)</td>
<td></td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Common-Mode Input Capacitance</td>
<td></td>
<td>( 3)</td>
<td>( 3)</td>
<td>( 3)</td>
<td>pF</td>
</tr>
<tr>
<td>( V_O )</td>
<td>Output Swing</td>
<td>( V^+ = 5V ) ( R_L = 100 \text{ k} \Omega )</td>
<td>( 4.99)</td>
<td>( 4.98)</td>
<td>( 4.98)</td>
<td>Vmin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 0.01)</td>
<td>( 0.02)</td>
<td>( 0.02)</td>
<td>Vmax</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 4.98)</td>
<td>( 4.9)</td>
<td>( 4.9)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 0.02)</td>
<td>( 0.1)</td>
<td>( 0.1)</td>
<td>Vmin</td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>Output Short Circuit Current</td>
<td>Sourcing, ( V_O = 0V )</td>
<td>( 7)</td>
<td>( 5)</td>
<td>( 5)</td>
<td>mA min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 3.5)</td>
<td>( 3.5)</td>
<td>( 3.5)</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking, ( V_O = 3V )</td>
<td>( 7)</td>
<td>( 5)</td>
<td>( 5)</td>
<td>mA min</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>( 3.5)</td>
<td>( 3.5)</td>
<td>( 3.5)</td>
<td>mA</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Voltage Gain</td>
<td>Sourcing</td>
<td>( 500)</td>
<td>( 500)</td>
<td>( 500)</td>
<td>V/mv min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>( 200)</td>
<td>( 200)</td>
<td>( 200)</td>
<td>V/mv</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td>( V^+ = +5V, V_O = V^-/2 )</td>
<td>( 25)</td>
<td>( 25)</td>
<td>( 25)</td>
<td>μA max</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Typical Values represent the most likely parametric norm.
\(^{(2)}\) All limits are specified by testing or statistical analysis.
\(^{(3)}\) Bias Current specified by design and processing.
5V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ C$, $V^+ = 5V$, $V^- = 0V$, $V_CM = V_O = V^+/2$ and $R_L > 1 \, M\Omega$. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (1)</th>
<th>LMC7111AI Limit(2)</th>
<th>LMC7111BI Limit(2)</th>
<th>Units</th>
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<tbody>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>Positive Going Slew Rate(3)</td>
<td>0.027</td>
<td>0.015</td>
<td>0.010</td>
<td>V/μs</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
</tbody>
</table>

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive slew rate. The negative slew rate is faster. Input referred, $V^+ = 5V$ and $R_L = 100 \, k\Omega$ connected to 1.5V. Amp excited with 1 kHz to produce $V_O = 1 \, V_{pp}$.

10V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ C$, $V^+ = 10V$, $V^- = 0V$, $V_CM = V_O = V^+/2$ and $R_L > 1 \, M\Omega$. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ (1)</th>
<th>LMC7111AI Limit(2)</th>
<th>LMC7111BI Limit(2)</th>
<th>Units</th>
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<tr>
<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>$V^+ = 10V$</td>
<td>0.9</td>
<td>3</td>
<td>7</td>
<td>mV/°C</td>
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<tr>
<td>$TCV_{OS}$</td>
<td>Input Offset Voltage Average Drift</td>
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<td></td>
<td></td>
<td>μV/°C</td>
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<td>$I_B$</td>
<td>Input Bias Current</td>
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<td>0.1</td>
<td>1</td>
<td>1</td>
<td>pA</td>
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<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current</td>
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<td>0.01</td>
<td>0.5</td>
<td>0.5</td>
<td>pA</td>
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<td>$R_N$</td>
<td>Input Resistance</td>
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<td></td>
<td></td>
<td>Tera Ω</td>
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<tr>
<td>$+PSRR$</td>
<td>Positive Power Supply Rejection Ratio</td>
<td>$5V \leq V^+ \leq 10V$, $V^- = 0V$, $V_O = 2.5V$</td>
<td>80</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$-PSRR$</td>
<td>Negative Power Supply Rejection Ratio</td>
<td>$-5V \leq V^- \leq 10V$, $V^+ = 0V$, $V_O = 2.5V$</td>
<td>80</td>
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<td></td>
<td>dB</td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Input Common-Mode Voltage Range</td>
<td>$V^+ = 10V$ For CMRR ≥ 50 dB</td>
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<td>V</td>
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<td></td>
<td></td>
<td>0.00</td>
<td>0.00</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10.2</td>
<td>10.15</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10.00</td>
<td>10.00</td>
<td>V</td>
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<td>$C_{IN}$</td>
<td>Common-Mode Input Capacitance</td>
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<td>mA</td>
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<td></td>
<td></td>
<td>Sinking, $V_O = 10V$</td>
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<td>20</td>
<td>20</td>
<td>mA</td>
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<td>$A_{VOL}$</td>
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<td></td>
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<td></td>
<td>Sinking</td>
<td>200</td>
<td>V/mv</td>
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<td></td>
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<td>$I_S$</td>
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<td>$V^+ = +10V$, $V_O = V^+/2$</td>
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<td>50</td>
<td>65</td>
<td>μA</td>
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<td></td>
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<td>60</td>
<td>75</td>
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<td>$V_O$</td>
<td>Output Swing</td>
<td>$V^+ = 10V$ $R_L = 100 , k\Omega$</td>
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<td>9.98</td>
<td>9.98</td>
<td>Vmin</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.01</td>
<td>0.02</td>
<td>Vmax</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^+ = 10V$ $R_L = 10 , k\Omega$</td>
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<td>9.9</td>
<td>9.9</td>
<td>Vmin</td>
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<tr>
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<td></td>
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<td></td>
<td>0.02</td>
<td>0.1</td>
<td>0.1 Vmin</td>
</tr>
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</table>

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Bias Current specified by design and processing.
10V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ C$, $V^+ = 10V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1 M\Omega$. **Boldface** limits apply at the temperature extremes.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ$^{(1)}$</th>
<th>LMC7111AI Limit$^{(2)}$</th>
<th>LMC7111BI Limit$^{(2)}$</th>
<th>Units</th>
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</thead>
<tbody>
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<td>SR</td>
<td>Slew Rate</td>
<td>See$^{(3)}$</td>
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<td></td>
<td>V/μs</td>
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<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td>kHz</td>
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<td>$\phi_m$</td>
<td>Phase Margin</td>
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<td></td>
<td></td>
<td></td>
<td>deg</td>
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<tr>
<td>$G_m$</td>
<td>Gain Margin</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>Input-Referred Voltage Noise</td>
<td>$f = 1$ kHz $V_{CM} = 1V$</td>
<td>110</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td></td>
<td>Input-Referred Current Noise</td>
<td>$f = 1$ kHz</td>
<td>0.03</td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
</tbody>
</table>

(1) Typical Values represent the most likely parametric norm.
(2) All limits are specified by testing or statistical analysis.
(3) Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, $V^+ = 10V$ and $R_L = 100 \, k\Omega$ connected to 5V. Amp excited with 1 kHz to produce $V_O = 2 \, V_{PP}$. 

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Typical Performance Characteristics

$T_A = 25^\circ C$ unless specified, Single Supply

**Supply Current vs. Supply Voltage**

Figure 4.

**Voltage Noise vs. Frequency**

Figure 5.

### 2.7V Performance

**Offset Voltage vs. Common Mode Voltage @ 2.7V**

Figure 6.

**Sinking Output vs. Output Voltage**

Figure 7.

**Sourcing Output vs. Output Voltage**

Figure 8.

**Gain and Phase vs. Capacitive Load @ 2.7V**

Figure 9.
2.7V Performance (continued)

Gain and Phase vs. Capacitive Load @ 2.7V

Figure 10.

Gain and Phase vs. Capacitive Load @ 2.7V

Figure 11.

3V Performance

Voltage Noise vs. Common Mode Voltage @ 3V

Figure 12.

Output Voltage vs. Input Voltage @ 3V

Figure 13.

Offset Voltage vs. Common Mode Voltage @ 3V

Figure 14.

Sourcing Output vs. Output Voltage

Figure 15.
3V Performance (continued)

Figure 16. Sinking Output vs. Output Voltage

Figure 17. Gain and Phase vs. Capacitive Load @ 3V

Figure 18. Gain and Phase vs. Capacitive Load @ 3V

5V Performance

Figure 19. Gain and Phase vs. Capacitive Load @ 3V

Figure 20. Voltage Noise vs. Common Mode Voltage @ 5V

Figure 21. Output Voltage vs. Input Voltage @ 5V
5V Performance (continued)

Offset Voltage vs. Common Mode Voltage @ 5V

Sourcing Output vs. Output Voltage

Sinking Output vs. Output Voltage

Gain and Phase vs. Capacitive Load @ 5V

Gain and Phase vs. Capacitive Load @ 5V

Gain and Phase vs. Capacitive Load @ 5V

Gain and Phase vs. Capacitive Load @ 5V

Figure 22.

Figure 23.

Figure 24.

Figure 25.

Figure 26.

Figure 27.
5V Performance (continued)

Non-Inverting Small Signal Pulse Response at 5V

- $V_G = \pm 2.5\text{V}$
- $R_I = 100k\Omega$
- $T_A = -55^\circ\text{C}$
- $A_V = +1$

50 mV/Div

20 $\mu$sec/Div

Figure 28.

Non-Inverting Small Signal Pulse Response at 5V

- $V_G = \pm 2.5\text{V}$
- $R_I = 100k\Omega$
- $T_A = 25^\circ\text{C}$
- $A_V = +1$

50 mV/Div

20 $\mu$sec/Div

Figure 29.

Non-Inverting Small Signal Pulse Response at 5V

- $V_G = \pm 2.5\text{V}$
- $R_I = 100k\Omega$
- $T_A = 125^\circ\text{C}$
- $A_V = +1$

50 mV/Div

20 $\mu$sec/Div

Figure 30.

Non-Inverting Large Signal Pulse Response at 5V

- $V_G = \pm 2.5\text{V}$
- $R_I = 100k\Omega$
- $T_A = -55^\circ\text{C}$
- $A_V = +1$

500 mV/Div

20 $\mu$sec/Div

Figure 31.

Non-Inverting Large Signal Pulse Response at 5V

- $V_G = \pm 2.5\text{V}$
- $R_I = 100k\Omega$
- $T_A = 25^\circ\text{C}$
- $A_V = +1$

500 mV/Div

20 $\mu$sec/Div

Figure 32.

Non-Inverting Large Signal Pulse Response at 5V

- $V_G = \pm 2.5\text{V}$
- $R_I = 100k\Omega$
- $T_A = 125^\circ\text{C}$
- $A_V = +1$

500 mV/Div

20 $\mu$sec/Div

Figure 33.

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Product Folder Links: LMC7111
5V Performance (continued)

Inverting Small Signal Pulse Response at 5V

\[ V_S = \pm 2.5\text{V} \]
\[ R_I = 100k\Omega \]
\[ T_A = -55^\circ\text{C} \]
\[ A_V = -1 \]

50 mV/Div

20 μsec/Div

Figure 34.

Inverting Large Signal Pulse Response at 5V

\[ V_S = \pm 2.5\text{V} \]
\[ R_I = 100k\Omega \]
\[ T_A = 125^\circ\text{C} \]
\[ A_V = -1 \]

500 mV/Div

20 μsec/Div

Figure 36.

Inverting Small Signal Pulse Response at 5V

\[ V_S = \pm 2.5\text{V} \]
\[ R_I = 100k\Omega \]
\[ T_A = 25^\circ\text{C} \]
\[ A_V = -1 \]

50 mV/Div

20 μsec/Div

Figure 35.

Inverting Large Signal Pulse Response at 5V

\[ V_S = \pm 2.5\text{V} \]
\[ R_I = 100k\Omega \]
\[ T_A = -55^\circ\text{C} \]
\[ A_V = -1 \]

500 mV/Div

20 μsec/Div

Figure 37.

Inverting Large Signal Pulse Response at 5V

\[ V_S = \pm 2.5\text{V} \]
\[ R_I = 100k\Omega \]
\[ T_A = 25^\circ\text{C} \]
\[ A_V = -1 \]

500 mV/Div

20 μsec/Div

Figure 38.

Inverting Large Signal Pulse Response at 5V

\[ V_S = \pm 2.5\text{V} \]
\[ R_I = 100k\Omega \]
\[ T_A = 125^\circ\text{C} \]
\[ A_V = -1 \]

500 mV/Div

20 μsec/Div

Figure 39.
10V Performance

**Voltage Noise vs. Common Mode Voltage @ 10V**

- $V_S = \pm 5V$
- $F = 100 \text{ Hz}$

**Output Voltage vs. Input Voltage @ 10V**

- $V_S = \pm 5V$
- $R_I = 100k$

**Offset Voltage vs. Common Mode Voltage @ 10V**

- $V_S = \pm 5V$

**Sourcing Output vs. Output Voltage**

- $V_S = 10V$

**Sinking Output vs. Output Voltage**

- $V_S = 10V$

**Gain and Phase vs. Capacitive Load @ 10V**

- $V_S = \pm 5V$
- $R_I = 100k$
- $T_A = -55^\circ C$

**Capacitive Load @ 10V**

- $C_L = 500 \text{ pf}$

**Frequency (Hz)**

- $10$ to $1M$

**Phase (deg)**

- $-30$ to $30$
10V Performance (continued)

**Gain and Phase vs. Capacitive Load @ 10V**

Figure 46.

**Non-Inverting Small Signal Pulse Response at 10V**

Figure 48.

**Inverting Small Signal Pulse Response at 10V**

Figure 50.

**Gain and Phase vs. Capacitive Load @ 10V**

Figure 47.

**Non-Inverting Large Signal Pulse Response at 10V**

Figure 49.

**Inverting Large Signal Pulse Response at 10V**

Figure 51.
APPLICATION INFORMATION

BENEFITS OF THE LMC7111 TINY AMP

Size
The small footprint of the SOT-23 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height
The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

Signal Integrity
Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

Simplified Board Layout
The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping
LMC7111 amplifiers packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Low Supply Current
The typical 25 μA supply current of the LMC7111 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range
The LMC7111 is characterized at 2.7V, 3V, 3.3V, 5V and 10V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7111 a good choice for devices where the voltage may vary over the life of the batteries.

INPUT COMMON MODE VOLTAGE RANGE
The LMC7111 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in Figure 52.

![Figure 52. R_I Input Current Protection for Voltages Exceeding the Supply Voltage](image-url)
CAPACITIVE LOAD TOLERANCE

The LMC7111 can typically directly drive a 300 pF load with $V_S = 10$V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp’s output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 53. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

![Figure 53. Resistive Isolation of a 330 pF Capacitive Load](image)

COMPENSATING FOR INPUT CAPACITANCE WHEN USING LARGE VALUE FEEDBACK RESISTORS

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 54), $C_f$ is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \leq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for $C_f$ may be different. The values of $C_f$ should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

![Figure 54. Cancelling the Effect of Input Capacitance](image)

OUTPUT SWING

The output of the LMC7111 will go to within 100 mV of either power supply rail for a 10 kΩ load and to 20 mV of the rail for a 100 kΩ load. This makes the LMC7111 useful for driving transistors which are connected to the same power supply. By going very close to the supply, the LMC7111 can turn the transistors all the way on or all the way off.
BIASING GaAs RF AMPLIFIERS

The capacitive load capability, low current draw, and small size of the SOT-23 LMC7111 make it a good choice for providing a stable negative bias to other integrated circuits. The very small size of the LMC7111 and the LM4040 reference take up very little board space.

![Figure 55. Stable Negative Bias](image)

C_F and R_isolation prevent oscillations when driving capacitive loads.

REFERENCE BUFFER FOR A-TO-D CONVERTERS

The LMC7111 can be used as a voltage reference buffer for analog-to-digital converters. This works best for A-to-D converters whose reference input is a static load, such as dual slope integrating A-to-Ds. Converters whose reference input is a dynamic load (the reference current changes with time) may need a faster device, such as the LMC7101 or the LMC7131.

The small size of the LMC7111 allows it to be placed close to the reference input. The low supply current (25 μA typical) saves power.

For A-to-D reference inputs which require higher accuracy and lower offset voltage, please see the LMC6462 datasheet. The LMC6462 has performance similar to the LMC7111. The LMC6462 is available in two grades with reduced input voltage offset.

DUAL AND QUAD DEVICES WITH SIMILAR PERFORMANCE

The LMC6462 and LMC6464 are dual and quad devices with performance similar to the LMC7111. They are available in both conventional through-hole and surface mount packaging. Please see the LMC6462/4 datasheet for details.

SPICE MACROMODEL

A SPICE macromodel is available for the LMC7111. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
• Quiescent and dynamic supply current
• Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Visit the LMC7111 product page on http://www.ti.com for the spice model.

ADDITIONAL SOT-23 TINY DEVICES
Additional parts are available in the space saving SOT-23 Tiny package, including amplifiers, voltage references, and voltage regulators. These devices include—

LMC7101 1 MHz gain-bandwidth rail-to-rail input and output amplifier—high input impedance and high gain, 700 μA typical current 2.7V, 3V, 5V and 15V specifications.
LM7131 Tiny Video amp with 70 MHz gain bandwidth. Specified at 3V, 5V and ± 5V supplies.
LMC7211 Comparator in a tiny package with rail-to-rail input and push-pull output. Typical supply current of 7 μA. Typical propagation delay of 7 μs. Specified at 2.7V, 5V and 15V supplies.
LMC7221 Comparator with an open drain output for use in mixed voltage systems. Similar to the LMC7211, except the output can be used with a pull-up resistor to a voltage different than the supply voltage.
LP2980 Micropower SOT 50 mA Ultra Low-Dropout Regulator.
LM4040 Precision micropower shunt voltage reference. Fixed voltages of 2.5000V, 4.096V, 5.000V, 8.192V and 10.000V.
LM4041 Precision micropower shunt voltage reference 1.225V and adjustable.

Visit http://www.ti.com for more information.
## REVISION HISTORY

### Changes from Revision D (March 2013) to Revision E

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<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
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<th>Op Temp (°C)</th>
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</tr>
<tr>
<td>LMC7111BIM5/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>A01B</td>
<td></td>
</tr>
<tr>
<td>LMC7111BIM5X</td>
<td>NRND</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 85</td>
<td>A01B</td>
<td></td>
</tr>
<tr>
<td>LMC7111BIM5X/NOPB</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
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<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>A01B</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **Eco Plan** - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Q1
- Q2
- Q3
- Q4

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMC7111BIM5</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LMC7111BIM5/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
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<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>LMC7111BIM5X</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
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<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMC7111BIM5</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LMC7111BIM5/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LMC7111BIM5X</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LMC7111BIM5X/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
EXAMPLE BOARD LAYOUT

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
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NOTES: (continued)

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7. Board assembly site may have different recommendations for stencil design.
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