LMH6321 300 mA High Speed Buffer with Adjustable Current Limit

Check for Samples: LMH6321

FEATURES

- High Slew Rate 1800 V/µs
- Wide Bandwidth 110 MHz
- Continuous Output Current ±300 mA
- Output Current Limit Tolerance ±5 mA ±5%
- Wide Supply Voltage Range 5V to ±15V
- Wide Temperature Range -40°C to +125°C
- Adjustable Current Limit
- High Capacitive Load Drive
- Thermal Shutdown Error Flag

DESCRIPTION

The LMH6321 is a high speed unity gain buffer that slews at 1800 V/µs and has a small signal bandwidth of 110 MHz while driving a 50Ω load. It can drive ±300 mA continuously and will not oscillate while driving large capacitive loads.

The LMH6321 features an adjustable current limit. The current limit is continuously adjustable from 10 mA to 300 mA with a ±5 mA ±5% accuracy. The current limit is set by adjusting an external reference current with a resistor. The current can be easily and instantly adjusted, as needed by connecting the resistor to a DAC to form the reference current. The sourcing and sinking currents share the same current limit.

The LMH6321 is available in a space saving 8-pin SO PowerPAD or a 7-pin DDPAK power package. The SO PowerPAD package features an exposed pad on the bottom of the package to increase its heat sinking capability. The LMH6321 can be used within the feedback loop of an operational amplifier to boost the current output or as a stand alone buffer.

APPLICATIONS

- Line Driver
- Pin Driver
- Sonar Driver
- Motor Control

CONNECTION DIAGRAM

Figure 1. 8-Pin SO PowerPAD

Figure 2. 7-Pin DDPAK(A)

A. V− pin is connected to tab on back of each package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ABSOLUTE MAXIMUM RATINGS** \(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human Body Model</td>
<td>2.5 kV</td>
</tr>
<tr>
<td>Machine Model</td>
<td>250V</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>36V (±18V)</td>
</tr>
<tr>
<td>Input to Output Voltage</td>
<td>±5V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>±V(_{\text{SUPPLY}})</td>
</tr>
<tr>
<td>Output Short-Circuit to GND</td>
<td>Continuous</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Junction Temperature (T(_{\text{JMAX}}))</td>
<td>+150°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 seconds)</td>
<td>260°C</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>(6)</td>
</tr>
<tr>
<td>C(_L) Pin to GND Voltage</td>
<td>±1.2V</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For specifications and the test conditions, see the Electrical Characteristics Table.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.

(4) If the input-output voltage differential exceeds ±5V, internal clamping diodes will turn on. The current through these diodes should be limited to 5 mA max. Thus for an input voltage of ±15V and the output shorted to ground, a minimum of 2 kΩ should be placed in series with the input.

(5) The maximum continuous current must be limited to 300mA. See APPLICATION HINTS for more details.

(6) The maximum power dissipation is a function of T\(_{\text{JMAX}}\), θ\(_{JA}\), and T\(_A\). The maximum allowable power dissipation at any ambient temperature is P\(_D\) = T\(_{\text{JMAX}}\) - T\(_A\)/θ\(_{JA}\). See THERMAL MANAGEMENT of APPLICATION HINTS.

**OPERATING RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature Range</td>
<td>−40°C to +125°C</td>
</tr>
<tr>
<td>Operating Supply Range</td>
<td>5V to ±16V</td>
</tr>
<tr>
<td>Thermal Resistance (θ(_{JA}))</td>
<td>(1)</td>
</tr>
<tr>
<td>SO PowerPAD Package</td>
<td>180°C/W</td>
</tr>
<tr>
<td>Thermal Resistance (θ(_{JC}))</td>
<td>DDPAK Package</td>
</tr>
<tr>
<td>Thermal Resistance (θ(_{JA}))</td>
<td>4°C/W</td>
</tr>
</tbody>
</table>

(1) Soldered to PC board with copper footprint equal to DAP size. Natural convection (no air flow). Board material is FR-4.
**±15V ELECTRICAL CHARACTERISTICS**

The following specifications apply for Supply Voltage = ±15V, \( V_{CM} = 0 \), \( R_L \geq 100 \, \text{kΩ} \) and \( R_S = 50\Omega \), \( C_L \) open, unless otherwise noted. **Boldface** limits apply for \( T_A = T_J = T_{MIN} \) to \( T_{MAX} \), all other limits \( T_A = T_J = 25°C \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( AV )</td>
<td>Voltage Gain</td>
<td>( R_L = 1 , \text{kΩ}, V_{IN} = \pm 10V )</td>
<td>0.99</td>
<td>0.995</td>
<td></td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 50\Omega, V_{IN} = \pm 10V )</td>
<td>0.86</td>
<td>0.92</td>
<td></td>
<td>V/V</td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>( R_L = 1 , \text{kΩ}, R_S = 0V )</td>
<td>±4</td>
<td>±35</td>
<td>±52</td>
<td>mV</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>( V_{IN} = 0V, R_L = 1 , \text{kΩ}, R_S = 0V )</td>
<td>±2</td>
<td>±15</td>
<td>±17</td>
<td>μA</td>
</tr>
<tr>
<td>( R_{IN} )</td>
<td>Input Resistance</td>
<td>( R_L = 50\Omega )</td>
<td>250</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td></td>
<td>3.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( R_O )</td>
<td>Output Resistance</td>
<td>( I_O = \pm 10 , \text{mA} )</td>
<td>5</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Power Supply Current</td>
<td>( R_L = \infty, V_{IN} = 0V )</td>
<td>11</td>
<td>14.5</td>
<td>16.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 750 , \mu\text{A} ) into ( C_L ) Pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{O1} )</td>
<td>Positive Output Swing</td>
<td>( I_O = 300 , \text{mA}, R_S = 0V, V_{IN} = \pm V_S )</td>
<td>11.2</td>
<td></td>
<td>11.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Negative Output Swing</td>
<td>( I_O = 300 , \text{mA}, R_S = 0V, V_{IN} = \pm V_S )</td>
<td>−11.3</td>
<td>−10.3</td>
<td>−9.8</td>
<td>V</td>
</tr>
<tr>
<td>( V_{O2} )</td>
<td>Positive Output Swing</td>
<td>( R_L = 1 , \text{kΩ}, R_S = 0V, V_{IN} = \pm V_S )</td>
<td>13.1</td>
<td></td>
<td>13.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Negative Output Swing</td>
<td>( R_L = 1 , \text{kΩ}, R_S = 0V, V_{IN} = \pm V_S )</td>
<td>−13.4</td>
<td>−12.9</td>
<td>−12.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{O3} )</td>
<td>Positive Output Swing</td>
<td>( R_L = 50\Omega, R_S = 0V, V_{IN} = \pm V_S )</td>
<td>11.6</td>
<td></td>
<td>12.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Negative Output Swing</td>
<td>( R_L = 50\Omega, R_S = 0V, V_{IN} = \pm V_S )</td>
<td>−11.9</td>
<td>−10.9</td>
<td>−10.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{EF} )</td>
<td>Error Flag Output Voltage</td>
<td>( R_L = \infty, V_{IN} = 0V ), EF pulled up with 5 kΩ to +5V</td>
<td>Normal</td>
<td>5.00</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>During Thermal Shutdown</td>
<td></td>
<td>0.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( T_{SH} )</td>
<td>Thermal Shutdown Temperature</td>
<td>Measure Quantity is Die (Junction)</td>
<td>168</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysteresis</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SH} )</td>
<td>Supply Current at Thermal Shutdown</td>
<td>EF pulled up with 5 kΩ to +5V</td>
<td>3</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( PSSR )</td>
<td>Power Supply Rejection Ratio</td>
<td>( R_L = 1 , \text{kΩ}, V_{IN} = 0V, V_S = \pm 5V ) to ±15V</td>
<td>Positive</td>
<td>58</td>
<td>66</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Negative</td>
<td>58</td>
<td>64</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( SR )</td>
<td>Slew Rate</td>
<td>( V_{IN} = \pm 11V, R_L = 1 , \text{kΩ} )</td>
<td>2900</td>
<td></td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{IN} = \pm 11V, R_L = 50\Omega )</td>
<td>1800</td>
<td></td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>( BW )</td>
<td>−3 dB Bandwidth</td>
<td>( V_{IN} = \pm 20 , \text{mVpp}, R_L = 50\Omega )</td>
<td>110</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( LSBW )</td>
<td>Large Signal Bandwidth</td>
<td>( V_{IN} = 2 , \text{Vpp}, R_L = 50\Omega )</td>
<td>48</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( HD2 )</td>
<td>2nd Harmonic Distortion</td>
<td>( V_O = 2 , \text{Vpp}, f = 100 , \text{kHz} )</td>
<td>( R_L = 50\Omega )</td>
<td>−59</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 100\Omega )</td>
<td>−70</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O = 2 , \text{Vpp}, f = 1 , \text{MHz} )</td>
<td>( R_L = 50\Omega )</td>
<td>−57</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 100\Omega )</td>
<td>−68</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
</tbody>
</table>
±15V ELECTRICAL CHARACTERISTICS (continued)
The following specifications apply for Supply Voltage = ±15V, \( V_{CM} = 0 \), \( R_L \geq 100 \, \Omega \) and \( R_S = 50 \, \Omega \), \( C_L \) open, unless otherwise noted. **Boldface** limits apply for \( T_A = T_J = T_{MIN} \) to \( T_{MAX} \); all other limits \( T_A = T_J = 25°C \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>HD3</td>
<td>3rd Harmonic Distortion</td>
<td>( V_O = 2 , V_{PP}, f = 100 , kHz ) ( R_L = 50 , \Omega )</td>
<td>(-59)</td>
<td>(-70)</td>
<td>(-73)</td>
<td>dBc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 100 , \Omega )</td>
<td>(-62)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O = 2 , V_{PP}, f = 1 , MHz ) ( R_L = 50 , \Omega )</td>
<td>(-62)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 100 , \Omega )</td>
<td>(-73)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( e_n )</td>
<td>Input Voltage Noise</td>
<td>( f \geq 10 , kHz )</td>
<td>( 2.8 )</td>
<td>( 2.4 )</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>( i_n )</td>
<td>Input Current Noise</td>
<td>( f \geq 10 , kHz )</td>
<td>( 2.4 )</td>
<td>( 2.4 )</td>
<td>pA/√Hz</td>
<td></td>
</tr>
<tr>
<td>( I_{SC1} )</td>
<td>Output Short Circuit Current Source (1)</td>
<td>( V_O = 0V, ) ( V_{IN} = +3V ) ( \frac{C_L}{25 , \mu A} )</td>
<td>( 4.5 )</td>
<td>( 4.5 )</td>
<td>( 10 )</td>
<td>( 15.5 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sourcing ( V_{IN} = +3V )</td>
<td>( 4.5 )</td>
<td>( 10 )</td>
<td>( 15.5 )</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking ( V_{IN} = -3V )</td>
<td>( 4.5 )</td>
<td>( 10 )</td>
<td>( 15.5 )</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O = 0V, ) ( V_{IN} = +3V ) ( \frac{C_L}{750 , \mu A} )</td>
<td>( 273 )</td>
<td>( 280 )</td>
<td>( 295 )</td>
<td>( 308 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sourcing ( V_{IN} = +3V )</td>
<td>( 273 )</td>
<td>( 280 )</td>
<td>( 295 )</td>
<td>( 308 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking ( V_{IN} = -3V )</td>
<td>( 273 )</td>
<td>( 280 )</td>
<td>( 295 )</td>
<td>( 308 )</td>
</tr>
<tr>
<td>( I_{SC2} )</td>
<td>Output Short Circuit Current Source</td>
<td>( R_S = 0V, ) ( V_{IN} = +3V ) (2)</td>
<td>( 320 )</td>
<td>( 300 )</td>
<td>( 570 )</td>
<td>( 750 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sourcing ( V_{IN} = +3V )</td>
<td>( 320 )</td>
<td>( 300 )</td>
<td>( 570 )</td>
<td>( 750 )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking ( V_{IN} = -3V )</td>
<td>( 320 )</td>
<td>( 300 )</td>
<td>( 570 )</td>
<td>( 750 )</td>
</tr>
<tr>
<td>V/I Section</td>
<td>Current Limit Input Offset Voltage</td>
<td>( R_L = 1 , k\Omega, GND = 0V )</td>
<td>( \pm 0.5 )</td>
<td>( \pm 4.0 )</td>
<td>( \pm 8.0 )</td>
<td>mV</td>
</tr>
<tr>
<td>CLIB</td>
<td>Current Limit Input Bias Current</td>
<td>( R_L = 1 , k\Omega )</td>
<td>(-0.5 )</td>
<td>(-0.8 )</td>
<td>(-0.2 )</td>
<td>μA</td>
</tr>
<tr>
<td>CLCMRR</td>
<td>Current Limit Common Mode Rejection Ratio</td>
<td>( R_L = 1 , k\Omega, GND = -13 ) ( +14V )</td>
<td>( 60 )</td>
<td>( 56 )</td>
<td>( 69 )</td>
<td>dB</td>
</tr>
</tbody>
</table>

(1) \( V_{IN} = + \) or \( -4V \) at \( T_J = -40°C \).
(2) For the condition where the \( C_L \) pin is left open the output current should not be continuous, but instead, should be limited to low duty cycle pulse mode such that the RMS output current is less than or equal to 300 mA.
±5V ELECTRICAL CHARACTERISTICS

The following specifications apply for Supply Voltage = ±5V, \( V_{CM} = 0 \), \( R_L \geq 100 \, k\Omega \) and \( R_S = 50\Omega \), \( C_L \) Open, unless otherwise noted. Boldface limits apply for \( T_A = T_J = T_{MIN} \) to \( T_{MAX} \); all other limits \( T_A = T_J = 25^\circ C \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_V )</td>
<td>Voltage Gain</td>
<td>( R_L = 1 , k\Omega, \ V_{IN} = \pm 3V )</td>
<td>0.99</td>
<td>0.94</td>
<td></td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L = 50\Omega, \ V_{IN} = \pm 3V )</td>
<td>0.86</td>
<td>0.92</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Offset Voltage</td>
<td>( R_L = 1 , k\Omega, \ R_S = 0V )</td>
<td>±2.5</td>
<td>±35</td>
<td>±50</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{B} )</td>
<td>Input Bias Current</td>
<td>( V_{IN} = 0V, \ R_L = 1 , k\Omega, \ R_S = 0V )</td>
<td>±2</td>
<td>±15</td>
<td>±17</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( R_{IN} )</td>
<td>Input Resistance</td>
<td>( R_L = 50\Omega )</td>
<td>250</td>
<td></td>
<td></td>
<td>k\Omega</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance</td>
<td></td>
<td>3.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( R_{O} )</td>
<td>Output Resistance</td>
<td>( I_{OUT} = \pm 10 , mA )</td>
<td>5</td>
<td></td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( I_{S} )</td>
<td>Power Supply Current</td>
<td>( R_L = \infty, \ V_{IN} = 0V )</td>
<td>10</td>
<td>13.5</td>
<td>14.7</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>750 ( \mu A ) into ( C_L ) Pin</td>
<td>14</td>
<td>17.5</td>
<td>19.5</td>
</tr>
<tr>
<td>( V_{O1} )</td>
<td>Positive Output Swing</td>
<td>( I_O = 300 , mA, \ R_S = 0V, \ V_{IN} = \pm V_S )</td>
<td>1.3</td>
<td>1.9</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Negative Output Swing</td>
<td>( I_O = 300 , mA, \ R_S = 0V, \ V_{IN} = \pm V_S )</td>
<td>−1.3</td>
<td>−0.5</td>
<td>−0.1</td>
</tr>
<tr>
<td>( V_{O2} )</td>
<td>Positive Output Swing</td>
<td>( R_L = 1 , k\Omega, \ R_S = 0V, \ V_{IN} = \pm V_S )</td>
<td>3.2</td>
<td>3.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Negative Output Swing</td>
<td>( R_L = 1 , k\Omega, \ R_S = 0V, \ V_{IN} = \pm V_S )</td>
<td>−3.5</td>
<td>−3.1</td>
<td>−2.9</td>
</tr>
<tr>
<td>( V_{O3} )</td>
<td>Positive Output Swing</td>
<td>( R_L = 50\Omega, \ R_S = 0V, \ V_{IN} = \pm V_S )</td>
<td>2.8</td>
<td>3.1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Negative Output Swing</td>
<td>( R_L = 50\Omega, \ R_S = 0V, \ V_{IN} = \pm V_S )</td>
<td>−3.0</td>
<td>−2.6</td>
<td>−2.4</td>
</tr>
<tr>
<td>PSSR</td>
<td>Power Supply Rejection Ratio</td>
<td>( R_L = 1 , k\Omega, \ V_{IN} = 0, \ V_S = \pm 5V ) to ( \pm 15V )</td>
<td>Positive</td>
<td>58</td>
<td>66</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>54</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Negative</td>
<td>58</td>
<td>64</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SC1} )</td>
<td>Output Short Circuit Current</td>
<td>( V_O = 0V, ) Program Current ( \text{into} \ C_L = 25 , \mu A )</td>
<td>Sourcing</td>
<td>4.5</td>
<td>9</td>
<td>14.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>4.5</td>
<td>9</td>
<td>14.0</td>
<td>15.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_O = 0V, ) Program Current ( \text{into} \ C_L = 750 , \mu A )</td>
<td>Sourcing</td>
<td>275</td>
<td>290</td>
<td>305</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>270</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sinking</td>
<td>275</td>
<td>290</td>
<td>310</td>
<td>320</td>
</tr>
<tr>
<td>( I_{SC2} )</td>
<td>Output Short Circuit Current</td>
<td>( R_S = 0V, \ V_{IN} = +3V ) ( ^{(1)} ) ( ^{(2)} )</td>
<td>Source</td>
<td>300</td>
<td>470</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>400</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sink</td>
<td>300</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew Rate</td>
<td>( V_{IN} = \pm 2 , V_{PP}, \ R_L = 1 , k\Omega )</td>
<td>450</td>
<td></td>
<td></td>
<td>V/\mu s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{IN} = \pm 2 , V_{PP}, \ R_L = 50\Omega )</td>
<td>210</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>−3 dB Bandwidth</td>
<td>( V_{IN} = \pm 20 , mV_{PP}, \ R_L = 50\Omega )</td>
<td>90</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>LSBW</td>
<td>Large Signal Bandwidth</td>
<td>( V_{IN} = 2 , V_{PP}, \ R_L = 50\Omega )</td>
<td>39</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( T_{SD} )</td>
<td>Thermal Shutdown</td>
<td>Temperature</td>
<td>170</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hysteresis</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

V/I Section

(1) For the condition where the \( C_L \) pin is left open the output current should not be continuous, but instead, should be limited to low duty cycle pulse mode such that the RMS output current is less than or equal to 300 mA.

(2) \( V_{IN} = +4V \) or \( −4V \) at \( T_J = −40^\circ C \).
±5V ELECTRICAL CHARACTERISTICS (continued)
The following specifications apply for Supply Voltage = ±5V, \( V_{CM} = 0 \), \( R_L \geq 100 \, \text{k}\Omega \) and \( R_S = 50\, \Omega \), \( C_L \) Open, unless otherwise noted. **Boldface** limits apply for \( T_A = T_J = T_{\text{MIN}} \) to \( T_{\text{MAX}} \); all other limits \( T_A = T_J = 25^\circ \text{C} \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLVOS</td>
<td>Current Limit Input Offset Voltage</td>
<td>( R_L = 1 , \text{k}\Omega ), GND = 0V</td>
<td>2.7</td>
<td>2.7</td>
<td>±5.0</td>
<td>mV</td>
</tr>
<tr>
<td>CLIb</td>
<td>Current Limit Input Bias Current</td>
<td>( R_L = 1 , \text{k}\Omega ), ( C_L = 0V )</td>
<td>−0.5</td>
<td>−0.5</td>
<td>−0.2</td>
<td>μA</td>
</tr>
<tr>
<td>CLCMR</td>
<td>Current Limit Common Mode Rejection Ratio</td>
<td>( R_L = 1 , \text{k}\Omega ), GND = −3V to +4V</td>
<td>60</td>
<td>60</td>
<td>65</td>
<td>dB</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Overshoot vs. Capacitive Load

Small Signal Step Response

Figure 3.

Slew Rate

Small Signal Step Response

Figure 4.

Figure 5.

Input Offset Voltage of Amplifier vs. Supply Voltage

Figure 7.

Figure 8.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Small Signal Step Response

Figure 9.

Large Signal Step Response — Leading Edge

Figure 11.

Large Signal Step Response — Trailing Edge

Figure 13.

Small Signal Step Response

Figure 10.

Large Signal Step Response — Leading Edge

Figure 12.

Large Signal Step Response — Trailing Edge

Figure 14.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Large Signal Step Response

Figure 15.

Figure 16.

Figure 17.

Figure 18.

Harmonic Distortion with 50Ω Load

Figure 19.

Figure 20.

Harmonic Distortion with 100Ω Load

Copyright © 2006–2013, Texas Instruments Incorporated

Submit Documentation Feedback

Product Folder Links: LMH6321
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

**Figure 21.**
Harmonic Distortion with 50Ω Load

**Figure 22.**
Noise vs. Frequency

**Figure 23.**
Gain vs. Frequency

**Figure 24.**
Gain vs. Frequency

**Figure 25.**
Gain vs. Frequency

**Figure 26.**
Gain vs. Frequency

---

LMH6321

Submit Documentation Feedback
Copyright © 2006–2013, Texas Instruments Incorporated

Product Folder Links: LMH6321
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Output Short Circuit Current—Sinking vs. Program Current

\[ V_S = \pm 5V \]

\[ 25 \quad 125 \quad 225 \quad 325 \quad 425 \quad 525 \quad 625 \quad 725 \quad 825 \]

PROGRAM CURRENT (\( \mu A \))

\[ 0 \quad 100 \quad 200 \quad 300 \quad 400 \]

OUTPUT CURRENT (mA)

\[ V_S = \pm 15V \]

\[ 25 \quad 125 \quad 225 \quad 325 \quad 425 \quad 525 \quad 625 \quad 725 \quad 825 \]

PROGRAM CURRENT (\( \mu A \))

\[ 0 \quad 100 \quad 200 \quad 300 \quad 400 \]

OUTPUT CURRENT (mA)

\[ V_S = \pm 5V \]

\[ 125^\circ C \quad 85^\circ C \quad -40^\circ C \]

\[ V_S = \pm 15V \]

\[ 125^\circ C \quad 85^\circ C \quad -40^\circ C \]

\[ V_S = \pm 5V \]

\[ V_S = \pm 15V \]

\[ V_{IN} = V^+ \]

\[ C_L = OPEN \]

Figure 33.

Output Short Circuit Current—Sourcing vs. Program Current

\[ V_S = \pm 5V \]

\[ 25 \quad 125 \quad 225 \quad 325 \quad 425 \quad 525 \quad 625 \quad 725 \quad 825 \]

PROGRAM CURRENT (\( \mu A \))

\[ 0 \quad 100 \quad 200 \quad 300 \quad 400 \]

OUTPUT CURRENT (mA)

\[ V_S = \pm 15V \]

\[ 25 \quad 125 \quad 225 \quad 325 \quad 425 \quad 525 \quad 625 \quad 725 \quad 825 \]

PROGRAM CURRENT (\( \mu A \))

\[ 0 \quad 100 \quad 200 \quad 300 \quad 400 \]

OUTPUT CURRENT (mA)

\[ V_S = \pm 5V \]

\[ V_S = \pm 15V \]

\[ V_{IN} = V^+ \]

\[ C_L = OPEN \]

Figure 34.

Positive Output Swing vs. Sourcing Current

\[ 0 \quad 100 \quad 200 \quad 300 \quad 400 \quad 500 \]

SOURCING CURRENT (mA)

\[ 0 \quad 0.5 \quad 1 \quad 1.5 \quad 2 \quad 2.5 \quad 3 \quad 3.5 \quad 4 \]

OUTPUT SWING (V)

\[ V_S = \pm 5V \]

\[ V_{IN} = V^+ \]

\[ C_L = OPEN \]

Figure 36.

Negative Output Swing vs. Sinking Current

\[ -500 \quad -400 \quad -300 \quad -200 \quad -100 \quad 0 \]

SINKING CURRENT (mA)

\[ -0.5 \quad -1 \quad -1.5 \quad -2 \quad -2.5 \quad -3 \quad -3.5 \quad -4 \]

OUTPUT SWING (V)

\[ V_S = \pm 5V \]

\[ V_{IN} = V^- \]

\[ C_L = OPEN \]

Figure 37.

Positive Output Swing vs. Sourcing Current

\[ 0 \quad 100 \quad 200 \quad 300 \quad 400 \]

SOURCING CURRENT (mA)

\[ 9 \quad 10 \quad 11 \quad 12 \quad 13 \quad 14 \]

OUTPUT SWING (V)

\[ V_S = \pm 5V \]

\[ V_{IN} = V^- \]

\[ C_L = OPEN \]

Figure 38.
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Negative Output Swing

Output Short Circuit Current—Sourcing vs. Supply Voltage

Figure 39.

Figure 40.

Output Short Circuit Current—Sinking vs. Supply Voltage

Positive Output Swing

Negative Output Swing

Figure 41.

Figure 42.

Figure 43.

Figure 44.

Copyright © 2006–2013, Texas Instruments Incorporated
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Negative Output Swing vs. Supply Voltage

INPUT OFFSET VOLTAGE (mV)
-3 -2 -1 0 1 3
COMMON MODE VOLTAGE (V)
-2
-1
0
1
2
3
4
5
V S  = ±5V

25° C
85° C
-40° C
125° C

Input Offset Voltage of Amplifier vs. Supply Voltage

INPUT OFFSET VOLTAGE (mV)
-25
-15
-5
0
5
15
25
-15
-12
-9
-6
-3
0
3
6
9
12
15
COMMON MODE VOLTAGE (V)
-40° C
85° C
25° C
125° C

Input Offset Voltage of Amplifier vs. Common Mode Voltage

V S  = ±15V

INPUT OFFSET VOLTAGE (mV)
-25
-15
-5
0
5
15
25
-15
-12
-9
-6
-3
0
3
6
9
12
15
COMMON MODE VOLTAGE (V)
-40° C
85° C
25° C
125° C

Input Offset Voltage of V/I Section vs. Common Mode Voltage

V S  = ±15V

INPUT OFFSET VOLTAGE (mV)
-2
-1
0
1
2
3
4
5
-1
0
1
2
3
4
5
COMMON MODE VOLTAGE (V)
-40° C
85° C
25° C
125° C

Input Offset Voltage of V/I Section vs. Common Mode Voltage

V S  = ±15V

INPUT OFFSET VOLTAGE (mV)
-2
-1
0
1
2
3
4
5
-10
-8
-6
-4
-2
0
2
4
6
8
10
12
14
COMMON MODE VOLTAGE (V)
-40° C
85° C
25° C
125° C

Figure 45.

Figure 46.

Figure 47.

Figure 48.

Figure 49.

Figure 50.
APPLICATION HINTS

BUFFERS

Buffers are often called voltage followers because they have largely unity voltage gain, thus the name has generally come to mean a device that supplies current gain but no voltage gain. Buffers serve in applications requiring isolation of source and load, i.e., high input impedance, low output impedance (high output current drive). In addition, they offer gain flatness and wide bandwidth.

Most operational amplifiers, that meet the other given requirements in a particular application, can be configured as buffers, though they are generally more complex and are, by and large, not optimized for unity gain operation. The commercial buffer is a cost effective substitute for an op amp. Buffers serve several useful functions, either in tandem with op amps or in standalone applications. As mentioned, their primary function is to isolate a high impedance source from a low impedance load, since a high Z source can't supply the needed current to the load. For example, in the case where the signal source to an analog to digital converter is a sensor, it is recommended that the sensor be isolated from the A/D converter. The use of a buffer ensures a low output impedance and delivery of a stable output to the converter. In A/D converter applications buffers need to drive varying and complex reactive loads.

Buffers come in two flavors: Open Loop and Closed Loop. While sacrificing the precision of some DC characteristics, and generally displaying poorer gain linearity, open loop buffers offer lower cost and increased bandwidth, along with less phase shift and propagation delay than do closed loop buffers. The LMH6321 is of the open loop variety.

Figure 51 shows a simplified diagram of the LMH6321 topology, revealing the open loop complementary follower design approach. Figure 52 shows the LMH6321 in a typical application, in this case, a 50Ω coaxial cable driver.

SUPPLY BYPASSING

The method of supply bypassing is not critical for frequency stability of the buffer, and, for light loads, capacitor values in the neighborhood of 1 nF to 10 nF are adequate. However, under fast slewing and large loads, large transient currents are demanded of the power supplies, and when combined with any significant wiring inductance, these currents can produce voltage transients. For example, the LMH6321 can slew typically at 1000 V/µs. Therefore, under a 50Ω load condition the load can demand current at a rate, di/dt, of 20 A/µs. This current flowing in an inductance of 50 nH (approximately 1.5" of 22 gage wire) will produce a 1V transient. Thus, it is recommended that solid tantalum capacitors of 5 µF to 10 µF, in parallel with a ceramic 0.1 µF capacitor be added as close as possible to the device supply pins.
For values of capacitors in the 10 \( \mu \)F to 100 \( \mu \)F range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of their very low ESR (typically less than 10 M\( \Omega \)) and low ESL.

**LOAD IMPEDANCE**

The LMH6321 is stable under any capacitive load when driven by a 50\( \Omega \) source. As shown by Figure 3 in TYPICAL PERFORMANCE CHARACTERISTICS, worst case overshoot is for a purely capacitive load of about 1 nF. Shunting the load capacitance with a resistor will reduce the overshoot.

**SOURCE INDUCTANCE**

Like any high frequency buffer, the LMH6321 can oscillate with high values of source inductance. The worst case condition occurs with no input resistor, and a purely capacitive load of 50 pF, where up to 100 nH of source inductance can be tolerated. With a 50\( \Omega \) load, this goes up to 200 nH. However, a 100\( \Omega \) resistor placed in series with the buffer input will ensure stability with a source inductances up to 400 nH with any load.

**OVERVOLTAGE PROTECTION**

(Refer to the simplified schematic in Figure 51).

If the input-to-output differential voltage were allowed to exceed the Absolute Maximum Rating of 5V, an internal diode clamp would turn on and divert the current around the compound emitter followers of Q1/Q3 (D1 – D11 for positive input), or around Q2/Q4 (D2 – D12 for negative inputs). Without this clamp, the input transistors Q1 – Q4 would zener, thereby damaging the buffer.

To limit the current through this clamp, a series resistor should be added to the buffer input (see \( R_1 \) in Figure 52). Although the allowed current in the clamp can be as high as 5 mA, which would suggest a 2 k\( \Omega \) resistor from a 15V source, it is recommended that the current be limited to about 1 mA, hence the 10 k\( \Omega \) shown.

The reason for this larger resistor is explained in the following: One way that the input/output voltage differential can exceed the Abs Max value is under a short circuit condition to ground while driving the input with up to ±15V. However, in the LMH6321 the maximum output current is set by the programmable Current Limit pin (\( C_L \)). The value set by this pin is specified to be accurate to 5 mA ±5%. If the input/output differential exceeds 5V while the output is trying to supply the maximum set current to a shorted condition or to a very low resistance load, a portion of that current will flow through the clamp diodes, thus creating an error in the total load current. If the input resistor is too low, the error current can exceed the 5 mA ±5% budget.
BANDWIDTH AND STABILITY

As can be seen in the schematic of Figure 52, a small capacitor is inserted in parallel with the series input resistors. The reason for this is to compensate for the natural band-limiting effect of the 1st order filter formed by this resistor and the input capacitance of the buffer. With a typical $C_{IN}$ of 3.5 pF (Figure 52), a pole is created at

$$f_p^2 = \frac{1}{(2\pi R_1 C_{IN})} = 4.5 \text{ MHz}$$  \hspace{1cm} (1)

This will band-limit the buffer and produce further phase lag. If used in an op amp-loop application with an amplifier that has the same order of magnitude of unity gain crossing as $f_p^2$, this additional phase lag will produce oscillation.

The solution is to add a small feed-forward capacitor (phase lead) around the input resistor, as shown in Figure 52. The value of this capacitor is not critical but should be such that the time constant formed by it and the input resistor that it is in parallel with ($R_{IN}C_{IN}$) be at least five times the time constant of $R_{IN}C_{IN}$. Therefore,

$$C_1 = \frac{(5R_{IN}/R_1)(C_{IN})}{(5R_{IN}/R_1)(C_{IN})}$$  \hspace{1cm} (2)

from Electrical Characteristics, $R_{IN}$ is 250 kΩ.

In the case of the example in Figure 52, $R_{IN}C_{IN}$ produces a time-constant of 870 ns, so $C_1$ should be chosen to be a minimum of 4.4 µs, or 438 pF. The value of $C_1$ (1000 pF) shown in Figure 52 gives 10 µs.

OUTPUT CURRENT AND SHORT CIRCUIT PROTECTION

The LMH6321 is designed to deliver a maximum continuous output current of 300 mA. However, the maximum available current, set by internal circuitry, is about 700 mA at room temperature. The output current is programmable up to 300 mA by a single external resistor and voltage source.

The LMH6321 is not designed to safely output 700 mA continuously and should not be used this way. However, the available maximum continuous current will likely be limited by the particular application and by the package type chosen, which together set the thermal conditions for the buffer (see THERMAL MANAGEMENT) and could require less than 300 mA.

The programming of both the sourcing and sinking currents into the load is accomplished with a single resistor. Figure 53 shows a simplified diagram of the V to I converter and $I_{SC}$ protection circuitry that, together, perform this task.

Referring to Figure 53, the two simplified functional blocks, labeled V/I Converter and Short Circuit Protection, comprise the circuitry of the Current Limit Control.

The V/I converter consists of error amplifier A1 driving two PNP transistors in a Darlington configuration. The two input connections to this amplifier are $V_{CL}$ (inverting input) and GND (non-inverting input). If GND is connected to zero volts, then the high open loop gain of A1, as well as the feedback through the Darlington, will force $C_{L}$, and thus one end $R_{EXT}$ to be at zero volts also. Therefore, a voltage applied to the other end of $R_{EXT}$ will force a current

$$I_{EXT} = \frac{V_{PROG}}{R_{EXT}}$$  \hspace{1cm} (3)

into this pin. Via this pin, $I_{OUT}$ is programmable from 10 mA to 300 mA by setting $I_{EXT}$ from 25 µA to 750 µA by means of a fixed $R_{EXT}$ of 10 kΩ and making $V_{CL}$ variable from 0.25V to 7.5V. Thus, an input voltage $V_{CL}$ is converted to a current $I_{EXT}$. This current is the output from the V/I converter. It is gained up by a factor of two and sent to the Short Circuit Protection block as $I_{PROG}$. $I_{PROG}$ sets a voltage drop across $R_{SC}$ which is applied to the non-inverting input of error amp A2. The other input is across $R_{SENSE}$. The current through $R_{SENSE}$, and hence the voltage drop across it, is proportional to the load current, via the current sense transistor $Q_{SENSE}$. The output of A2 controls the drive ($I_{DRIVE}$) to the base of the NPN output transistor, Q3 which is, proportional to the amount and polarity of the voltage differential ($V_{DIFF}$) between AMP2 inputs, that is, how much the voltage across $R_{SENSE}$ is greater than or less than the voltage across $R_{SC}$. This loop gains $I_{EXT}$ up by another 200, thus

$$I_{SC} = 2 \times 200 (I_{EXT}) = 400 I_{EXT}$$  \hspace{1cm} (4)

Therefore, combining Equation 3 and Equation 4, and solving for $R_{EXT}$, we get

$$R_{EXT} = 400 \frac{V_{PROG}}{I_{SC}}$$  \hspace{1cm} (5)

If the $V_{CL}$ pin is left open, the output short circuit current will default to about 700 mA. At elevated temperatures this current will decrease.
Only the NPN output $I_{\text{SC}}$ protection is shown. Depending on the polarity of $V_{\text{DIFF}}$, AMP2 will turn $I_{\text{DRIVE}}$ either on or off.

Figure 53. Simplified Diagram of Current Limit Control

THERMAL MANAGEMENT

Heatsinking

For some applications, a heat sink may be required with the LMH6321. This depends on the maximum power dissipation and maximum ambient temperature of the application. To accomplish heat sinking, the tabs on DDPAK and SO PowerPAD package may be soldered to the copper plane of a PCB for heatsinking (note that these tabs are electrically connected to the most negative point in the circuit, i.e., $V^-$).

Heat escapes from the device in all directions, mainly through the mechanisms of convection to the air above it and conduction to the circuit board below it and then from the board to the air. Natural convection depends on the amount of surface area that is in contact with the air. If a conductive plate serving as a heatsink is thick enough to ensure perfect thermal conduction (heat spreading) into the far recesses of the plate, the temperature rise would be simply inversely proportional to the total exposed area. PCB copper planes are, in that sense, an aid to convection, the difference being that they are not thick enough to ensure perfect conduction. Therefore, eventually we will reach a point of diminishing returns (as seen in Figure 55). Very large increases in the copper area will produce smaller and smaller improvement in thermal resistance. This occurs, roughly, for a 1 inch square of 1 oz copper board. Some improvement continues until about 3 square inches, especially for 2 oz boards and better, but beyond that, external heatsinks are required. Ultimately, a reasonable practical value attainable for the junction to ambient thermal resistance is about 30 °C/W under zero air flow.

A copper plane of appropriate size may be placed directly beneath the tab or on the other side of the board. If the conductive plane is placed on the back side of the PCB, it is recommended that thermal vias be used per JEDEC Standard JESD51-5.
Determining Copper Area

One can determine the required copper area by following a few basic guidelines:

1. Determine the value of the circuit’s power dissipation, $P_D$.
2. Specify a maximum operating ambient temperature, $T_{A(MAX)}$. Note that when specifying this parameter, it must be kept in mind that, because of internal temperature rise due to power dissipation, the die temperature, $T_J$, will be higher than $T_A$ by an amount that is dependent on the thermal resistance from junction to ambient, $\theta_{JA}$. Therefore, $T_A$ must be specified such that $T_J$ does not exceed the absolute maximum die temperature of 150°C.
3. Specify a maximum allowable junction temperature, $T_{J(MAX)}$, which is the temperature of the chip at maximum operating current. Although no strict rules exist, typically one should design for a maximum continuous junction temperature of 100°C to 130°C, but no higher than 150°C which is the absolute maximum rating for the part.
4. Calculate the value of junction to ambient thermal resistance, $\theta_{JA}$.
5. Choose a copper area that will ensure the specified $T_{J(MAX)}$ for the calculated $\theta_{JA}$, $\theta_{JA}$ as a function of copper area in square inches is shown in Figure 54.

The maximum value of thermal resistance, junction to ambient $\theta_{JA}$, is defined as:

$$\theta_{JA} = (T_{J(MAX)} - T_{A(MAX)}) / P_{D(MAX)}$$

where

- $T_{J(MAX)}$ = the maximum recommended junction temperature
- $T_{A(MAX)}$ = the maximum ambient temperature in the user’s environment
- $P_{D(MAX)}$ = the maximum recommended power dissipation

**NOTE**

The allowable thermal resistance is determined by the maximum allowable heat rise, $T_{RISE} = T_{J(MAX)} - T_{A(MAX)} = (\theta_{JA}) (P_{D(MAX)})$. Thus, if ambient temperature extremes force $T_{RISE}$ to exceed the design maximum, the part must be de-rated by either decreasing $P_D$ to a safe level, reducing $\theta_{JA}$, further, or, if available, using a larger copper area.

**Procedure**

1. First determine the maximum power dissipated by the buffer, $P_{D(MAX)}$. For the simple case of the buffer driving a resistive load, and assuming equal supplies, $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = I_S (2V^*) + V^+2/4R_L$$

where

- $I_S$ = quiescent supply current

2. Determine the maximum allowable die temperature rise,

$$T_{R(MAX)} = T_{J(MAX)} - T_{A(MAX)} = P_{D(MAX)}\theta_{JA}$$

3. Using the calculated value of $T_{R(MAX)}$ and $P_{D(MAX)}$ the required value for junction to ambient thermal resistance can be found:

$$\theta_{JA} = T_{R(MAX)} / P_{D(MAX)}$$

4. Finally, using this value for $\theta_{JA}$ choose the minimum value of copper area from Figure 54.

**Example**

Assume the following conditions:

$V^+ = V^- = 15V$, $R_L = 50\Omega$, $I_S = 15$ mA $T_{J(MAX)} = 125^\circ C$, $T_{A(MAX)} = 85^\circ C$.

1. From Equation 7
   
   $P_{D(MAX)} = I_S (2V^*) + V^+2/4R_L = (15$ mA$)(30V) + 15V^2/200\Omega = 1.58W$

2. From Equation 8
   
   $T_{R(MAX)} = 125^\circ C - 85^\circ C = 40^\circ C$

3. From Equation 9
   
   $\theta_{JA} = 40^\circ C/1.58W = 25.3^\circ C/W$
Examining Figure 54, we see that we cannot attain this low of a thermal resistance for one layer of 1 oz copper. It will be necessary to derate the part by decreasing either the ambient temperature or the power dissipation. Other solutions are to use two layers of 1 oz foil, or use 2 oz copper (see Table 1), or to provide forced air flow. One should allow about an extra 15% heat sinking capability for safety margin.

Figure 54. Thermal Resistance (typ) for 7-L DDPAK Package Mounted on 1 oz. (0.036 mm) PC Board Foil

![Figure 54. Thermal Resistance (typ) for 7-L DDPAK Package Mounted on 1 oz. (0.036 mm) PC Board Foil](image)

Figure 55. Derating Curve for DDPAK package. No Air Flow

![Figure 55. Derating Curve for DDPAK package. No Air Flow](image)

Table 1. \( \theta_{JA} \) vs. Copper Area and \( P_D \) for DDPAK. 1.0 oz cu Board. No Air Flow. Ambient Temperature = 24°C

<table>
<thead>
<tr>
<th>Copper Area</th>
<th>( \theta_{JA} ) @ 1.0W (°C/W)</th>
<th>( \theta_{JA} ) @ 2.0W (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Layer = 1&quot;x2&quot; cu Bottom</td>
<td>62.4</td>
<td>54.7</td>
</tr>
<tr>
<td>2 Layer = 1&quot;x2&quot; cu Top &amp; Bottom</td>
<td>36.4</td>
<td>32.1</td>
</tr>
<tr>
<td>2 Layer = 2&quot;x2&quot; cu Top &amp; Bottom</td>
<td>23.5</td>
<td>22.0</td>
</tr>
<tr>
<td>2 Layer = 2&quot;x4&quot; cu Top &amp; Bottom</td>
<td>19.8</td>
<td>17.2</td>
</tr>
</tbody>
</table>
As seen in the previous example, buffer dissipation in DC circuit applications is easily computed. However, in AC circuits, signal wave shapes and the nature of the load (reactive, non-reactive) determine dissipation. Peak dissipation can be several times the average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

A selection of thermal data for the SO PowerPAD package is shown in Table 2. The table summarizes θ_{JA} for both 0.5 watts and 0.75 watts. Note that the thermal resistance, for both the DDPAK and the SO PowerPAD package is lower for the higher power dissipation levels. This phenomenon is a result of Newton's Law of Cooling. Restated in term of heatsink cooling, this principle says that the rate of cooling and hence the thermal conduction, is proportional to the temperature difference between the junction and the outside environment (ambient). This difference increases with increasing power levels, thereby producing higher die temperatures with more rapid cooling.

### Table 2. θ_{JA} vs. Copper Area and P_D for SO PowerPAD. 1.0 oz cu Board. No Airflow. Ambient Temperature = 22°C

<table>
<thead>
<tr>
<th>Copper Area/Vias</th>
<th>θ_{JA} @ 0.5W (°C/W)</th>
<th>θ_{JA} @ 0.75W (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Layer = 0.05 sq. in. (Bottom) + 3 Via Pads</td>
<td>141.4</td>
<td>138.2</td>
</tr>
<tr>
<td>1 Layer = 0.1 sq. in. (Bottom) + 3 Via Pads</td>
<td>134.4</td>
<td>131.2</td>
</tr>
<tr>
<td>1 Layer = 0.25 sq. in. (Bottom) + 3 Via Pads</td>
<td>115.4</td>
<td>113.9</td>
</tr>
<tr>
<td>1 Layer = 0.5 sq. in. (Bottom) + 3 Via Pads</td>
<td>105.4</td>
<td>104.7</td>
</tr>
<tr>
<td>1 Layer = 1.0 sq. in. (Bottom) + 3 Via Pads</td>
<td>100.5</td>
<td>100.2</td>
</tr>
<tr>
<td>2 Layer = 0.5 sq. in. (Top)/ 0.5 sq. in. (Bottom) + 33 Via Pads</td>
<td>93.7</td>
<td>92.5</td>
</tr>
<tr>
<td>2 Layer = 1.0 sq. in. (Top)/ 1.0 sq. in. (Bottom) + 53 Via Pads</td>
<td>82.7</td>
<td>82.2</td>
</tr>
</tbody>
</table>

**ERROR FLAG OPERATION**

The LMH6321 provides an open collector output at the EF pin that produces a low voltage when the Thermal Shutdown Protection is engaged, due to a fault condition. Under normal operation, the Error Flag pin is pulled up to V^+ by an external resistor. When a fault occurs, the EF pin drops to a low voltage and then returns to V^+ when the fault disappears. This voltage change can be used as a diagnostic signal to alert a microprocessor of a system fault condition. If the function is not used, the EF pin can be either tied to ground or left open. If this function is used, a 10 kΩ, or larger, pull-up resistor (R_2 in Figure 52) is recommended. The larger the resistor the lower the voltage will be at this pin under thermal shutdown. Table 3 shows some typical values of V_{EF} for 10 kΩ and 100 kΩ.

### Table 3. V_{EF} vs. R_2

<table>
<thead>
<tr>
<th>R_2 (in Figure 52)</th>
<th>@ V^+ = 5V</th>
<th>@ V^+ = 15V</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kΩ</td>
<td>0.24V</td>
<td>0.55V</td>
</tr>
<tr>
<td>100 kΩ</td>
<td>0.036V</td>
<td>0.072V</td>
</tr>
</tbody>
</table>

**SINGLE SUPPLY OPERATION**

If dual supplies are used, then the GND pin can be connected to a hard ground (0V) (as shown in Figure 52). However, if only a single supply is used, this pin must be set to a voltage of one V_{BE} (~0.7V) or greater, or more commonly, mid rail, by a stiff, low impedance source. This precludes applying a resistive voltage divider to the GND pin for this purpose. Figure 56 shows one way that this can be done.
Figure 56. Using an Op Amp to Bias the GND Pin to \( \frac{1}{2} V^+ \) for Single Supply Operation

In Figure 56, the op amp circuit pre-biases the GND pin of the buffer for single supply operation. The GND pin can be driven by an op amp configured as a constant voltage source, with the output voltage set by the resistor voltage divider, \( R_1 \) and \( R_2 \). It is recommended that these resistors be chosen so as to set the GND pin to \( V^+/2 \), for maximum common mode range.

SLEW RATE

Slew rate is the rate of change of output voltage for large-signal step input changes. For resistive load, slew rate is limited by internal circuit capacitance and operating current (in general, the higher the operating current for a given internal capacitance, the faster is the slew rate). Figure 57 shows the slew capabilities of the LMH6321 under large signal input conditions, using a resistive load.

![Figure 57. Slew Rate vs. Peak-to-Peak Input Voltage](image)

However, when driving capacitive loads, the slew rate may be limited by the available peak output current according to the following expression.

\[
\frac{dv}{dt} = \frac{I_{PK}}{C_L}
\]
and rapidly changing output voltages will require large output load currents. For example if the part is required to slew at 1000 V/μs with a load capacitance of 1 nF the current demand from the LMH6321 would be 1A. Therefore, fast slew rate is incompatible with large $C_L$. Also, since $C_L$ is in parallel with the load, the peak current available to the load decreases as $C_L$ increases.

Figure 58 illustrates the effect of the load capacitance on slew rate. Slew rate tests are specified for resistive loads and/or very small capacitive loads, otherwise the slew rate test would be a measure of the available output current. For the highest slew rate, it is obvious that stray load capacitance should be minimized. Peak output current should be kept below 500 mA. This translates to a maximum stray capacitance of 500 pF for a slew rate of 1000 V/μs.

Figure 58. Slew Rate vs. Load Capacitance
# REVISION HISTORY

## Changes from Revision B (March 2013) to Revision C

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>23</td>
</tr>
</tbody>
</table>
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PINS</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6321MR</td>
<td>NRND</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>95</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td>LMH6321MR</td>
<td></td>
</tr>
<tr>
<td>LMH6321MR/NOPB</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>95</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>LMH6321MR</td>
<td></td>
</tr>
<tr>
<td>LMH6321MRX/NOPB</td>
<td>ACTIVE</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 125</td>
<td>LMH6321MR</td>
<td></td>
</tr>
<tr>
<td>LMH6321TS</td>
<td>NRND</td>
<td>DDPACK/TO-263</td>
<td>KTW</td>
<td>7</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td>LMH6321TS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LMH6321TS/NOPB</td>
<td>ACTIVE</td>
<td>DDPACK/TO-263</td>
<td>KTW</td>
<td>7</td>
<td>45</td>
<td>Pb-Free (RoHS Exempt)</td>
<td>CU SN</td>
<td>Level-3-245C-168 HR</td>
<td>-40 to 125</td>
<td>LMH6321TS</td>
<td></td>
</tr>
<tr>
<td>LMH6321TSX/NOPB</td>
<td>ACTIVE</td>
<td>DDPACK/TO-263</td>
<td>KTW</td>
<td>7</td>
<td>500</td>
<td>Pb-Free (RoHS Exempt)</td>
<td>CU SN</td>
<td>Level-3-245C-168 HR</td>
<td>-40 to 125</td>
<td>LMH6321TS</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
TAPE AND REEL INFORMATION

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6321MRX/NOPB</td>
<td>SO Power PAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.5</td>
<td>5.4</td>
<td>2.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>LMH6321TSX/NOPB</td>
<td>DDPACK/TO-263</td>
<td>KTW</td>
<td>7</td>
<td>500</td>
<td>330.0</td>
<td>24.4</td>
<td>10.75</td>
<td>14.85</td>
<td>5.0</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
# TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMH6321MRX/NOPB</td>
<td>SO PowerPAD</td>
<td>DDA</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>LMH6321TSX/NOPB</td>
<td>DDAK/TO-263</td>
<td>KTW</td>
<td>7</td>
<td>500</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
</tbody>
</table>
Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designers are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY TECHNICAL, PROPRIETARY OR OTHER RIGHTS TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection. Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.