

LMK61E0M Ultra-Low Jitter Programmable Oscillator With Internal EEPROM

1 Features

- Ultra-Low Noise, High Performance
 - Jitter: 500-fs RMS Typical $f_{OUT} > 50$ MHz on LMK61E0M
- LMK61E0M Supports 3.3-V LVCMOS Output up to 200 MHz
- Total Frequency Tolerance of ± 25 ppm
- System Level Features
 - Glitch-Less Frequency Margining: Up to ± 1000 ppm From Nominal
 - Internal EEPROM: User Configurable Start-Up Settings
- Other Features
 - Device Control: Fast Mode I²C up to 1000 kHz
 - 3.3-V Operating Voltage
 - Industrial Temperature Range (-40°C to $+85^{\circ}\text{C}$)
 - 7-mm \times 5-mm 8-Pin Package
- Default Frequency: 70.656 MHz

2 Applications

- High-Performance Replacement for Crystal, SAW, or Silicon-Based Oscillators
- Switches, Routers, Network Line Cards, Base Band Units (BBU), Servers, Storage/SAN
- Test and Measurement
- Medical Imaging
- FPGA, Processor Attach
- xDSL, Broadcast Video

3 Description

The LMK61E0 family of ultra-low jitter PLLatinum™ programmable oscillators use fractional-N frequency synthesizers with integrated VCOs to generate commonly used reference clocks. The LMK61E0M supports 3.3-V LVCMOS outputs. The device features self start-up from on-chip EEPROM to generate a factory programmed default output frequency, or the device registers and EEPROM settings are fully programmable in-system through I²C serial interface. The device provides fine and coarse frequency margining control through I²C serial interface, making it a digitally-controlled oscillator (DCXO).

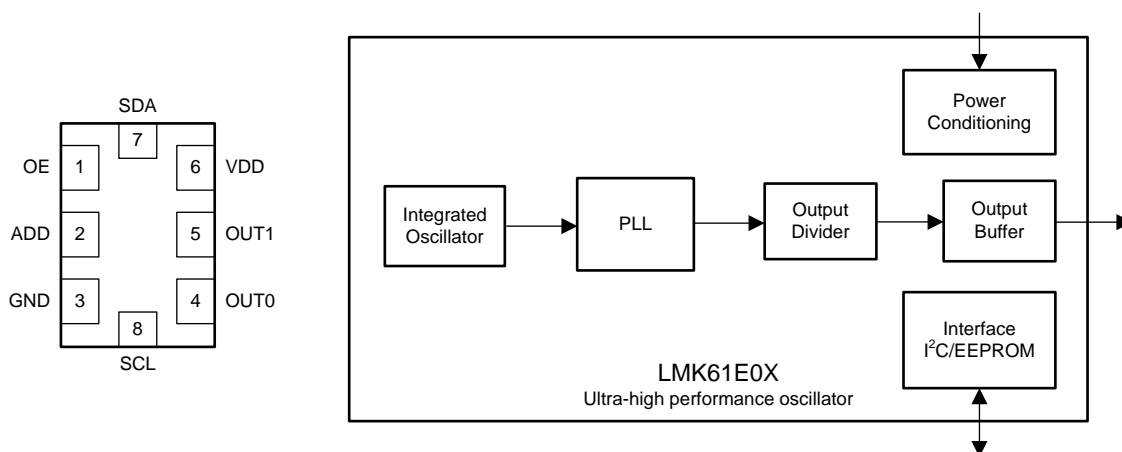
The PLL feedback divider can be updated to adjust the output frequency without spikes or glitches in steps of <1 ppb using a PFD of 12.5 MHz (R divider=4, doubler disabled) for compatibility with xDSL requirements, or in steps of <5.2 ppb using a PFD of 100 MHz (R divider=1, doubler enabled) for compatibility with broadcast video requirements. The frequency margining features also facilitate system design verification tests (DVT), such as standards compliance and system timing margin testing.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMK61E0M	QFM (8)	7.00 mm \times 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Pinout and Simplified Block Diagram



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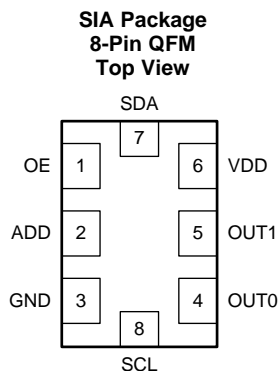
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4 Revision History

Changes from Original (January 2017) to Revision A	Page
• Updated data sheet text to the latest documentation and translations standards	1
• Corrected recommended junction temperature	4
• Corrected junction temperature	5
• Updated register names	20
• Typical application schematic added	35

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
POWER			
GND	3	Ground	Device Ground.
VDD	6	Power	3.3-V Power Supply.
OUTPUT BLOCK			
OUT0, OUT1	4, 5	Output	3.3-V LVCMOS Output Pair (Outputs can be individually set to same polarity, opposite polarity, or tri-state) in LMK61E0M. By default, OUT0 is enabled and OUT1 is disabled and set at high impedance on power-up.
DIGITAL CONTROL / INTERFACES			
ADD	2	LVCMOS	When left open, LSB of I ² C slave address is set to 01. When tied to VDD, LSB of I ² C slave address is set to 11. When tied to GND, LSB of I ² C slave address is set to 00.
OE	1	LVCMOS	Output Enable (internal pullup). In LMK61E0M, when set to low, output on OUT0 is disabled and set at high impedance.
SCL	8	LVCMOS	I ² C Serial Clock (open-drain). Requires an external pullup resistor to VDD.
SDA	7	LVCMOS	I ² C Serial Data (bi-directional, open-drain). Requires an external pullup resistor to VDD.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
VDD	Device supply voltage	-0.3	3.6	V
V _{IN}	Input voltage range for logic inputs	-0.3	VDD + 0.3	V
V _{OUT}	Output voltage range for clock outputs	-0.3	VDD + 0.3	V
T _J	Junction temperature		150	°C
T _{STG}	Storage temperature	-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	
		±2000	
		±500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device supply voltage	3.135	3.3	3.465	V
T _A	Ambient temperature	–40	25	85	°C
T _J	Junction temperature			115	°C
t _{RAMP}	VDD power-up ramp time	0.1		100	ms

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	LMK61E0 ^{(2) (3) (4)}			UNIT	
	SIA (QFM)				
	8 PINS				
	Airflow (LFM) 0	Airflow (LFM) 200	Airflow (LFM) 400		
R _{θJA}	Junction-to-ambient thermal resistance	54	44	41.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	34	n/a	n/a	°C/W
R _{θJB}	Junction-to-board thermal resistance	36.7	n/a	n/a	°C/W
ψ _{JT}	Junction-to-top characterization parameter	11.2	16.9	21.9	°C/W
ψ _{JB}	Junction-to-board characterization parameter	36.7	37.8	38.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) The package thermal resistance is calculated on a 4-layer JEDEC board.

(3) Connected to GND with 3 thermal vias (0.3-mm diameter).

(4) ψ_{JB} (junction-to-board) is used when the main heat flow is from the junction to the GND pad. See [Layout Guidelines](#) for more information on ensuring good system reliability and quality.

6.5 Electrical Characteristics - Power Supply⁽¹⁾

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD	Device current consumption LVCMOS		140	180	mA
IDD-PD	Device current consumption when output is disabled OE = GND		120		mA

(1) Refer to Parameter Measurement Information for relevant test conditions.

6.6 3.3-V LVCMOS Output Characteristics⁽¹⁾

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C, outputs loaded with 2 pF to GND

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT}	Output frequency Fast mode, R22[7:6] = 0x0	50		200	MHz
V _{OH}	Output high voltage I _{OH} = 1 mA	2.5			V
V _{OL}	Output low voltage I _{OL} = 1 mA			0.6	V
I _{OH}	Output high current		–33		mA
I _{OL}	Output low current		33		mA

(1) Refer to [Parameter Measurement Information](#) for relevant test conditions.

3.3-V LVCMOS Output Characteristics⁽¹⁾ (continued)

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C, outputs loaded with 2 pF to GND

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _R /t _F ⁽²⁾ Output rise/fall time	20% to 80%, R22[7:6] = 0x2		1.1		ns
	20% to 80%, R22[7:6] = 0x0		0.2		ns
PN-Floor Output phase noise floor (f _{OFFSET} > 10 MHz)	70.656 MHz		–150		dBc/Hz
ODC ⁽²⁾ Output duty cycle	Fast mode, R22[7:6] = 0x0	45%		55%	
R _{OUT} Output impedance			50		Ω

(2) Ensured by characterization.

6.7 OE Input Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH} Input high voltage		1.4			V
V _{IL} Input low voltage				0.6	V
I _{IH} Input high current	V _{IH} = VDD	–40		40	μA
I _{IL} Input low current	V _{IL} = GND	–40		40	μA
C _{IN} Input capacitance			2		pF

6.8 ADD Input Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH} Input high voltage		1.4			V
V _{IL} Input low voltage				0.4	V
I _{IH} Input high current	V _{IH} = VDD	–40		40	μA
I _{IL} Input low current	V _{IL} = GND	–40		40	μA
C _{IN} Input capacitance			2		pF

6.9 Frequency Tolerance Characteristics⁽¹⁾

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _T Total frequency tolerance	All frequency bands and device junction temperature up to 115°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow, and 5 year aging at 40°C ambient temperature	–25		25	ppm

(1) Ensured by characterization.

6.10 Frequency Margining Characteristics

VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _T Frequency margining range from nominal		–1000		1000	ppm

6.11 Power-On/Reset Characteristics (VDD)

 VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{THRESH}	Threshold voltage ⁽¹⁾	2.72		2.95	V
V _{DROOP}	Allowable voltage droop ⁽²⁾			0.1	V
t _{STARTUP}	Start-up time ⁽¹⁾	Time elapsed from VDD at 3.135 V to output enabled		10	ms
t _{OE-EN}	Output enable time ⁽²⁾	Time elapsed from OE at V _{IH} to output enabled		50	μs
t _{OE-DIS}	Output disable time ⁽²⁾	Time elapsed from OE at V _{IL} to output disabled		50	μs

(1) Ensured by characterization.

(2) Ensured by design.

6.12 I²C-Compatible Interface Characteristics (SDA, SCL)⁽¹⁾⁽²⁾

 VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	Input high voltage	1.2			V
V _{IL}	Input low voltage			0.6	V
I _{IH}	Input leakage	–40		40	μA
C _{IN}	Input capacitance		2		pF
C _{OUT}	Input capacitance			400	pF
V _{OL}	Output low voltage	I _{OL} = 3 mA		0.6	V
f _{SCL}	I ² C clock rate	100		1000	kHz
t _{SU_STA}	START condition setup time	SCL high before SDA low			μs
t _{H_STA}	START condition hold time	SCL low after SDA low			μs
t _{PH_SCL}	SCL pulse width high	0.6			μs
t _{PL_SCL}	SCL pulse width low	1.3			μs
t _{H_SDA}	SDA hold time	SDA valid after SCL low		0.9	μs
t _{SU_SDA}	SDA setup time	115			ns
t _{R_IN} / t _{F_IN}	SCL/SDA input rise and fall time			300	ns
t _{F_OUT}	SDA output fall time	C _{BUS} = 10 pF to 400 pF		250	ns
t _{SU_STOP}	STOP condition setup time	0.6			μs
t _{BUS}	Bus free time between STOP and START	1.3			μs

(1) Total capacitive load for each bus line ≤ 400 pF.

(2) Ensured by design.

6.13 Other Characteristics

 VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{VCO}	VCO frequency range	4.6		5.6	GHz

6.14 PLL Clock Output Jitter Characteristics⁽¹⁾⁽²⁾

 VDD = 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
RJ	RMS phase jitter ⁽³⁾ (12 kHz – 20 MHz)	f _{OUT} ≥ 50 MHz, Fractional-N PLL, LVCMOS output		500	1000	fs RMS

(1) Refer to Parameter Measurement Information for relevant test conditions.

(2) Phase jitter measured with Agilent E5052 signal source analyzer.

(3) Ensured by characterization.

6.15 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

6.16 Typical Characteristics

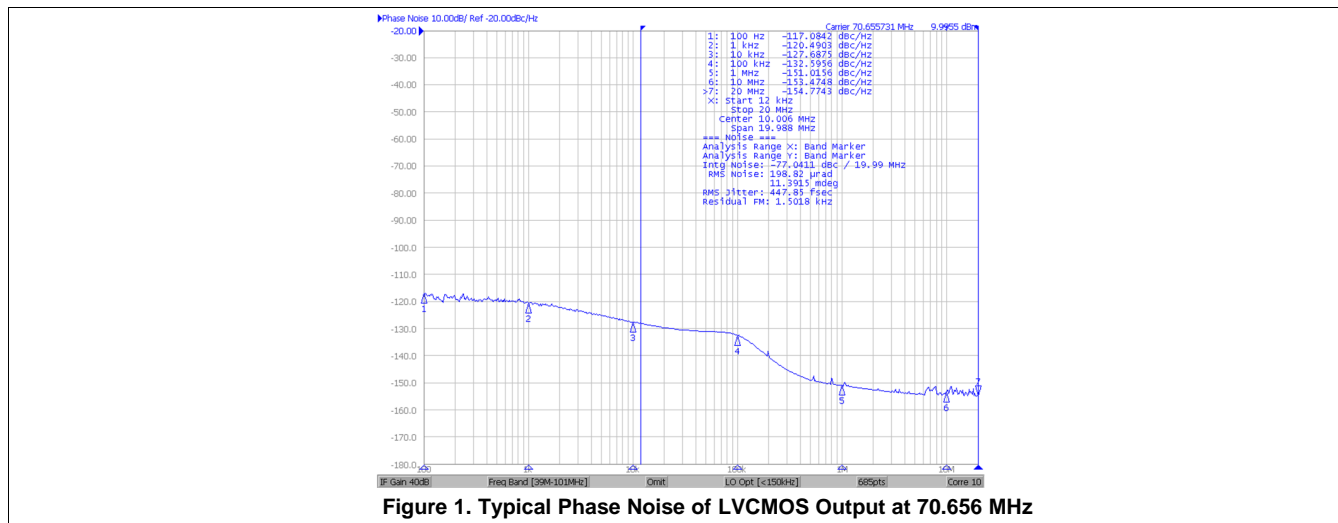
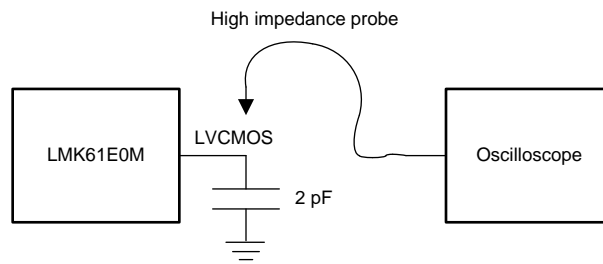


Figure 1. Typical Phase Noise of LVC MOS Output at 70.656 MHz

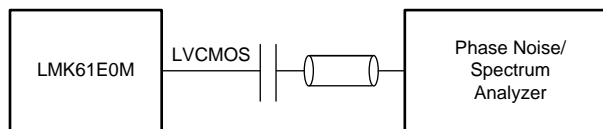
7 Parameter Measurement Information

7.1 Device Output Configurations



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Figure 2. LVC MOS Output DC Configuration During Device Test



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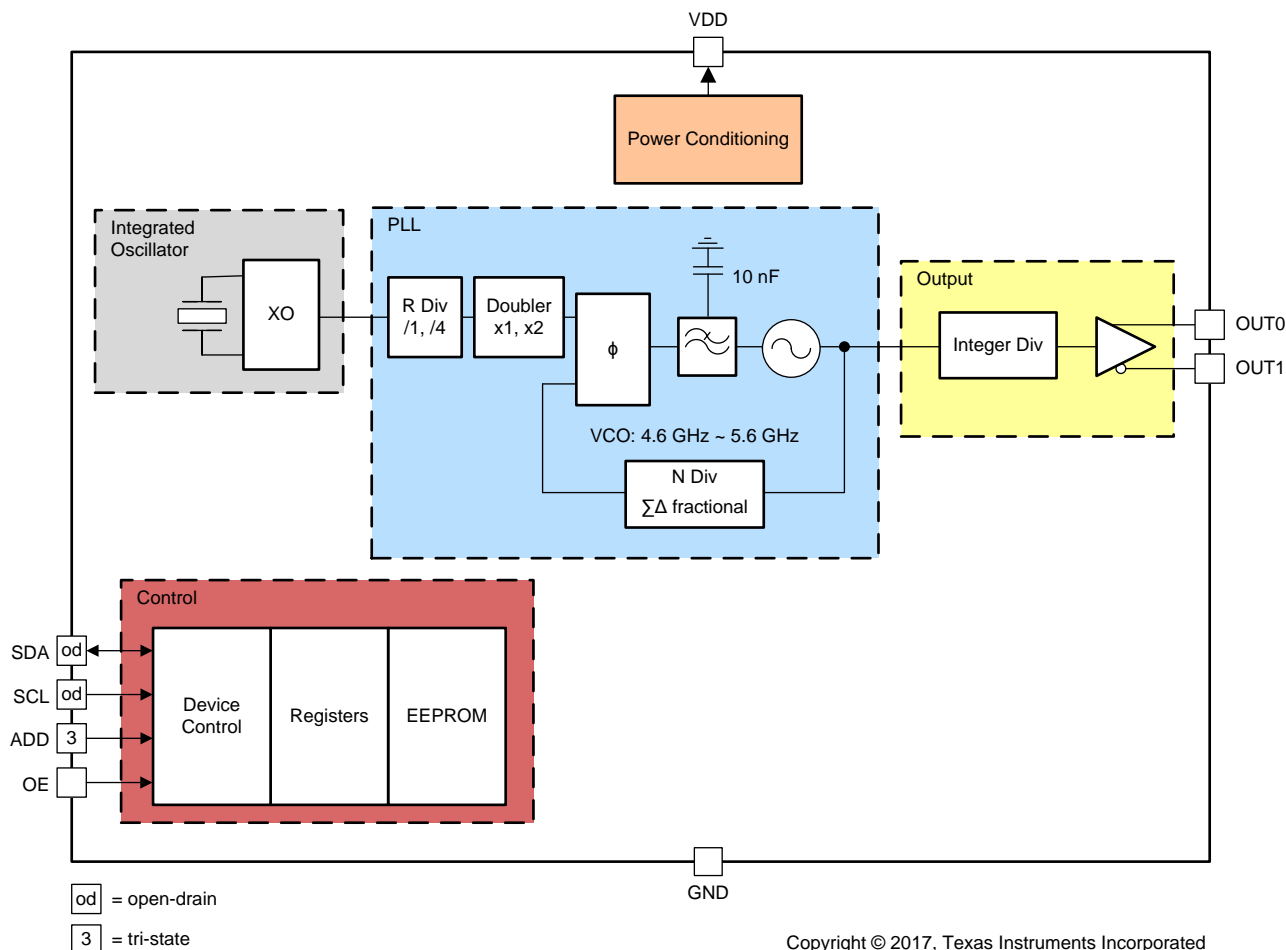
Figure 3. LVC MOS Output AC Configuration During Device Test

8 Detailed Description

8.1 Overview

The LMK61E0 is a programmable oscillator family that generates commonly used reference clocks. LMK61E0M supports 3.3-V LVCMOS outputs with less than 1000-fs RMS max jitter in integer PLL and fractional PLL modes.

8.2 Functional Block Diagram



NOTE

Control blocks are compatible with 1.8-V, 2.5-V, and 3.3-V I/O voltage levels.

8.3 Feature Description

8.3.1 Device Block-Level Description

The LMK61E0 is an integrated oscillator that includes a 50-MHz crystal and a fractional PLL with integrated VCO that supports a frequency range of 4.6 GHz to 5.6 GHz. The PLL block consists of a phase frequency detector (PFD), charge pump, integrated passive loop filter, a feedback divider that can support both integer and fractional values and a delta-sigma engine for noise suppression in fractional PLL mode. Completing the device is the combination of an integer output divider and an LVCMOS output buffer. The PLL is powered by on-chip low dropout (LDO) linear voltage regulators and the regulated supply network is partitioned such that the sensitive analog supplies are running from separate LDOs than the digital supplies which use their own LDO. The LDOs provide isolation to the PLL from any noise in the external power supply rail. The device supports fine and coarse frequency margining by changing the settings of the integrated oscillator and the output divider respectively.

Feature Description (continued)

8.3.2 Device Configuration Control

The LMK61E0 supports I²C programming interface where an I²C host can update any device configuration after the device enables the host interface and the host writes a sequence that updates the device registers. Once the device configuration is set, the host can also write to the on-chip EEPROM for a new set of power-up defaults based on the configuration pin settings in the soft pin configuration mode.

8.3.3 Register File Reference Convention

Figure 4 shows the method that this document employs to refer to an individual register bit or a grouping of register bits. If a drawing or text references an individual bit the format is to specify the register number first and the bit number second. The LMK61E0 contains 38 registers that are 8 bits wide. The register addresses and the bit positions both begin with the number zero (0). The bit address is placed in brackets or after a period. The first bit in the register file is address R0[0] or R0.0 meaning that it is located in Register 0 and is bit position 0. The last bit in the register file is address R72[7] or R72.7 referring to the 8th bit of register address 72 (the 73rd register in the device). Figure 4 also lists specific bit positions as a number contained within a box. A box with the register address encloses the group of boxes that represent the bits relevant to the specific device circuitry in context.

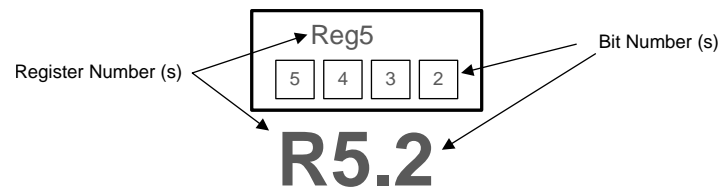


Figure 4. LMK61E0 Register Reference Format

8.3.4 Configuring the PLL

The PLL in LMK61E0 can be configured to accommodate various output frequencies either through I²C programming interface or, in the absence of programming the PLL defaults stored in EEPROM are loaded on power up. The PLL can be configured by setting the Reference Doubler, Integrated PLL Loop Filter, Feedback Divider, and Output Divider. The corresponding register addresses and configurations are detailed in the description section of each block below.

For the PLL to operate in closed-loop mode, the following condition in Equation 1 has to be met.

$$F_{VCO} = F_{REF} \times (D/R) \times [(INT + NUM/DEN)]$$

where

- F_{VCO}: PLL/VCO Frequency (4.6 GHz to 5.6 GHz)
- F_{REF}: 50-MHz reference input
- D: Reference input doubler, 1=Disabled, 2=Enabled
- R: Reference input divider, 1=Divider bypass, 4=Divide-by-4
- INT: PLL feedback divider integer value (12 bits, 1 to 4095)
- NUM: PLL feedback divider fractional numerator value (22 bits, 0 to 4194303)
- DEN: PLL feedback divider fractional denominator value (22 bits, 1 to 4194303)

On LMK61E0M, the output frequency is related to the VCO frequency as given in Equation 2.

$$F_{OUT} = F_{VCO} / (P \times OUTDIV)$$

where

- P: VCO post-divider value, selectable between 4 or 5
- OUTDIV: Output divider value (9 bits, 6 to 256)

The output frequency step size for every bit change in the numerator of the PLL fractional feedback divider is given in Equation 3.

$$STEPSIZE = (F_{REF} \times D) / (R \times P \times OUTDIV \times DEN)$$

Feature Description (continued)

8.3.5 Integrated Oscillator

The integrated oscillator in LMK61E0 features programmable load capacitances that can be set for the device to either operate at exactly its nominal oscillation frequency or operate at a fixed frequency offset from its nominal oscillation frequency. This is done by programming R16 and R17. More details on frequency margining are provided in [Fine Frequency Margining](#).

8.3.6 Reference Divider and Doubler

The reference path has a divider and frequency doubler. The reference divider can be bypassed by programming R24[0] = 0 or can be set to divide-by-4 by programming R24[0] = 1. Enabling the divider results in a lower comparison frequency for the PLL and would result in a 6-dB increase in the in-band phase noise at the output of the LMK61E0 but would result in a finer frequency resolution at the output for every bit change in the numerator of fractional feedback divider. The reference doubler can be enabled by programming R34[5] = 1. Bypassing the divider allows for a higher comparison rate and improved in-band phase noise at the output of the LMK61E0. Enabling the doubler allows a higher comparison frequency for the PLL and would result in a 3-dB reduction in the in-band phase noise at the output of the LMK61E0. Enabling the doubler also results in higher reference and phase detector spurs which will be minimized by enabling the higher order components (R3, C3) of the loop filter and programming them to appropriate values. Disabling the doubler would result in a finer frequency resolution at the output for every bit change in the numerator of the fractional feedback divider and higher in-band phase noise on the device output than when the doubler is enabled. However, the reference and phase detector spurs would be lower on the device output than when the doubler is enabled.

8.3.7 Phase Frequency Detector

The Phase Frequency Detector (PFD) of the PLL takes inputs from the reference path and the feedback divider output and produces an output that is dependent on the phase and frequency difference between the two inputs. The input frequency of the PFD is equal to the 50-MHz reference frequency doubled if the reference doubler is enabled and then divided by 4 if the reference divider is enabled. The feedback frequency to the PFD must equal the reference path frequency to the PFD for the PLL to lock.

8.3.8 Feedback Divider (N)

The N divider of the PLL includes fractional compensation and can achieve any fractional denominator (DEN) from 1 to 4,194,303. The integer portion, INT (valid range 1-4095), is the whole part of the N divider value and the fractional portion, NUM / DEN, is the remaining fraction. INT, NUM, and DEN are programmed in R25/R26, R27/R28/R29, and R30/R31/R32, respectively. The total programmed N divider value, N, is determined by: $N = INT + NUM / DEN$. The output of the N divider sets the PFD frequency to the PLL. The feedback frequency to the PFD must equal the reference path frequency to the PFD for the PLL to lock. In DCXO mode, the NUM registers can be reprogrammed MSB first and LSB last to update the output frequency without glitches or spikes.

8.3.9 Fractional Engine

The delta signal modulator is a key component of the fractional engine and is involved in noise shaping for better phase noise and spurs in the band of interest. The order of the delta sigma modulator is selectable between integer mode and third order for fractional PLL mode, and it can be programmed in R33[1:0]. Dithering can be programmed in R33[3:2] and should be disabled for integer PLL mode and set to weak for fractional PLL mode.

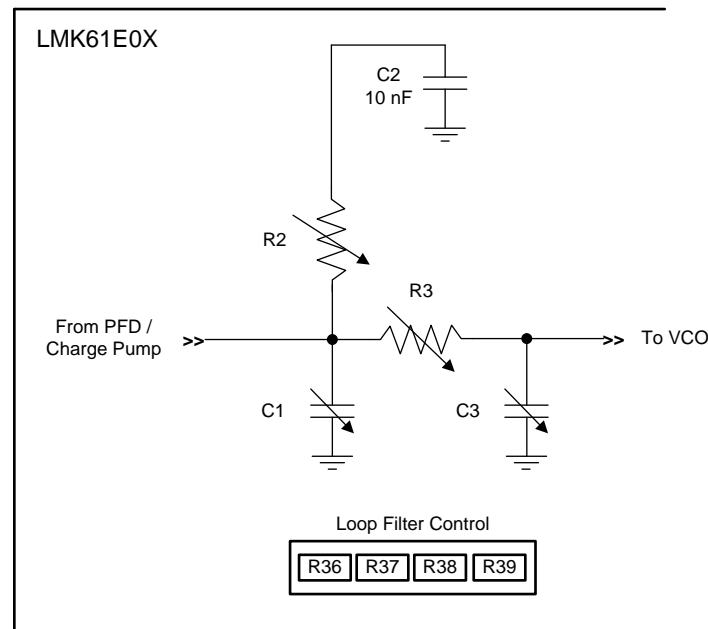
8.3.10 Charge Pump

The PLL has charge pump slices of 1.6 mA, to be used when PLL is set to fractional mode, or 6.4 mA, to be used when PLL is set to integer mode. These slices can be selected by programming R34[3:0]. When PLL is set to fractional mode, a phase shift needs to be introduced to maintain a linear response and ensure consistent performance across operating conditions and a value of 0x2 should be programmed in R35[6:4]. When PLL is set to integer mode, a value of 0x0 should be programmed in R35[6:4].

Feature Description (continued)

8.3.11 Loop Filter

The LMK61E0 features a fully integrated loop filter for the PLL and supports programmable loop bandwidth from 100 kHz to 1 MHz. The loop filter components, R2, C1, R3, C3, can be configured by programming R36, R37, R38 and R39 respectively. The LMK61E0 features a fixed value of C2 of 10 nF. When PLL is configured in the fractional mode, R35[2] should be set to 1. When reference doubler is disabled for integer mode PLL, R35[2] should be set to 0 and R38[6:0] should be set to 0x00. When reference doubler is enabled for integer mode PLL, R35[2] should be set to 1 and R38 and R39 are written with the appropriate values. Figure 5 shows the loop filter structure of the PLL. It is important to set the PLL to best possible bandwidth to minimize output jitter.



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Figure 5. Loop Filter Structure of PLL

8.3.12 VCO Calibration

The PLL in LMK61E0 is made of LC VCO that is designed using high-Q monolithic inductors to oscillate between 4.6 GHz and 5.6 GHz and has low phase noise characteristics. The VCO must be calibrated to ensure that the clock outputs deliver optimal phase noise performance. Fundamentally, a VCO calibration establishes an optimal operating point within the tuning range of the VCO. Setting R72[1] to 1 causes a VCO recalibration and is necessary after device reconfiguration. VCO calibration automatically occurs on device power up.

8.3.13 High-Speed Output Divider

LMK61E0M has two integer dividers in series in the output signal path. The VCO post-divider divides the VCO frequency by 4 or 5 and is programmed in R22[5]. The following high-speed output divider supports divide values of 6 to 256 and is programmed in R22 and R23. The output divider also supports coarse frequency margining that can initiate as low as a 5% change in the output frequency. To change the output divider, R23 needs to be programmed first and then R22. This is necessary for the CMOS divider to load the correct divide value.

8.3.14 High-Speed Clock Output

The clock outputs on LMK61E0M support 3.3-V LVCMOS levels. Both pins can be individually set to be the same polarity or opposite polarity of the other, or can be set to high impedance or tri-state. By default, OUT0 is enabled and OUT1 is tristate. OUT0 is controlled by R20[2] and OUT1 is controlled by R24[4]. The slew rate of the LVCMOS output can be set to fast or slow by programming R22[7:6] = 0x0 or 0x2.

Feature Description (continued)

8.3.15 Device Status

The PLL loss of lock and PLL calibration status can be monitored by reading R66[1:0]. These bits represent a logic-high interrupt output and are self-cleared once the readback is complete.

8.3.15.1 Loss of Lock

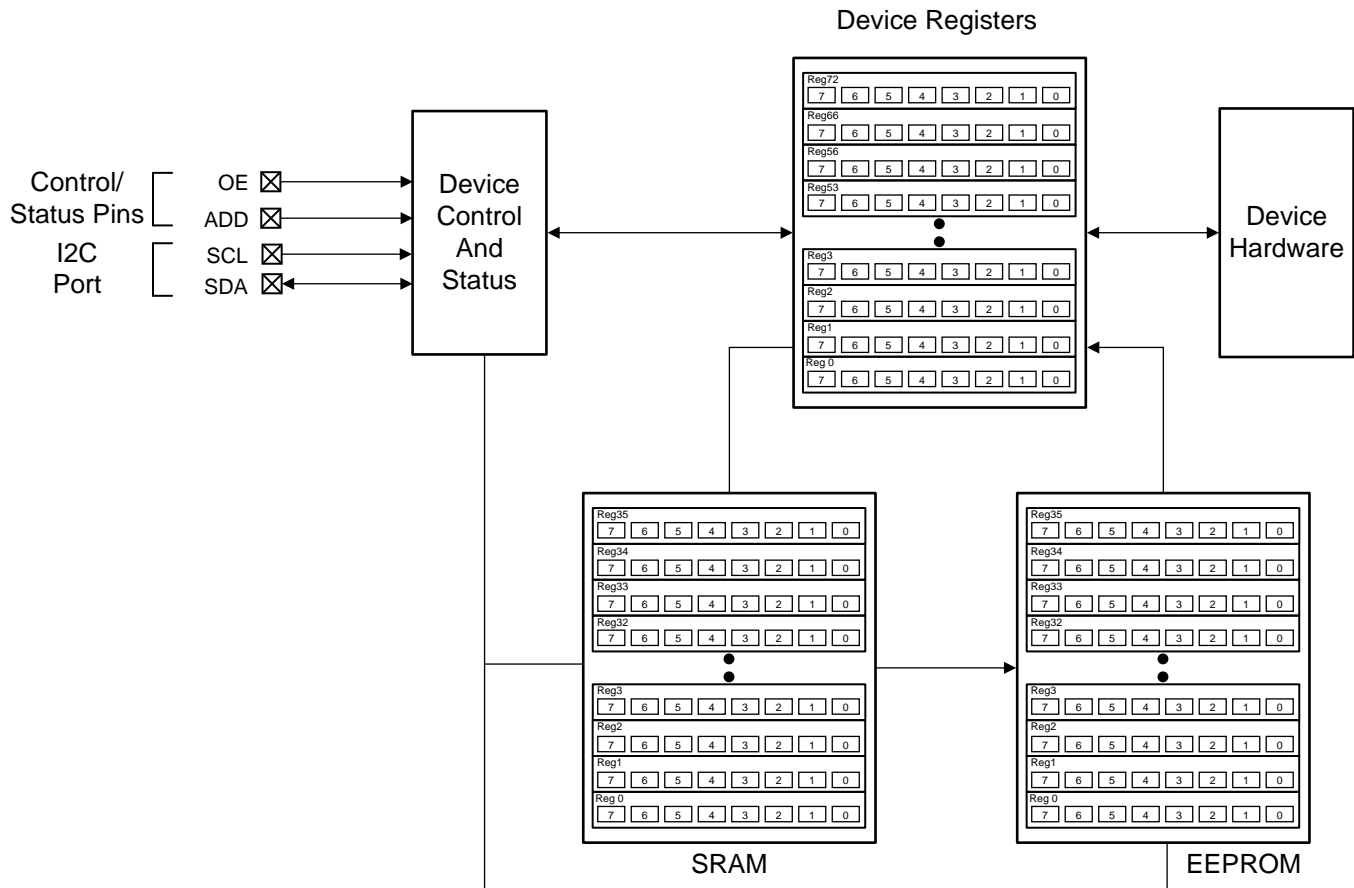
The PLL loss of lock detection circuit is a digital circuit that detects any frequency error, even a single cycle slip. Loss of lock may occur when an incorrect PLL configuration is programmed or the VCO has not been recalibrated.

8.4 Device Functional Modes

8.4.1 Interface and Control

The host (DSP, Microcontroller, FPGA, etc) configures and monitors the LMK61E0 through the I²C port. The host reads and writes to a collection of control and status bits called the register map. The device blocks can be controlled and monitored through a specific grouping of bits located within the register file. The host controls and monitors certain device Wide critical parameters directly through register control and status bits. In the absence of the host, the LMK61E0 can be configured to operate from its on-chip EEPROM. The EEPROM array is automatically copied to the device registers upon power up. The user has the flexibility to rewrite the contents of EEPROM from the SRAM up to 100 times.

Within the device registers, there are certain bits that have read or write access. Other bits are read-only (an attempt to write to a read-only bit will not change the state of the bit). Certain device registers and bits are reserved meaning that they must not be changed from their default reset state. [Figure 6](#) shows interface and control blocks within LMK61E0 and the arrows refer to read access from and write access to the different embedded memories (EEPROM, SRAM).

Device Functional Modes (continued)

Figure 6. LMK61E0 Interface and Control Block
8.4.2 DCXO Mode and Frequency Margining
8.4.2.1 DCXO Mode

In applications that require the LMK61E0 as part of a PLL that is implemented in another device like an FPGA, it can be used as a digitally controlled oscillator (DCXO) where the frequency control word can be passed along through I²C to the LMK61E0 on a regular basis which in turn updates the numerator of its fractional feedback divider by the required amount. In such a scenario, the entire portion of numerator for the fractional feedback divider must be written on every attempt MSB first and LSB last to ensure that the output frequency does not jump during the update, as described in [Feedback Divider \(N\)](#). In every update cycle, a total of 46 bits needs to be updated leading to a maximum update rate of 8.7 kHz with a maximum I²C rate of 1 Mbps. The minimum step size of 0.55 ppb (parts per billion) is achieved for the maximum VCO frequency of 5.6 GHz and when reference input doubler is disabled and reference divider is set to 4. The minimum step size of 4.96 ppb (parts per billion) is achieved for the maximum VCO frequency of 4.8 GHz and when reference input doubler is enabled and reference divider is bypassed.

Device Functional Modes (continued)

8.4.2.2 Fine Frequency Margining

IEEE802.3 dictates that Ethernet frames stay compliant to the standard specifications when clocked with a reference clock that is within ± 100 ppm of its nominal frequency. In the worst case, an RX node with its local reference clock at -100 ppm from its nominal frequency should be able to work seamlessly with a TX node that has its own local reference clock at $+100$ ppm from its nominal frequency. Without any clock compensation on the RX node, the read pointer will severely lag behind the write pointer and cause FIFO overflow errors. On the contrary, when the RX node's local clock operates at $+100$ ppm from its nominal frequency and the TX node's local clock operates at -100 ppm from its nominal frequency, FIFO underflow errors occur without any clock compensation.

To prevent such overflow and underflow errors from occurring, modern ASICs and FPGAs include a clock compensation scheme that introduces elastic buffers. Such a system, shown in Figure 7, is validated thoroughly during the validation phase by interfacing slower nodes with faster ones and ensuring compliance to IEEE802.3. The LMK61E0 provides the ability to fine tune the frequency of its outputs based on changing its load capacitance for the integrated oscillator. This fine tuning can be done through I²C as described in [Integrated Oscillator](#). The change in load capacitance is implemented in a manner such that the output of LMK61E0 undergoes a smooth monotonic change in frequency.

8.4.2.3 Coarse Frequency Margining

Certain systems require the processors to be tested at clock frequencies that are slower or faster by 5% or 10%. The LMK61E0 offers the ability to change its output divider for the desired change from its nominal output frequency as explained in [High-Speed Output Divider](#).

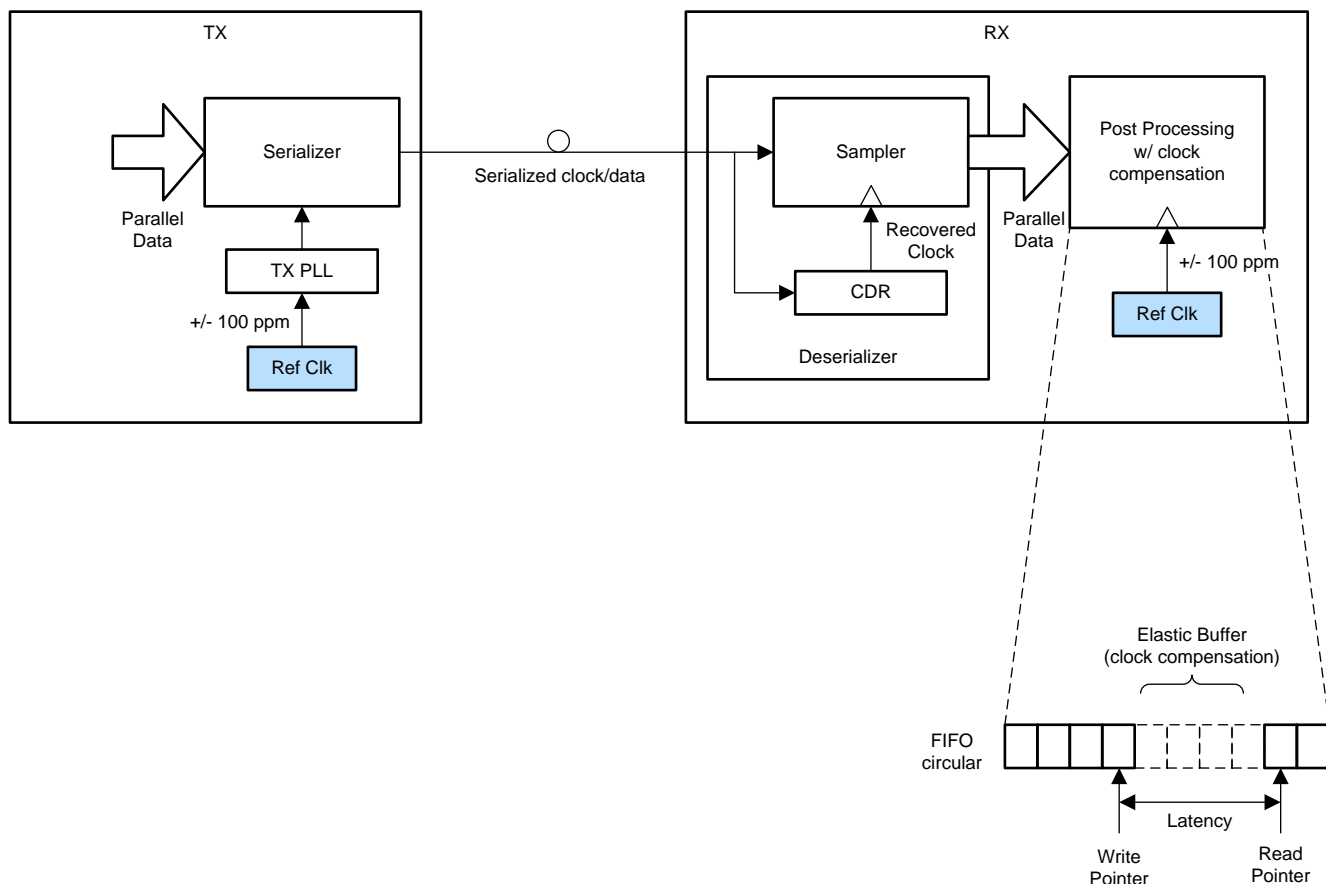


Figure 7. System Implementation With Clock Compensation for Standards Compliance

8.5 Programming

8.5.1 I²C Serial Interface

The I²C port on the LMK61E0 works as a slave device and supports both the 100-kHz standard mode and 1-MHz fast mode operations. Fast mode imposes a glitch tolerance requirement on the control signals. Therefore, the input receivers ignore pulses of less than 50-ns duration. The I²C timing is given in [I²C-Compatible Interface Characteristics \(SDA, SCL\)](#)⁽¹⁾⁽²⁾. The timing diagram is given in [Figure 8](#).

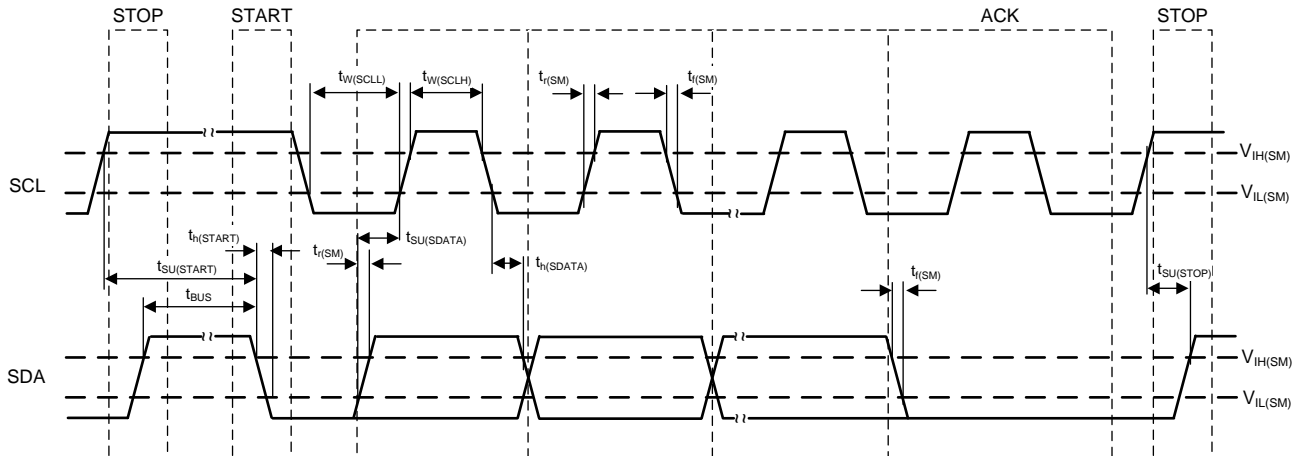


Figure 8. I²C Timing Diagram

In an I²C bus system, the LMK61E0 acts as a slave device and is connected to the serial bus (data bus SDA and lock bus SCL). These are accessed via a 7-bit slave address transmitted as part of an I²C packet. Only the device with a matching slave address responds to subsequent I²C commands. In soft pin mode, the LMK61E0 allows up to three unique slave devices to occupy the I²C bus based on the pin strapping of ADD (tied to VDD, GND or left open). The device slave address is 10110xx (the two LSBs are determined by the ADD pin).

During the data transfer through the I²C interface, one clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. The start data transfer condition is characterized by a high-to-low transition on the SDA line while SCL is high. The stop data transfer condition is characterized by a low-to-high transition on the SDA line while SCL is high. The start and stop conditions are always initiated by the master. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit and bytes are sent MSB first. The I²C register structure of the LMK61E0 is shown in [Figure 9](#).

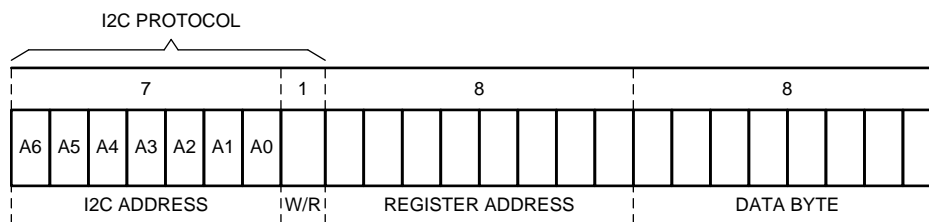


Figure 9. I²C Register Structure

The acknowledge bit (A) or non-acknowledge bit (A') is the 9th bit attached to any 8-bit data byte and is always generated by the receiver to inform the transmitter that the byte has been received (when A = 0) or not (when A' = 0). A = 0 is done by pulling the SDA line low during the 9th clock pulse and A' = 0 is done by leaving the SDA line high during the 9th clock pulse.

(1) Total capacitive load for each bus line ≤ 400 pF.

(2) Ensured by design.

Programming (continued)

The I²C master initiates the data transfer by asserting a start condition which initiates a response from all slave devices connected to the serial bus. Based on the 8-bit address byte sent by the master over the SDA line (consisting of the 7-bit slave address (MSB first) and an R/W' bit), the device whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data transfer with the master.

After the data transfer has occurred, stop conditions are established. In write mode, the master asserts a stop condition to end data transfer during the 10th clock pulse following the acknowledge bit for the last data byte from the slave. In read mode, the master receives the last data byte from the slave but does not pull SDA low during the 9th clock pulse. This is known as a non-acknowledge bit. By receiving the non-acknowledge bit, the slave knows the data transfer is finished and enters the idle mode. The master then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition. A generic transaction is shown in Figure 10.

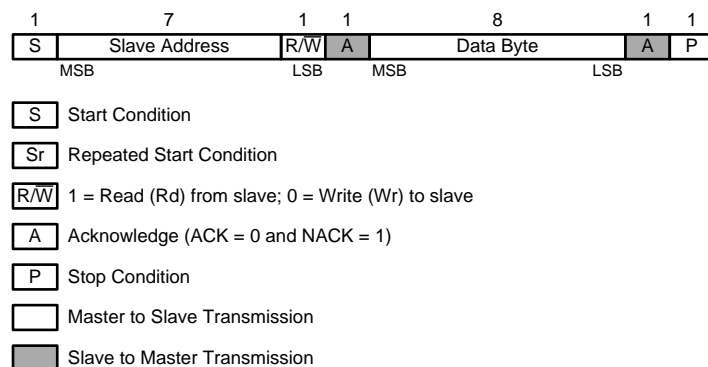


Figure 10. Generic Programming Sequence

The LMK61E0 I²C interface supports *Block Register Write/Read*, *Read/Write SRAM*, and *Read/Write EEPROM* operations. For *Block Register Write/Read* operations, the I²C master can individually access addressed registers that are made of an 8-bit data byte. The offset of the indexed register is encoded in the register address, as described in Table 1 below.

Table 1. Slave Address Byte

DEVICE	A6	A5	A4	A3	A2	ADD pin	R/W
LMK61E0	1	0	1	1	0	0x0, 0x1 or 0x3	1/0

8.5.2 Block Register Write

The I²C *Block Register Write* transaction is illustrated in Figure 11 and consists of the following sequence.

1. Master issues a Start Condition.
2. Master writes the 7-bit Slave Address following by a Write bit.
3. Master writes the 8-bit Register address as the CommandCode of the programming sequence.
4. Master writes one or more data bytes each of which should be acknowledged by the slave. The slave increments the internal register address after each byte.
5. Master issues a Stop Condition to terminate the transaction.

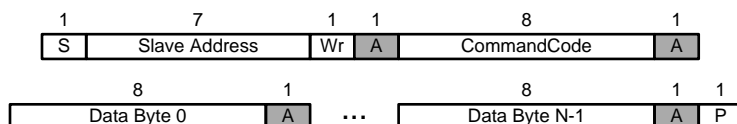


Figure 11. Block Register Write Programming Sequence

8.5.3 Block Register Read

The I²C *Block Register Read* transaction is illustrated in [Figure 12](#) and consists of the following sequence.

1. Master issues a Start Condition.
2. Master writes the 7-bit Slave Address followed by a Write bit.
3. Master writes the 8-bit Register address as the CommandCode of the programming sequence.
4. Master issues a Repeated Start Condition.
5. Master writes the 7-bit Slave Address following by a Read bit.
6. Slave returns one or more data bytes as long as the Master continues to acknowledge them. The slave increments the internal register address after each byte.
7. Master issues a Stop Condition to terminate the transaction.

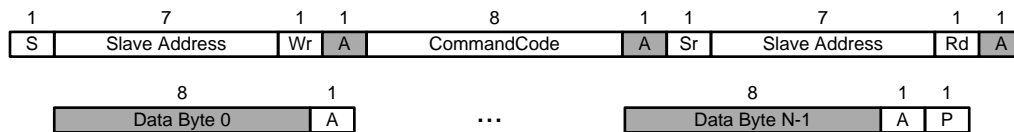


Figure 12. Block Register Read Programming Sequence

8.5.4 Write SRAM

The on-chip SRAM is a volatile, shadow memory array used to temporarily store register data, and is intended only for programming the non-volatile EEPROM. The SRAM has the identical data format as the EEPROM map. The register configuration data can be transferred to the SRAM array through special memory access registers in the register map. To successfully program the SRAM, the complete base array and at least one page should be written. The following details the programming sequence to transfer the device registers into the SRAM.

1. Program the device registers to match a desired setting.
2. Write a 1 to R49[6]. This ensures that the device registers are copied to the SRAM.

The SRAM can also be written with particular values according to the following programming sequence.

1. Write the SRAM address in R51.
2. Write the desired data byte in R53 in the same I²C transaction and this data byte will be written to the address specified in the step above. Any additional access that is part of the same transaction will cause the SRAM address to be incremented and a write will take place to the next SRAM address. Access to SRAM will terminate at the end of current I²C transaction.

NOTE

It is possible to increment SRAM address incorrectly when 2 successive accesses are made to R51.

8.5.5 Write EEPROM

The on-chip EEPROM is a non-volatile memory array used to permanently store register data for a custom device start-up configuration setting to initialize registers upon power up or POR. The EEPROM is comprised of bits shown in the EEPROM Map. The transfer must first happen to the SRAM and then to the EEPROM. During "EEPROM write", R49[2] is a 1 and the EEPROM contents cannot be accessed. The following details the programming sequence to transfer the entire contents of SRAM to EEPROM.

1. Make sure the "Write SRAM" procedure (Write SRAM) was done to commit the register settings to the SRAM with start-up configurations intended for programming to the EEPROM.
2. Write 0xBE to R56. This provides basic protection from inadvertent programming of EEPROM.
3. Write a 1 to R49[0]. This programs the entire SRAM contents to EEPROM. Once completed, the contents in R48 will increment by 1. R48 contains the total number of EEPROM programming cycles that are successfully completed.
4. Write 0x00 to R56 to protect against inadvertent programming of EEPROM.

8.5.6 Read SRAM

The contents of the SRAM can be read out, one word at a time, starting with that of the requested address. Following details the programming sequence for an SRAM read by address.

1. Write the SRAM address in R51.
2. The SRAM data located at the address specified in the step above can be obtained by reading R53 in the same I²C transaction. Any additional access that is part of the same transaction will cause the SRAM address to be incremented and a read will take place of the next SRAM address. Access to SRAM will terminate at the end of current I²C transaction.

NOTE

It is possible to increment SRAM address incorrectly when 2 successive accesses are made to R51.

8.5.7 Read EEPROM

The contents of the EEPROM can be read out, one word at a time, starting with that of the requested address. Following details the programming sequence for an EEPROM read by address.

1. Write the EEPROM address in R51.
2. The EEPROM data located at the address specified in the step above can be obtained by reading R52 in the same I²C transaction. Any additional access that is part of the same transaction will cause the EEPROM address to be incremented and a read will take place of the next EEPROM address. Access to EEPROM will terminate at the end of current I²C transaction.

NOTE

It is possible to increment EEPROM address incorrectly when 2 successive accesses are made to R51.

8.6 Register Maps

Any bit that is labeled as *RESERVED* should be written with a 0.

Table 2. EEPROM Map

BYTE NO.	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
3	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
4	NVMSCRC[7]	NVMSCRC[6]	NVMSCRC[5]	NVMSCRC[4]	NVMSCRC[3]	NVMSCRC[2]	NVMSCRC[1]	NVMSCRC[0]
5	NVMCNT[7]	NVMCNT[6]	NVMCNT[5]	NVMCNT[4]	NVMCNT[3]	NVMCNT[2]	NVMCNT[1]	NVMCNT[0]
6	1	RESERVED	RESERVED	RESERVED	RESERVED	1	RESERVED	RESERVED
7	RESERVED	RESERVED	1	RESERVED	RESERVED	RESERVED	RESERVED	1
8	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
9	SLAVEADR[7]	SLAVEADR[6]	SLAVEADR[5]	SLAVEADR[4]	SLAVEADR[3]	RESERVED	RESERVED	RESERVED
10	EEREV[7]	EEREV[6]	EEREV[5]	EEREV[4]	EEREV[3]	EEREV[2]	EEREV[1]	EEREV[0]
11	RESERVED	PLL_PDN	RESERVED	RESERVED	RESERVED	RESERVED	AUTOSTRT	RESERVED
14	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	1	RESERVED	1
15	RESERVED	XO_CAPCTRL[1]	XO_CAPCTRL[0]	XO_CAPCTRL[9]	XO_CAPCTRL[8]	XO_CAPCTRL[7]	XO_CAPCTRL[6]	XO_CAPCTRL[5]
16	XO_CAPCTRL[4]	XO_CAPCTRL[3]	XO_CAPCTRL[2]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
19	RESERVED	RESERVED	OUT0_HIZ	CMOS_MUTE	RESERVED	OUT1_INV	OUT0_INV	RESERVED
20	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
21	RESERVED	RESERVED	RESERVED	OUT1_HIZ	RESERVED	RESERVED	RESERVED	PLL_RDIV
22	PLL_NDIV[11]	PLL_NDIV[10]	PLL_NDIV[9]	PLL_NDIV[8]	PLL_NDIV[7]	PLL_NDIV[6]	PLL_NDIV[5]	PLL_NDIV[4]
23	PLL_NDIV[3]	PLL_NDIV[2]	PLL_NDIV[1]	PLL_NDIV[0]	PLL_NUM[21]	PLL_NUM[20]	PLL_NUM[19]	PLL_NUM[18]
24	PLL_NUM[17]	PLL_NUM[16]	PLL_NUM[15]	PLL_NUM[14]	PLL_NUM[13]	PLL_NUM[12]	PLL_NUM[11]	PLL_NUM[10]
25	PLL_NUM[9]	PLL_NUM[8]	PLL_NUM[7]	PLL_NUM[6]	PLL_NUM[5]	PLL_NUM[4]	PLL_NUM[3]	PLL_NUM[2]
26	PLL_NUM[1]	PLL_NUM[0]	PLL_DEN[21]	PLL_DEN[20]	PLL_DEN[19]	PLL_DEN[18]	PLL_DEN[17]	PLL_DEN[16]
27	PLL_DEN[15]	PLL_DEN[14]	PLL_DEN[13]	PLL_DEN[12]	PLL_DEN[11]	PLL_DEN[10]	PLL_DEN[9]	PLL_DEN[8]
28	PLL_DEN[7]	PLL_DEN[6]	PLL_DEN[5]	PLL_DEN[4]	PLL_DEN[3]	PLL_DEN[2]	PLL_DEN[1]	PLL_DEN[0]
29	PLL_DTHRMODE[1]	PLL_DTHRMODE[0]	PLL_ORDER[1]	PLL_ORDER[0]	RESERVED	RESERVED	PLL_D	PLL_CP[3]
30	PLL_CP[2]	PLL_CP[1]	PLL_CP[0]	PLL_CP_PHASE_SHIFT[2]	PLL_CP_PHASE_SHIFT[1]	PLL_CP_PHASE_SHIFT[0]	PLL_ENABLE_C3[2]	PLL_ENABLE_C3[1]
31	PLL_ENABLE_C3[0]	PLL_LF_R2[7]	PLL_LF_R2[6]	PLL_LF_R2[5]	PLL_LF_R2[4]	PLL_LF_R2[3]	PLL_LF_R2[2]	PLL_LF_R2[1]

Register Maps (continued)
Table 2. EEPROM Map (continued)

BYTE NO.	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
32	PLL_LF_R2[0]	PLL_LF_C1[2]	PLL_LF_C1[1]	PLL_LF_C1[0]	PLL_LF_R3[6]	PLL_LF_R3[5]	PLL_LF_R3[4]	PLL_LF_R3[3]
33	PLL_LF_R3[2]	PLL_LF_R3[1]	PLL_LF_R3[0]	PLL_LF_C3[2]	PLL_LF_C3[1]	PLL_LF_C3[0]	CMOS_SLEWRATE[1]	CMOS_SLEWRATE[0]
34	PRE_DIV	OUT_DIV[8]	OUT_DIV[7]	OUT_DIV[6]	OUT_DIV[5]	OUT_DIV[4]	OUT_DIV[3]	OUT_DIV[2]
35	OUT_DIV[1]	OUT_DIV[0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

The default/reset values for each register is specified for LMK61E0.

Table 3. Register Map

NAME	ADDR	RESET	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
VNDRID_BY1	0	0x10	VNDRID[15:8]								
VNDRID_BY0	1	0x0B	VNDRID[7:0]								
PRODID	2	0x33	PRODID[7:0]								
REVID	3	0x00	REVID[7:0]								
SLAVEADR	8	0xB0	SLAVEADR[7:1]							RESERVED	
EEREV	9	0x00	EEREV[7:0]								
DEV_CTL	10	0x01	RESERVED	PLL_PDN	RESERVED				ENCAL	AUTOSTRT	
XO_CAPCTRL_BY1	16	0x00	RESERVED							XO_CAPCTRL[1:0]	
XO_CAPCTRL_BY0	17	0x00	XO_CAPCTRL[9:2]								
CMOSCTL	20	0x00	RESERVED					OUT0_HIZ	CMOS_MUTE	RESERVED	
DIFFCTL	21	0x01	RESERVED		OUT1_INV	OUT0_INV	RESERVED				
OUTDIV_BY1	22	0x00	CMOS_SLEWRATE[1:0]		PRE_DIV	RESERVED			OUT_DIV[8]		
OUTDIV_BY0	23	0x20	OUT_DIV[7:0]								
RDIVCMOSCTL	24	0x00	RESERVED			OUT1_HIZ	RESERVED			PLL_RDIV	
PLL_NDIV_BY1	25	0x00	RESERVED				PLL_NDIV[11:8]				
PLL_NDIV_BY0	26	0x64	PLL_NDIV[7:0]								
PLL_FRACNUM_BY2	27	0x00	RESERVED		PLL_NUM[21:16]						
PLL_FRACNUM_BY1	28	0x00	PLL_NUM[15:8]								
PLL_FRACNUM_BY0	29	0x00	PLL_NUM[7:0]								
PLL_FRACDEN_BY2	30	0x00	RESERVED		PLL_DEN[21:16]						
PLL_FRACDEN_BY1	31	0x00	PLL_DEN[15:8]								
PLL_FRACDEN_BY0	32	0x00	PLL_DEN[7:0]								
PLL_MASHCTRL	33	0x0C	RESERVED				PLL_DTHRMODE[1:0]		PLL_ORDER[1:0]		
PLL_CTRL0	34	0x24	RESERVED		PLL_D	RESERVED	PLL_CP[3:0]				
PLL_CTRL1	35	0x03	RESERVED	PLL_CP_PHASE_SHIFT[2:0]			RESERVED	PLL_ENABLE_C3[2:0]			
PLL_LF_R2	36	0x28	PLL_LF_R2[7:0]								
PLL_LF_C1	37	0x00	RESERVED						PLL_LF_C1[2:0]		
PLL_LF_R3	38	0x00	RESERVED	PLL_LF_R3[6:0]							
PLL_LF_C3	39	0x00	RESERVED						PLL_LF_C3[2:0]		

Table 3. Register Map (continued)

NAME	ADDR	RESET	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	
PLL_CALCTRL	42	0x00	RESERVED				PLL_CLSDWAIT[1:0]	PLL_VCOWAIT[1:0]			
NVMSCRC	47	0x00	NVMSCRC[7:0]								
NVMCNT	48	0x00	NVMCNT[7:0]								
NVMCTL	49	0x10	RESERVED	REGCOMMIT	NVMCRCE RR	NVMAUTO CRC	NVMCOMMIT	NVMBUSY	NVMERASE	NVMPROG	
NVMLCRC	50	0x00	NVMLCRC[7:0]								
MEMADR	51	0x00	RESERVED	MEMADR[6:0]							
NVMDAT	52	0x00	NVMDAT[7:0]								
RAMDAT	53	0x00	RAMDAT[7:0]								
NVMUNLK	56	0x00	NVMUNLK[7:0]								
INT_LIVE	66	0x00	RESERVED						LOL	CAL	
SWRST	72	0x00	RESERVED						SWR2PLL	RESERVED	

8.6.1 Register Descriptions

8.6.1.1 VNDRID_BY1 Register; R0

VNDRID_BY1 and VNDRID_BY0 registers are used to store the unique 16-bit Vendor Identification number assigned to I²C vendors.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	VNDRID[15:8]	R	0x10	N	Vendor Identification Number Byte 1.

8.6.1.2 VNDRID_BY0 Register; R1

VNDRID_BY1 and VNDRID_BY0 registers are used to store the unique 16-bit Vendor Identification number assigned to I²C vendors.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	VNDRID[7:0]	R	0x0B	N	Vendor Identification Number Byte 0.

8.6.1.3 PRODID Register; R2

The Product Identification Number is a unique 8-bit identification number used to identify the LMK61E0.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	PRODID[7:0]	R	0x33	N	Product Identification Number.

8.6.1.4 REVID Register; R3

The REVID register is used to identify the LMK61E0 mask revision.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	REVID[7:0]	R	0x00	N	Device Revision Number. The Device Revision Number is used to identify the LMK61E0 mask-set revision used to fabricate this device.

8.6.1.5 SLAVEADR Register; R8

The SLAVEADR register reflects the 7-bit I²C Slave Address value initialized from from on-chip EEPROM.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION	
[7:1]	SLAVEADR[7:1]	R	0x58	Y	I ² C Slave Address. This field holds the 7-bit Slave Address used to identify this device during I ² C transactions. The two least significant bits of the address can be configured using ADD pin as shown.	
					SLAVEADR[2:1]	ADD pin
					0 (0x0)	0
					1 (0x1)	Float
					3 (0x3)	1
[0]	RESERVED	-	-	N	Reserved.	

8.6.1.6 EEREV Register; R9

The EEREV register provides an EEPROM image revision record. EEPROM Image Revision is automatically retrieved from EEPROM and stored in the EEREV register after a reset or after a EEPROM commit operation.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	EEREV[7:0]	R	0x00	Y	EEPROM Image Revision ID

8.6.1.7 DEV_CTL Register; R10

The DEV_CTL register holds the control functions described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION						
[7]	RESERVED	-	0	Y	Reserved.						
[6]	PLL_PDN	RW	0	Y	PLL Powerdown. The PLL_PDN bit determines whether PLL is automatically enabled and calibrated after a hardware reset. If the PLL_PDN bit is set to 1 during normal operation then PLL is disabled and the calibration circuit is reset. When PLL_PDN is then cleared to 0 PLL is re-enabled and the calibration sequence is automatically restarted. <table border="1" data-bbox="922 772 1479 877"> <thead> <tr> <th>PLL_PDN</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>PLL Enabled</td> </tr> <tr> <td>1</td> <td>PLL Disabled</td> </tr> </tbody> </table>	PLL_PDN	Value	0	PLL Enabled	1	PLL Disabled
PLL_PDN	Value										
0	PLL Enabled										
1	PLL Disabled										
[5]	CMOS_SEL	RW	1	Y	Set to 1 for LMK61E0M.						
[4:2]	RESERVED[5:2]	RW	0	Y	Reserved.						
[1]	ENCAL	RWSC	0	N	Enable Frequency Calibration. Triggers PLL/VCO calibration on both PLLs in parallel on 0 → 1 transition of ENCAL. This bit is self-clearing and set to a 0 after PLL/VCO calibration is complete. In powerup or software rest mode, AUTOSTRT takes precedence.						
[0]	AUTOSTRT	RW	1	Y	Autostart. If AUTOSTRT is set to 1 the device will automatically attempt to achieve lock and enable outputs after a device reset. A device reset can be triggered by the power-on-reset, RESETh pin or by writing to the RESETh_SW bit. If AUTOSTRT is 0 then the device will halt after the configuration phase, a subsequent write to set the AUTOSTRT bit to 1 will trigger the PLL Lock sequence.						

8.6.1.8 XO_CAPCTRL_BY1 Register; R16

XO Margining Offset Value bits[9:8]

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:2]	RESERVED[5:0]	-	-	N	Reserved.
[1:0]	XO_CAPCTRL [1:0]	RW	0x0	Y	XO Offset Value bits [1:0]

8.6.1.9 XO_CAPCTRL_BY0 Register; R17

XO Margining Offset Value bits[7:0]

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	XO_CAPCTRL [9:2]	RW	0x80	Y	XO Offset Value bits[9:2]

8.6.1.10 CMOSCTL Register; R20

The CMOSCTL register provides control over Output for LMK61E0M.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:3]	RESERVED	-	-	N	Reserved.
[2]	OUT0_HIZ	RW	0	Y	Controls OUT0 in LMK61E0M. When set to 1, the output is tri-stated with high impedance. When set to 0, the output is in normal operation.
[1]	CMOS_MUTE	RW	0	Y	Output channel mute in LMK61E0M.
[0]	RESERVED	-	-	N	Reserved.

8.6.1.11 DIFFCTL Register; R21

LVC MOS channel inversion is controlled by the OUT0_INV and OUT1_INV registers.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:6]	RESERVED	-	-	N	Reserved.
[5]	OUT1_INV	RW	0	Y	Inversion for CMOS output channel 1.
[4]	OUT0_INV	RW	0	Y	Inversion for CMOS output channel 0.
[3:0]	RESERVED	-	-	N	Reserved.

8.6.1.12 OUTDIV_BY1 Register; R22

The 9-bit output integer divider value is set by the OUTDIV_BY1 and OUTDIV_BY0 registers.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION												
[7:6]	CMOS_SLEWRATE[1:0]	RW	0x0	Y	Sets LVCMOS output slew rate in LMK61E0M. 0x0 sets to fast mode and 0x2 sets to slow mode.												
[5]	PRE_DIV	RW	0	Y	Sets LVCMOS output pre-divider in LMK61E0M. 0 sets to divide-by-4 and 1 sets to divide-by-5.												
[4:1]	RESERVED	RW	0x0	Y	Reserved.												
[0]	OUT_DIV[8]	RW	0	Y	Channel's Output Divider Byte 1 (Bit 8). The Channel Divider, OUT_DIV, is a 9-bit divider. The valid register values range from 5-255, which correspond with divide ratios of 6-256. To change the output divider, R23 needs to be programmed first and then R22. This is necessary for the CMOS divider to load the correct divide value.												
					<table border="1"> <thead> <tr> <th>OUT_DIV</th> <th>DIVIDE RATIO</th> </tr> </thead> <tbody> <tr> <td>0-4</td> <td>RESERVED</td> </tr> <tr> <td>5 (0x006)</td> <td>6</td> </tr> <tr> <td>6 (0x007)</td> <td>7</td> </tr> <tr> <td>254 (0x0FF)</td> <td>255</td> </tr> <tr> <td>255 (0x100)</td> <td>256</td> </tr> </tbody> </table>	OUT_DIV	DIVIDE RATIO	0-4	RESERVED	5 (0x006)	6	6 (0x007)	7	254 (0x0FF)	255	255 (0x100)	256
OUT_DIV	DIVIDE RATIO																
0-4	RESERVED																
5 (0x006)	6																
6 (0x007)	7																
254 (0x0FF)	255																
255 (0x100)	256																

8.6.1.13 OUTDIV_BY0 Register; R23

The 9-bit output integer divider value is set by the OUTDIV_BY1 and OUTDIV_BY0 registers.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	OUT_DIV[7:0]	RW	0x20	Y	Channel's Output Divider Byte 0 (Bits 7-0). To change the output divider, R23 needs to be programmed first and then R22. This is necessary for the CMOS divider to load the correct divide value.

8.6.1.14 RDIVCMOSCTL Register; R24

Sets R divider and CMOS OUT1 control for LMK61E0M.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:5]	RESERVED	-	-	N	Reserved.
[4]	OUT1_HIZ	RW	1	Y	Controls OUT1 in LMK61E0M. When set to 1, the output is tri-stated with high impedance. When set to 0, the output is in normal operation.
[3:1]	RESERVED	-	-	N	Reserved.
[0]	PLL_RDIV	RW	0	Y	On LMK61E0M, R divider is set to divide-by-4 when set to 1 and R divider is bypassed when set to 0.

8.6.1.15 PLL_NDIV_BY1 Register; R25

The 12-bit N integer divider value for PLL is set by the PLL_NDIV_BY1 and PLL_NDIV_BY0 registers.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:4]	RESERVED	-	-	N	Reserved.
[3:0]	PLL_NDIV[11:8]	RW	0x0	Y	PLL N Divider Byte 1. PLL Integer N Divider bits [11:8].

8.6.1.16 PLL_NDIV_BY0 Register; R26

The PLL_NDIV_BY0 register is described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	PLL_NDIV[7:0]	RW	0x32	Y	PLL N Divider Byte 0. PLL Integer N Divider bits [7:0].

8.6.1.17 PLL_FRACNUM_BY2 Register; R27

The 22-bit Fractional Divider Numerator value for PLL is set by registers PLL_FRACNUM_BY2, PLL_FRACNUM_BY1 and PLL_FRACNUM_BY0.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:6]	RESERVED	-	-	N	Reserved.
[5:0]	PLL_NUM[21:16]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 2. Bits [21:16]

8.6.1.18 PLL_FRACNUM_BY1 Register; R28

The PLL_FRACNUM_BY1 register is described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	PLL_NUM[15:8]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 1. Bits [15:8].

8.6.1.19 PLL_FRACNUM_BY0 Register; R29

The PLL_FRACNUM_BY0 register is described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	PLL_NUM[7:0]	RW	0x00	Y	PLL Fractional Divider Numerator Byte 0. Bits [7:0]. When using DCXO mode, the fractional numerator bits in R27, R28, and R29 should be written in that order (MSB first and LSB last) to avoid intermediate frequency jumps.

8.6.1.20 PLL_FRACDEN_BY2 Register; R30

The 22-bit Fractional Divider Denominator value for PLL is set by registers PLL_FRACDEN_BY2, PLL_FRACDEN_BY1 and PLL_FRACDEN_BY0.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:6]	RESERVED	-	-	N	Reserved.
[5:0]	PLL_DEN[21:16]	RW	0x00	Y	PLL Fractional Divider Denominator Byte 2. Bits [21:16].

8.6.1.21 PLL_FRACDEN_BY1 Register; R31

The PLL_FRACDEN_BY1 register is described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	PLL_DEN[15:8]	RW	0x00	Y	PLL Fractional Divider Denominator Byte 1. Bits [15:8].

8.6.1.22 PLL_FRACDEN_BY0 Register; R32

The PLL_FRACDEN_BY0 register is described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	PLL_DEN[7:0]	RW	0x00	Y	PLL Fractional Divider Denominator Byte 0. Bits [7:0].

8.6.1.23 PLL_MASHCTRL Register; R33

The PLL_MASHCTRL register provides control of the fractional divider for PLL.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION										
[7:4]	RESERVED	-	-	N	Reserved.										
[3:2]	PLL_DTHRMODE[1:0]	RW	0x3	Y	Mash Engine dither mode control. <table border="1" data-bbox="906 604 1479 779"> <thead> <tr> <th>DITHERMODE</th> <th>Dither Configuration</th> </tr> </thead> <tbody> <tr> <td>0 (0x0)</td> <td>Weak</td> </tr> <tr> <td>1 (0x1)</td> <td>Reserved</td> </tr> <tr> <td>2 (0x2)</td> <td>Reserved</td> </tr> <tr> <td>3 (0x3)</td> <td>Dither Disabled</td> </tr> </tbody> </table>	DITHERMODE	Dither Configuration	0 (0x0)	Weak	1 (0x1)	Reserved	2 (0x2)	Reserved	3 (0x3)	Dither Disabled
DITHERMODE	Dither Configuration														
0 (0x0)	Weak														
1 (0x1)	Reserved														
2 (0x2)	Reserved														
3 (0x3)	Dither Disabled														
[1:0]	PLL_ORDER[1:0]	RW	0x0	Y	Mash Engine Order. <table border="1" data-bbox="906 814 1479 984"> <thead> <tr> <th>ORDER</th> <th>Order Configuration</th> </tr> </thead> <tbody> <tr> <td>0 (0x0)</td> <td>Integer Mode Divider</td> </tr> <tr> <td>1 (0x1)</td> <td>Reserved</td> </tr> <tr> <td>2 (0x2)</td> <td>Reserved</td> </tr> <tr> <td>3 (0x3)</td> <td>3rd order</td> </tr> </tbody> </table>	ORDER	Order Configuration	0 (0x0)	Integer Mode Divider	1 (0x1)	Reserved	2 (0x2)	Reserved	3 (0x3)	3rd order
ORDER	Order Configuration														
0 (0x0)	Integer Mode Divider														
1 (0x1)	Reserved														
2 (0x2)	Reserved														
3 (0x3)	3rd order														

8.6.1.24 PLL_CTRL0 Register; R34

The PLL_CTRL1 register provides control of PLL. The PLL_CTRL1 register fields are described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION						
[7:6]	RESERVED	RW	0x0	Y	Reserved.						
[5]	PLL_D	RW	1	Y	PLL R Divider Frequency Doubler Enable. If PLL_D is 1 the R Divider Frequency Doubler is enabled.						
[4]	RESERVED	-	-	N	Reserved.						
[3:0]	PLL_CP[3:0]	RW	0x8	Y	PLL Charge Pump Current. Other combinations of PLL_CP[3:0] not in table below are reserved and not supported. <table border="1" data-bbox="906 1402 1479 1497"> <thead> <tr> <th>PLL_CP[3:0]</th> <th>PLL Charge Pump Current</th> </tr> </thead> <tbody> <tr> <td>4 (0x4)</td> <td>1.6 mA</td> </tr> <tr> <td>8 (0x8)</td> <td>6.4 mA</td> </tr> </tbody> </table>	PLL_CP[3:0]	PLL Charge Pump Current	4 (0x4)	1.6 mA	8 (0x8)	6.4 mA
PLL_CP[3:0]	PLL Charge Pump Current										
4 (0x4)	1.6 mA										
8 (0x8)	6.4 mA										

8.6.1.25 PLL_CTRL1 Register; R35

The PLL_CTRL3 register provides control of PLL. The PLL_CTRL3 register fields are described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION																		
[7]	RESERVED	-	-	N	Reserved.																		
[6:4]	PLL_CP_PHASE_SHIFT [2:0]	RW	0x0	Y	Program Charge Pump Phase Shift. <table border="1"> <thead> <tr> <th>PLL_CP_PHASE_SHIFT[2:0]</th> <th>Phase Shift</th> </tr> </thead> <tbody> <tr> <td>0 (0x0)</td> <td>No delay</td> </tr> <tr> <td>1 (0x1)</td> <td>1.3 ns for 100 MHz f_{PD}</td> </tr> <tr> <td>2 (0x2)</td> <td>1 ns for 100 MHz f_{PD}</td> </tr> <tr> <td>3 (0x3)</td> <td>0.9 ns for 100 MHz f_{PD}</td> </tr> <tr> <td>4 (0x4)</td> <td>1.3 ns for 50 MHz f_{PD}</td> </tr> <tr> <td>5 (0x5)</td> <td>1 ns for 50 MHz f_{PD}</td> </tr> <tr> <td>6 (0x6)</td> <td>0.9 ns for 50 MHz f_{PD}</td> </tr> <tr> <td>7 (0x7)</td> <td>0.7 ns for 50 MHz f_{PD}</td> </tr> </tbody> </table>	PLL_CP_PHASE_SHIFT[2:0]	Phase Shift	0 (0x0)	No delay	1 (0x1)	1.3 ns for 100 MHz f_{PD}	2 (0x2)	1 ns for 100 MHz f_{PD}	3 (0x3)	0.9 ns for 100 MHz f_{PD}	4 (0x4)	1.3 ns for 50 MHz f_{PD}	5 (0x5)	1 ns for 50 MHz f_{PD}	6 (0x6)	0.9 ns for 50 MHz f_{PD}	7 (0x7)	0.7 ns for 50 MHz f_{PD}
PLL_CP_PHASE_SHIFT[2:0]	Phase Shift																						
0 (0x0)	No delay																						
1 (0x1)	1.3 ns for 100 MHz f_{PD}																						
2 (0x2)	1 ns for 100 MHz f_{PD}																						
3 (0x3)	0.9 ns for 100 MHz f_{PD}																						
4 (0x4)	1.3 ns for 50 MHz f_{PD}																						
5 (0x5)	1 ns for 50 MHz f_{PD}																						
6 (0x6)	0.9 ns for 50 MHz f_{PD}																						
7 (0x7)	0.7 ns for 50 MHz f_{PD}																						
[3]	RESERVED	-	-	N	Reserved.																		
[2]	PLL_ENABLE_C3	RW	0	Y	Disable third order capacitor in the low pass filter. <table border="1"> <thead> <tr> <th>PLL_ENABLE_C3</th> <th>MODE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>2nd order loop filter recommended setting</td> </tr> <tr> <td>1</td> <td>Enables C3, 3rd order loop filter enabled</td> </tr> </tbody> </table>	PLL_ENABLE_C3	MODE	0	2nd order loop filter recommended setting	1	Enables C3, 3rd order loop filter enabled												
PLL_ENABLE_C3	MODE																						
0	2nd order loop filter recommended setting																						
1	Enables C3, 3rd order loop filter enabled																						
[1:0]	RESERVED	-	0x3	Y	Reserved.																		

8.6.1.26 PLL_LF_R2 Register; R36

The PLL_LF_R2 register controls the value of the PLL Loop Filter R2.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION														
[7:0]	PLL_LF_R2[7:0]	RW	0x08	Y	PLL Loop Filter R2. NOTE: Table below lists commonly used R2 values but more selections are available. <table border="1"> <thead> <tr> <th>PLL_LF_R2[7:0]</th> <th>R2 (Ω)</th> </tr> </thead> <tbody> <tr> <td>1 (0x01)</td> <td>200</td> </tr> <tr> <td>4 (0x04)</td> <td>500</td> </tr> <tr> <td>8 (0x08)</td> <td>700</td> </tr> <tr> <td>32 (0x20)</td> <td>1600</td> </tr> <tr> <td>48 (0x30)</td> <td>2400</td> </tr> <tr> <td>64 (0x40)</td> <td>3200</td> </tr> </tbody> </table>	PLL_LF_R2[7:0]	R2 (Ω)	1 (0x01)	200	4 (0x04)	500	8 (0x08)	700	32 (0x20)	1600	48 (0x30)	2400	64 (0x40)	3200
PLL_LF_R2[7:0]	R2 (Ω)																		
1 (0x01)	200																		
4 (0x04)	500																		
8 (0x08)	700																		
32 (0x20)	1600																		
48 (0x30)	2400																		
64 (0x40)	3200																		

8.6.1.27 PLL_LF_C1 Register; R37

The PLL_LF_C1 register controls the value of the PLL Loop Filter C1.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:3]	RESERVED	-	-	N	Reserved.
[2:0]	PLL_LF_C1[2:0]	RW	0x0	Y	PLL Loop Filter C1. The value in pF is given by $5 + 50 * \text{PLL_LF_C1}$ (in decimal).

8.6.1.28 PLL_LF_R3 Register; R38

The PLL_LF_R3 register controls the value of the PLL Loop Filter R3.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7]	RESERVED	-	-	N	Reserved.
[6:0]	PLL_LF_R3[6:0]	RW	0x00	Y	PLL Loop Filter R3. NOTE: Table below lists commonly used R3 values but more selections are available.
	PLL_LF_R3[6:0]				R3 (Ω)
	0 (0x00)				18
	3 (0x03)				205
	8 (0x08)				854
	9 (0x09)				1136
	12 (0x0C)				1535
	17 (0x11)				1936
	20 (0x14)				2335

8.6.1.29 PLL_LF_C3 Register; R39

The PLL_LF_C3 register controls the value of the PLL Loop Filter C3.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:3]	RESERVED	-	-	N	Reserved.
[2:0]	PLL_LF_C3[2:0]	RW	0x0	Y	PLL Loop Filter C3. The value in pF is given by 5 * PLL_LF_C3 (in decimal).

8.6.1.30 PLL_CALCTRL Register; R42

The PLL_CALCTRL register is described in the following table.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:4]	RESERVED	-	-	N	Reserved.
[3:2]	PLL_CLSDWAIT[1:0]	RW	0x2	Y	Closed Loop Wait Period. The CLSDWAIT field sets the closed loop wait period. Recommended value is 0x2.
	CLSDWAIT				Anlog closed loop VCO stabilization time
	0 (0x0)				150 μ s
	1 (0x1)				300 μ s
	2 (0x2)				500 μ s
	3 (0x3)				2000 μ s
[1:0]	PLL_VCOWAIT[1:0]	RW	0x1	Y	VCO Wait Period. Recommended value is 0x1.
	VCOWAIT				VCO stabilization time
	0 (0x0)				20 μ s
	1 (0x1)				400 μ s
	2 (0x2)				4000 μ s
	3 (0x3)				10000 μ s

8.6.1.31 NVMSCRC Register; R47

The NVMSCRC register holds the Stored CRC (Cyclic Redundancy Check) byte that has been retrieved from on-chip EEPROM.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	NVMSCRC[7:0]	R	0x00	Y	EEPROM Stored CRC.

8.6.1.32 NVMCNT Register; R48

The NVMCNT register is intended to reflect the number of on-chip EEPROM Erase/Program cycles that have taken place in EEPROM. The count is automatically incremented by hardware and stored in EEPROM.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	NVMCNT[7:0]	R	0x00	Y	EEPROM Program Count. The NVMCNT increments automatically after every EEPROM Erase/Program Cycle. The NVMCNT value is retrieved automatically after reset, after a EEPROM Commit operation or after a Erase/Program cycle. The NVMCNT register will increment until it reaches its maximum value of 255 after which no further increments will take place.

8.6.1.33 NVMCTL Register; R49

The NVMCTL register allows control of the on-chip EEPROM Memories.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7]	RESERVED	-	-	N	Reserved.
[6]	REGCOMMIT	RWSC	0	N	REG Commit to EEPROM SRAM Array. The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the EEPROM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete.
[5]	NVMCRCERR	R	0	N	EEPROM CRC Error Indication. The NVMCRCERR bit is set to 1 if a CRC Error has been detected when reading back from on-chip EEPROM during device configuration.
[4]	NVMAUTOCRC	RW	1	N	EEPROM Automatic CRC. When NVMAUTOCRC is 1 then the EEPROM Stored CRC byte is automatically calculated whenever a EEPROM program takes place.
[3]	NVMCOMMIT	RWSC	0	N	EEPROM Commit to Registers. The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The I ² C registers cannot be read while a EEPROM Commit operation is taking place.
[2]	NVMBUSY	R	0	N	EEPROM Program Busy Indication. The NVMBUSY bit is 1 during an on-chip EEPROM Erase/Program cycle. While NVMBUSY is 1 the on-chip EEPROM cannot be accessed.
[1]	NVMERASE	RWSC	0	N	EEPROM Erase Start. The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I ² C transaction was a write to the NVMUNLK register with the appropriate code. The NVMERASE bit is automatically cleared to 0. The EEPROM Erase operation takes around 115ms.
[0]	NVMPROG	RWSC	0	N	EEPROM Program Start. The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I ² C transaction was a write to the NVMUNLK register with the appropriate code. The NVMPROG bit is automatically cleared to 0. If the NVMERASE and NVMPROG bits are set simultaneously then an ERASE/PROGRAM cycle will be executed The EEPROM Program operation takes around 115ms.

8.6.1.34 MEMADR Register; R51

The MEMADR register holds 7-bits of the starting address for on-chip SRAM or EEPROM access.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7]	RESERVED	-	-	N	Reserved.
[6:0]	MEMADR[6:0]	RW	0x00	N	Memory Address. The MEMADR value determines the starting address for on-chip SRAM read/write access or on-chip EEPROM access. The internal address to access SRAM or EEPROM is automatically incremented; however the MEMADR register does not reflect the internal address in this way. When the SRAM or EEPROM arrays are accessed using the I ² C interface only bits [4:0] of MEMADR are used to form the byte Wise address.

8.6.1.35 NVMDAT Register; R52

The NVMDAT register returns the on-chip EEPROM contents from the starting address specified by the MEMADR register.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	NVMDAT[7:0]	R	0x00	N	EEPROM Read Data. The first time an I ² C read transaction accesses the NVMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, the read transaction will return the EEPROM data located at the address specified by the MEMADR register. Any additional read's which are part of the same transaction will cause the EEPROM address to be incremented and the next EEPROM data byte will be returned. The I ² C address will no longer be auto-incremented, i.e the I ² C address will be locked to the NVMDAT register after the first access. Access to the NVMDAT register will terminate at the end of the current I ² C transaction.

8.6.1.36 RAMDAT Register; R53

The RAMDAT register provides read and write access to the SRAM that forms part of the on-chip EEPROM module.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	RAMDAT[7:0]	RW	0x00	N	RAM Read/Write Data. The first time an I ² C read or write transaction accesses the RAMDAT register address, either because it was explicitly targeted or because the address was auto-incremented, a read transaction will return the RAM data located at the address specified by the MEMADR register and a write transaction will cause the current I ² C data to be written to the address specified by the MEMADR register. Any additional accesses which are part of the same transaction will cause the RAM address to be incremented and a read or write access will take place to the next SRAM address. The I ² C address will no longer be auto-incremented, i.e the I ² C address will be locked to the RAMDAT register after the first access. Access to the RAMDAT register will terminate at the end of the current I ² C transaction.

8.6.1.37 NVMUNLK Register; R56

The NVMUNLK register provides a rudimentary level of protection to prevent inadvertent programming of the on-chip EEPROM.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:0]	NVMUNLK[7:0]	RW	0x00	N	EEPROM Prog Unlock. The NVMUNLK register must be written immediately prior to setting the NVMPROG bit of register NVMCTL, otherwise the Erase/Program cycle will not be triggered. NVMUNLK must be written with a value of 0xBE.

8.6.1.38 INT_LIVE Register; R66

The INT_LIVE register reflects the current status of the interrupt sources.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:2]	RESERVED	-	-	N	Reserved.
[1]	LOL	R	0	N	Loss of Lock PLL.
[0]	CAL	R	0	N	Calibration Active PLL.

8.6.1.39 SWRST Register; R72

The SWRST1 register provides software reset control for specific on-chip modules. Each bit in this register is individually self cleared after a write operation. The SWRST1 register will always return 0x00 in a read transaction.

BIT NO.	FIELD	TYPE	RESET	EEPROM	DESCRIPTION
[7:2]	RESERVED	-	-	N	Reserved.
[1]	SWR2PLL	RWSC	0	N	Software Reset PLL. Setting SWR2PLL to 1 resets the PLL calibrator and clock dividers. This bit is automatically cleared to 0.
[0]	RESERVED	-	-	N	Reserved.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMK61E0 features fine and coarse frequency margining capabilities which allow it to be used in applications requiring the output frequency to be adjusted on the fly. In fractional PLL mode, the numerator of the PLL fractional feedback divider can be updated over I²C to update the output frequency without glitches or spikes, allowing the device to be used as a DCXO. The output frequency step size for every bit change in the numerator of the PLL fractional feedback divider is given in [Configuring the PLL](#). The [Application Curves](#) section below illustrates the glitch-less switch in output frequency when the numerator is updated. The frequency margining features can also aid the hardware designer during the system debug and validation phase.

9.2 Typical Application

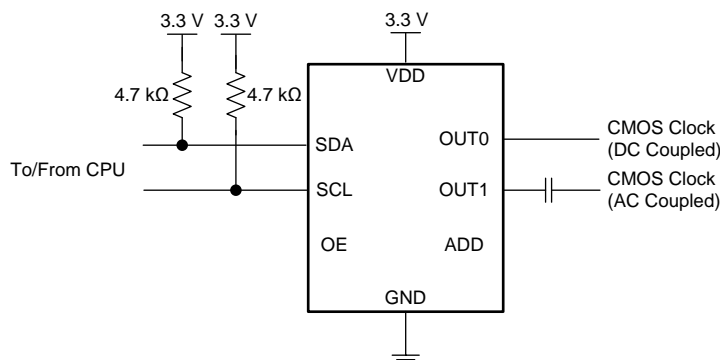


Figure 13. LMK61E0M Typical Application

9.2.1 Design Requirements

Consider a typical digital subscriber line (DSL) application, in which a local modem must track the clock signal of a network modem to ensure accurate and efficient data transfer. In such systems, a DCXO is implemented to allow a local processor to digitally control the oscillator frequency to maintain synchronization. An example of such a clock frequency would be 70.656 MHz.

The typical schematic above shows the I²C connection to the processor and output configurations for AC or DC coupling. OE and ADD can be left floating. The internal pullup resistor on OE enables OUT0. Leaving ADD floating sets the LSB of the I²C slave address to 01.

The [Detailed Design Procedure](#) below describes the procedure to generate and adjust the required output frequency for the above scenario using LMK61E0M.

9.2.2 Detailed Design Procedure

This design procedure will give a quick outline of the process of configuring the LMK61E0M in the above use case. Typically, the easiest approach to configuring the PLL is to start with the desired output frequency and work backwards.

1. VCO Frequency Selection

- The first step is to calculate the possible VCO frequencies given the required output frequency of 70.656 MHz. The LMK61E0M output dividers consist of the VCO post divider that can be set to /4 or /5, and the output divider that can be set from /6 to /256. The VCO can output frequencies from 4.6 GHz to 5.6 GHz. Therefore, the output frequency multiplied by the total divide value must fall within this range.
- To determine the boundary of the total divide value, we can divide the VCO frequency limits by the output

Typical Application (continued)

frequency, resulting in a range of 65.1 to 79.3. Any combination of dividers that result in a total divide value within this range will result in a valid VCO frequency. The possible divider combinations and the resulting VCO frequencies are listed in columns 1 and 2, respectively, of [Table 4](#), below.

2. Input Divider and Doubler/Phase Detector Frequency Configuration

- The next step is to set the reference divider and doubler in the reference frequency path to the PLL. The reference divider can be set to /1 or /4, and the doubler can be set to x1 or x2. The main trade-off is that a higher phase detector frequency will result in better output phase noise performance and a lower phase detector frequency will result in a finer output frequency step size when adjusting the feedback divider numerator in DCXO mode.
- In the DSL application, a finer step size is desired so the reference divider will be set to /4 and the doubler to x1 to minimize the phase detector frequency. The phase detector frequency can then be calculated by multiplying and dividing the reference frequency of 50 MHz by those values, resulting in 12.5 MHz.
- Note that in some applications, a trade-off in step size to obtain better phase noise performance is acceptable. In that case the design procedure can be continued, substituting the relevant reference divider and doubler configuration and phase detector frequency.

Typical Application (continued)

3. Feedback Divider Selection

- The possible feedback divider values can then be calculated by dividing the VCO frequency by the phase detector frequency. The possible values are listed in column 3 of [Table 4](#).
- Glitch-less frequency margining in DCXO mode is achieved by adjusting the numerator of the feedback divider without changing the integer value of the divider, which could cause a frequency glitch. Therefore, the output frequency tuning range is limited by which VCO frequency and feedback divider we select out of the valid combinations. To obtain as equal of a tuning range above and below the nominal output frequency as possible, a feedback divider value with fractional portion as close to 1/2 as possible should be chosen.
- The VCO frequency of 5369.856 MHz results in a feedback divider of 429.58848, which has a fractional portion closest to 1/2. The decimal converted to a fraction is 429+58848/100000. To minimize step size, the fraction can be converted to the maximum equivalent fraction of 2412768/4100000 as limited by the maximum denominator of 4194303.

4. Frequency Margining

- With the device configured to output the nominal frequency of 70.656 MHz, the numerator can be adjusted over I²C to tune the output frequency.
- Using equation 3 in [Configuring the PLL](#), the step size of this configuration can be calculated to be approximately 4×10^{-8} MHz or 0.58 ppb.
- The maximum and minimum tuning range limits can be determined by calculating the maximum shift in frequency from nominal without changing the integer portion of the feedback divider (including setting the numerator to zero or equal to the denominator). In this case, the limits are a maximum of +955 ppm and a minimum of –1365 ppm from nominal.

Table 4. PLL Configuration Options

1. POSSIBLE OUTPUT DIVIDER COMBINATIONS	2. POSSIBLE VCO FREQUENCIES (MHz)	3. FEEDBACK DIVIDER WITH PDF=12.5 MHz	4. EQUIVALENT FRACTIONAL FEEDBACK DIVIDER VALUES
68 (/4, /17)	4804.608	384.36864	384+1511424/4100000
70 (/5, /14)	4945.92	395.6736	395+2822384/4190000
72 (/4, /18)	5087.232	406.97856	406+4012096/4100000
75 (/5, /15)	5299.2	423.936	423+3925584/4194000
76 (/4, /19)	5369.856	429.58848	429+2412768/4100000

9.2.2.1 PLL Loop Filter Design

The EVM software tool TICS Pro/Oscillator Programming Tool can be used to aid loop filter design. The Easy Configuration GUI is able to generate a suggested set of loop filter values given a desired output frequency. The tool recommends a PLL configuration that is designed to minimize jitter. As of the publication of this document, it is not yet able to optimize for desired tuning range in DCXO mode. When configuring the device for operation in DCXO mode, TI recommends using the software suggested loop filter settings as a starting point and then perform the procedure described in [Detailed Design Procedure](#) to optimize the PLL configuration to suit the application needs.

A general set of loop filter design guidelines are given below:

- There are many device configurations to achieve the desired output frequency from a device. However there are some optimizations and trade-offs to be considered.
- The guidelines below may be followed when configuring PLL related dividers or other related registers:
 - For lowest possible in-band PLL flat noise, maximize phase detector frequency to minimize N divide value.
 - For fractional divider values, keep the denominator at highest value possible to minimize spurs. It is also best to use a higher order modulator whenever possible for the same reason.
 - As a rule of thumb, keep the phase detector frequency approximately between $10 \times$ PLL loop bandwidth and $100 \times$ PLL loop bandwidth. A phase detector frequency less than $5 \times$ PLL bandwidth may be unstable.
 - While designing the loop filter, adjusting the charge pump current or N value can help with loop filter component selection. Lower charge pump currents and larger N values result in smaller component values

but may increase impacts of leakage and reduce PLL phase noise performance.

- A more detailed understanding of loop filter design can be found in Dean Banerjee's [PLL Performance, Simulation, and Design](#).

9.2.2.2 Spur Mitigation Techniques

The LMK61E0M offers several programmable features for optimizing fractional spurs. To get the best out of these features, it makes sense to understand the different kinds of spurs as well as their behaviors, causes, and remedies. Although optimizing spurs may involve some trial and error, there are ways to make this process more systematic. TI offers the [Clock Design Tool](#) (SNAU082) for more information and estimation of fractional spurs.

9.2.2.2.1 Phase Detection Spur

The phase detector spur occurs at an offset from the carrier equal to the phase detector frequency, f_{PD} . To minimize this spur, consider a lower phase detector frequency. In some cases where the loop bandwidth is very wide relative to the phase detector frequency, some benefit might be gained from using a narrower loop bandwidth or adding poles to the loop filter by using R3 and C3 if previously unused, but otherwise the loop filter has minimal impact. Bypassing at the supply pins and board layout can also have an impact on this spur, especially at higher phase detector frequencies.

9.2.2.2.2 Integer Boundary Fractional Spur

This spur occurs at an offset equal to the difference between the VCO frequency and the closest integer channel for the VCO. For instance, if the phase detector frequency is 100 MHz and the VCO frequency is 5003 MHz, then the integer boundary spur would be at 3-MHz offset. This spur can be either PLL or VCO dominated. If it is PLL dominated, decreasing the loop bandwidth and some of the programmable fractional words may impact this spur. If the spur is VCO dominated, then reducing the loop filter will not help, but rather reducing the phase detector and having good slew rate and signal integrity at the selected reference input will help.

9.2.2.2.3 Primary Fractional Spur

These spurs occur at multiples of f_{PD}/DEN and are not the integer boundary spur. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, the primary fractional spurs would be at 1 MHz, 2 MHz, 4 MHz, 5 MHz, 6 MHz, and so forth. These are impacted by the loop filter bandwidth and modulator order. If a small frequency error is acceptable, then a larger equivalent fraction may improve these spurs. This larger unequivalent fraction pushes the fractional spur energy to much lower frequencies that where they are not impactful to the system performance.

9.2.2.2.4 Sub-Fractional Spur

These spurs appear at a fraction of f_{PD}/DEN and depend on modulator order. With the first order modulator, there are no sub-fractional spurs. The second order modulator can produce 1/2 sub-fractional spurs if the denominator is even. A third order modulator can produce sub-fractional spurs at 1/2, 1/3, or 1/6 of the offset, depending if it is divisible by 2 or 3. For instance, if the phase detector frequency is 100 MHz and the fraction is 3/100, no sub-fractional spurs for a first order modulator or sub-fractional spurs at multiples of 1.5 MHz for a second or third order modulator would be expected. Aside from strategically choosing the fractional denominator and using a lower order modulator, another tactic to eliminate these spurs is to use dithering and express the fraction in larger equivalent terms. Because dithering also adds phase noise, its level needs to be managed to achieve acceptable phase noise and spurious performance.

[Table 5](#) summarizes spur and mitigation techniques.

Table 5. Spur and Mitigation Techniques

SPUR TYPE	OFFSET	WAYS TO REDUCE	TRADE-OFFS
Phase Detector	f_{PD}	Reduce Phase Detector Frequency.	Although reducing the phase detector frequency does improve this spur, it also degrades phase noise.

Table 5. Spur and Mitigation Techniques (continued)

SPUR TYPE	OFFSET	WAYS TO REDUCE	TRADE-OFFS
Integer Boundary	$f_{VCO} \text{ mod } f_{PD}$	Methods for PLL Dominated Spurs	Reducing the loop bandwidth may degrade the total integrated noise if the bandwidth is too narrow.
		- Avoid the worst case VCO frequencies if possible.	
		- Ensure good slew rate and signal integrity at reference input.	
		- Reduce loop bandwidth or add more filter poles to suppress out of band spurs.	Reducing the phase detector may degrade the phase noise.
		Methods for VCO Dominated Spurs	
		- Avoid the worst case VCO frequencies if possible.	
- Reduce Phase Detector Frequency.			
- Ensure good slew rate and signal integrity at reference input.			
Primary Fractional	f_{PD}/DEN	- Decrease Loop Bandwidth.	Decreasing the loop bandwidth may degrade in-band phase noise. Also, larger unequivalent fractions don't always reduce spurs.
		- Change Modulator Order.	
		- Use Larger Unequivalent Fractions.	
Sub-Fractional	$f_{PD}/DEN/k$ k=2,3, or 6	- Use Dithering.	Dithering and larger fractions may increase phase noise.
		- Use Larger Equivalent Fractions.	
		- Use Larger Unequivalent Fractions.	
		- Reduce Modulator Order.	
		- Eliminate factors of 2 or 3 in denominator.	

9.2.2.3 Device Programming

The EVM software tool TICS Pro/Oscillator Programming Tool can be used to program the device with the desired configuration. Simply select the *Program EEPROM* option and the software will automatically load the current configuration to EEPROM. The settings will then be available upon subsequent startup without the need to reload the registers over I²C.

9.2.3 Application Curves

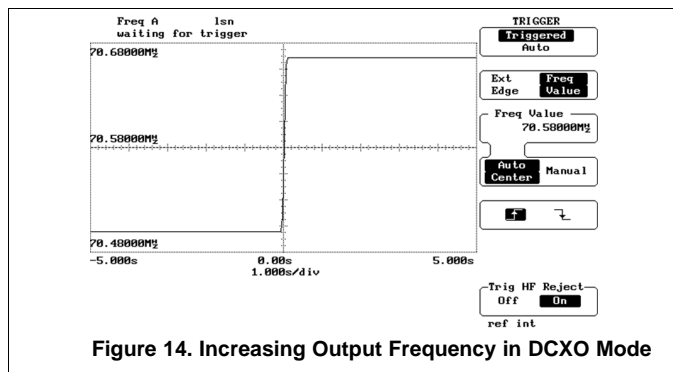


Figure 14. Increasing Output Frequency in DCXO Mode

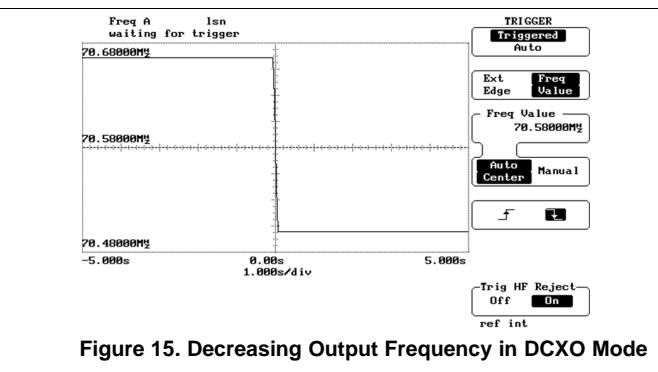


Figure 15. Decreasing Output Frequency in DCXO Mode

10 Power Supply Recommendations

For best electrical performance of the LMK61E0 device, TI recommends using a combination of 10 μF , 1 μF and 0.1 μF on its power supply bypass network. TI also recommends using component side mounting of the power supply bypass capacitors, and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. [Figure 16](#) shows the layout recommendation for power supply decoupling of LMK61E0.

11 Layout

11.1 Layout Guidelines

[Ensured Thermal Reliability](#), [Best Practices for Signal Integrity](#) and [Recommended Solder Reflow Profile](#) provide recommendations for board layout, solder reflow profile and power supply bypassing when using LMK61E0 to ensure good thermal and electrical performance and overall signal integrity of entire system.

11.1.1 Ensured Thermal Reliability

The LMK61E0 is a high performance device. Therefore careful attention must be paid to device configuration and printed-circuit board (PCB) layout with respect to power consumption. The ground pin needs to be connected to the ground plane of the PCB through three vias or more, as shown in [Figure 16](#), to maximize thermal dissipation out of the package.

[Equation 4](#) describes the relationship between the PCB temperature around the LMK61E0 and its junction temperature.

$$T_B = T_J - \Psi_{JB} * P$$

where

- T_B : PCB temperature around the LMK61E0
 - T_J : Junction temperature of LMK61E0
 - Ψ_{JB} : Junction-to-board thermal resistance parameter of LMK61E0 (36.7°C/W without airflow)
 - P: On-chip power dissipation of LMK61E0
- (4)

To ensure that the maximum junction temperature of LMK61E0 is below 115°C, it can be calculated that the maximum PCB temperature without airflow should be at 93°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.6 W.

11.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK61E0, TI recommends routing vias into decoupling capacitors and then into the LMK61E0. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high-frequency current flow. [Figure 16](#) shows the layout recommendation for LMK61E0.

11.1.3 Recommended Solder Reflow Profile

TI also recommends following the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferable for the LMK61E0 to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufactures recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

11.2 Layout Example

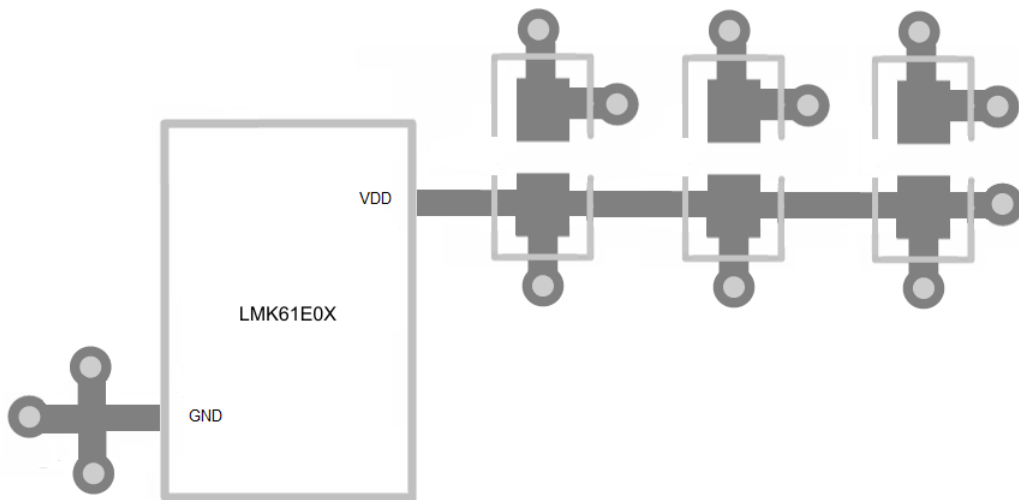


Figure 16. LMK61E0 Layout Recommendation for Power Supply and Ground

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [Clock Design Tool](#) (SNAU082)
- [PLL Performance, Simulation, and Design](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK61E0M-SIAR	ACTIVE	QFM	SIA	8	2500	Green (RoHS & no Sb/Br)	Call TI NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E0 M	Samples
LMK61E0M-SIAT	ACTIVE	QFM	SIA	8	250	Green (RoHS & no Sb/Br)	Call TI NIAU	Level-3-260C-168 HR	-40 to 85	LMK61E0 M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

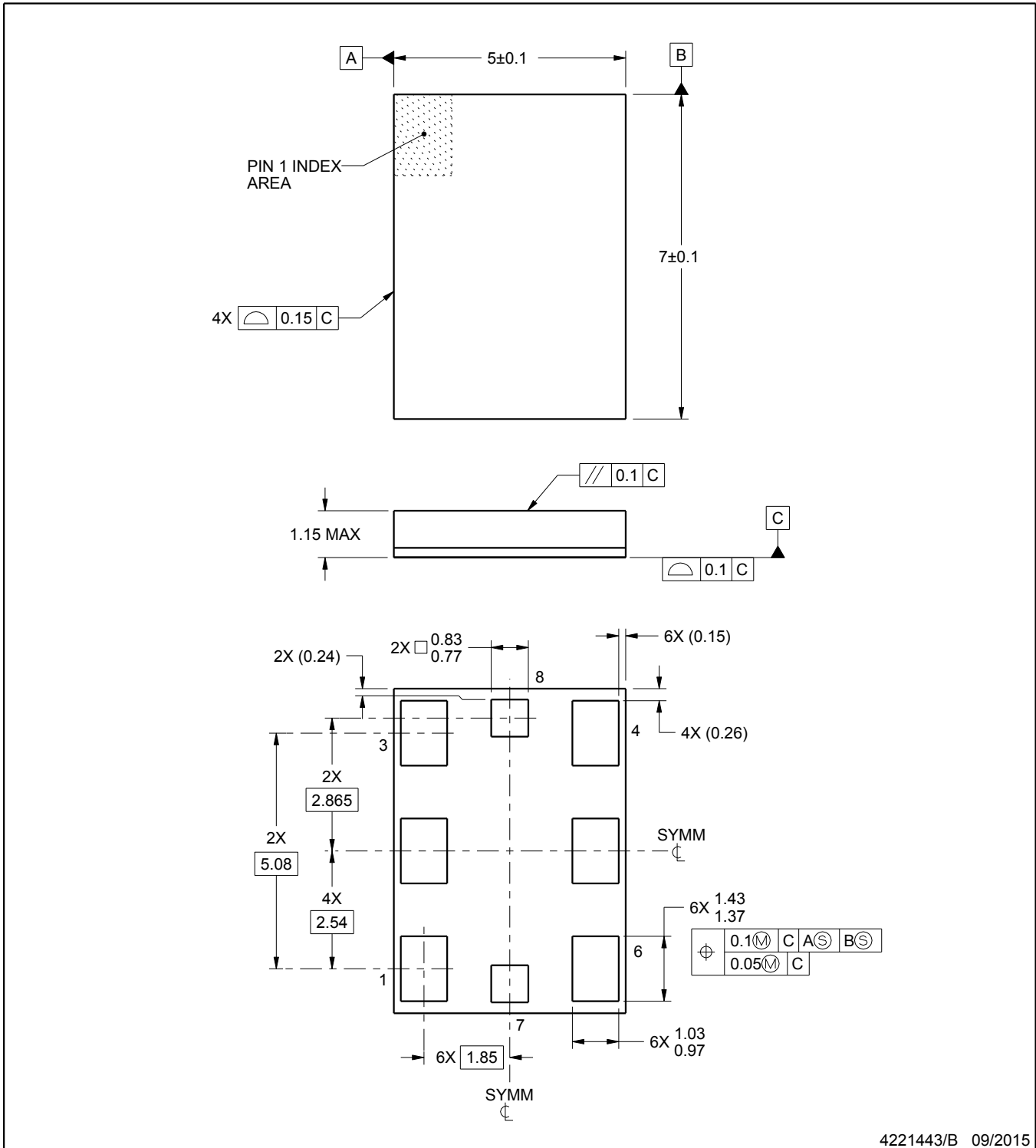
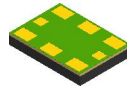
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

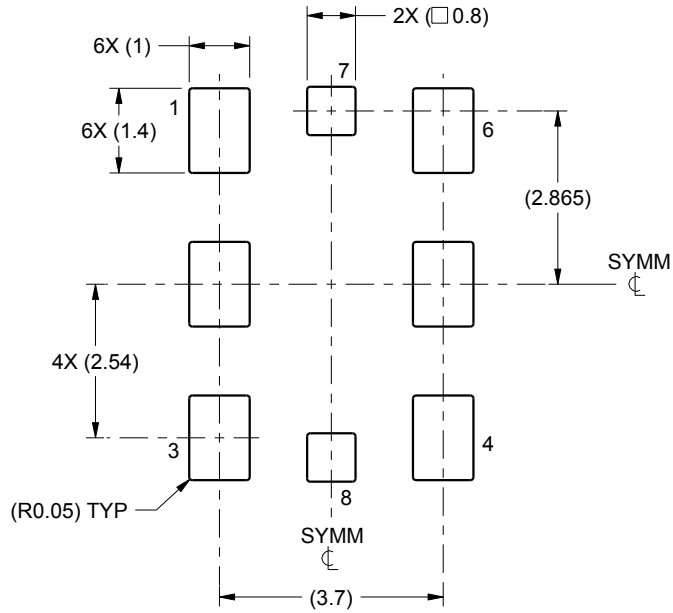
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

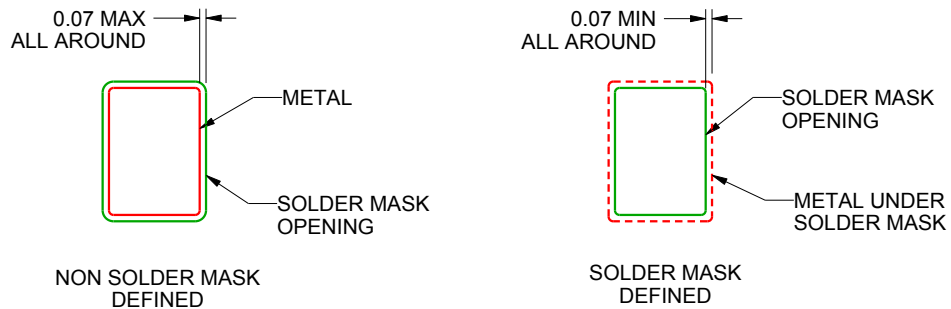
SIA0008B

QFM - 1.15 mm max height

QUAD FLAT MODULE



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

4221443/B 09/2015

NOTES: (continued)

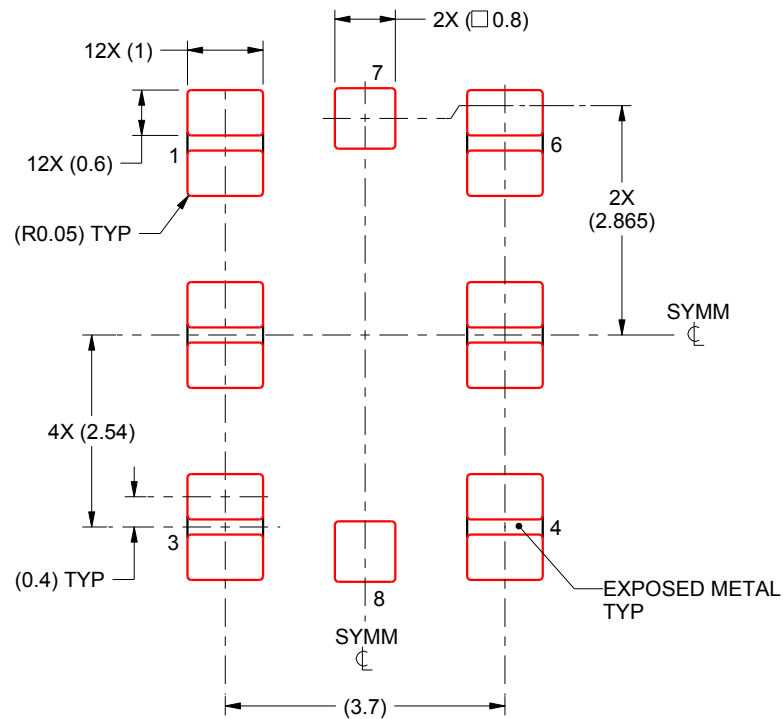
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

SIA0008B

QFM - 1.15 mm max height

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
PRINTED SOLDER COVERAGE BY AREA
PADS 1-3 & 4-6: 86%
SCALE:10X

4221443/B 09/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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