LMV3xx-N/Q1 Single, Dual, and Quad General Purpose, Low-Voltage, Rail-to-Rail Output Operational Amplifiers

1 Features

• (For $V^+ = 5$ V and $V^- = 0$ V, Unless Otherwise Specified)
• LMV321-N, LMV358-N, and LMV324-N are available in Automotive AEC-Q100 Grade 1 and 3 versions
• Ensured 2.7-V and 5-V Performance
• No Crossover Distortion
• Industrial Temperature Range $-40^\circ$C to $+125^\circ$C
• Gain-Bandwidth Product 1 MHz
• Low Supply Current
• LMV321-N 130 $\mu$A
• LMV358-N 210 $\mu$A
• LMV324-N 410 $\mu$A
• Rail-to-Rail Output Swing At 10 k$\Omega$ $V^{+/-}$ 10 mV & $V^+ - 65$ mV
• $V_{\text{CM}}$ Range $-0.2$ V to $V^{+/-} 0.8$ V

2 Applications

• Active Filters
• General Purpose Low Voltage Applications
• General Purpose Portable Devices

3 Description

The LMV358-N and LMV324-N are low-voltage (2.7 V to 5.5 V) versions of the dual and quad commodity op amps LM358 and LM324 (5 V to 30 V). The LMV321-N is the single channel version. The LMV321-N, LMV358-N, and LMV324-N are the most cost-effective solutions for applications where low-voltage operation, space efficiency, and low price are important. They offer specifications that meet or exceed the familiar LM358 and LM324. The LMV321-N, LMV358-N, and LMV324-N have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed to power ratio, achieving 1 MHz of bandwidth and 1-V/μs slew rate with low supply current.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMV321-N</td>
<td>SOT-23 (5)</td>
<td>2.90 mm x 1.60 mm</td>
</tr>
<tr>
<td></td>
<td>SC70 (5)</td>
<td>2.00 mm x 1.25 mm</td>
</tr>
<tr>
<td>LMV321-N-Q1</td>
<td>SOT-23 (5)</td>
<td>2.90 mm x 1.60 mm</td>
</tr>
<tr>
<td>LMV324-N</td>
<td>SOIC (14)</td>
<td>8.65 mm x 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (14)</td>
<td>5.00 mm x 4.40 mm</td>
</tr>
<tr>
<td>LMV324-N-Q1</td>
<td>SOIC (14)</td>
<td>8.65 mm x 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (14)</td>
<td>5.00 mm x 4.40 mm</td>
</tr>
<tr>
<td>LMV358-N</td>
<td>SOIC (8)</td>
<td>4.90 mm x 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
<tr>
<td>LMV358-N-Q1</td>
<td>SOIC (8)</td>
<td>4.90 mm x 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8)</td>
<td>3.00 mm x 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Gain and Phase vs. Capacitive Load

Output Voltage Swing vs. Supply Voltage

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (February 2013) to Revision J Page

- Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ............................................. 1

Changes from Revision H (February 2013) to Revision I Page

- Changed layout of National Data Sheet to TI format ................................................................. 32
5 Description (Continued)
The LMV321-N is available in the space saving 5-Pin SC70, which is approximately half the size of the 5-Pin SOT23. The small package saves space on PC boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The chips are built with Texas Instruments's advanced submicron silicon-gate BiCMOS process. The LMV321-N/LMV358-N/LMV324-N have bipolar input and output stages for improved noise performance and higher output current drive.

6 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>+IN</td>
<td>I</td>
<td>Noninverting input</td>
</tr>
<tr>
<td>IN A+</td>
<td>I</td>
<td>Noninverting input, channel A</td>
</tr>
<tr>
<td>IN B+</td>
<td>I</td>
<td>Noninverting input, channel B</td>
</tr>
<tr>
<td>IN C+</td>
<td>I</td>
<td>Noninverting input, channel C</td>
</tr>
<tr>
<td>IN D+</td>
<td>I</td>
<td>Noninverting input, channel D</td>
</tr>
<tr>
<td>-IN</td>
<td>I</td>
<td>Inverting input</td>
</tr>
<tr>
<td>IN A-</td>
<td>I</td>
<td>Inverting input, channel A</td>
</tr>
<tr>
<td>IN B-</td>
<td>I</td>
<td>Inverting input, channel B</td>
</tr>
<tr>
<td>IN C-</td>
<td>I</td>
<td>Inverting input, channel C</td>
</tr>
<tr>
<td>IN D-</td>
<td>I</td>
<td>Inverting input, channel D</td>
</tr>
<tr>
<td>OUTPUT</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>OUT A</td>
<td>O</td>
<td>Output, channel A</td>
</tr>
<tr>
<td>OUT B</td>
<td>O</td>
<td>Output, channel B</td>
</tr>
<tr>
<td>OUT C</td>
<td>O</td>
<td>Output, channel C</td>
</tr>
<tr>
<td>OUT D</td>
<td>O</td>
<td>Output, channel D</td>
</tr>
<tr>
<td>V+</td>
<td>P</td>
<td>Positive (highest) power supply</td>
</tr>
<tr>
<td>V-</td>
<td>P</td>
<td>Negative (lowest) power supply</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings

See (1)(2).

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Input Voltage</td>
<td>±Supply Voltage</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage</td>
<td>−0.3</td>
<td>+Supply Voltage</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage (V⁺−V⁻)</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Short Circuit</td>
<td>(3)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>to V⁺</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>to V⁻</td>
<td>(4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soldering Information: Infrared or Convection (30 sec)</td>
<td>260</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.

(3) Shorting output to V⁺ will adversely affect reliability.

(4) Shorting output to V⁻ will adversely affect reliability.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

7.2 ESD Ratings - Commercial

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(ESD) Electrostatic discharge</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)</td>
<td>±2000 V</td>
</tr>
<tr>
<td></td>
<td>Machine model</td>
<td>±100</td>
</tr>
</tbody>
</table>

7.3 ESD Ratings - Automotive

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(ESD) Electrostatic discharge</td>
<td>Human-body model (HBM), per AEC Q100-002(1)</td>
<td>±2000 V</td>
</tr>
<tr>
<td></td>
<td>Machine model</td>
<td>±100</td>
</tr>
</tbody>
</table>

7.4 Recommended Operating Conditions

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Temperature Range (1): LMV321-N, LMV358-N, LMV324-N</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Temperature Range (1): LMV321-N-Q1, LMV358-N-Q1, LMV324-N-Q1</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Temperature Range (1): LMV321-N-Q3, LMV358-N-Q3, LMV324-N-Q3</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{JA}$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{JA}$. All numbers apply for packages soldered directly onto a PC Board.
7.5 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>LMV321-N, LMV321-N-Q1, LMV321-N-Q3</th>
<th>LMV324-N, LMV324-N-Q1, LMV324-N-Q3</th>
<th>LMV358-N, LMV358-N-Q1, LMV358-N-Q3</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{thJA}$ Junction-to-ambient thermal resistance</td>
<td>265</td>
<td>478</td>
<td>145</td>
<td>155</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.6 2.7-V DC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ \text{C}$, $V^+ = 2.7 \text{ V}$, $V^- = 0 \text{ V}$, $V_{CM} = 1.0 \text{ V}$, $V_O = V^+/2$ and $R_L > 1 \text{ M\Omega}$.

<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>MIN(1)</th>
<th>TYP(2)</th>
<th>MAX(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS}$ Input Offset Voltage</td>
<td>1.7</td>
<td>7</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$TCV_{OS}$ Input Offset Voltage Average Drift</td>
<td>5</td>
<td></td>
<td>$\mu \text{V/}^\circ \text{C}$</td>
<td></td>
</tr>
<tr>
<td>$I_B$ Input Bias Current</td>
<td>11</td>
<td>250</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$ Input Offset Current</td>
<td>5</td>
<td>50</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>CMRR Common Mode Rejection Ratio</td>
<td>0 ≤ $V_{CM} ≤ 1.7 \text{ V}$</td>
<td>50</td>
<td>63</td>
<td>dB</td>
</tr>
<tr>
<td>PSRR Power Supply Rejection Ratio</td>
<td>$2.7 \text{ V} ≤ V^+ ≤ 5 \text{ V}$ $V_O = 1 \text{ V}$</td>
<td>50</td>
<td>60</td>
<td>dB</td>
</tr>
<tr>
<td>$V_{CM}$ Input Common-Mode Voltage Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>For CMRR ≥ 50 dB</td>
<td>0</td>
<td>−0.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>For CMRR ≥ 50 dB</td>
<td>1.9</td>
<td>1.7</td>
<td>V</td>
</tr>
<tr>
<td>$V_O$ Output Swing</td>
<td>$R_L = 10 \text{ k}\Omega$ to 1.35 V</td>
<td>$V^+ - 100$</td>
<td>$V^+ - 10$</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60</td>
<td>180</td>
<td>mV</td>
</tr>
<tr>
<td>$I_S$ Supply Current</td>
<td>Single</td>
<td>80</td>
<td>170</td>
<td>$\mu \text{A}$</td>
</tr>
<tr>
<td></td>
<td>Dual</td>
<td></td>
<td>140</td>
<td>340</td>
</tr>
<tr>
<td></td>
<td>Both amplifiers</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Quad</td>
<td>All four amplifiers</td>
<td>260</td>
<td>680</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

7.7 2.7-V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ \text{C}$, $V^+ = 2.7 \text{ V}$, $V^- = 0 \text{ V}$, $V_{CM} = 1.0 \text{ V}$, $V_O = V^+/2$ and $R_L > 1 \text{ M\Omega}$.

<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>MIN(1)</th>
<th>TYP(2)</th>
<th>MAX(1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBWP Gain-Bandwidth Product</td>
<td>$C_L = 200 \text{ pF}$</td>
<td>1</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$\Phi_m$ Phase Margin</td>
<td></td>
<td>60</td>
<td></td>
<td>Deg</td>
</tr>
<tr>
<td>$G_m$ Gain Margin</td>
<td></td>
<td>10</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$e_n$ Input-Reflected Voltage Noise</td>
<td>$f = 1 \text{ kHz}$</td>
<td>46</td>
<td></td>
<td>$\text{mV} / \sqrt{\text{Hz}}$</td>
</tr>
<tr>
<td>$I_n$ Input-Reflected Current Noise</td>
<td>$f = 1 \text{ kHz}$</td>
<td>0.17</td>
<td></td>
<td>$\text{pA} / \sqrt{\text{Hz}}$</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
## 5.8 5-V DC Electrical Characteristics

Unless otherwise specified, all limits specified for \( T_J = 25^\circ C, \ V^+ = 5 \ V, \ V^- = 0 \ V, \ V_{CM} = 2 \ V, \ V_O = V^+/2 \) and \( R_L > 1 \ M\Omega \).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TEST CONDITIONS</th>
<th>MIN(^\langle1\rangle)</th>
<th>TYP(^\langle2\rangle)</th>
<th>MAX(^\langle3\rangle)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} ) Input Offset Voltage</td>
<td>Over Temperature</td>
<td>1.7</td>
<td>7</td>
<td>9</td>
<td>mV</td>
</tr>
<tr>
<td>( TCV_{OS} ) Input Offset Voltage Average Drift</td>
<td></td>
<td>5</td>
<td></td>
<td>5 ( \mu V/^\circ C )</td>
<td></td>
</tr>
<tr>
<td>( I_B ) Input Bias Current</td>
<td>Over Temperature</td>
<td>15</td>
<td>250</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( I_{OS} ) Input Offset Current</td>
<td>Over Temperature</td>
<td>5</td>
<td>50</td>
<td>150</td>
<td>nA</td>
</tr>
<tr>
<td>( CMRR ) Common Mode Rejection Ratio</td>
<td>0 ( V \leq V_{CM} \leq 4 \ V )</td>
<td>50</td>
<td>65</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( PSRR ) Power Supply Rejection Ratio</td>
<td>2.7 ( V \leq V^+ \leq 5 \ V ) ( V_{O} = 1 \ V, \ V_{CM} = 1 \ V )</td>
<td>50</td>
<td>60</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( V_{CM} ) Input Common-Mode Voltage Range</td>
<td>For CMRR ( \geq 50 ) dB</td>
<td>0</td>
<td>-0.2</td>
<td>4.2</td>
<td>V</td>
</tr>
<tr>
<td>( A_V ) Large Signal Voltage Gain (^\langle3\rangle)</td>
<td>( R_L = 2 \ k\Omega ), Over Temperature</td>
<td>15</td>
<td>100</td>
<td>10</td>
<td>V/mV</td>
</tr>
<tr>
<td>( V_O ) Output Swing</td>
<td>( R_L = 2 \ k\Omega ) to 2.5 V</td>
<td>( V^+ - 300 )</td>
<td>( V^+ - 40 )</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( R_L = 2 \ k\Omega ), Over Temperature</td>
<td>( V^+ - 400 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_L = 2 \ k\Omega ) to 2.5 V</td>
<td>120</td>
<td>300</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>( R_L = 2 \ k\Omega ), Over Temperature</td>
<td>400</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_L = 10 \ k\Omega ) to 2.5 V</td>
<td>( V^+ - 100 )</td>
<td>( V^+ - 10 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_L = 10 \ k\Omega ), Over Temperature</td>
<td>( V^+ - 200 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_L = 2 \ k\Omega ) to 2.5 V</td>
<td>65</td>
<td>180</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( R_L = 2 \ k\Omega ), 125°C</td>
<td>280</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_O ) Output Short Circuit Current</td>
<td>Sourcing, ( V_O = 0 \ V )</td>
<td>5</td>
<td>60</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Sinking, ( V_O = 5 \ V )</td>
<td>10</td>
<td>160</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_S ) Supply Current</td>
<td>Single</td>
<td>130</td>
<td>250</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>Single, Over Temperature</td>
<td></td>
<td>350</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dual (both amps)</td>
<td>210</td>
<td>440</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Dual (both amps), Over Temperature</td>
<td>615</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Quad (all four amps)</td>
<td>410</td>
<td>830</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Quad (all four amps), Over Temperature</td>
<td>1160</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^\langle1\rangle\) All limits are ensured by testing or statistical analysis.

\(^\langle2\rangle\) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

\(^\langle3\rangle\) \( R_L \) is connected to \( V^- \). The output voltage is \( 0.5 \ V \leq V_O \leq 4.5 \ V \).
7.9 5-V AC Electrical Characteristics

Unless otherwise specified, all limits specified for $T_J = 25^\circ\text{C}$, $V^+ = 5\ \text{V}$, $V^- = 0\ \text{V}$, $V_{\text{CM}} = 2.0\ \text{V}$, $V_O = V^+/2$ and $R_L > 1\ \text{M\Omega}$.

<table>
<thead>
<tr>
<th>TEST CONDITIONS</th>
<th>MIN$^{(1)}$</th>
<th>TYP$^{(2)}$</th>
<th>MAX$^{(1)}$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td></td>
<td>1</td>
<td></td>
<td>V/\mu s</td>
</tr>
<tr>
<td>Gain-Bandwidth Product</td>
<td></td>
<td>1</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td></td>
<td>60</td>
<td></td>
<td>Deg</td>
</tr>
<tr>
<td>Gain Margin</td>
<td></td>
<td>10</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input-Referred Voltage Noise</td>
<td></td>
<td>39</td>
<td></td>
<td>nV/\sqrt{Hz}</td>
</tr>
<tr>
<td>Input-Referred Current Noise</td>
<td></td>
<td>0.21</td>
<td></td>
<td>pA/\sqrt{Hz}</td>
</tr>
</tbody>
</table>

$^{(1)}$ All limits are ensured by testing or statistical analysis.
$^{(2)}$ Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
$^{(3)}$ Connected as voltage follower with 3-V step input. Number specified is the slower of the positive and negative slew rates.
7.10 Typical Characteristics

Unless otherwise specified, $V_S = 5\, \text{V}$, single supply, $T_A = 25^\circ\text{C}$.

![Figure 1. Supply Current vs. Supply Voltage (LMV321-N)](image1)
![Figure 2. Input Current vs. Temperature](image2)
![Figure 3. Sourcing Current vs. Output Voltage](image3)
![Figure 4. Sourcing Current vs. Output Voltage](image4)
![Figure 5. Sinking Current vs. Output Voltage](image5)
![Figure 6. Sinking Current vs. Output Voltage](image6)
Typical Characteristics (continued)

Unless otherwise specified, $V_S = 5\, \text{V}$, single supply, $T_A = 25^{\circ}\text{C}$.

- **Figure 7.** Output Voltage Swing vs. Supply Voltage
- **Figure 8.** Input Voltage Noise vs. Frequency
- **Figure 9.** Input Current Noise vs. Frequency
- **Figure 10.** Input Current Noise vs. Frequency
- **Figure 11.** Crosstalk Rejection vs. Frequency
- **Figure 12.** PSRR vs. Frequency
**Typical Characteristics (continued)**

Unless otherwise specified, $V_S = 5\, \text{V}$, single supply, $T_A = 25^\circ\text{C}$.

**Figure 13. CMRR vs. Frequency**

**Figure 14. CMRR vs. Input Common Mode Voltage**

**Figure 15. CMRR vs. Input Common Mode Voltage**

**Figure 16. $\Delta V_{OS}$ vs. CMR**

**Figure 17. $\Delta V_{OS}$ vs. CMR**

**Figure 18. Input Voltage vs. Output Voltage**
Typical Characteristics (continued)

Unless otherwise specified, \( V_S = 5 \) V, single supply, \( T_A = 25^\circ C \).

Figure 19. Input Voltage vs. Output Voltage

Figure 20. Open Loop Frequency Response

Figure 21. Open Loop Frequency Response

Figure 22. Open Loop Frequency Response vs. Temperature

Figure 23. Gain and Phase vs. Capacitive Load

Figure 24. Gain and Phase vs. Capacitive Load
Typical Characteristics (continued)

Unless otherwise specified, $V_S = 5\, \text{V}$, single supply, $T_A = 25\, ^\circ\text{C}$.

**Figure 25. Slew Rate vs. Supply Voltage**

<table>
<thead>
<tr>
<th>Supply Voltage (V)</th>
<th>Slew Rate (V/µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5</td>
<td>0.5</td>
</tr>
<tr>
<td>3.0</td>
<td>0.7</td>
</tr>
<tr>
<td>3.5</td>
<td>0.9</td>
</tr>
<tr>
<td>4.0</td>
<td>1.0</td>
</tr>
<tr>
<td>4.5</td>
<td>1.1</td>
</tr>
<tr>
<td>5.0</td>
<td>1.3</td>
</tr>
</tbody>
</table>

**Figure 26. Non-Inverting Large Signal Pulse Response**

**Figure 27. Non-Inverting Large Signal Pulse Response**

**Figure 28. Non-Inverting Large Signal Pulse Response**

**Figure 29. Non-Inverting Small Signal Pulse Response**

**Figure 30. Non-Inverting Small Signal Pulse Response**
Typical Characteristics (continued)

Unless otherwise specified, $V_S = 5\, \text{V}$, single supply, $T_A = 25^\circ\text{C}$.

\begin{align*}
\text{Figure 31. Non-Inverting Small Signal Pulse Response} & \quad \text{Figure 32. Inverting Large Signal Pulse Response} \\
\text{Figure 33. Inverting Large Signal Pulse Response} & \quad \text{Figure 34. Inverting Large Signal Pulse Response} \\
\text{Figure 35. Inverting Small Signal Pulse Response} & \quad \text{Figure 36. Inverting Small Signal Pulse Response}
\end{align*}
Typical Characteristics (continued)

Unless otherwise specified, $V_S = 5\, \text{V}$, single supply, $T_A = 25^\circ\text{C}$.

Figure 37. Inverting Small Signal Pulse Response

Figure 38. Stability vs. Capacitive Load

Figure 39. Stability vs. Capacitive Load

Figure 40. Stability vs. Capacitive Load

Figure 41. Stability vs. Capacitive Load

Figure 42. THD vs. Frequency
Typical Characteristics (continued)

Unless otherwise specified, \( V_S = 5 \text{ V} \), single supply, \( T_A = 25^\circ \text{C} \).

**Figure 43. Open Loop Output Impedance vs. Frequency**

**Figure 44. Short Circuit Current vs. Temperature (Sinking)**

**Figure 45. Short Circuit Current vs. Temperature (Sourcing)**
8 Detailed Description

8.1 Overview
The LMV358-N/LMV324-N are low voltage (2.7 V to 5.5 V) versions of the dual and quad commodity op amps LM358/LM324 (5 V to 30 V). The LMV321-N is the single channel version. The LMV321-N/LMV358-N/LMV324-N are the most cost effective solutions for applications where low voltage operation, space efficiency, and low price are important. They offer specifications that meet or exceed the familiar LM358/LM324. The LMV321-N/LMV358-N/LMV324-N have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed to power ratio, achieving 1 MHz of bandwidth and 1-V/µs slew rate with low supply current.

8.1.1 Benefits of the LMV321-N/LMV358-N/LMV324-N

8.1.1.1 Size
The small footprints of the LMV321-N/LMV358-N/LMV324-N packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. The low profile of the LMV321-N/LMV358-N/LMV324-N make them possible to use in PCMCIA type III cards.

8.1.1.2 Signal Integrity
Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LMV321-N/LMV358-N/LMV324-N can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

8.1.1.3 Simplified Board Layout
These products help you to avoid using long PC traces in your PC board layout. This means that no additional components, such as capacitors and resistors, are needed to filter out the unwanted signals due to the interference between the long PC traces.

8.1.1.4 Low Supply Current
These devices will help you to maximize battery life. They are ideal for battery powered systems.

8.1.1.5 Low Supply Voltage
Texas Instruments provides ensured performance at 2.7 V and 5 V. These specifications ensure operation throughout the battery lifetime.

8.1.1.6 Rail-to-Rail Output
Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

8.1.1.7 Input Includes Ground
Allows direct sensing near GND in single supply operation.

Protection should be provided to prevent the input voltages from going negative more than −0.3V (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

8.1.1.8 Ease of Use and Crossover Distortion
The LMV321-N/LMV358-N/LMV324-N offer specifications similar to the familiar LM324-N. In addition, the new LMV321-N/LMV358-N/LMV324-N effectively eliminate the output crossover distortion. The scope photos in Figure 46 and Figure 47 compare the output swing of the LMV324-N and the LM324-N in a voltage follower configuration, with $V_S = \pm 2.5V$ and $R_L(=2\,\text{kΩ})$ connected to GND. It is apparent that the crossover distortion has been eliminated in the new LMV324-N.
Overview (continued)

Figure 46. Output Swing of LMV324

Figure 47. Output Swing of LM324

8.2 Functional Block Diagram

![Functional Block Diagram](image)

Figure 48. Each Amplifier

8.3 Feature Description

8.3.1 Capacitive Load Tolerance

The LMV321-N/LMV358-N/LMV324-N can directly drive 200 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, the circuit in Figure 49 can be used.

![Indirect Driving Circuit](image)

Figure 49. Indirectly Driving a Capacitive Load Using Resistive Isolation

In Figure 49, the isolation resistor $R_{ISO}$ and the load capacitor $C_L$ form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of $R_{ISO}$. The bigger the $R_{ISO}$ resistor value, the more stable $V_{OUT}$ will be. Figure 50 is an output waveform of Figure 49 using 620Ω for $R_{ISO}$ and 510 pF for $C_L$. 
The circuit in Figure 51 is an improvement to the one in Figure 49 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 49, the output would be voltage divided by $R_{ISO}$ and the load resistor. Instead, in Figure 51, $R_F$ provides the DC accuracy by using feed-forward techniques to connect $V_{IN}$ to $R_L$. Caution is needed in choosing the value of $R_F$ due to the input bias current of the LMV321-N/LMV358-N/LMV324-N. $C_F$ and $R_{ISO}$ serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of $C_F$. This in turn will slow down the pulse response.

8.3.2 Input Bias Current Cancellation

The LMV321-N/LMV358-N/LMV324-N family has a bipolar input stage. The typical input bias current of LMV321-N/LMV358-N/LMV324-N is 15 nA with 5V supply. Thus a 100 kΩ input resistor will cause 1.5 mV of error voltage. By balancing the resistor values at both inverting and non-inverting inputs, the error caused by the amplifier's input bias current will be reduced. The circuit in Figure 52 shows how to cancel the error caused by input bias current.
**Feature Description (continued)**

![Circuit Diagram](image)

**Figure 52. Cancelling the Error Caused by Input Bias Current**

### 8.4 Device Functional Modes

The LMV321-N/LMV321-N-Q1/LMV358-N/LMV358-N-Q1/LMV324-N/LMV324-N-Q1 are powered on when the supply is connected. They can be operated as a single supply or a dual supply operational amplifier depending on the application.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMV32x-N family of amplifiers is specified for operation from 2.7 V to 5 V (±1.35 V to ±2.5 V). Many of the specifications apply from –40°C to 125°C. They provide ground-sensing inputs as well as rail-to-rail output swing. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

9.2 Typical Applications

9.2.1 Simple Low-Pass Active Filter

A simple active low-pass filter is shown in Figure 53.

![Figure 53. Simple Low-Pass Active Filter](image)

9.2.1.1 Design Requirements

The simple single pole active lowpass filter shown in Figure 53 will pass low frequencies and attenuate frequencies above corner frequency (fc) at a roll-off rate of 20dB/Decade.

9.2.1.2 Detailed Design Procedure

The values of R1, R2, R3 and C1 are selected using the formulas in Figure 54. The low-frequency gain (\(\omega \rightarrow 0\)) is defined by \(-\frac{R_3}{R_1}\). This allows low-frequency gains other than unity to be obtained. The filter has a –20 dB/decade roll-off after its corner frequency fc. R2 should be chosen equal to the parallel combination of R1 and R3 to minimize errors due to bias current. The frequency response of the filter is shown in Figure 55.

\[
A_L = -\frac{R_3}{R_1} \\
\]

\[
f_c = \frac{1}{2\pi R_3 C_1} \\
R_2 = R_1 \parallel R_3
\]

Figure 54. Simple Low-Pass Active Filter Equations
Typical Applications (continued)

9.2.1.3 Application Curves

Note that the single-op-amp active filters are used in the applications that require low quality factor, \( Q \leq 10 \), low frequency \( \leq 5 \) kHz, and low gain \( \leq 10 \), or a small value for the product of gain times \( Q \leq 100 \). The op amp should have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp should have a slew rate that meets the following requirement:

\[
\text{Slew Rate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6} \text{ V/µsec}
\]

where \( \omega_H \) is the highest frequency of interest, and \( V_{OPP} \) is the output peak-to-peak voltage.

9.2.2 Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.

\[
V_{OUT} = \left(\frac{R_1 + R_2}{R_3 + R_4}\right) \frac{R_4}{R_1} V_2 - \frac{R_2}{R_1} V_1 + \left(\frac{R_1 + R_2}{R_3 + R_4}\right) \frac{R_3}{R_1} \frac{V_{OPP}}{2}
\]

for \( R_1 = R_3 \) and \( R_2 = R_4 \)

\[
V_{OUT} = \frac{R_2}{R_1} (V_2 - V_1) + \frac{V_{OPP}}{2}
\]

Figure 56. Difference Amplifier

9.2.3 Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistors \( R_1, R_2, R_3, \) and \( R_4 \). To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.
Typical Applications (continued)

9.2.3.1 Three-Op-Amp Instrumentation Amplifier

The quad LMV324 can be used to build a three-op-amp instrumentation amplifier as shown in Figure 57.

![Figure 57. Three-Op-Amp Instrumentation Amplifier](image)

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100 MΩ. The gain of this instrumentation amplifier is set by the ratio of $R_2/R_1$. $R_3$ should equal $R_1$, and $R_4$ equal $R_2$. Matching of $R_3$ to $R_1$ and $R_4$ to $R_2$ affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making $R_4$ slightly smaller than $R_2$ and adding a trim pot equal to twice the difference between $R_2$ and $R_4$ will allow the CMRR to be adjusted for optimum performance.

9.2.3.2 Two-Op-Amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input-impedance DC differential amplifier (Figure 58). As in the three-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR. $R_4$ should equal $R_1$ and, $R_3$ should equal $R_2$.

![Figure 58. Two-Op-Amp Instrumentation Amplifier](image)

$$V_0 = \left(1 + \frac{R_4}{R_3}\right)(V_2 - V_1), \text{ where } R_1 = R_4 \text{ and } R_2 = R_3$$

As shown: $V_0 = 2(V_2 - V_1)$
Typical Applications (continued)

9.2.3.3 Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using $R_3$ and $R_4$ is implemented to bias the amplifier so the input signal is within the input common-mode voltage range of the amplifier. The capacitor $C_1$ is placed between the inverting input and resistor $R_1$ to block the DC signal going into the AC signal source, $V_{IN}$. The values of $R_1$ and $C_1$ affect the cutoff frequency, $f_c = \frac{1}{2\pi R_1 C_1}$.

As a result, the output signal is centered around mid-supply (if the voltage divider provides $V^+/2$ at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

![Figure 59. Single-Supply Inverting Amplifier](image)

9.2.4 Sallen-Key 2nd-Order Active Low-Pass Filter

The Sallen-Key 2nd-order active low-pass filter is illustrated in Figure 60. The DC gain of the filter is expressed as

$$A_{LP} = \frac{R_3}{R_4} + 1$$

(2)

Its transfer function is

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{s^2 + s \left(\frac{1}{C_1 R_1} + \frac{1}{C_2 R_2}\right) + \frac{A_{LP}}{C_1 R_1 R_2}}$$

(3)

![Figure 60. Sallen-Key 2nd-Order Active Low-Pass Filter](image)
Typical Applications (continued)

9.2.4.1 Detailed Design Procedure

The following paragraphs explain how to select values for $R_1$, $R_2$, $R_3$, $R_4$, $C_1$, and $C_2$ for given filter requirements, such as $A_{LP}$, $Q$, and $f_c$.

The standard form for a 2nd-order low pass filter is

$$\frac{V_{OUT}(s)}{V_{IN}} = \frac{A_{LP} \omega_c^2}{s^2 + \left(\frac{\omega_c}{Q}\right)s + \omega_c^2}$$

(4)

where

$Q$: Pole Quality Factor

$\omega_c$: Corner Frequency

A comparison between Equation 3 and Equation 4 yields

$$\omega_c^2 = \frac{1}{C_1 C_2 R_1 R_2}$$

(5)

$$\frac{\omega_c}{Q} = \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2}$$

(6)

To reduce the required calculations in filter design, it is convenient to introduce normalization into the components and design parameters. To normalize, let $\omega_c = \omega_n = 1$ rad/s, and $C_1 = C_2 = C_n = 1$ F, and substitute these values into Equation 5 and Equation 6. From Equation 5, we obtain

$$R_1 = \frac{1}{R_2}$$

(7)

From Equation 6, we obtain

$$R_2 = \frac{1 \pm \sqrt{1 - 4Q^2(2 - A_{LP})}}{2Q}$$

(8)

For minimum DC offset, $V^+ = V^-$, the resistor values at both inverting and non-inverting inputs should be equal, which means

$$R_1 + R_2 = \frac{R_3 R_4}{R_3 + R_4}$$

(9)

From Equation 2 and Equation 9, we obtain

$$R_3 = \left(R_1 + R_2\right)A_{LP}$$

(10)

$$R_4 = \left(\frac{A_{LP}}{A_{LP} - 1}\right)\left(R_1 + R_2\right)$$

(11)

The values of $C_1$ and $C_2$ are normally close to or equal to

$$C = \frac{10}{f_c} \mu F$$

(12)

As a design example:

Require: $A_{LP} = 2$, $Q = 1$, $f_c = 1$ kHz

Start by selecting $C_1$ and $C_2$. Choose a standard value that is close to

$$C = \frac{10}{f_c} \mu F$$

(13)

$$C_1 = C_2 = \frac{10}{1 \times 10^{-3}} \mu F = 0.01 \mu F$$

(14)
Typical Applications (continued)

From Equation 7, Equation 8, Equation 10, and Equation 11,
\[ R_1 = 1\, \Omega \quad (15) \]
\[ R_2 = 1\, \Omega \quad (16) \]
\[ R_3 = 4\, \Omega \quad (17) \]
\[ R_4 = 4\, \Omega \quad (18) \]

The above resistor values are normalized values with \( \omega_n = 1 \text{ rad/s} \) and \( C_1 = C_2 = C_n = 1\, \text{F} \). To scale the normalized cutoff frequency and resistances to the real values, two scaling factors are introduced, frequency scaling factor \( (k_f) \) and impedance scaling factor \( (k_m) \).

\[ k_f = \frac{\omega_c}{\omega_n} = \frac{2\pi \times 1 \times 10^3}{1} = 2\pi \times 10^3 \]
\[ k_m k_f = \frac{C_n}{C_1} \]
\[ k_m = 1.59 \times 10^4 \quad (19) \]

Scaled values:
\[ R_2 = R_1 = 15.9\, \text{k}\Omega \quad (20) \]
\[ R_3 = R_4 = 63.6\, \text{k}\Omega \quad (21) \]
\[ C_1 = C_2 = 0.01\, \text{µF} \quad (22) \]

An adjustment to the scaling may be made in order to have realistic values for resistors and capacitors. The actual value used for each component is shown in the circuit.

9.2.5 2nd-Order High Pass Filter

A 2nd-order high pass filter can be built by simply interchanging those frequency selective components \( (R_1, R_2, C_1, C_2) \) in the Sallen-Key 2nd-order active low pass filter. As shown in Figure 61, resistors become capacitors, and capacitors become resistors. The resulted high pass filter has the same corner frequency and the same maximum gain as the previous 2nd-order low pass filter if the same components are chosen.

![Sallen-Key 2nd-Order Active High-Pass Filter](image)

Figure 61. Sallen-Key 2nd-Order Active High-Pass Filter

9.2.6 State Variable Filter

A state variable filter requires three op amps. One convenient way to build state variable filters is with a quad op amp, such as the LMV324 (Figure 62).
Typical Applications (continued)

This circuit can simultaneously represent a low-pass filter, high-pass filter, and bandpass filter at three different outputs. The equations for these functions are listed below. It is also called "Bi-Quad" active filter as it can produce a transfer function which is quadratic in both numerator and denominator.

\[
V_{LP} = \left(\frac{2R_3}{R_2 + R_3}\right)\frac{1}{S^2 + \frac{1}{R^2C^2}} V_{IN}
\]

\[
V_{HP} = \left(\frac{2R_3}{R_2 + R_3}\right)\frac{S^2}{S^2 + \frac{1}{R^2C^2}} V_{IN}
\]

\[
V_{BP} = \left(\frac{2R_3}{R_2 + R_3}\right)\frac{1}{S^2 + \frac{1}{R^2C^2}} V_{IN}
\]

where for all three filters,

\[
Q = \frac{R_2 + R_3}{2R_2}
\]

\[
\omega_0 = \frac{1}{RC} \quad \text{(resonant frequency)}
\]

9.2.6.1 Detailed Design Procedure

Assume the system design requires a bandpass filter with \(f_o = 1\) kHz and \(Q = 50\). What needs to be calculated are capacitor and resistor values.

First choose convenient values for \(C_1\), \(R_1\) and \(R_2\):

\[
C_1 = 1200 \, \text{pF}
\]
Typical Applications (continued)

\[ 2R_2 = R_1 = 30 \, \text{k}\Omega \]  
(27)

Then from Equation 24,

\[ R_3 = R_2 \times (2Q-1) \]

\[ R_3 = 15 \, \text{k}\Omega \times (2 \times 50 - 1) \]

\[ = 1.5 \, \text{M}\Omega \]  
(28)

From Equation 25,

\[ R = \frac{1}{\omega_0 C_1} \]

\[ R = \frac{1}{(2 \pi \times 10^3)(1.2 \times 10^{-9})} \]

\[ = 132.7 \, \text{k}\Omega \]  
(29)

From the above calculated values, the midband gain is \( H_0 = R_3/R_2 = 100 \) (40 dB). The nearest 5% standard values have been added to Figure 62.

9.2.7 Pulse Generators and Oscillators

A pulse generator is shown in Figure 63. Two diodes have been used to separate the charge and discharge paths to capacitor C.

When the output voltage \( V_O \) is first at its high, \( V_{OH} \), the capacitor C is charged toward \( V_{OH} \) through \( R_2 \). The voltage across C rises exponentially with a time constant \( \tau = R_2C \), and this voltage is applied to the inverting input of the op amp. Meanwhile, the voltage at the non-inverting input is set at the positive threshold voltage \( (V_{TH^+}) \) of the generator. The capacitor voltage continually increases until it reaches \( V_{TH^-} \), at which point the output of the generator will switch to its low, \( V_{OL} \), which 0V is in this case. The voltage at the non-inverting input is switched to the negative threshold voltage \( (V_{TH^-}) \) of the generator. The capacitor then starts to discharge toward \( V_{OL} \) exponentially through \( R_1 \), with a time constant \( \tau = R_1C \). When the capacitor voltage reaches \( V_{TH^-} \), the output of the pulse generator switches to \( V_{OH} \). The capacitor starts to charge, and the cycle repeats itself.
Typical Applications (continued)

As shown in the waveforms in Figure 64, the pulse width ($T_1$) is set by $R_2$, $C$ and $V_{OH}$, and the time between pulses ($T_2$) is set by $R_1$, $C$ and $V_{OL}$. This pulse generator can be made to have different frequencies and pulse width by selecting different capacitor value and resistor values.

Figure 65 shows another pulse generator, with separate charge and discharge paths. The capacitor is charged through $R_1$ and is discharged through $R_2$. 

Figure 64. Waveforms of the Circuit in Figure 16

$$V_{TH+} = \frac{1}{3}(V^+ + V_{OH})$$
$$V_{TH-} = \frac{1}{3}V^+$$

$$T_1 = R_2 C \ln \frac{3V_{OH} - V_{OL} - V^+}{2V_{OH} - V^+}$$
$$T_2 = R_1 C \ln \frac{3V_{OL} - V_{OH} - V^+}{2V_{OL} - V^+}$$

$$T_1 = R_2 C \ln \frac{3V_{OH} - V^+}{2V_{OH} - V^+}$$
$$T_2 = R_1 C \ln \left(1 + \frac{V_{OH}}{V^+}\right)$$

When $V_{OL} = 0$V
Typical Applications (continued)

Figure 65. Pulse Generator

Figure 66 is a squarewave generator with the same path for charging and discharging the capacitor.

Figure 66. Squarewave Generator

9.2.8 Current Source and Sink

The LMV321-N/LMV358-N/LMV324-N can be used in feedback loops which regulate the current in external PNP transistors to provide current sources or in external NPN transistors to provide current sinks.

9.2.8.1 Fixed Current Source

A multiple fixed current source is shown in Figure 67. A voltage \( V_{\text{REF}} = 2V \) is established across resistor \( R_3 \) by the voltage divider \((R_3 \text{ and } R_4)\). Negative feedback is used to cause the voltage drop across \( R_1 \) to be equal to \( V_{\text{REF}} \). This controls the emitter current of transistor \( Q_1 \) and if we neglect the base current of \( Q_1 \) and \( Q_2 \), essentially this same current is available out of the collector of \( Q_1 \).

Large input resistors can be used to reduce current loss and a Darlington connection can be used to reduce errors due to the \( \beta \) of \( Q_1 \).

The resistor, \( R_2 \), can be used to scale the collector current of \( Q_2 \) either above or below the 1 mA reference value.
9.2.8.2 High Compliance Current Sink

A current sink circuit is shown in Figure 68. The circuit requires only one resistor ($R_E$) and supplies an output current which is directly proportional to this resistor value.
Typical Applications (continued)

9.2.9 Power Amplifier

A power amplifier is illustrated in Figure 69. This circuit can provide a higher output current because a transistor follower is added to the output of the op amp.

![Figure 69. Power Amplifier](image)

9.2.10 LED Driver

The LMV321-N/LMV358-N/LMV324-N can be used to drive an LED as shown in Figure 70.

![Figure 70. LED Driver](image)

9.2.11 Comparator With Hysteresis

The LMV321-N/LMV358-N/LMV324-N can be used as a low power comparator. Figure 71 shows a comparator with hysteresis. The hysteresis is determined by the ratio of the two resistors.

\[
\begin{align*}
V_{TH+} &= V_{REF}(1+R_1/R_2)+V_{OH}(1+R_2/R_1) \\
V_{TH-} &= V_{REF}(1+R_1/R_2)+V_{OL}(1+R_2/R_1) \\
V_H &= (V_{OH}-V_{OL})(1+R_2/R_1)
\end{align*}
\]

where

- \(V_{TH+}\): Positive Threshold Voltage
- \(V_{TH-}\): Negative Threshold Voltage
- \(V_{OH}\): Output Voltage at High
- \(V_{OL}\): Output Voltage at Low
- \(V_H\): Hysteresis Voltage

Since LMV321-N/LMV358-N/LMV324-N have rail-to-rail output, the \((V_{OH}-V_{OL})\) is equal to \(V_S\), which is the supply voltage.

\[
V_H = V_S/(1+R_2/R_1)
\]
Typical Applications (continued)

The differential voltage at the input of the op amp should not exceed the specified absolute maximum ratings. For real comparators that are much faster, we recommend you use Texas Instruments's LMV331/LMV93/LMV339, which are single, dual and quad general purpose comparators for low voltage operation.

![Comparator with Hysteresis](image)

**Figure 71. Comparator with Hysteresis**

10 Power Supply Recommendations

The LMV3xx-N is specified for operation from 2.7 V to 5.5 V; many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the Layout Guidelines section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.

- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to Circuit Board Layout Techniques, SLOA089.

- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Layout Example.

- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
11.2 Layout Example

Figure 72. Operational Amplifier Board Layout for Noninverting Configuration

- Run the input trace far away from the supply lines.
- Place components close to device and to each other to reduce parasitic errors.
- Use a low ESR ceramic bypass capacitor.

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12 Device and Documentation Support

12.1 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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12.2 Trademarks
All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — Ti Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
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## Orderable Device

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<th>Package Drawing</th>
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<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
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</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LMV321-N, LMV321-N-Q1, LMV324-N, LMV324-N-Q1, LMV358-N, LMV358-N-Q1:**
- Catalog: LMV321-N, LMV324-N, LMV358-N
Automotive: LMV321-N-Q1, LMV324-N-Q1, LMV358-N-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

- **Reel Diameter**

#### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Sprocket Holes**
- **User Direction of Feed**
- **Pocket Quadrants**

*All dimensions are nominal.

<table>
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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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*All dimensions are nominal

### TAPE AND REEL BOX DIMENSIONS

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<th>Package Drawing</th>
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
EXAMPLE BOARD LAYOUT
SOT-23 - 1.45 mm max height
SMALL OUTLINE TRANSISTOR

NOTES: (continued)
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AB.
NOTES:  
A. All linear dimensions are in millimeters. 
B. This drawing is subject to change without notice. 
C. Publication IPC-7351 is recommended for alternate designs. 
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations. 
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.  
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.  
E. Falls within JEDEC MO-153
NOTES:  
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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