The LMV393-N is available in 8-pin SOIC and VSSOP packages. The LMV339-N is available in 14-pin SOIC and TSSOP packages.

The LMV331-N/393-N/339-N is the most cost-effective solution where space, low voltage, low power, and price are the primary specification in circuit design for portable consumer products. They offer specifications that meet or exceed the familiar LM393/339 at a fraction of the supply current.

The chips are built with TI’s advanced Submicron Silicon-Gate BiCMOS process. The LMV331-N/393-N/339-N have bipolar input and output stages for improved noise performance.

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMV331-N</td>
<td>SC70 (5)</td>
<td>2.00 mm × 1.25 mm</td>
</tr>
<tr>
<td></td>
<td>SOT-23 (5)</td>
<td>2.90 mm × 1.6 mm</td>
</tr>
<tr>
<td>LMV339-N</td>
<td>SOIC (14)</td>
<td>8.65 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (14)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
<tr>
<td>LMV393-N</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (February 2013) to Revision H Page

• Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ............................ 1
5 Pin Configuration and Functions

### Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>LMV331-N DVB,DCK</td>
<td>LMV339-N D,DGK</td>
</tr>
<tr>
<td>+IN</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>+IN A</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>+IN B</td>
<td>-</td>
<td>5</td>
</tr>
<tr>
<td>+IN C</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>+IN D</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>-IN</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>-IN A</td>
<td>-</td>
<td>2</td>
</tr>
<tr>
<td>-IN B</td>
<td>-</td>
<td>6</td>
</tr>
<tr>
<td>-IN C</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>-IN D</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>OUT</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>OUT A</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>OUT B</td>
<td>-</td>
<td>7</td>
</tr>
<tr>
<td>OUT C</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>OUT D</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>V+</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>V-</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>
# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Input Voltage</td>
<td>±Supply Voltage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage on any pin (referred to V(^-) pin)</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Soldering Information</td>
<td>235</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Infrared or Convection (20 sec)</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature (^{(3)})</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature, T(_{stg})</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.

(3) The maximum power dissipation is a function of \(T_{J(MAX)}\), \(\theta_{JA}\). The maximum allowable power dissipation at any ambient temperature is \(P_D = (T_{J(MAX)} - T_A)/\theta_{JA}\). All numbers apply for packages soldered directly onto a PC board.

## 6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Voltage (ESD)</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±800</td>
<td>V</td>
</tr>
<tr>
<td>Machine model</td>
<td>±120</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>2.7</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>Temperature Range(^{(2)})</td>
<td>−40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Recommended Operating Conditions**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The maximum power dissipation is a function of \(T_{J(MAX)}\), \(\theta_{JA}\). The maximum allowable power dissipation at any ambient temperature is \(P_D = (T_{J(MAX)} - T_A)/\theta_{JA}\). All numbers apply for packages soldered directly onto a PC board.

## 6.4 Thermal Information

<table>
<thead>
<tr>
<th>Thermal Metric(^{(1)})</th>
<th>LMV331-N</th>
<th>LMV339-N</th>
<th>LMV393-N</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>478</td>
<td>265</td>
<td>145</td>
<td>155</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the **IC Package Thermal Metrics** application report, SPRA953.

## 6.5 2.7-V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for \(T_J = 25°C\), \(V^+ = 2.7V\), \(V^- = 0V\).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TEST CONDITIONS</th>
<th>MIN (^{(1)})</th>
<th>TYP (^{(2)})</th>
<th>MAX (^{(1)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{OS})</td>
<td>Input Offset Voltage</td>
<td></td>
<td>1.7</td>
<td>7</td>
<td>mV</td>
</tr>
<tr>
<td>TCV(_{OS})</td>
<td>Input Offset Voltage Average Drift</td>
<td>At the temperature extremes</td>
<td>5</td>
<td></td>
<td>μV/°C</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
### 2.7-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for \(T_J = 25°C, V^+ = 2.7V, V^- = 0V\).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN (1)</th>
<th>TYP (2)</th>
<th>MAX (1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_B)</td>
<td>Input Bias Current</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Input Offset Current</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{CM})</td>
<td>Input Voltage Range</td>
<td></td>
<td></td>
<td>−0.1</td>
<td>V</td>
</tr>
<tr>
<td>(V_{SAT})</td>
<td>Saturation Voltage</td>
<td></td>
<td></td>
<td>120</td>
<td>mV</td>
</tr>
<tr>
<td>(I_{O})</td>
<td>Output Sink Current</td>
<td></td>
<td></td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>(I_S)</td>
<td>Supply Current</td>
<td></td>
<td></td>
<td>40</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Output Offset Current</td>
<td></td>
<td></td>
<td>150</td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Output Leakage Current</td>
<td></td>
<td></td>
<td>.003</td>
<td>(\mu)A</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 6.6 2.7-V AC Electrical Characteristics

\(T_J = 25°C, V^+ = 2.7\) V, \(R_L = 5.1\) kΩ, \(V^- = 0\) V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN (1)</th>
<th>TYP (2)</th>
<th>MAX (1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{PHL})</td>
<td>Propagation Delay (High to Low)</td>
<td></td>
<td></td>
<td>1000</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 10 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 100 mV</td>
<td></td>
<td></td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{PLH})</td>
<td>Propagation Delay (Low to High)</td>
<td></td>
<td></td>
<td>500</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 10 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 100 mV</td>
<td></td>
<td></td>
<td>400</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

### 6.7 5-V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for \(T_J = 25°C, V^+ = 5\) V, \(V^- = 0\) V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN (1)</th>
<th>TYP (2)</th>
<th>MAX (1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OS})</td>
<td>Input Offset Voltage</td>
<td>1.7</td>
<td>7</td>
<td>9</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(TC_{VOS})</td>
<td>Input Offset Voltage Average Drift</td>
<td>5</td>
<td></td>
<td></td>
<td>(\mu)V/°C</td>
</tr>
<tr>
<td>(I_B)</td>
<td>Input Bias Current</td>
<td>25</td>
<td>250</td>
<td>400</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{OS})</td>
<td>Input Offset Current</td>
<td>2</td>
<td>50</td>
<td>150</td>
<td>nA</td>
</tr>
<tr>
<td>(V_{CM})</td>
<td>Input Voltage Range</td>
<td>−0.1</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(A_V)</td>
<td>Voltage Gain</td>
<td>4.2</td>
<td></td>
<td></td>
<td>V/mV</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
5-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for $T_J = 25^\circ C$, $V^+ = 5$ V, $V^- = 0$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN (1)</th>
<th>TYP (2)</th>
<th>MAX (1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{sat}$ Saturation Voltage</td>
<td>$I_{SINK} \leq 4$ mA At the temperature extremes</td>
<td>200</td>
<td>400</td>
<td>700</td>
<td>mV</td>
</tr>
<tr>
<td>$I_O$ Output Sink Current</td>
<td>$V_O \leq 1.5$V</td>
<td>84</td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_S$ Supply Current LMV331-N</td>
<td>60 At the temperature extremes</td>
<td>100</td>
<td>200</td>
<td>250</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>LMV393-N Both Comparators</td>
<td>170</td>
<td>300</td>
<td>350</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LMV339-N All four Comparators</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>.003 At the temperature extremes</td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

6.8 5-V AC Electrical Characteristics

$T_J = 25^\circ C$, $V^+ = 5$ V, $R_L = 5.1$ kΩ, $V^- = 0$ V.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN (1)</th>
<th>TYP (2)</th>
<th>MAX (1)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PHL}$ Propagation Delay (High to Low)</td>
<td>Input Overdrive = 10 mV</td>
<td>600</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 100 mV</td>
<td>200</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$ Propagation Delay (Low to High)</td>
<td>Input Overdrive = 10 mV</td>
<td>450</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>Input Overdrive = 100 mV</td>
<td>300</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
6.9 Typical Characteristics

Unless otherwise specified, $V_S = +5V$, single supply, $T_A = 25^\circ C$

---

**Figure 1. Supply Current vs. Supply Voltage Output High (LMV331-N)**

**Figure 2. Supply Current vs. Supply Voltage Output Low (LMV331-N)**

**Figure 3. Output Voltage vs. Output Current at 5-V Supply**

**Figure 4. Output Voltage vs. Output Current at 2.7-V Supply**

**Figure 5. Input Bias Current vs. Supply Voltage**

**Figure 6. Response Time vs. Input Overdrive Negative Transition**
Typical Characteristics (continued)

Unless otherwise specified, $V_S = +5V$, single supply, $T_A = 25^\circ C$

Figure 7. Response Time for Input Overdrive Positive Transition

Figure 8. Response Time vs. Input Overdrive Negative Transition

Figure 9. Response Time for Input Overdrive Positive Transition
7 Detailed Description

7.1 Overview
The LMV331-N/393-N/339-N comparators feature a supply voltage range of 2.7 V to 5 V with a low supply current of 55 μA/channel with propagation delays as low as 200ns. They are available in small, space-saving packages, which makes these comparators versatile for use in a wide range of applications, from portable to industrial. The open collector output configuration allows the device to be used in wired-OR configurations, such as a window comparators.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Open Collector Output
The output of the LMV331-N/393-N/339-N series is the uncommitted collector of a grounded-emitter NPN output transistor, which requires a pull-up resistor to a positive supply voltage for the output to switch properly. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted V+ supply voltage range. The output pull-up resistor should be chosen high enough so as to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever load circuitry is used on the comparator output. On the LMV331-N/393-N/339-N the pull-up resistor should range between 1 kΩ to 10 kΩ.

7.3.2 Ground Sensing Input
The LMV331-N/393-N/339-N has a typical input common mode voltage range of −0.1V below the ground to 0.8V below Vcc.

7.4 Device Functional Modes
A basic comparator circuit is used for converting analog signals to a digital output.
The output is HIGH when the voltage on the non-inverting (+IN) input is greater than the inverting (-IN) input.
The output is LOW when the voltage on the non-inverting (+IN) input is less than the inverting (-IN) input.
The inverting input (-IN) is also commonly referred to as the "reference" or "VREF" input.
8 Application and Implementation

8.1 Application Information

8.1.1 Basic Comparator

The comparator compares the input voltage \( V_{\text{IN}} \) at the non-inverting pin to the reference voltage \( V_{\text{REF}} \) at the inverting pin. If \( V_{\text{IN}} \) is less than \( V_{\text{REF}} \), the output voltage \( V_{\text{O}} \) is at the saturation voltage. On the other hand, if \( V_{\text{IN}} \) is greater than \( V_{\text{REF}} \), the output voltage \( V_{\text{O}} \) is at \( V_{\text{CC}} \).

8.1.2 Comparator With Hysteresis

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by the addition of hysteresis or positive feedback.

8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage \( V_{\text{CC}} \) of the comparator. When \( V_{\text{IN}} \) at the inverting input is less than \( V_{\text{a}1} \), the voltage at the non-inverting node of the comparator \( (V_{\text{IN}} < V_{\text{a}1}) \), the output voltage is high (for simplicity assume \( V_{\text{O}} \) switches as high as \( V_{\text{CC}} \)). The three network resistors can be represented as \( R_1 \| R_3 \) in series with \( R_2 \). The lower input trip voltage \( V_{\text{a}1} \) is defined as:

\[
V_{\text{a}1} = \frac{V_{\text{CC}} R_2}{(R_1 \| R_3) + R_2}
\]  

(1)

When \( V_{\text{IN}} \) is greater than \( V_{\text{a}} \) \( (V_{\text{IN}} > V_{\text{a}}) \), the output voltage is low very close to ground. In this case the three network resistors can be presented as \( R_2 \| R_3 \) in series with \( R_1 \). The upper trip voltage \( V_{\text{a}2} \) is defined as:

\[
V_{\text{a}2} = \frac{V_{\text{CC}}(R_2 \| R_3)}{R_1 + (R_2 \| R_3)}
\]  

(2)
Application Information (continued)

The total hysteresis provided by the network is defined as:

$$\Delta V_a = V_{a1} - V_{a2}$$  \hspace{1cm} (3)

To assure that the comparator will always switch fully to $V_{CC}$ and not be pulled down by the load the resistors values should be chosen as follow:

$$R_{\text{PULL-UP}} << R_{\text{LOAD}}$$ \hspace{1cm} (4)

and

$$R_1 > R_{\text{PULL-UP}}.$$ \hspace{1cm} (5)

8.1.2.1.1 Non-inverting Comparator With Hysteresis

Non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference ($V_{\text{ref}}$) at the inverting input. When $V_{in}$ is low, the output is also low. For the output to switch from low to high, $V_{in}$ must rise up to $V_{in1}$ where $V_{in1}$ is calculated by:

$$V_{in1} = \frac{V_{\text{ref}} (R_1 + R_2)}{R_2}$$ \hspace{1cm} (6)

When $V_{in}$ is high, the output is also high. To make the comparator switch back to its low state, $V_{in}$ must equal $V_{\text{ref}}$. $V_{in}$ can be calculated by:

$$V_{in2} = \frac{V_{\text{ref}} (R_1 + R_2) - V_{CC} R_1}{R_2}$$ \hspace{1cm} (7)

The hysteresis of this circuit is the difference between $V_{in1}$ and $V_{in2}$. 

---

Figure 11. Inverting Comparator With Hysteresis
Application Information (continued)

$$\Delta V_{in} = V_{CC} R_1 / R_2$$  \hspace{1cm} (8)

Figure 12. Noninverting Comparator With Hysteresis

Figure 13. Hysteresis Threshold Points

8.1.3 ORing the Output

By the inherit nature of an open-collector comparator, the outputs of several comparators can be tied together with a shared pull-up resistor to $V_{CC}$. If one or more of the comparators outputs goes low, the output $V_O$ will go low.
8.1.4 Driving CMOS and TTL

The output of the comparator is capable of driving CMOS and TTL Logic circuits. The pull-up resistor may be pulled-up to any voltage equal to, or less than the supply voltage on V+. However, it must not be pulled-up to a voltage higher than V+.
8.1.5 AND Gates

The comparator can be used as three input AND gate. The operation of the gate is as follows:

The resistor divider at the inverting input establishes a reference voltage at that node. The non-inverting input is the sum of the voltages at the inputs divided by the voltage dividers. The output will go high only when all three inputs are high, casing the voltage at the non-inverting input to go above that at inverting input. The circuit values shown work for a 0 equal to ground and a 1 equal to 5 V.

The resistor values can be altered if different logic levels are desired. If more inputs are required, diodes are recommended to improve the voltage margin when all but one of the inputs are high.

8.1.6 OR Gates

A three input OR gate is achieved from the basic AND gate simply by increasing the resistor value connected from the inverting input to \( V_{cc} \), thereby reducing the reference voltage.

A logic 1 at any of the inputs will produce a logic 1 at the output.
Application Information (continued)

8.1.7 Large Fan-In Gate

Extra logic inputs may be added by ORing the input with multiple diodes.

Figure 19. Large Fan-In and Gate
8.2 Typical Applications

8.2.1 Squarewave Oscillator

**Figure 20. Squarewave Oscillator**

**8.2.1.1 Design Requirements**

Comparators are ideal for oscillator applications. This square wave generator uses the minimum number of components. The output frequency is set by the RC time constant of the capacitor $C_1$ and the resistor in the negative feedback $R_4$. The maximum frequency is limited only by the large signal propagation delay of the comparator in addition to any capacitive loading at the output, which would degrade the output slew rate.

**8.2.1.2 Detailed Design Procedure**

To analyze the circuit, assume that the output is initially high. For this to be true, the voltage at the inverting input $V_c$ has to be less than the voltage at the non-inverting input $V_a$. For $V_c$ to be low, the capacitor $C_1$ has to be discharged and will charge up through the negative feedback resistor $R_4$. When it has charged up to value equal to the voltage at the positive input $V_{a1}$, the comparator output will switch.

$V_{a1}$ will be given by:

$$V_{a1} = \frac{V_{CC} R_2}{R_2 + (R_1//R_2)}$$  \hspace{1cm} (9)
Typical Applications (continued)

If:
\[ R_1 = R_2 = R_3 \]  

Then:
\[ V_{a1} = 2V_{CC}/3 \]  

When the output switches to ground, the value of \( V_a \) is reduced by the hysteresis network to a value given by:
\[ V_{a2} = V_{CC}/3 \]

Capacitor \( C_1 \) must now discharge through \( R_4 \) towards ground. The output will return to its high state when the voltage across the capacitor has discharged to a value equal to \( V_{a2} \).

For the circuit shown, the period for one cycle of oscillation will be twice the time it takes for a single RC circuit to charge up to one half of its final value. The time to charge the capacitor can be calculated from:
\[ V_C = V_{max} e^{-t/RC} \]  

Where \( V_{max} \) is the max applied potential across the capacitor = \( 2V_{CC}/3 \)
and \( V_C = V_{max}/2 = V_{CC}/3 \)

One period will be given by:
\[ 1/freq = 2t \]  

or calculating the exponential gives:
\[ 1/freq = 2(0.694) R_4 C_1 \]  

Resistors \( R_3 \) and \( R_4 \) must be at least two times larger than \( R_5 \) to ensure that \( V_O \) will go all the way up to \( V_{CC} \) in the high state. The frequency stability of this circuit should strictly be a function of the external components.

8.2.1.3 Application Curve

![Figure 22. Waveforms for Circuit in Typical Applications](image)
Typical Applications (continued)

8.2.2 Crystal Controlled Oscillator

![Crystal Controlled Oscillator Diagram]

Figure 23. Crystal Controlled Oscillator

A simple yet very stable oscillator that generates a clock for slower digital systems can be obtained by using a resonator as the feedback element. It is similar to the squarewave oscillator, except that the positive feedback is obtained through a quartz crystal. The circuit oscillates when the transmission through the crystal is at a maximum, so the crystal in its series-resonant mode.

The value of $R_1$ and $R_2$ are equal so that the comparator will switch symmetrically about $+V_{CC}/2$. The RC constant of $R_3$ and $C_1$ is set to be several times greater than the period of the oscillating frequency, insuring a 50% duty cycle by maintaining a DC voltage at the inverting input equal to the absolute average of the output waveform.

When specifying the crystal, be sure to order series resonant with the desired temperature coefficient.
Typical Applications (continued)

8.2.3 Pulse Generator With Variable Duty Cycle

The pulse generator with variable duty cycle is just a minor modification of the basic square wave generator. Providing a separate charge and discharge path for capacitor $C_1$ generates a variable duty cycle. One path, through $R_2$ and $D_2$ will charge the capacitor and set the pulse width ($t_1$). The other path, $R_1$ and $D_1$ will discharge the capacitor and set the time between pulses ($t_2$).

By varying resistor $R_1$, the time between pulses of the generator can be changed without changing the pulse width. Similarly, by varying $R_2$, the pulse width will be altered without affecting the time between pulses. Both controls will change the frequency of the generator. The pulse width and time between pulses can be found from:

$$V_1 = V_{\text{max}} \left(1 - e^{-t_1 / R_4 C_1}\right) \quad \text{rise time}$$

$$V_1 = V_{\text{max}} e^{-t_2 / R_5 C_1} \quad \text{fall time}$$

Where

$$V_{\text{max}} = \frac{2 V_{CC}}{3}$$

and

$$V_1 = \frac{V_{\text{max}}}{3} = \frac{V_{CC}}{3}$$

Which gives

$$\frac{1}{2} = e^{-t_1 / R_4 C_1}$$

$t_2$ is then given by:

$$\frac{1}{2} = e^{-t_2 / R_5 C_1}$$

(16)
Typical Applications (continued)

Solving these equations for \( t_1 \) and \( t_2 \)

\[
\begin{align*}
    t_1 &= R_4 C_1 \ln 2 \\
    t_2 &= R_5 C_1 \ln 2
\end{align*}
\]  

(17)  

(18)  

These terms will have a slight error due to the fact that \( V_{\text{max}} \) is not exactly equal to \( 2/3 \ V_{\text{CC}} \) but is actually reduced by the diode drop to:

\[
\begin{align*}
    V_{\text{max}} &= \frac{2}{3} (V_{\text{CC}} - V_{\text{BE}}) \\
    \frac{1}{2 (1 - V_{\text{BE}})} &= e^{-t_1/R_4 C_1} \\
    \frac{1}{2 (1 - V_{\text{BE}})} &= e^{-t_2/R_5 C_1}
\end{align*}
\]  

(19)  

(20)  

(21)  

8.2.4 Positive Peak Detector

![Figure 25. Positive Peak Detector](image)

Positive peak detector is basically the comparator operated as a unit gain follower with a large holding capacitor from the output to ground. Additional transistor is added to the output to provide a low impedance current source. When the output of the comparator goes high, current is passed through the transistor to charge up the capacitor. The only discharge path will be the 1-M\( \Omega \) resistor shunting \( C_1 \) and any load that is connected to the output. The decay time can be altered simply by changing the 1-M\( \Omega \) resistor. The output should be used through a high impedance follower to avoid loading the output of the peak detector.

8.2.5 Negative Peak Detector

![Figure 26. Negative Peak Detector](image)

For the negative detector, the output transistor of the comparator acts as a low impedance current sink. The only discharge path will be the 1-M\( \Omega \) resistor and any load impedance used. Decay time is changed by varying the 1-M\( \Omega \) resistor.
9 Power Supply Recommendations

The TLV170x is specified for operation from 2.2 V to 36 V (±1.1 to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

CAUTION

Supply voltages larger than 5.5 V can permanently damage the device; see the Specifications section.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the Layout Guidelines section.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, the following layout guidelines should be maintained:

• Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the comparator.

• Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.

• Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to SLOA089, Circuit Board Layout Techniques.

• In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

• Place the external components as close to the device as possible, as shown in Layout Example.

• Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

• For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. Run the topside ground plane between the output and inputs.
10.2 Layout Example

Run the input traces as far away from the supply lines as possible.

Use low-ESR, ceramic bypass capacitor.

Only needed for dual-supply operation.

Figure 27. Comparator Board Layout
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support
LMV331-N PSPICE Model, SNOM073
LMV339-N PSPICE Model, SNOM074
LMV393-N PSPICE Model, SNOM059

11.2 Documentation Support

11.2.1 Related Documentation
AN-74 - A Quad of Independently Functioning Comparators, SNOA654

11.3 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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11.4 Trademarks
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary
SLYZ022 — *Ti Glossary.*
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# Packaging Information

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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF LMV331-N, LMV393-N :**
• Automotive: LMV331-Q1, LMV393-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
### TAPE AND REEL INFORMATION

#### Reel Dimensions

- **Reel Diameter**: 178.0 mm
- **Reel Width (W1)**: 8.4 mm

#### TAPE Dimensions

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### Quadrant Assignments for Pin 1 Orientation in Tape

- **Q1**: Upper right
- **Q2**: Lower right
- **Q3**: Upper left
- **Q4**: Lower left

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (W1) (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
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## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

8. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
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