FEATURES
The LMX5453 is a drop in replacement for the LMX5452. The LMX5453 has new features added:
- eSCO
- eSCO over USB HCI transport
- Enhanced scatternet
- Interlaced scan
- Flushing
- Audio PCM slave mode support
- Generic PCM configuration
- Compliant with the Bluetooth 2.0 Core Specification
- Better than -80 dBm input sensitivity
- Class 2 operation
- Low power consumption:
  - Accepts external clock or crystal input:
    - Clocking option 12/13 MHz with PLL bypass mode for power reduction
    - 10-20 MHz external clock or crystal network
    - Secondary 32.768 kHz oscillator for low-power modes
    - Advanced power management features
- High integration:
  - Implemented in 0.18 μm CMOS technology
  - RF includes on-chip antenna filter and switch
- On-chip firmware with complete HCI
- Embedded ROM (200K) and Patch RAM (16.6K) memory
- Up to 7 Asynchronous Connection Less (ACL) links
- Support for two simultaneous voice or Extended Synchronous Connection Oriented (eSCO) and Synchronous Connection Oriented (SCO) links.
- Enhanced scatternet
- Interlaced scan
- Flushing
- Audio PCM slave mode support
- Generic PCM configuration
- Fractional-N Sigma/Delta modulator
- Operating voltage range 2.5–3.6V
- I/O voltage range 1.6–3.6V
- 60-pad micro-module BGA package (6.1 mm × 9.1 mm × 1.2 mm)

APPLICATIONS
- Mobile Handsets
- USB Dongles
- Stereo Headsets
- Personal Digital Assistants
- Personal Computers
- Automotive Telematics

DESCRIPTION
The LMX5453 is a highly integrated Bluetooth 2.0 compliant solution. The integrated baseband controller and 2.4 GHz radio combine to form a complete, small form-factor (6.1 mm × 9.1 mm × 1.2 mm) Bluetooth node.

The on-chip memory, ROM, and Patch RAM provide lowest cost and minimize design risk with the flexibility of firmware upgrades.

The firmware supplied in the on-chip ROM supports a complete Bluetooth Link Manager and HCI with communication through a UART or USB interface. This firmware features point-to-point and point-to-multipoint link management, supporting data rates up to 723 kbps.

The radio employs an integrated antenna filter and switch to minimize the number of external components.

The radio has a heterodyne receiver architecture with a low intermediate frequency (IF), which enables the IF filters to be integrated on-chip. The transmitter uses direct IQ-modulation with Gaussian-filtered bit-stream data, a voltage-controlled oscillator (VCO) buffer, and a power amplifier.

The LMX5453 module is lead free and RoHS (Restriction of Hazardous Substances) compliant. For more information on those quality standards, please visit our green compliance website at http://www.national.com/quality/green/
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**INTERFACES**

- Full-duplex UART supporting transfer rates up to 921.6 kbps including baud rate detection for HCI
- Full speed (12 Mbps) USB 2.0 for HCI
- ACCESS.bus and SPI/Microwire for interfacing with external non-volatile memory
- Advanced Audio Interface (AAI) for interfacing with external 8-kHz PCM codec
- Up to 3 GPIO port pins (OP4/PG4, PG6, PG7) controllable by HCI commands
- JTAG based serial on-chip debug interface
- Single Rx/Tx-pad radio interface
**Figure 1. X-ray - Top View**
### SIGNAL DESCRIPTIONS

#### Table 1. Signal Descriptions

<table>
<thead>
<tr>
<th>Pad Name</th>
<th>Pad Location</th>
<th>Type</th>
<th>Default Layout</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1_CKO</td>
<td>F7</td>
<td>O</td>
<td></td>
<td>Crystal 10-20 MHz</td>
</tr>
<tr>
<td>X1_CKI</td>
<td>E7</td>
<td>I</td>
<td></td>
<td>Crystal or External Clock 10-20 MHz</td>
</tr>
<tr>
<td>X2_CKI</td>
<td>F5</td>
<td>I</td>
<td>GND (if not used)</td>
<td>32.768 kHz Crystal Oscillator</td>
</tr>
<tr>
<td>X2_CKO</td>
<td>E5</td>
<td>O</td>
<td>NC (if not used)</td>
<td>32.768 kHz Crystal Oscillator</td>
</tr>
<tr>
<td>RESET_RA#</td>
<td>B8</td>
<td>I</td>
<td></td>
<td>Radio Reset Input (active low)</td>
</tr>
<tr>
<td>B_RESET_RA#</td>
<td>B6</td>
<td>O</td>
<td></td>
<td>Buffered Radio Reset Output (active low)</td>
</tr>
<tr>
<td>RESET_BB#</td>
<td>B7</td>
<td>I</td>
<td></td>
<td>Baseband Controller Reset (active low)</td>
</tr>
<tr>
<td>ENV1</td>
<td>C6</td>
<td>I</td>
<td>NC</td>
<td>ENV1: Environment Select used for manufacturing test only</td>
</tr>
<tr>
<td>TE</td>
<td>A9</td>
<td>I</td>
<td>GND</td>
<td>Test Enable - Used for manufacturing test only</td>
</tr>
<tr>
<td>TST1/DIV2#</td>
<td>B10</td>
<td>I</td>
<td>NC</td>
<td>TST1: Test Mode. Leave not connected to permit use with VTune automatic tuning algorithm. DIV2#: No longer supported</td>
</tr>
<tr>
<td>TST2</td>
<td>C7</td>
<td>I</td>
<td>GND</td>
<td>Test Mode, Connect to GND</td>
</tr>
<tr>
<td>TST3</td>
<td>C8</td>
<td>I</td>
<td>GND</td>
<td>Test Mode, Connect to GND</td>
</tr>
<tr>
<td>TST4</td>
<td>C9</td>
<td>I</td>
<td>GND</td>
<td>Test Mode, Connect to GND</td>
</tr>
<tr>
<td>TST5</td>
<td>D8</td>
<td>I</td>
<td>GND</td>
<td>Test Mode, Connect to GND</td>
</tr>
<tr>
<td>TST6</td>
<td>D9</td>
<td>I</td>
<td>VCO_OUT</td>
<td>Test Input, Connect to VCO_OUT through a zero-ohm resistor to permit use with VTune automatic tuning algorithm</td>
</tr>
<tr>
<td>USB_D-</td>
<td>A3</td>
<td>I</td>
<td></td>
<td>USB Data (negative)</td>
</tr>
<tr>
<td>USB_D+</td>
<td>A2</td>
<td>I</td>
<td></td>
<td>USB Data (positive)</td>
</tr>
<tr>
<td>MDODI(1)</td>
<td>D1</td>
<td>I/O</td>
<td></td>
<td>SPI Master Data Out/Slave Data In</td>
</tr>
<tr>
<td>OP6/SCL/MSK</td>
<td>C1</td>
<td></td>
<td>OP6: I SCL/MSK: I/O</td>
<td>See Table 20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OP6: Pin checked during the start-up sequence for configuration option SCL: ACCESS.Bus Clock MSK: SPI Shift</td>
</tr>
<tr>
<td>OP7/SDA/MDIDO</td>
<td>D4</td>
<td></td>
<td>OP7: I SDA/MDIDO O: I/O</td>
<td>See Table 20</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OP7: Pin checked during the start-up sequence for configuration option SDA: ACCESS.Bus Serial Data MDIDO: SPI Master Data In/Slave Data Out</td>
</tr>
<tr>
<td>OP3/MWCS#</td>
<td>D3</td>
<td></td>
<td>See Table 20 and Table 21</td>
<td>OP3: Pin checked during the start-up sequence for configuration option MWCS#: SPI Slave Select Input (active low)</td>
</tr>
<tr>
<td>OP4/PG4</td>
<td>D6</td>
<td></td>
<td>See Table 20 and Table 21</td>
<td>OP4: Pin checked during the start-up sequence for configuration option PG4: GPIO</td>
</tr>
<tr>
<td>OP5/SFS1</td>
<td>F4</td>
<td>I/O</td>
<td>See Table 20 and Table 21</td>
<td>OP5: Pin checked during the start-up sequence for configuration option SFS1: Audio PCM Interface - Frame Synchronization for second codec</td>
</tr>
<tr>
<td>SCLK</td>
<td>F1</td>
<td>I/O</td>
<td></td>
<td>Audio PCM Interface Clock</td>
</tr>
<tr>
<td>SFS</td>
<td>F2</td>
<td>I/O</td>
<td></td>
<td>Audio PCM Interface Frame Synchronization</td>
</tr>
<tr>
<td>SRD</td>
<td>F3</td>
<td>I</td>
<td></td>
<td>Audio PCM Interface Receive Data Input</td>
</tr>
<tr>
<td>STD</td>
<td>E3</td>
<td>O</td>
<td></td>
<td>Audio PCM Interface Transmit Data Output</td>
</tr>
<tr>
<td>XOSCEN</td>
<td>A6</td>
<td>O</td>
<td></td>
<td>Clock Request. Toggles with X2 (LP0) crystal enable/disable</td>
</tr>
<tr>
<td>PG6</td>
<td>A7</td>
<td>O</td>
<td>See NVS Table 21</td>
<td>GPIO - Default setup USB status indication</td>
</tr>
<tr>
<td>PG7</td>
<td>D2</td>
<td>O</td>
<td>See NVS Table 21</td>
<td>GPIO - Default setup TL (Transport Layer) traffic LED indication</td>
</tr>
</tbody>
</table>

(1) Must use 1k ohm pull up

Submit Documentation Feedback

Product Folder Links: LMX5453

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Table 1. Signal Descriptions (continued)

<table>
<thead>
<tr>
<th>Pad Name</th>
<th>Pad Location</th>
<th>Type</th>
<th>Default Layout</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTS#</td>
<td>C2</td>
<td>I</td>
<td>GND (if not used)</td>
<td>Host Serial Port Clear To Send (active low)</td>
</tr>
<tr>
<td>RXD</td>
<td>B3</td>
<td>I</td>
<td></td>
<td>Host Serial Port Receive Data</td>
</tr>
<tr>
<td>RTS#</td>
<td>B1</td>
<td>O</td>
<td>NC (if not used)</td>
<td>Host Serial Port Request To Send (active low)</td>
</tr>
<tr>
<td>TXD</td>
<td>C3</td>
<td>O</td>
<td></td>
<td>Host Serial Port Transmit Data</td>
</tr>
<tr>
<td>RDY#</td>
<td>A4</td>
<td>I</td>
<td>NC</td>
<td>JTAG Ready Output (active low)</td>
</tr>
<tr>
<td>TCK</td>
<td>B4</td>
<td>I</td>
<td>NC</td>
<td>JTAG Test Clock Input</td>
</tr>
<tr>
<td>TDI</td>
<td>B5</td>
<td>I</td>
<td>NC</td>
<td>JTAG Test Data Input</td>
</tr>
<tr>
<td>TDO</td>
<td>D5</td>
<td>O</td>
<td>NC</td>
<td>JTAG Test Data Output</td>
</tr>
<tr>
<td>TMS</td>
<td>A5</td>
<td>I</td>
<td>NC</td>
<td>JTAG Test Mode Select Input</td>
</tr>
<tr>
<td>VCO_OUT</td>
<td>F8</td>
<td>O</td>
<td></td>
<td>Charge Pump Output, connect to loop filter</td>
</tr>
<tr>
<td>VCO_IN</td>
<td>F9</td>
<td>I</td>
<td></td>
<td>VCO Tuning Input, feedback from loop filter</td>
</tr>
<tr>
<td>ANT</td>
<td>D10</td>
<td>O</td>
<td></td>
<td>RF Antenna, 50-ohm nominal impedance</td>
</tr>
<tr>
<td>VCC_PLL</td>
<td>F6</td>
<td>O</td>
<td></td>
<td>1.8V Core Logic Power Supply Output</td>
</tr>
<tr>
<td>VCC_CORE</td>
<td>C5</td>
<td>O</td>
<td></td>
<td>1.8V Voltage Regulator Output</td>
</tr>
<tr>
<td>VDD_X1</td>
<td>E8</td>
<td>I</td>
<td></td>
<td>Power Supply Crystal Oscillator</td>
</tr>
<tr>
<td>VDD_VCO</td>
<td>F10</td>
<td>I</td>
<td></td>
<td>Power Supply VCO</td>
</tr>
<tr>
<td>VDD_RF</td>
<td>A10</td>
<td>I</td>
<td></td>
<td>Power Supply RF</td>
</tr>
<tr>
<td>VDD_IOR</td>
<td>E6</td>
<td>I</td>
<td></td>
<td>Power Supply I/O Radio/BB</td>
</tr>
<tr>
<td>VDD_IF</td>
<td>A8</td>
<td>I</td>
<td></td>
<td>Power Supply IF</td>
</tr>
<tr>
<td>VCC_USB</td>
<td>A1</td>
<td>I</td>
<td></td>
<td>Power Supply USB Transceiver</td>
</tr>
<tr>
<td>VCC_IOP</td>
<td>E4</td>
<td>I</td>
<td></td>
<td>Power Supply Audio Interface</td>
</tr>
<tr>
<td>VCC_IO</td>
<td>C4</td>
<td>I</td>
<td></td>
<td>Power Supply I/O</td>
</tr>
<tr>
<td>VCC</td>
<td>E1</td>
<td>I</td>
<td></td>
<td>Voltage Regulator Input</td>
</tr>
<tr>
<td>GND_VCO</td>
<td>E9</td>
<td></td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>GND_USB</td>
<td>B2</td>
<td></td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>GND_RF</td>
<td>B9, C10, E10</td>
<td></td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>GND_IF</td>
<td>D7</td>
<td></td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>GND</td>
<td>E2</td>
<td></td>
<td></td>
<td>Ground</td>
</tr>
</tbody>
</table>

(2) Connect to GND if CTS is not used
(3) Treat as No Connect if RTS is not used. Pad required for mechanical stability
Electrical Specifications

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. This device is ESD sensitive. Handling and assembly of this device should be performed at ESD-free workstations. All pads are rated 2 kV. This device operates between -40 and +85°C.

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>–0.2</td>
<td>4.0</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;1&lt;/sub&gt;</td>
<td>–0.2</td>
<td>VCC + 0.2</td>
<td>V</td>
</tr>
<tr>
<td>VDD&lt;sub&gt;RF&lt;/sub&gt;</td>
<td>0.2</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>VDD&lt;sub&gt;IF&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD&lt;sub&gt;X1&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD&lt;sub&gt;VCO&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin&lt;sub&gt;RF&lt;/sub&gt;</td>
<td>0</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>V&lt;sub&gt;ANT&lt;/sub&gt;</td>
<td>1.95</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>T&lt;sub&gt;S&lt;/sub&gt;</td>
<td>–65</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>T&lt;sub&gt;L&lt;/sub&gt;</td>
<td>225</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>T&lt;sub&gt;NOPB&lt;/sub&gt;</td>
<td>260</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>ESD&lt;sub&gt;HBM&lt;/sub&gt;</td>
<td>2000</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ESD&lt;sub&gt;MM&lt;/sub&gt;</td>
<td>200</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ESD&lt;sub&gt;CDM&lt;/sub&gt;</td>
<td>1000</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

(1) Reference IPC/JEDEC J-STD-020C spec.
(2) NOPB = No Pb (No Lead)

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>2.5</td>
<td>2.75</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>T&lt;sub&gt;R&lt;/sub&gt;</td>
<td></td>
<td>10</td>
<td></td>
<td>µS</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>–40</td>
<td>+25</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>VCC&lt;sub&gt;IO&lt;/sub&gt;</td>
<td>1.6</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VCC&lt;sub&gt;USB&lt;/sub&gt;</td>
<td>2.97</td>
<td>3.3</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>VCC&lt;sub&gt;P LL&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD&lt;sub&gt;RF&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD&lt;sub&gt;IF&lt;/sub&gt;</td>
<td>2.5</td>
<td>2.75</td>
<td>3.0</td>
<td>V</td>
</tr>
<tr>
<td>VDD&lt;sub&gt;X1&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD&lt;sub&gt;VCO&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD&lt;sub&gt;I OR&lt;/sub&gt;</td>
<td>1.6</td>
<td>2.75</td>
<td>VDD&lt;sub&gt;RF&lt;/sub&gt;</td>
<td>V</td>
</tr>
<tr>
<td>VCC&lt;sub&gt;I OP&lt;/sub&gt;</td>
<td>1.6</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VCC&lt;sub&gt;CORE&lt;/sub&gt;</td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
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<td>VCC&lt;sub&gt;CORE&lt;/sub&gt;&lt;sub&gt;MAX&lt;/sub&gt;</td>
<td>5</td>
<td>1.8</td>
<td>2.0</td>
<td>mA</td>
</tr>
<tr>
<td>VCC&lt;sub&gt;CORE&lt;/sub&gt;&lt;sub&gt;S&lt;/sub&gt;&lt;sub&gt;HORT&lt;/sub&gt;</td>
<td>1.6</td>
<td>1.8</td>
<td>2.0</td>
<td>V</td>
</tr>
</tbody>
</table>
### Power Supply Requirements\(^{(1)(2)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>During Receive DM5</th>
<th>During Transmit DM5</th>
<th>During Receive DH5</th>
<th>During Transmit DH5</th>
<th>During Receive HV1</th>
<th>During Transmit HV1</th>
<th>Receive Power Supply Current (Receive in Continuous Mode)</th>
<th>Transmit Power Supply Current (Transmit in Continuous Mode)</th>
<th>Power-down Current (Standby, XO off)</th>
<th>Active Mode - Page/Inquiry Scan Enabled</th>
<th>Sniff Mode - Sniff Interval 1.28 sec.</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{RXDM5})</td>
<td>26 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td>34 µA</td>
<td>6 mA</td>
<td>5 mA</td>
</tr>
<tr>
<td>(I_{TXDM5})</td>
<td>27 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{RXDH5})</td>
<td>26 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{TXDH5})</td>
<td>27 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{RXHV1})</td>
<td>12 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{TXHV1})</td>
<td>12 mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{CC-RX})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{CC-TX})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{CC-PWDN})</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65 mA</td>
<td>65 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Power supply requirements are based on Class 2 output power.
(2) \(VCC = 2.75V, T_A = +25°C\)

### DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IH})</td>
<td>Logical 1 Input Voltage High (except oscillator I/O) (1.6V \leq VCC_IO \leq 3.0) (3.0V \leq VCC_IO \leq 3.6)</td>
<td>(0.7 \times VCC_IO \div 2.0)</td>
<td>(0.2 \times VCC_IO \div 0.2)</td>
<td>(VCC_IO)</td>
<td>(V)</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Logical 1 Input Voltage Low (except oscillator I/O) (1.6V \leq VCC_IO \leq 3.0) (3.0V \leq VCC_IO \leq 3.6)</td>
<td>(-0.2)</td>
<td>(-0.2)</td>
<td>(0.25 \times VCC_IO \div 0.8)</td>
<td>(V)</td>
</tr>
<tr>
<td>(I_{OH})(^{(1)})</td>
<td>Logical 1 Output Current (V_{OH} = 2.4V, VCC_IO = 3.0V)</td>
<td>-10</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>(I_{OL})(^{(1)})</td>
<td>Logical 0 Output Current (V_{OL} = 0.4V, VCC_IO = 3.0V)</td>
<td>10</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

(1) Maximum current is 50mA per VCC\_IO/GND pair.

### USB Transceiver

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(VCC_USB)</td>
<td>USB Power Supply Voltage</td>
<td>2.97</td>
<td>3.3</td>
<td>3.63</td>
<td>(V)</td>
</tr>
<tr>
<td>(V_{DI})</td>
<td>Differential Input Sensitivity ((D^+) - (D^-))</td>
<td>-0.2</td>
<td></td>
<td>+0.2</td>
<td>(V)</td>
</tr>
<tr>
<td>(V_{CM})</td>
<td>Differential Common Mode Range</td>
<td>0.8</td>
<td></td>
<td>2.5</td>
<td>(V)</td>
</tr>
<tr>
<td>(V_{SE})</td>
<td>Single Ended Received Threshold</td>
<td>0.8</td>
<td></td>
<td>2.0</td>
<td>(V)</td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Output Low Voltage (R_L = 1.5k, to 3.6V)</td>
<td>0.3</td>
<td></td>
<td></td>
<td>(V)</td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>Output High Voltage</td>
<td>2.8</td>
<td></td>
<td></td>
<td>(V)</td>
</tr>
<tr>
<td>(I_{OZ})</td>
<td>TRI-STATE Data Line Leakage (0V &lt; V_{IN} &lt; 3.3V)</td>
<td>-10</td>
<td></td>
<td>+10</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(C_{TRN})</td>
<td>Transceiver Capacitance</td>
<td>20</td>
<td></td>
<td></td>
<td>(pF)</td>
</tr>
</tbody>
</table>
## RF Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX\textsubscript{sense}</td>
<td>Receive Sensitivity, BER &lt; 0.001</td>
<td>2.402 GHz</td>
<td>–80</td>
<td>–76</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.441 GHz</td>
<td>–80</td>
<td>–76</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.480 GHz</td>
<td>–80</td>
<td>–76</td>
<td>dBm</td>
</tr>
<tr>
<td>PinRF</td>
<td>Maximum Input Level</td>
<td>–10</td>
<td>0</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>IMP \textsuperscript{(2)}, \textsuperscript{(3)}</td>
<td>Intermodulation Performance, ( F_1 = +3 \text{ MHz}, F_2 = +6 \text{ MHz}, P_{p,RF} = -64 \text{ dBm} )</td>
<td>–38</td>
<td>–36</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>RSSI</td>
<td>RSSI Dynamic Range at LNA Input</td>
<td>–72</td>
<td>–52</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>( Z_{RFIN} \textsuperscript{(2)} )</td>
<td>Input Impedance of RF Port (RF_inout), ( Z_{RFIN} = 32 \Omega )</td>
<td></td>
<td>32</td>
<td></td>
<td>( \Omega )</td>
</tr>
<tr>
<td>Return Loss</td>
<td>Return Loss</td>
<td></td>
<td>–8</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>OOB \textsuperscript{(2)}, \textsuperscript{(3)}</td>
<td>Out of Band Blocking Performance, ( P_{p,RF} = -10 \text{ dBm}, 30 \text{ MHz} &lt; F_{CW} &lt; 2 \text{ GHz}, BER &lt; 0.001 )</td>
<td></td>
<td>–10</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–27</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–27</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>–10</td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>

(1) Typical operating conditions are at 2.75V operating voltage and 25°C ambient temperature.

(2) The \( f_0 = -64 \text{ dBm} \) Bluetooth modulated signal, \( f_1 = -39 \text{ dbm} \) sine wave, \( f_2 = -39 \text{ dBm} \) Bluetooth modulated signal, \( f_0 = 2f_1 - f_2 \), and \(|f_2 - f_1| = n \times 1 \text{ MHz} \), where \( n \) is 3, 4, or 5. For the typical case, \( n = 3 \).

(3) Not tested in production.

## Transmitter Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( P_{OUT} \times f_0 \textsuperscript{(2)} )</td>
<td>PA 2nd Harmonic Suppression, Maximum gain setting: ( f_0 = 2402 \text{ MHz}, P_{out} = 4804 \text{ MHz} )</td>
<td>–30</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>( Z_{RFOUT} \textsuperscript{θ} )</td>
<td>RF Output Impedance/Input Impedance of RF Port (RF_inout), ( P_{out} @ 2.5 \text{ GHz} )</td>
<td>47</td>
<td></td>
<td></td>
<td>( \Omega )</td>
</tr>
</tbody>
</table>

(1) Typical operating conditions are at 2.75V operating voltage and 25°C ambient temperature.

(2) Out-of-Band spurs only exist at 2nd and 3rd harmonics of the CW frequency for each channel.

## Synthesizer Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{VCO} )</td>
<td>VCO Frequency Range</td>
<td>2402</td>
<td>2480</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( t_{LACK} )</td>
<td>Lock Time, ( t_0 \pm 20 \text{ kHz} )</td>
<td></td>
<td>120</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
<tr>
<td>( Δf_{offset} \textsuperscript{(1)} )</td>
<td>Initial Carrier Frequency Tolerance, During preamble</td>
<td>–75</td>
<td>0</td>
<td>75</td>
<td>kHz</td>
</tr>
<tr>
<td>( Δf_{drift} \textsuperscript{(1)} )</td>
<td>Initial Carrier Frequency Drift, DH1 data packet, DH3 data packet, DH5 data packet, Drift Rate</td>
<td>–25</td>
<td>0</td>
<td>25</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–40</td>
<td>0</td>
<td>40</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–40</td>
<td>0</td>
<td>40</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–20</td>
<td>0</td>
<td>20</td>
<td>kHz/50 ( \mu\text{s} )</td>
</tr>
<tr>
<td>( t_{O-Tx} )</td>
<td>Transmitter Delay Time, From Tx data to antenna</td>
<td></td>
<td>4</td>
<td></td>
<td>( \mu\text{s} )</td>
</tr>
</tbody>
</table>

(1) Frequency accuracy is dependent on crystal oscillator chosen. The crystal must have a cumulative accuracy of <20 ppm to meet Bluetooth specifications.
Crystal Requirements

The LMX5453 provides an on-chip driver that may be used with an external crystal and capacitors to form an oscillator. Figure 2 shows the recommended crystal circuit. Table 5 specifies the system clock requirements.

The RF local oscillator and internal digital clocks for the LMX5453 are derived from the reference clock at the CLK+ input. This reference may come from either an external clock signal or the oscillator using the on-chip driver.

When the on-chip driver is used, the board- and design dependent capacitance must be considered in tuning the crystal circuit. Equations that provide a close approximation of the crystal tuning capacitance are used as a starting point, but the optimal values will vary with the capacitive properties of the circuit board. As a result, fine tuning of the crystal circuit must be performed experimentally, by testing different values of load capacitance.

Many different crystals can be used with the LMX5453. A key requirement from the Bluetooth specification is a cumulative accuracy of <20 ppm. Additionally, ESR (Equivalent Series Resistance) must be carefully considered. The LMX5453 can support a maximum ESR of 230Ω, but it is recommended to stay <100Ω for best performance over voltage and temperature. See Figure 3 for ESR as part of the crystal circuit for more information. The ESR of the crystal also has an impact on the start-up time of the crystal oscillator circuit. See ** Section 15.0 and Table 18 for system start-up timing.

Crystal

The crystal appears inductive near its resonant frequency. It forms a resonant circuit with its load capacitors. The resonant frequency may be trimmed with the crystal load capacitance.

Load Capacitance

For resonance at the correct frequency, the crystal should be loaded with its specified load capacitance. Load capacitance is a parameter specified by the crystal vendor, typically expressed in pF. The crystal circuit shown in Figure 3 is composed of:

- C1 (motional capacitance)
- R1 (motional resistance)
- L1 (motional inductance)
- C0 (static or shunt capacitance)

The LMX5453 provides some of the load with internal capacitors C_{int} and XOC_{TUNE}. The remainder must come from the external capacitors labeled Ct1 and Ct2 shown in Figure 2. For best noise performance, Ct1 and Ct2 should have the same the value.

The value of XOC_{TUNE} can be programmed in register 2. There are 7 bits of tuning for XOC_{TUNE}. The default value is 0028h, which results in an additional 2.6 pF internal capacitance. This register can be used in production testing for additional tuning, if necessary. See Table 19 for the range of XOC_{TUNE} values.

The crystal load capacitance (C_L) is calculated as:

\[ C_L = C_{int} + XOC_{TUNE} + Ct1 / Ct2 \]  \hspace{1cm} (1)

The C_L above does not include the crystal internal self capacitance C_0 as shown in Figure 3, so the total capacitance is:

\[ C_{total} = C_L + C_0 \]  \hspace{1cm} (2)

Based on the crystal specification and equation:

\[ C_L = C_{int} + XOC_{TUNE} + Ct1 / Ct2 \]  \hspace{1cm} (3)

\[ C_L = 8 \text{ pF} + 2.6 \text{ pF} + 6 \text{ pF} = 16.6 \text{ pF} \]  \hspace{1cm} (4)

16.6 pF is very close to the TEW crystal requirement of 16 pF load capacitance. With the internal shunt capacitance C_{total}:

\[ C_{total} = 16.6 \text{ pF} + 5 \text{ pF} = 21.6 \text{ pF} \]  \hspace{1cm} (5)
Crystal Pullability

Pullability is another important crystal parameter, which is the change in frequency of a crystal with units of ppm/pF, either from the natural resonant frequency to a load resonant frequency, or from one load resonant frequency to another. The frequency can be pulled in a parallel resonant circuit by changing the value of load capacitance. A decrease in load capacitance causes an increase in frequency, and an increase in load capacitance causes a decrease in frequency.

Frequency Tuning

Frequency tuning is performed by adjusting the crystal load capacitance with external capacitors. It is a Bluetooth requirement that the frequency is always within 20 ppm. The crystal/oscillator must have cumulative accuracy specifications of 15 ppm to provide margin for frequency drift with aging and temperature.

TEW Crystal

The LMX5453 has been tested with the TEW TAS-4025A crystal (see Table 3). Because the internal capacitance of the crystal circuit is 8 pF and the load capacitance is 16 pF, 12 pF is a good starting point for both Ct1 and Ct2. The 2480 MHz RF frequency offset is then tested. Figure 5 shows the RF frequency offset test results.

Figure 5 shows the results are -20 kHz off the center frequency, which is -1 ppm. The pullability of the crystal is 2 ppm/pF, so the load capacitance must be decreased by about 1.0 pF. By changing Ct1 or Ct2 to 10 pF, the total load capacitance is decreased by 1.0 pF. Figure 6 shows the frequency offset test results. The frequency offset is now zero with Ct1 = 10 pF and Ct2 = 10 pF.

See Table 3 for crystal tuning values used on the Phoenix Development Board with the TEW crystal.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>4.0 × 2.5 × 0.65 mm - 4 pads</td>
</tr>
<tr>
<td>Frequency</td>
<td>13.000 MHz</td>
</tr>
<tr>
<td>Mode</td>
<td>Fundamental</td>
</tr>
<tr>
<td>Stability</td>
<td>&lt;15 ppm @ -40 to +85°C</td>
</tr>
<tr>
<td>CL Load Capacitance</td>
<td>16 pF</td>
</tr>
<tr>
<td>ESR</td>
<td>80Ω max</td>
</tr>
<tr>
<td>CO Shunt Capacitance</td>
<td>5 pF</td>
</tr>
</tbody>
</table>

Table 2. TEW TAS-4025A
TCXO (Temperature Compensated Crystal Oscillator)
The LMX5453 also can operate with an external TCXO (Temperature Compensated Crystal Oscillator). The TCXO signal is directly connected to the CLK+.

1. Input Impedance

The LMX5453 CLK+ pin has an input impedance of 2pF capacitance in parallel with >400kΩ resistance

Optional 32 KHZ Oscillator

A second oscillator is provided (see Figure 4) that is tuned to provide optimum performance and low-power consumption while operating with a 32.768 kHz crystal. An external crystal clock network is required between the 32kHz_CLKI clock input (pad B13) and the 32kHz_CLKO clock output (pad C13) signals. The oscillator is built in a Pierce configuration and uses two external capacitors. Figure 4 provides the oscillator’s specifications.

In case the 32Khz is placed optionally, it is recommended to remove C2 and replace C1 with a zero ohm resistor.

![Figure 4. 32.768 kHz Oscillator](image)

Table 2. TEW TAS-4025A (continued)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive Level</td>
<td>50 ± 10uV</td>
</tr>
<tr>
<td>Pullability</td>
<td>2 ppm/pF (minimum)</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>−40 to +85°C</td>
</tr>
</tbody>
</table>

Table 3. TEW on Phoenix Board

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ct1</td>
<td>10 pF</td>
</tr>
<tr>
<td>Ct2</td>
<td>10 pF</td>
</tr>
</tbody>
</table>

Table 4. 32.768 kHz Oscillator Specifications

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage</td>
<td></td>
<td>1.62</td>
<td>1.8</td>
<td>1.98</td>
<td>V</td>
</tr>
<tr>
<td>IDD_ACT</td>
<td>Supply Current (Active)</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>f</td>
<td>Nominal Output Frequency</td>
<td></td>
<td>32.768</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>VPOS</td>
<td>Oscillating Amplitude</td>
<td></td>
<td>1.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td></td>
<td></td>
<td>40</td>
<td>60</td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

Table 5. System Clock Requirements

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CREF</td>
<td>External Reference Clock Frequency</td>
<td>10</td>
<td>13</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td>C_TOL</td>
<td>Frequency Tolerance (over full operating temperature and aging)</td>
<td>−20</td>
<td>15</td>
<td>20</td>
<td>ppm</td>
</tr>
<tr>
<td>XOCTUNE</td>
<td>Digital Crystal Tuning Load Range</td>
<td></td>
<td>8</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_OSC</td>
<td>Crystal Oscillator</td>
<td>10</td>
<td>13</td>
<td>20</td>
<td>MHz</td>
</tr>
</tbody>
</table>

(1) Frequencies supported: 10.00, 10.368, 12.00, 12.60, 12.80, 13.00, 13.824, 14.40, 15.36, 16.00, 16.20, 16.80, 19.20, 19.44, 19.68, and 19.80 MHz
Table 5. System Clock Requirements (continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{ESR}$</td>
<td>Crystal Serial Resistance</td>
<td>230</td>
<td></td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$C_{REF-PS}$</td>
<td>External Reference Clock Power Swing (peak to peak)</td>
<td>100</td>
<td>200</td>
<td>400</td>
<td>mV</td>
</tr>
<tr>
<td>$C_{int}$</td>
<td>Internal Load Capacitance</td>
<td>8</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{AGE}$</td>
<td>Aging</td>
<td>1</td>
<td></td>
<td></td>
<td>ppm/year</td>
</tr>
</tbody>
</table>

Figure 5. Frequency Offset with 12 pF//12 pF Capacitors

Figure 6. Frequency Offset with 10 pF//10 pF Capacitors
## Table 6. Register 2: XOCTUNE Tuning Load Range

<table>
<thead>
<tr>
<th>Binary Value</th>
<th>Hex Value</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>000 0000</td>
<td>00</td>
<td>0</td>
<td>pF</td>
</tr>
<tr>
<td>010 1000</td>
<td>28(1)</td>
<td>2.6</td>
<td>pF</td>
</tr>
<tr>
<td>111 1111</td>
<td>7F</td>
<td>8</td>
<td>pF</td>
</tr>
</tbody>
</table>

(1) Default value for RF initialization register 2.

**Figure 7. ESR vs. Load Capacitance for the Crystal**

**Antenna Matching and Front-End Filtering**

Figure 8 shows the recommended component layout to be used between RF output and antenna input. Allows for versatility in the design such that the match to the antenna maybe improved and/or the blocking margin increased by addition of a LC filter. Refer to antenna application note for further details.

**Figure 8. Front End Layout**
Loop Filter Design

Since the LMX5453 has an external loop filter that determines the performance of the device to a great extent, it is important that it is designed correctly. Texas Instruments will provide the starting component values but the end customer may have to make adjustments to optimize the performance. Please refer to Loop Filter application note and also Texas Instrument’s Webench design tool for detailed information.

Component Calculations

The following parameters are required for component value calculation of a third order passive loop filter.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>η</td>
<td>N counter value</td>
<td>None</td>
</tr>
<tr>
<td>Fc</td>
<td>Loop Bandwidth</td>
<td>rad/s</td>
</tr>
<tr>
<td>Fcomp</td>
<td>Comparison Frequency</td>
<td>rad/s</td>
</tr>
<tr>
<td>KVOC</td>
<td>VCO gain</td>
<td>None</td>
</tr>
<tr>
<td>KCP</td>
<td>Charge Pump gain</td>
<td>None</td>
</tr>
<tr>
<td>FOUT</td>
<td>Mean RF output frequency</td>
<td>rad/s</td>
</tr>
<tr>
<td>T31</td>
<td>Ratio of the poles T3 to T1 in a 3rd order filter</td>
<td></td>
</tr>
<tr>
<td>Symbol?</td>
<td>Gamma optimization parameter</td>
<td></td>
</tr>
</tbody>
</table>

The third order loop filter being defined has the topology shown in Figure 10.

![Third Order Loop Filter](image)

Figure 9. Third Order Loop Filter

\[
\phi = \tan^{-1}\left(\frac{\gamma}{\omega_C \cdot T1 \cdot T1 + T31}\right) - \tan^{-1}(\omega_C \cdot T1) - \tan^{-1}(\omega_C \cdot T1 \cdot T31)
\]

(6)

Calculate the poles and zeros. Use exact method to solve for T1 using numerical methods.

\[
T3 = T31 \cdot T1 \\
T2 = \frac{\gamma}{\omega_C \cdot (T1 + T3)}
\]

(7)

\[
A0 = \frac{K_{\phi} \cdot K_{VCO}}{\omega_C \cdot R2 \cdot C2 \cdot N} \sqrt{\frac{1 + \omega_C^2 \cdot T2^2}{(1 + \omega_C^2 \cdot T1^2)(1 + \omega_C^2 \cdot T3^2)}}
\]

(8)

Calculate the loop filter coefficients,

\[
A1 = A0 \cdot (T1 + T3) \\
A2 = A0 \cdot T1 \cdot T3
\]

(9)

\[
C1 = \frac{A2}{T2^2} \left(1 + \sqrt{\frac{T2 \cdot A0 - T2 \cdot A1}{A2}}\right)
\]

(10)

Summary:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>η</td>
<td>N counter value</td>
<td>None</td>
</tr>
<tr>
<td>Fc</td>
<td>Loop Bandwidth</td>
<td>rad/s</td>
</tr>
<tr>
<td>T1</td>
<td>Loop filter pole</td>
<td>S</td>
</tr>
</tbody>
</table>
Components can then be calculated from loop filter coefficients

\[ C_3 = \frac{1 \cdot T_2^2 \cdot C_1^2 + T_2 \cdot A_1 \cdot C_1 - A_2 \cdot A_0}{T_2^2 \cdot C_1 - A_2} \]
\[ C_2 = A_0 - C_1 - C_3 \]
\[ R_2 = \frac{T_2}{C_2} \quad R_3 = \frac{A_2}{C_1 - C_3 \cdot T_2} \]
\[ \text{LT} = \frac{400}{F_c} (1 - \log_{10} \Delta F) \quad \text{where} \quad \Delta F = \frac{\text{Frequency} - \text{tolerance}}{\text{Frequency} - \text{jump}} \]

Some typical values for the LMX5453 are:

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>T2</td>
<td>Loop filter zero</td>
<td>S</td>
</tr>
<tr>
<td>T3</td>
<td>Loop filter zero</td>
<td>S</td>
</tr>
<tr>
<td>A0</td>
<td>Total capacitance</td>
<td>nF</td>
</tr>
<tr>
<td>A1</td>
<td>First order loop filter coeff</td>
<td>nFs</td>
</tr>
<tr>
<td>A2</td>
<td>Second order loop filter coeff</td>
<td>nFs2</td>
</tr>
<tr>
<td>C1</td>
<td></td>
<td>nF</td>
</tr>
<tr>
<td>C2</td>
<td></td>
<td>nF</td>
</tr>
<tr>
<td>C3</td>
<td></td>
<td>nF</td>
</tr>
<tr>
<td>R2</td>
<td></td>
<td>ohms</td>
</tr>
<tr>
<td>R3</td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

Phase Noise and Lock-Time Calculations

Phase noise has three sources, the VCO, crystal oscillator and the rest of the PLL consisting of the phase detector, dividers, charge pump and loop filter. Assuming the VCO and crystal are very low noise, it is possible to put down approximate equations that govern the phase noise of the PLL.

Phase noise (in-band) = \( PN_{1Hz} + 20\log[N] + 10\log [F_{comp}] \)

Where \( PN_{1Hz} \) is the PLL normalized noise floor in 1 Hz resolution bandwidth.

Further out from the carrier, the phase noise will be affected by the loop filter roll-off and hence its bandwidth.

As a rule-of-thumb; \( \Delta \text{Phase noise} = 40\log [\Delta F_c] \)

Where \( F_c \) is the relative change in loop BW expressed as a fraction.

For example if the loop bandwidth is reduced from 100kHz to 50kHz or by one half, then the change in phase noise will be -12dB. Loop BW in reality should be selected to meet the lower limit of the modulation deviation, this will yield the best possible phase noise.
Even further out from the carrier, the phase noise will be mainly dominated by the VCO noise assuming the crystal is relatively clean.

Lock-time is dependent on three factors, the loop bandwidth, the maximum frequency jump that the PLL must make and the final tolerance to which the frequency must settle. As a rule-of-thumb it is given by:

$$LT = \frac{400}{F_C} (1 - \log_{10} \Delta F)$$

where $$\Delta F = \frac{\text{Frequency - tolerance}}{\text{Frequency - jump}}$$

(14)

These equations are approximations of the ones used by Webench to calculate phase noise and lock-time.

**Practical Optimisation**

In an example where frequency drift and drift rate can be improved though loop filter tweaks, consider the results taken below. The drift rate is 26.1 kHz per 50us and the maximum drift is 25 kHz for DH1 packets, both of which are exceeding or touching the Bluetooth pass limits. These measurements are taken with component values shown above.

<table>
<thead>
<tr>
<th>Table 7. TRM/CA/09/C (Carrier Drift)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hopping On - Low Channel</td>
</tr>
<tr>
<td>DH1</td>
</tr>
<tr>
<td>Drift Rate / 50us</td>
</tr>
<tr>
<td>Max Drift</td>
</tr>
<tr>
<td>Average Drift</td>
</tr>
<tr>
<td>Packets Tested</td>
</tr>
<tr>
<td>Packets Failed</td>
</tr>
<tr>
<td>Overall Result</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DH3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us: N/A</td>
</tr>
<tr>
<td>Max Drift</td>
</tr>
<tr>
<td>Average Drift</td>
</tr>
<tr>
<td>Packets Tested</td>
</tr>
<tr>
<td>Packets Failed</td>
</tr>
<tr>
<td>Overall Result</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DH5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us: −30,5 kHz</td>
</tr>
<tr>
<td>Max Drift</td>
</tr>
<tr>
<td>Average Drift</td>
</tr>
<tr>
<td>Packets Tested</td>
</tr>
<tr>
<td>Packets Failed</td>
</tr>
<tr>
<td>Overall Result</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DH3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us: N/A</td>
</tr>
<tr>
<td>Max Drift</td>
</tr>
<tr>
<td>Average Drift</td>
</tr>
<tr>
<td>Packets Tested</td>
</tr>
<tr>
<td>Packets Failed</td>
</tr>
<tr>
<td>Overall Result</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DH5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us: 15,6 kHz</td>
</tr>
<tr>
<td>Max Drift</td>
</tr>
<tr>
<td>Average Drift</td>
</tr>
<tr>
<td>Packets Tested</td>
</tr>
<tr>
<td>Packets Failed</td>
</tr>
<tr>
<td>Overall Result</td>
</tr>
</tbody>
</table>

Results below were taken on the same board with three loop filter values changed. C2 and R2 have been increased in value and C1 has been reduced. The drift rate has improved by 13 kHz per 50 μs and the maximum drift has improved by 10 kHz.

![Table 8. TRM/CA/09/C (Carrier Drift) Hopping On - Low Channel](image)

The effect of changing these three components is to reduce the loop bandwidth which reduces the phase noise. The reduction in this noise level corresponds directly to the reduction of noise in the payload area where drift is measured. This noise reduction comes at the expense of locktime which can be increased to 120 μs without suffering any ill effects, however if we continue to reduce the loop BW further the lock-time will increase such that the PLL does not have time to lock before data transmission and the drift will again increase. Before the lock-time goes out of spec, the modulation index will start to fall since it is being cut by the reducing loop BW. Therefore a compromise has to be found between lock-time, phase noise and modulation, which yields best performance.

Note: The values shown on the LMX5453 datasheet are the best case optimized values that have been shown to produce the best overall results and are recommended as a starting point for all designs.

Another example of how the loop filter values can affect frequency drift rate, these results below show the DUT with maximum drift on mid and high channels failing. Adjusting the loop bandwidth as shown provides the improvement required to pass qualification.
Table 9. Original results:

<table>
<thead>
<tr>
<th>Hopping OFF - Low Channel</th>
<th>DH1</th>
<th>DH3</th>
<th>DH5</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us</td>
<td>-15.00 kHz</td>
<td>-28.10 kHz</td>
<td>-19.10 kHz</td>
<td>+/- 20 kHz</td>
</tr>
<tr>
<td>Maximum Drift</td>
<td>-19 kHz</td>
<td>-37 kHz</td>
<td>-20 kHz</td>
<td>DH1: +/- 25 kHz</td>
</tr>
<tr>
<td>Average Drift</td>
<td>-11 kHz</td>
<td>-32 kHz</td>
<td>-10 kHz</td>
<td>DH3: +/- 40 kHz</td>
</tr>
<tr>
<td>Packets Tested</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Packets Failed</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Result</td>
<td>Pass</td>
<td>Fail</td>
<td>Pass</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hopping OFF - Med Channel</th>
<th>DH1</th>
<th>DH3</th>
<th>DH5</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us</td>
<td>-18.60 kHz</td>
<td>16.30 kHz</td>
<td>-18.00 kHz</td>
<td>+/- 20 kHz</td>
</tr>
<tr>
<td>Maximum Drift</td>
<td>-29 kHz</td>
<td>-44 kHz</td>
<td>-28 kHz</td>
<td>DH1: +/- 25 kHz</td>
</tr>
<tr>
<td>Average Drift</td>
<td>-19 kHz</td>
<td>-37 kHz</td>
<td>-19 kHz</td>
<td>DH3: +/- 40 kHz</td>
</tr>
<tr>
<td>Packets Tested</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Packets Failed</td>
<td>2</td>
<td>2</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Result</td>
<td>Fail</td>
<td>Fail</td>
<td>Pass</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hopping OFF - High Channel</th>
<th>DH1</th>
<th>DH3</th>
<th>DH5</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us</td>
<td>-16.30 kHz</td>
<td>16.80 kHz</td>
<td>-17.70 kHz</td>
<td>+/- 20 kHz</td>
</tr>
<tr>
<td>Maximum Drift</td>
<td>-36 kHz</td>
<td>-61 kHz</td>
<td>-38 kHz</td>
<td>DH1: +/- 25 kHz</td>
</tr>
<tr>
<td>Average Drift</td>
<td>-31 kHz</td>
<td>-48 kHz</td>
<td>-29 kHz</td>
<td>DH3: +/- 40 kHz</td>
</tr>
<tr>
<td>Packets Tested</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Packets Failed</td>
<td>10</td>
<td>8</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Result</td>
<td>Fail</td>
<td>Fail</td>
<td>Pass</td>
<td></td>
</tr>
</tbody>
</table>

Table 10. New Results:

<table>
<thead>
<tr>
<th>Hopping OFF - Low Channel</th>
<th>DH1</th>
<th>DH3</th>
<th>DH5</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us</td>
<td>-12.00 kHz</td>
<td>-15.10 kHz</td>
<td>18.80 kHz</td>
<td>+/- 20 kHz</td>
</tr>
<tr>
<td>Maximum Drift</td>
<td>-15 kHz</td>
<td>-35 kHz</td>
<td>-19 kHz</td>
<td>DH1: +/- 25 kHz</td>
</tr>
<tr>
<td>Average Drift</td>
<td>-6 kHz</td>
<td>-25 kHz</td>
<td>-9 kHz</td>
<td>DH3: +/- 40 kHz</td>
</tr>
<tr>
<td>Packets Tested</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Packets Failed</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Result</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hopping OFF - Med Channel</th>
<th>DH1</th>
<th>DH3</th>
<th>DH5</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us</td>
<td>-14.20 kHz</td>
<td>-16.10 kHz</td>
<td>17.20 kHz</td>
<td>+/- 20 kHz</td>
</tr>
<tr>
<td>Maximum Drift</td>
<td>-16 kHz</td>
<td>-34 kHz</td>
<td>-22 kHz</td>
<td>DH1: +/- 25 kHz</td>
</tr>
<tr>
<td>Average Drift</td>
<td>-11 kHz</td>
<td>-27 kHz</td>
<td>-9 kHz</td>
<td>DH3: +/- 40 kHz</td>
</tr>
<tr>
<td>Packets Tested</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Packets Failed</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Result</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td></td>
</tr>
</tbody>
</table>

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Product Folder Links: LMX5453
Hopping OFF - High Channel

<table>
<thead>
<tr>
<th></th>
<th>DH1</th>
<th>DH3</th>
<th>DH5</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drift Rate / 50us</td>
<td>~12.70 kHz</td>
<td>~17.40 kHz</td>
<td>~16.50 kHz</td>
<td>+/- 20 kHz</td>
</tr>
<tr>
<td>Maximum Drift</td>
<td>-23 kHz</td>
<td>-29 kHz</td>
<td>-25 kHz</td>
<td>DH1: +/- 25 kHz</td>
</tr>
<tr>
<td>Average Drift</td>
<td>-12 kHz</td>
<td>-25 kHz</td>
<td>-16 kHz</td>
<td>DH3: +/- 40 kHz</td>
</tr>
<tr>
<td>Packets Tested</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>DH5: +/- 40 kHz</td>
</tr>
<tr>
<td>Packets Failed</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Result</td>
<td>Pass</td>
<td>Pass</td>
<td>Pass</td>
<td></td>
</tr>
</tbody>
</table>

Reference Starting Values

Recommended starting values for the LMX5453 as also stated in the reference design towards the end of this datasheet are as shown in Table 11. These values have been optimized through testing to yield the best results from the design. However minor changes to the layout could mean the values need re-optimization.

Table 11. Loop Filter Values

<table>
<thead>
<tr>
<th>Device</th>
<th>C1</th>
<th>C2</th>
<th>C3</th>
<th>R2</th>
<th>R3</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMX5453</td>
<td>220 pF</td>
<td>2200 pF</td>
<td>39 pF</td>
<td>4.7k</td>
<td>10k</td>
</tr>
</tbody>
</table>

Functional Blocks

Baseband Processor And Link Management Processor

Baseband and lower link control functions are implemented using a combination of a CompactRISC 16-bit processor and the Bluetooth Lower Link Controller (LLC). These processors operate from integrated ROM memory and RAM. They execute on-board firmware implementing all Bluetooth functions.

Bluetooth Lower Link Controller

The integrated Bluetooth Lower Link Controller complies with the Bluetooth Specification version 2.0 and implements the following functions:

- Faster connection
- Interlaced Scanning
- Adaptive frequency hopping (AFH)
- Enhanced Error detection
- Support for 1-, 3-, and 5-slot packet types
- 79 channel hop-frequency generation circuitry
- Fast frequency hopping at 1600 hops per second
- Power management control
- Access code correlation and slot timing recovery

Memory

The LMX5453 provides 16K of combined system and Patch RAM memory that can be used for data and/or code upgrades of the ROM-based firmware. Due to the flexible startup used for the LMX5453, operating parameters like the Bluetooth Device Address (BD_ADDR) are defined during boot time. This allows reading the parameters from an external EEPROM or programming them directly over HCI.

External Memory Interfaces

Because the LMX5453 is a ROM-based device with no onchip non-volatile storage, the operation parameters will be lost after a power cycle or hardware reset. To avoid reinitializing operation parameters, patches, or user data, the LMX5453 offers two options for connecting with an external EEPROM:

- Microwire/SPI
- ACCESS.bus (I2C compatible)
The interface is selected during start-up, based on states sampled from the option pins. See Table 20 for the option pin descriptions.

**Microwire/SPI Interface**

If the configuration selected by the option pins uses a Microwire/SPI interface, the LMX5453 activates that interface and attempts to read the EEPROM. The external memory must be compatible with the features listed in Table 12.

The largest size EEPROM supported is limited by the addressing format of the selected EEPROM. The device must have a page size equal to \( N \times 32 \) bytes.

The LMX5453 firmware requires that the EEPROM supports page write. The clock must be high when idle.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supplier</td>
<td>ST Microelectronics</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8 - 3.6 V</td>
</tr>
<tr>
<td>Interface</td>
<td>SPI compatible (positive clock SPI modes)</td>
</tr>
<tr>
<td>Memory Size</td>
<td>8K x 8 (64 Kbits)</td>
</tr>
<tr>
<td>Clock Rate(1)</td>
<td>2 MHz</td>
</tr>
<tr>
<td>Access</td>
<td>Byte and page write (up to 32 bytes)</td>
</tr>
</tbody>
</table>

(1) Parameter range reduced to requirements of Texas Instruments’ reference design.

**ACCESS.bus Interface**

If the configuration selected by the option pins uses an ACCESS.bus or I2C-compatible interface, the LMX5453 activates that interface and attempts to read the EEPROM. The external memory must be compatible with the features listed in Table 13.

The largest size EEPROM supported is limited by the addressing format of the selected EEPROM. The device must have a page size equal to \( N \times 32 \) bytes. The device uses a 16-bit address format. The device address must be 000.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supplier</td>
<td>Atmel</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.7 - 5.5 V</td>
</tr>
<tr>
<td>Interface</td>
<td>2-wire serial interface</td>
</tr>
<tr>
<td>Memory Size</td>
<td>8K x 8 (64 Kbits)</td>
</tr>
<tr>
<td>Clock Rate(1)</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Access</td>
<td>32-byte page-write mode</td>
</tr>
</tbody>
</table>

(1) Parameter range reduced to requirements of Texas Instruments’ reference design.

**Host Controller Interface Port**

**UART Interface**

The LMX5453 provides one Universal Asynchronous Receiver Transmitter (UART). It supports 8-bit data with or without parity, and with one or two stop bits. The UART can operate at standard baud rates from 300 baud up to a maximum of 921.6 kbaud. DMA transfers are supported to allow for fast processor-independent receive and transmit operation. The UART implements flow-control signals (RTS# and CTS#) for hardware handshaking.

The reference clock and UART baud rate are configured during start-up by sampling option pins OP3, OP4, and OP5. If the auto baud rate detect option is selected, the firmware checks an area in non-volatile storage (NVS) for a valid UART baud rate stored during a previous session. If no value was saved, the LMX5453 will switch to auto baud rate detection and wait for an incoming reference signal.
The UART can detect a BREAK signal, which forces the LMX5453 to reset. This is useful when the only connection between the LMX5453 and the host system is the HCI port.

The UART offers wake-up from low-power modes through its Multi-Input Wake-Up module (MIWU). When the LMX5453 is in a low-power mode, RTS# and CTS# can function as Host_WakeUp and Bluetooth_WakeUp, respectively. Table 14 represents the operational modes supported by the LMX5453 firmware for implementing the HCI transport port with the UART.

### Table 14. UART Operation Modes

<table>
<thead>
<tr>
<th>Modes</th>
<th>Range</th>
<th>Default at Power-Up</th>
<th>With Auto Baud Detect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud Rate</td>
<td>0.3 to 921.6 kbaud</td>
<td>Configured by option pins, NVS parameter, or auto baud rate detection</td>
<td>0.3 to 921.6 kbaud</td>
</tr>
<tr>
<td>Flow Control</td>
<td>RTS#/CTS# or None</td>
<td>RTS#/CTS#</td>
<td>RTS#/CTS#</td>
</tr>
<tr>
<td>Parity</td>
<td>Odd, Even, or None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Stop Bits</td>
<td>1 or 2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Data Bits</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

### USB Interface

The LMX5453 USB node controller features enhanced DMA support with many automatic data handling features. It is certifiable to USB specification version 2.0. The USB interface is the standard 12 Mbit/s. An internal PLL provides the necessary 48 MHz clock.

The USB node controller integrates the required USB transceiver, a Serial Interface Engine (SIE) and USB endpoint FIFOs. Seven endpoint pipelines are supported: one for the mandatory control endpoint and six to support interrupt, bulk, and isochronous endpoints. Each endpoint pipeline has a dedicated FIFO (8 bytes for the control endpoint, and 64 bytes for the other endpoints).

### Audio Port

#### Advanced Audio Interface

The Advanced Audio Interface (AAI) is an advanced version of the Synchronous Serial Interface (SSI) that provides a full-duplex communications port to a variety of industry-standard 13/14/15/16-bit linear or 8-bit log PCM codecs, DSPs, and other serial audio devices.

The interface supports up to two codecs or interfaces. The firmware selects the desired audio path and interface configuration using a parameter in RAM (imported from nonvolatile storage or programmed during boot-up). The audio path options include 16-bit two’s complement linear audio through the HCI transport, the Motorola MC145483 codec, and the OKI MSM7717 codec through the AAI, or No Audio. See NVS Table 21.

If an external codec or DSP is used, the LMX5453 audio interface generates the necessary bit and frame clock for driving the interface.

**Table 15** summarizes the audio path selection and the configuration of the audio interface at the specific modes.

The LMX5453 supports two simultaneous SCO links.

### Table 15. Audio Path configuration

<table>
<thead>
<tr>
<th>Audio setting</th>
<th>Interface</th>
<th>Freq</th>
<th>Format</th>
<th>AAI Bit Clock</th>
<th>AAI Frame Clock</th>
<th>AAI Frame Sync Pulse Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>OKI MSM7717</td>
<td>Advanced audio interface</td>
<td>ANY (1)</td>
<td>8-bit log PCM (a-law only)</td>
<td>480 KHz</td>
<td>8 KHz</td>
<td>14 Bits</td>
</tr>
<tr>
<td>Motorola MC145483 (2)</td>
<td>Advanced audio interface</td>
<td>13-bit linear</td>
<td>480 KHz</td>
<td>8 KHz</td>
<td>13 Bits</td>
<td></td>
</tr>
</tbody>
</table>

(1) For supported frequencies see Table 5
(2) Due to internal clock divider limitations the optimum of 512KHz, 8KHz can not be reached. The values are set to the best possible values. The clock mismatch does not result in any discernible loss in audio quality.
### Table 15. Audio Path configuration (continued)

<table>
<thead>
<tr>
<th>Audio setting</th>
<th>Interface</th>
<th>Freq</th>
<th>Format</th>
<th>AAI Bit Clock</th>
<th>AAI Frame Clock</th>
<th>AAI Frame Sync Pulse Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>OKI MSM7717</td>
<td>Advanced audio interface</td>
<td>13MHz</td>
<td>8-bit log PCM (a-law only)</td>
<td>520 KHz</td>
<td>8 KHz</td>
<td>14 Bits</td>
</tr>
<tr>
<td>Motorola MC145483(3)</td>
<td>Advanced audio interface</td>
<td></td>
<td>13-bit linear</td>
<td>520 KHz</td>
<td>8 KHz</td>
<td>13 Bits</td>
</tr>
<tr>
<td>Winbond W881310</td>
<td>Advanced audio interface</td>
<td>13MHz</td>
<td>8 bit log PCM A-law and u-law</td>
<td>520 KHz</td>
<td>8 KHz</td>
<td>14 Bits</td>
</tr>
<tr>
<td>Winbond W881360</td>
<td>Advanced audio interface</td>
<td>13MHz</td>
<td>13-bit linear</td>
<td>520 KHz</td>
<td>8 KHz</td>
<td>13 Bits</td>
</tr>
<tr>
<td>PCM slave(4)</td>
<td>Advanced audio interface</td>
<td>ANY(1)</td>
<td>8/16 bits</td>
<td>128 - 1024 KHz</td>
<td>8 KHz</td>
<td>8/16 Bits</td>
</tr>
<tr>
<td>Audio over HCI</td>
<td>HCI Transport</td>
<td></td>
<td>16-Bit Two’s Complement Linear</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>

(3) Due to internal clock divider limitations the optimum of 512KHz, 8KHz can not be reached. The values are set to the best possible values. The clock mismatch does not result in any discernible loss in audio quality.

(4) In PCM slave mode, parameters are stored in NVS. Bit clock and frame clock must be generated by the host interface.

**PCM slave configuration example:** PCM slave uses the slot 0, 1 slot per frame, 16 bit linear mode, long frame sync, normal frame sync. In this case, 0x03E0 should be stored in NVS. See **“LMX5453 Software User’s Guide”** for more details.

### Auxiliary Ports

**RESET#**

There are two reset inputs: RESET_RA# for the radio and RESET_BB# for the baseband. Both are active low.

There is also a reset output, B_RESET_RA# (Buffered Radio Reset), which is also active low. This output follows input RESET_RA#. When RESET_RA# is released, going high, B_RESET_RA# stays low until the clock has started.

See **Section 15.0 for details and Section 16.0 for schematics.**

### General Purpose I/O Ports

The LMX5453 provides 3 GPIO ports which either can be used as indication and configuration pins or can be used for general-purpose functionality. The states which select these options are sampled during the start-up sequence.

In a general-purpose configuration, the pins are controlled by hardware-specific HCI commands. These commands provide the ability to set the direction of the pin, drive the pin high or low, and enable a weak pull-up on the pin.

In the alternate-function configuration, the pins have predefined indication functions. See **Table 16 for a description of the alternate-function configuration.**

### Table 16. Alternate GPIO Pin Configuration

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP4/PG4</td>
<td>Operation mode pin to configure transport layer settings during boot-up</td>
</tr>
<tr>
<td>PG6</td>
<td>USB status indication</td>
</tr>
<tr>
<td>PG7</td>
<td>TL (Transport Layer) traffic indication</td>
</tr>
</tbody>
</table>

### System Power-Up

To power-up the LMX5453 the following sequence must be performed:

1. Apply VCC_IO and VCC to the LMX5453.
2. The RESET_RA# should be driven high.
3. Then RESET_BB# should be driven high at a recommended time of 1ms after the LMX5453 voltage rails are high. The LMX5453 is properly reset. (See Figure 10).

![Figure 10. LMX5453 Power-On Reset Timing](image)

Table 17. LMX5453 Power to Reset Timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{P TORRA} )</td>
<td>Power to Reset</td>
<td>VCC and VCC_IO at operating voltage level to valid reset</td>
<td>&lt;500(^{(1)})</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{P TORBB} )</td>
<td>Reset to Reset</td>
<td>VCC and VCC_IO at operating voltage level to valid reset</td>
<td>1(^{(2)})</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Rise time on power must switch on fast, rise time <500 µs
(2) Recommended value.

Table 18. ESR vs. Start-Up Time

<table>
<thead>
<tr>
<th>ESR (Ω)</th>
<th>Typical(^{(1)(2)})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>12</td>
<td>ms</td>
</tr>
<tr>
<td>25</td>
<td>13</td>
<td>ms</td>
</tr>
<tr>
<td>40</td>
<td>16</td>
<td>ms</td>
</tr>
<tr>
<td>50</td>
<td>24</td>
<td>ms</td>
</tr>
<tr>
<td>80</td>
<td>30</td>
<td>ms</td>
</tr>
</tbody>
</table>

(1) Frequency, loading caps, and ESR all must be considered for determining the start-up time. (2) For reference only, must be tested on each system to accurately determine the start-up time.

Start-Up Sequence

During start-up, the LMX5453 samples the option inputs OP3 to OP7 for configuration, external clock source, HCI transport layer, and available non-volatile storage EEPROM interface. The start-up options are described in Table 20.

Options Register

The states sampled from the OP inputs listed in Table 20 are latched in this register at the end of reset. The Options register can be read by the LMX5453 firmware at any time.

All pads are inputs with weak on-chip pull-up/down resistors during reset. The resistors are disconnected at the end of RESET_BB#.

1 = Pull-up resistor connected in application
0 = Pull-down resistor connected in application
x = Don’t care

Start-Up With External EEPROM

To read information from an external EEPROM, the OP inputs have to be strapped according to Table 20.

The start-up sequence performs these operations:
1. From the Options register bits OP6 and OP7, the firmware checks whether a serial EEPROM is available to use (ACCESS.bus or Microwire/SPI).
2. If a serial EEPROM is available, the permanent parameter block, patch block, and non-volatile storage (NVS) are initialized from it.
3. From the Options register bits OP3, OP4, and OP5, the firmware checks for clocking information and transport layer settings. If the NVS information are not sufficient, the firmware will send the Await Initialization event on the TL and wait for additional information (see ** Section 15.1.3)
4. The firmware compensates the UART for new BBCLK information from the NVS.
5. The firmware starts up the Bluetooth core.

Start-Up Without External EEPROM

The following sequence will take place if OP6 and OP7 have selected No external memory, as described in Table 20.

The start-up sequence performs these operations:
1. From the Options registers OP6 and OP7, the firmware checks if an EEPROM is available to use.
2. From the Options register OP3, OP4 and OP5, the firmware checks the clocking mode and transport layer settings.
3. The firmware sends the Await Initialization event on the transport layer and waits for NVS configuration commands. The configuration is finalized by sending the Enter Bluetooth Mode command.
4. The firmware compensates the UART for new BBCLK information from the NVS.
5. The firmware starts up the Bluetooth core.

Table 19. Start-Up Sequence Options

<table>
<thead>
<tr>
<th>Package Pad</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP3</td>
<td>OP4</td>
</tr>
<tr>
<td>PD</td>
<td>PD</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>T_SCLK</td>
<td>x</td>
</tr>
</tbody>
</table>

(1) I/O pull-up/down resistor connected in application.
Table 20. Fixed Frequencies

<table>
<thead>
<tr>
<th>Osc Freq (MHz)</th>
<th>BBLCK (MHz)</th>
<th>PLL (48 MHz)</th>
<th>OP3</th>
<th>OP4</th>
<th>OP5</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>12</td>
<td>Off</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Off</td>
</tr>
<tr>
<td>13</td>
<td>13</td>
<td>Off</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>layer with baud rate detection</td>
</tr>
<tr>
<td>10-20</td>
<td>10-20(1)</td>
<td>On</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>layer 115.2 kbaud</td>
</tr>
<tr>
<td>13</td>
<td>13</td>
<td>Off</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>layer 921.6 kbaud</td>
</tr>
<tr>
<td>12</td>
<td>12</td>
<td>On</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>layer</td>
</tr>
<tr>
<td>13</td>
<td>13</td>
<td>On</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>layer</td>
</tr>
<tr>
<td>10-20</td>
<td>10-20(1)</td>
<td>On</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>layer</td>
</tr>
</tbody>
</table>

(1) See Table 5 for supported frequencies.

Configuring the LMX5453 Through the Transport Layer

As described in Section 15.0, the LMX5453 checks the Options register during start-up to determine whether an external EEPROM is available. If the EEPROM information is incomplete or no EEPROM is installed, the LMX5453 will boot into the initialization mode. The mode is confirmed by the Await Initialization event.

The following information is needed to enter Bluetooth mode:

- Bluetooth Device Address (BD_ADDR)
- External clock source (only if 10–20 MHz has been selected)
- UART baud rate (only needed if auto baud rate detection has been selected)
In general, the following procedure will initialize the LMX5453:

1. Wait for the Await initialization event. The event will only appear if the transport layer speed is set or after successful baud rate detection.
2. Send Set Clock and Baudrate command for temporary clock frequency and UART configuration.
3. Send Write BD_Addr to configure local Bluetooth device address.
4. Send Enter Bluetooth Mode. The LMX5453 will use the configured clock frequency and UART baud rate to start the HCI transport layer interface.

**Note:** These clock and baud rate settings are only valid until the next power-on or hardware reset.

---

**Figure 11. Flow Chart for the Start-Up Sequence**

In general, the following procedure will initialize the LMX5453:

1. Wait for the Await initialization event. The event will only appear if the transport layer speed is set or after successful baud rate detection.
2. Send Set Clock and Baudrate command for temporary clock frequency and UART configuration.
3. Send Write BD_Addr to configure local Bluetooth device address.
4. Send Enter Bluetooth Mode. The LMX5453 will use the configured clock frequency and UART baud rate to start the HCI transport layer interface.

**Note:** These clock and baud rate settings are only valid until the next power-on or hardware reset.
Auto Baud Rate Detection

The LMX5453 supports an auto baud rate detection in case the external clock is different from 12, 13 MHz or the range 10-20 MHz or the baud rate is different from 115.2 or 921.6 kbaud.

The baud rate detection is based on the measurement of a single character. The following issues need to be considered:

- The flow control pin CTS# must be low, otherwise the host is held in flow stop mode.
- The auto baud rate detector measures the length of the 0x01 character from the positive edge of bit 0 to the positive edge of the stop bit.
- Therefore, the very first received character must always be 0x01.
- The host can restrict itself to send only a 0x01 character or it can send an HCI command.
- If an HCI command is used for baud rate detection, the second received character must be 0x00.
- The host must flush the TX buffer within 50–100 milliseconds, depending on the clock frequency of the host controller.
- After 50–100 milliseconds, the UART is about to be initialized. Then, the host should receive an Await Initialization event or a Command Status event.

![Figure 12. Auto Baud Rate Detection](image_url)

Using an External EEPROM for Nonvolatile Storage

The LMX5453 offers two interfaces for connecting to external EEPROM used for non-volatile storage (NVS). The interface is selected by the states sampled from the option inputs during the start-up sequence. See Table 20 for the available options.

The external memory is used to store mandatory parameters such as the Bluetooth device address (BD_ADDR) as well as many optional parameters such as link keys or user data.

The firmware uses fixed addresses to reference the parameters, which allows the EEPROM to be preprogrammed with default parameters in manufacturing. See Table 21 for the organization of the NVS parameter map.

If the EEPROM is empty, during the first start-up the LMX5453 will behave as though no memory is connected. (see **Section 15.1.3). During the start-up sequence, parameters can be written directly to the EEPROM so that they can be used during subsequent sessions. Patches supplied over the transport layer will be stored automatically into the EEPROM.

Table 21. Non Volatile Storage Map

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00-05(1)</td>
<td>BD_ADDR</td>
<td>Bluetooth Device Address          LAP(lsb), LAP, UAP, NAP, NAP (msb)</td>
</tr>
<tr>
<td>06</td>
<td>Audio Path Selection</td>
<td>0x00: One motorola MC145483 codec 0x01: Two motorola MC145483 codecs 0x02: One OKI MSM7717 codec 0x03: Two OKI MSM7717 codecs 0x04: Generic PCM Slave. For this setting the generic slave configuration and the generic slave frame clock prescaler must also be set to correct values in the NVS. 0x05 0xFE: No audio path 0x0F: HCI used for SCO transfer</td>
</tr>
<tr>
<td>07-0A</td>
<td>Baudrate</td>
<td></td>
</tr>
</tbody>
</table>

(1) Parameters located at these addresses are requested by the Bluetooth Core for proper operation.
### Table 21. Non Volatile Storage Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0B</td>
<td>Frame settings(2)</td>
<td></td>
</tr>
<tr>
<td>0C-0D</td>
<td>USB Vid</td>
<td></td>
</tr>
<tr>
<td>0E-0F</td>
<td>USB PID</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>USB Self powered</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>USB max power</td>
<td></td>
</tr>
<tr>
<td>12-15</td>
<td>Frequency(3)</td>
<td></td>
</tr>
</tbody>
</table>

#### Core parameters

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-BD(1)</td>
<td>Link Keys</td>
<td>Internal use, 24 bytes per key</td>
</tr>
<tr>
<td>BE(1)</td>
<td>Local Name Length</td>
<td>Length of Local Device Name</td>
</tr>
<tr>
<td>BF-1B6(1)</td>
<td>Local Device Name</td>
<td>Friendly bluetooth name of the bluetooth device</td>
</tr>
<tr>
<td>1B7(1)</td>
<td>Link Key Type</td>
<td></td>
</tr>
<tr>
<td>1B8(1)</td>
<td>Unit Key Present</td>
<td></td>
</tr>
<tr>
<td>1B9-1C8(1)</td>
<td>Unit Key</td>
<td></td>
</tr>
</tbody>
</table>

#### Debugging info

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1C9-1D7</td>
<td>Assert Information</td>
<td>Internal use only.</td>
</tr>
<tr>
<td>1D8-1E9</td>
<td>Runtime Information</td>
<td>Internal use only.</td>
</tr>
</tbody>
</table>

#### Reserved

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1EA</td>
<td>Options</td>
<td>Bit 0: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 1: Low power operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Disable low power operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Enable low power operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 2: Traffic LED Indication</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Enable traffic LED indication on PG7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Disable traffic LED indication on PG7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 3: USB status</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Enable USB status on PG6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Disable USB status on PG6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Bit 4: TLKAS (Transport Layer Keep Alive during Scans)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Normal TL power off</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Only power off TL if page/inquiry scans disabled Bit4 has no effect on USB TL. The USB TL will always use halt in order to comply with USB power constraints. This option does not affect the protocol for TL power management, only the internal operation of the firmware. TLKAS == 0 requires a stable clock when exiting from HALT mode. Normal TL power off Bit 5-7: Unused.</td>
</tr>
<tr>
<td>1EB</td>
<td>Vtune_Desired_Threshold</td>
<td>Internal use only.</td>
</tr>
<tr>
<td>1EC</td>
<td>Vtune_on</td>
<td>Internal use only.</td>
</tr>
<tr>
<td>1ED</td>
<td>Vtune_enable</td>
<td>Internal use only.</td>
</tr>
<tr>
<td>1EE</td>
<td>AclAndScoBufferMode</td>
<td>0: 8 339 byte ACL buffers, 2 SCO buffers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: 8 ACL 339 bytes, 1 eSCO/SCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2: 4 339 byte ACL, 2 eSCO/SCO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0xFF: specifies same set-up as 1.</td>
</tr>
</tbody>
</table>

(2) This parameter can only be used with a pre-programming external EEPROM.
(3) The frequency parameter is only needed when the firmware starts up in a mode with unknown crystal frequency (10-20MHz). FSEL pins are used to determine if the crystal frequency is unknown. Reference Table 5 for supported frequencies.
Table 21. Non Volatile Storage Map (continued)

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1F1-1F2</td>
<td>Generic PCM slave config</td>
<td>This 16-bit value (LSB first) is used to store the PCM format configuration for the PCM generic slave. The Fcprs value must also be set in order to use the generic PCM slave. Attention: Some values are not mapped directly to the parameter values, because we want 0xFF to select the default behavior. <strong>Bit 0-1: Slot selection:</strong> 11: use slot 0 00: use slot 1 01: use slot 2 10: use slot 3 <strong>Bit 2-3: Number of slots per frame:</strong> 11: 1 slot 00: 2 slots 01: 3 slots 10: 4 slots <strong>Bit 4-6: PCM data format:</strong> 000: 8 bit A-law 001: 8 bit u-law 010: 13 bit linear 011: 14 bit linear 100: 15 bit linear 101: 16 bit linear 110: 16 bit linear 111: 16 bit linear <strong>Bit 7: Frame sync length:</strong> 0: short frame sync 1: long frame sync <strong>Bit 8: Data word length:</strong> 0: 8-bit data word length 1: 16-bit data word length <strong>Bit 9: Frame sync polarity:</strong> 0: use normal frame sync 1: use inverted frame sync <strong>Bit 10-15: Unused, set to 1</strong></td>
</tr>
<tr>
<td>1F3</td>
<td>Generic PCM slave Fcprs</td>
<td>Frame clock prescaler for generic PCM slave. The ratio between the bit clock and the frame clock must be written into this register for the generic PCM slave to operate correctly. <strong>BIT0-6: Fcprs</strong> This value is an unsigned integer indicating the prescaler. The following equation must be true: bit_clock/(Fcprs + 1) = frame_clock. Example: bit clock = 480000, frame sync rate = 8000, Fcprs must be set to 59 since 480000/(59 + 1) = 8000 <strong>BIT7: Unused, set to 1</strong></td>
</tr>
</tbody>
</table>

Production Parameters

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1F0(4)</td>
<td>XOC TUNE</td>
</tr>
<tr>
<td>1F4-1F7</td>
<td>RfReg4</td>
</tr>
<tr>
<td>1F8-1FB</td>
<td>RfReg15</td>
</tr>
<tr>
<td>1FC-1FF</td>
<td>Unused</td>
</tr>
</tbody>
</table>

Reserved for RF development

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>200-2FF</td>
<td>RF Develop</td>
</tr>
</tbody>
</table>

Patch Code Area

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>300-1CFF</td>
<td>Patch code</td>
</tr>
</tbody>
</table>

Application Data

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1D00-2000</td>
<td>User Data</td>
<td>Available space if 8K EEPROM is used</td>
</tr>
<tr>
<td>1D00-4000</td>
<td>User Data</td>
<td>Available space if 16K EEPROM is used</td>
</tr>
<tr>
<td>1D00-8000</td>
<td>User Data</td>
<td>Available space if 32K EEPROM is used</td>
</tr>
</tbody>
</table>

(4) Reference Section 11.0 "Crystal Requirements" on page 12 for details on crystal tuning.
Low-Power Operation

The LMX5453 provides low-power modes which cover the main usage scenarios in a Bluetooth environment. Each of the low-power modes is optimized for minimal power consumption in that particular scenario. The modular structure of the LMX5453 allows the firmware to power down unused modules or to switch to a low-speed clock. Because the LMX5453 firmware supports these modes transparently, no power-control mechanisms need to be implemented by application code to use these modes.

To reduce power consumption, the LMX5453 can disable the UART transport layer, which switches off the UART module and enables a wake-up mechanism triggered by the UART interface.

Power Modes

The LMX5453 has six operating power modes, which are selected by the activity level of the HCI transport layer and the Bluetooth baseband processor. Mode switching is triggered by a change in the baseband processor activity or by enabling/disabling the UART transport layer.

The baseband processor activity depends on application requirements and is defined by standard Bluetooth operations such as inquiry/page scanning and link establishment.

A remote device establishing or disconnecting a link may also indirectly change the baseband processor activity and therefore the power mode.

The HCI transport layer is enabled on device power-up by default. To disable the transport layer, the vendor-specific HCI command HCI_DISABLE_TL is used. Therefore, only the host side of the HCI can disable the transport layer. Reenabling the transport layer is controlled by the hardware wake-up signalling. This can be performed from either the host or the LMX5453 side of the interface. See Section 15.5 for detailed information.

Note: The HCI_Disable_TL command is only supported with the UART transport layer. The Main clock can disabled for PM0. The Main clock itself may be 12, 13, or 10-20 MHz. The PLL will always be enabled if the transport layer is USB or if the transport layer is UART but the Main clock is not 12 or 13 MHz. Also, in PM2, the Main and System clocks will be disabled by Host Controller when not needed by the Lower Link Controller.

<table>
<thead>
<tr>
<th>Power Mode</th>
<th>UART Mode</th>
<th>Baseband Activity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM0</td>
<td>Disabled</td>
<td>Wake-Up Trigger</td>
<td>Standby mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enabled</td>
<td></td>
</tr>
<tr>
<td>PM1</td>
<td>Enabled</td>
<td>None</td>
<td>Transport layer ready to receive commands, no baseband processor activity.</td>
</tr>
<tr>
<td>PM2</td>
<td>Disabled</td>
<td>Wake-Up Trigger</td>
<td>LMX5453 discoverable/connectable for other devices. UART disabled. Wake-up trigger enabled to wake-up host on incoming connection.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enabled</td>
<td></td>
</tr>
<tr>
<td>PM3</td>
<td>Enabled</td>
<td>Scanning</td>
<td>LMX5453 discoverable/connectable for other devices. UART enabled.</td>
</tr>
<tr>
<td>PM4</td>
<td>Disabled</td>
<td>Wake-Up Trigger</td>
<td>LMX5453 handling at least one link. UART disabled. Wake-up trigger enabled to wake-up host on incoming data or connections.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enabled</td>
<td></td>
</tr>
<tr>
<td>PM5</td>
<td>Enabled</td>
<td>Active Link</td>
<td>Standard active mode. LMX5453 handling at least one link.</td>
</tr>
</tbody>
</table>

Table 22. LMX5453 Power Modes
The LMX5453 switches between power modes in response to certain changes in activity. Because any of the parameters can be changed dynamically, there is no limitation on which mode can be reached from another. Figure 13 shows an overview of the power modes and the transitions between modes.

Controlling the UART

Hardware Wake-Up Function

In certain usage scenarios, the host may switch off the transport layer of the LMX5453 to reduce power consumption. Then, both devices are able to shut down their UART interfaces. In this mode, the firmware will configure the UART interface to enable a hardware wake-up trigger.

The hardware interface between the host and the UART interface on the LMX5453 is shown in Figure 14.

Disabling the UART

The host can disable the UART transport layer by sending the Disable Transport Layer command. In response, the LMX5453 will empty its buffers, send the confirmation event, and disable its UART interface. Then, the UART interface will be reconfigured to wake-up the LMX5453 when a rising edge occurs on the CTS# input.

When the HCI transport layer is disabled, both the host and the LMX5453 will drive RTS=0, because they will be in a Not Ready to Receive mode. The hardware wake-up signal is then defined as a falling edge on the CTS input i.e. a device wakes up the other device by asserting its own Ready to Receive output (i.e. Setting RTS active).

If the LMX5453 redefines the CTS input from flow-control input to wake-up input when the UART has shifted out the last byte of the HCI_COMMAND_COMPLETE (for HCI_DISABLE_TL) event and the host redefines its RTS output when it has received the last byte of the HCI_COMMAND_COMPLETE event there will be a short period of time during which the signalling is ambiguous. To avoid this, delays are introduced as illustrated in Figure 15.

LMX5453 To Host Wake-Up and UART Enable

Because the transport layer can be disabled in any situation, the LMX5453 must first verify that the transport layer is enabled before sending data to the host. Possible scenarios in which the LMX5453 must wake up the host include incoming data or incoming link indicators. If the UART is not enabled, the LMX5453 assumes that it must wake up the host by asserting RTS#. To respond to this assertion, the host must monitor its CTS# input.
When CTS# is asserted, the host must wake up its UART interface and confirm the UART status by sending the HCI_RTX_WAKEUP_COMPLETE event. This event should not be sent until the HCI transport layer is ready for transferring data. When the host receives the HCI_RTX_WAKEUP_COMPLETE debug event, both sides know that the HCI transport layer is enabled.

![Diagram](image)

**Figure 15. Disabling the UART Transport Layer**

The LMX5453 should now send the pending HCI events that triggered the wake-up. See Figure 16 for the complete process.

**Figure 16. LMX5453 Wake-Up to Host**

**Host to LMX5453 Wake-Up and UART Enable**

If the host needs to send data or commands to the LMX5453 while the UART transport layer is disabled, it must first assume that the LMX5453 is sleeping and wake it up by asserting its RTS signal. When the LMX5453 detects the wake-up signal, it enables the UART and acknowledges the wake-up signal by asserting its RTS signal. Additionally, the wake up will be confirmed by a confirmation event. When the host has received this HCI_WAKEUP_COMPLETE event, the LMX5453 is ready to receive commands. The host may now send the pending HCI events that triggered the wake-up. See Figure 17 for the complete process.

**Note:** Even though the LMX5453 sets RTS active (indicating Ready to Receive mode), the host must not send any HCI commands to the LMX5453 before receiving the HCI_WAKEUP_COMPLETE event.
Figure 17. Host Wake-Up to LMX5453

Applications Information

USB Dongle Reference Schematic
Soldering

The LMX5453 bumps are composed of a solder alloy and reflow (melt and reform) during the Surface Mount Assembly (SMA) process. In order to ensure reflow of all solder bumps and maximum solder joint reliability while minimizing damage to the package, recommended reflow profiles should be used. Table 23, Table 24, and Figure 18 provide the soldering details required to properly solder the LMX5453 to standard PCBs. The illustration serves only as a guide and Texas Instruments is not liable if a selected profile does not work.

### Table 23. Soldering Details

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Land Pad Diameter</td>
<td>13 mil</td>
</tr>
<tr>
<td>PCB Solder Mask Opening</td>
<td>19 mil</td>
</tr>
<tr>
<td>PCB Finish</td>
<td>Defined by customer or manufacturing facility</td>
</tr>
<tr>
<td>Stencil Aperture</td>
<td>17 mil</td>
</tr>
<tr>
<td>Stencil Thickness</td>
<td>5 mil</td>
</tr>
<tr>
<td>Solder Paste Used</td>
<td>Defined by customer or manufacturing facility</td>
</tr>
<tr>
<td>Flux Cleaning Process</td>
<td>Defined by customer or manufacturing facility</td>
</tr>
</tbody>
</table>

### Table 24. Classification Reflow Profiles (1)(2)

<table>
<thead>
<tr>
<th>Profile Feature</th>
<th>NOPB Assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Ramp-Up Rate (TsMAX to Tp)</td>
<td>150°C</td>
</tr>
<tr>
<td>Preheat:</td>
<td>200°C</td>
</tr>
<tr>
<td>Temperature Min (TsMIN)</td>
<td>60–180 seconds</td>
</tr>
<tr>
<td>Temperature Max (TsMAX)</td>
<td>217°C</td>
</tr>
<tr>
<td>Time (tMIN to tMAX)</td>
<td>60–150 seconds</td>
</tr>
<tr>
<td>Time maintained above:</td>
<td>260 ± 0°C</td>
</tr>
<tr>
<td>Temperature (T_L)</td>
<td>20–40 seconds</td>
</tr>
<tr>
<td>Time within 5°C of actual Peak Temperature (tp)</td>
<td></td>
</tr>
<tr>
<td>Ramp-Down Rate</td>
<td>6°C/second maximum</td>
</tr>
<tr>
<td>Time 25°C to Peak Temperature</td>
<td>8 minutes maximum</td>
</tr>
<tr>
<td>Reflow Profiles</td>
<td>See Figure 18</td>
</tr>
</tbody>
</table>

(2) All temperatures refer to the top side of the package, measured on the package body surface.

![Figure 18. Typical Reflow Profiles](image-url)
REVISION HISTORY

Changes from Revision C (June 2013) to Revision D | Page
---|---
* Added data to Recommended Operating Conditions because data was missing from old National version | 6
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMX5453SM/NOPB</td>
<td>ACTIVE</td>
<td>NFBGA</td>
<td>NZB</td>
<td>60</td>
<td>320</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SNAGCU</td>
<td>Level-4-260C-72 HR</td>
<td>-40 to 85</td>
<td>5453SM</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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