LMZ12003 3-A Simple Switcher® Power Module with 20-V Maximum Input Voltage

1 Features
- Integrated Shielded Inductor
- Simple PCB Layout
- Flexible Start-up Sequencing Using External Soft-start Capacitor and Precision Enable
- Protection Against Inrush Currents and Faults such as Input UVLO and Output Short Circuit
- Junction Temperature Range –40°C to 125°C
- Single Exposed Pad and Standard Pinout for Easy Mounting and Manufacturing
- Fast Transient Response for FPGAs and ASICs
- Low Output Voltage Ripple
- Pin-to-Pin Compatible With Devices:
  - LMZ14203/2/1 (42-V Maximum 3 A, 2 A, 1 A)
  - LMZ12003/2/1 (20-V Maximum 3 A, 2 A, 1 A)
- Fully WEBENCH® Power Designer Enabled

2 Applications
- Point-of-load Conversions from 5-V and 12-V Input Rail
- Time-Critical Projects
- Space-Constrained High Thermal Requirement Applications
- Negative Output Voltage Applications (See AN-2027) SNVA425

3 Description
The LMZ12003 SIMPLE SWITCHER® power module is an easy-to-use step-down DC-DC solution capable of driving up to 3-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy. The LMZ12003 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ12003 can accept an input voltage rail between 4.5 V and 20 V and can deliver an adjustable and highly accurate output voltage as low as 0.8 V. The LMZ12003 only requires three external resistors and four external capacitors to complete the power solution. The LMZ12003 is a reliable and robust design with the following protection features: thermal shutdown, input undervoltage lockout, output overvoltage protection, short circuit protection, output current limit, and this device allows start-up into a prebiased output. A single resistor adjusts the switching frequency up to 1 MHz.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMZ12003</td>
<td>NDW (7)</td>
<td>9.85 mm × 10.16 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Peak reflow temperature equals 245°C. See SNA214 for more details.
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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (October 2013) to Revision O Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ................................................................. 1

Changes from Revision M (March 2013) to Revision N Page

• Deleted 12 mils ................................................................ 4
• Changed 10 mils ............................................................ 17
• Changed 10 mils ............................................................ 20
• Added Power Module SMT Guidelines ........................... 20

Product Folder Links: LMZ12003
5 Pin Configuration and Functions

NDW Package
7-Pin
Top View

Exposed Pad
Connect to GND

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>3</td>
<td>Analog</td>
</tr>
<tr>
<td>EP</td>
<td>—</td>
<td>Ground</td>
</tr>
<tr>
<td>FB</td>
<td>6</td>
<td>Analog</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>Ground</td>
</tr>
<tr>
<td>RON</td>
<td>2</td>
<td>Analog</td>
</tr>
<tr>
<td>SS</td>
<td>5</td>
<td>Analog</td>
</tr>
<tr>
<td>VIN</td>
<td>1</td>
<td>Power</td>
</tr>
<tr>
<td>VOUT</td>
<td>7</td>
<td>Power</td>
</tr>
</tbody>
</table>

PIN
TYPE
DESCRIPTION

Enable — Input to the precision enable comparator. Rising threshold is 1.18-V nominal; 90-mV hysteresis nominal. Maximum recommended input level is 6.5 V.
Exposed Pad — Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.
Feedback — Internally connected to the regulation, overvoltage, and short circuit comparators. The regulation reference point is 0.8 V at this input pin. Connected the feedback resistor divider between the output and ground to set the output voltage.
Ground — Reference point for all stated voltages. Must be externally connected to EP.
ON-Time Resistor — An external resistor from VIN to this pin sets the ON-time of the application. Typical values range from 25 kΩ to 124 kΩ.
Soft-Start — An internal 8-µA current source charges an external capacitor to produce the soft-start function. This node is discharged at 200 µA during disable, overcurrent, thermal shutdown and internal UVLO conditions.
Supply input — Nominal operating range is 4.5 V to 20 V. A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and exposed pad.
Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and exposed pad.

6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN, RON to GND</td>
<td>–0.3</td>
<td>25</td>
</tr>
<tr>
<td>EN, FB, SS to GND</td>
<td>–0.3</td>
<td>7</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td></td>
<td>150</td>
</tr>
<tr>
<td>Peak Reflow Case Temperature (30 sec)</td>
<td></td>
<td>245</td>
</tr>
<tr>
<td>Storage Temperature, Tstg</td>
<td>–65</td>
<td>150</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) For soldering specifications, refer to the following document: SNOA549

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.

(2) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114.
6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>4.5</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>EN</td>
<td>0</td>
<td>6.5</td>
<td>V</td>
</tr>
<tr>
<td>Operation Junction Temperature</td>
<td>−40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>LMZ12003</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$ 4-layer JEDEC Printed-Circuit-Board, 100 vias, No air flow</td>
<td>19.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$ 2-layer JEDEC Printed-Circuit-Board, No air flow</td>
<td>21.5</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPR4953.
(2) $R_{JA}$ measured on a 1.705-in × 3.0-in 4-layer board, with 1-oz. copper, thirty five thermal vias, no air flow, and 1-W power dissipation. Refer to PCB layout diagrams.

6.5 Electrical Characteristics

Limits are for $T_J = 25°C$ unless otherwise specified. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25°C$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 12$ V, $V_{OUT} = 1.8$ V(1).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(2)</th>
<th>TYP(3)</th>
<th>MAX(2)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{EN}$ EN threshold trip point</td>
<td>$V_{EN}$ rising over the junction temperature ($T_J$) range of −40°C to +125°C</td>
<td>1.18</td>
<td></td>
<td>1.25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EN-HYS}$ EN threshold hysteresis</td>
<td>$V_{EN}$ falling</td>
<td>90</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SOFT-START</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{SS}$ SS source current</td>
<td>$V_{SS} = 0$ V  over the junction temperature ($T_J$) range of −40°C to +125°C</td>
<td>8</td>
<td>5</td>
<td>11</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{SS-DIS}$ SS discharge current</td>
<td></td>
<td>−200</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CURRENT LIMIT</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CL}$ Current limit threshold</td>
<td>DC average $V_{IN} = 12$ V to 20 V over the junction temperature ($T_J$) range of −40°C to +125°C</td>
<td>4.2</td>
<td>3.2</td>
<td>5.25</td>
<td>A</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ON/OFF Timer</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{ON-MIN}$ ON timer minimum pulse width</td>
<td></td>
<td>150</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{OFF}$ OFF timer pulse width</td>
<td></td>
<td>260</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

(2) Minimum and Maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) Typical numbers are at 25°C and represent the most likely parametric norm.
Electrical Characteristics (continued)

Limits are for $T_J = 25^\circ$C unless otherwise specified. Minimum and Maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^\circ$C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 12$ V, $V_{OUT} = 1.8$ V$^{(1)}$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN$^{(2)}$</th>
<th>TYP$^{(3)}$</th>
<th>MAX$^{(2)}$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FB}$</td>
<td>In-regulation feedback voltage</td>
<td>$V_{SS} &gt; +0.8$ V</td>
<td>$T_J = -40^\circ$C to $125^\circ$C</td>
<td>0.793</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>over the junction temperature ($T_J$) range of $-40^\circ$C to $+125^\circ$C</td>
<td>$I_O = 3$ A</td>
<td></td>
<td>0.773</td>
<td>0.813</td>
</tr>
<tr>
<td></td>
<td>$V_{SS} &gt; +0.8$ V</td>
<td>$T_J = 25^\circ$C</td>
<td>0.784</td>
<td>0.8</td>
<td>0.816</td>
</tr>
<tr>
<td></td>
<td>$I_O = 10$ mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FB-OV}$</td>
<td>Feedback overvoltage protection threshold</td>
<td></td>
<td>0.92</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{FB}$</td>
<td>Feedback input bias current</td>
<td></td>
<td>5</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Non-switching input current</td>
<td>$V_{FB} = 0.86$ V</td>
<td></td>
<td>1</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{SD}$</td>
<td>Shutdown quiescent current</td>
<td>$V_{EN} = 0$ V</td>
<td></td>
<td>25</td>
<td>μA</td>
</tr>
</tbody>
</table>

**THERMAL CHARACTERISTICS**

| $T_{SD}$  | Thermal shutdown | Rising | 165 | °C |
| $T_{SD-HYST}$ | Thermal shutdown hysteresis | Falling | 15 | °C |

**PERFORMANCE PARAMETERS**

| $\Delta V_O$  | Output voltage ripple | 8 | mV$_{PP}$ |
| $\Delta V_O/\Delta V_{IN}$ | Line regulation | $V_{IN} = 8$ V to $20$ V, $I_O = 3$ A | 0.01% |
| $\Delta V_O/\Delta V_{IN}$ | Load regulation | $V_{IN} = 12$ V | 1.5 | mV/A |
| $\eta$ | Efficiency | $V_{IN} = 12$ V, $V_O = 1.8$ V, $I_O = 1$ A | 87% |
|         |           | $V_{IN} = 12$ V, $V_O = 1.8$ V, $I_O = 3$ A | 77% |
6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: $V_{IN} = 12\,\text{V}$; $C_{IN} = 10-\mu\text{F X7R Ceramic}$; $C_{O} = 100-\mu\text{F X7R Ceramic}$; $T_A = 25^\circ\text{C}$ for efficiency curves and waveforms.

Figure 1. Efficiency 6-V Input at 25°C

Figure 2. Dissipation 6-V Input at 25°C

Figure 3. Efficiency 12-V Input at 25°C

Figure 4. Dissipation 12-V Input at 25°C

Figure 5. Efficiency 6-V Input at 85°C

Figure 6. Dissipation 6-V Input at 85°C
Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{IN} = 12$ V; $C_{IN} = 10$-$\mu$F X7R Ceramic; $C_{O} = 100$-$\mu$F X7R Ceramic; $T_A = 25^\circ$C for efficiency curves and waveforms.

<table>
<thead>
<tr>
<th>OUTPUT VOLTAGE (V)</th>
<th>OUTPUT CURRENT (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.5</td>
<td>0 0.5 1 1.5 2 2.5 3</td>
</tr>
<tr>
<td>4.75</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>5.25</td>
<td></td>
</tr>
<tr>
<td>5.5</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DISSIPATION (W)</th>
<th>OUTPUT CURRENT (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0</td>
<td>0 0.5 1 1.5 2 2.5 3</td>
</tr>
<tr>
<td>3.3</td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>EFFICIENCY (%)</th>
<th>OUTPUT CURRENT (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.0</td>
<td>0 0.5 1 1.5 2 2.5 3</td>
</tr>
<tr>
<td>3.3</td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td></td>
</tr>
</tbody>
</table>

Figure 7. Efficiency 8-V Input at 85°C

Figure 8. Dissipation 8-V Input at 85°C

Figure 9. Efficiency 12-V Input at 85°C

Figure 10. Dissipation 12-V Input at 85°C

Figure 11. Line and Load Regulation at 25°C

Figure 12. Output Ripple
Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: $V_{IN} = 12\, V$; $C_{IN} = 10\, \mu F$ X7R Ceramic; $C_O = 100\, \mu F$ X7R Ceramic; $T_A = 25^\circ C$ for efficiency curves and waveforms.

Figure 13. Transient Response

Figure 14. Thermal Derating
7 Detailed Description

7.1 Overview
The LMZ12003 power module is an easy-to-use step-down DC-DC solution capable of driving up to 3-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 COT Control Circuit Overview
Constant ON-Time control is based on a comparator and an ON-time one-shot, with the output voltage feedback compared with an internal 0.8-V reference. If the feedback voltage is below the reference, the main MOSFET is turned on for a fixed ON-time determined by a programming resistor $R_{ON}$. $R_{ON}$ is connected to $V_{IN}$ such that ON-time is reduced with increasing input supply voltage. Following this ON-time, the main MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the ON-time cycle is repeated. Regulation is achieved in this manner.

7.3.2 Output Overvoltage Comparator
The voltage at FB is compared to a 0.92-V internal reference. If FB rises above 0.92 V the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET ON-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

7.3.3 Current Limit
Current limit detection is carried out during the OFF-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 4.2 A (typical) the current limit comparator disables the start of the next ON-time period. The next switching cycle will occur only if the FB input is less than 0.8 V and the inductor current has decreased below 4.2 A. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds 4.2 A, further ON-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer OFF-time.
Feature Description (continued)

7.3.4 Thermal Protection
The junction temperature of the LMZ12003 should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165°C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing $V_O$ to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20°C) the SS pin is released, $V_O$ rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require application derating at elevated temperatures.

7.3.5 Zero Coil Current Detection
The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

7.3.6 Prebiased Start-Up
The LMZ12003 will properly start up into a prebiased output. This startup situation is common in multiple rail logic applications where current paths may exist between different power rails during the start-up sequence. The following scope capture shows proper behavior during this event.

![Figure 15. Prebiased Start-Up](image)

7.4 Device Functional Modes

7.4.1 Discontinuous Conduction and Continuous Conduction Modes
At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the OFF-time. Note that during the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next ON-time period starts when the voltage on the at the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained because conduction and switching losses are reduced with the smaller load and lower switching frequency.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The LMZ12003 is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LMZ12003. Alternately, the WEBENCH software may be used to generate complete designs. When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. Please go to www.ti.com for more details.

8.2 Typical Application

![Figure 16. Evaluation Board Schematic Diagram](image)

8.2.1 Design Requirements
For this example the following application parameters exist.
- \(V_{\text{IN}}\) Range = Up to 20 V
- \(V_{\text{OUT}}\) = 0.8 V to 6 V
- \(I_{\text{OUT}}\) = 3 A

8.2.2 Detailed Design Procedure
The LMZ12003 is fully supported by WEBENCH and offers the following: component selection, electrical and thermal simulations, as well as the build-it board for a reduction in design time. The following list of steps can be used to manually design the LMZ12003 application.

1. Select minimum operating \(V_{\text{IN}}\) with enable divider resistors
2. Program \(V_{\text{O}}\) with divider resistor selection
Typical Application (continued)

3. Program turn on time with soft-start capacitor selection
4. Select $C_O$
5. Select $C_{IN}$
6. Set operating frequency with $R_{ON}$

8.2.2.1 Enable Divider, $R_{ENT}$ and $R_{ENB}$ Selection

The enable input provides a precise 1.18-V band-gap rising threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as $V_{IN}$. The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09 V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage.

The function of this resistive divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turnon of the supply as the main input voltage rail rises at power-up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems where a lower boundary of operation must be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ12003 output rail. The two resistors must be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN} / 1.18V) - 1 \quad (1)$$

The LMZ12003 demonstration and evaluation boards use 11.8 kΩ for $R_{ENB}$ and 32.4 kΩ for $R_{ENT}$ resulting in a rising UVLO of 4.5 V. This divider presents 5.34 V to the EN input when the divider input is raised to 20 V.

The EN pin is internally pulled up to $V_{IN}$ and can be left floating for always-on operation.

8.2.2.2 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between $V_O$ and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8-V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The main MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur.

The regulated output voltage determined by the external divider resistors $R_{FBT}$ and $R_{FBB}$ is:

$$V_O = 0.8V \times (1 + R_{FBT} / R_{FBB}) \quad (2)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.8V) - 1 \quad (3)$$

These resistors must be chosen from values in the range of 1.0 kΩ to 10.0 kΩ.

For $V_O = 0.8$ V the FB pin can be connected to the output directly so long as an output preload resistor remains that draws more than 20 µA. Converter operation requires this minimum load to create a small inductor ripple current and maintain proper regulation when no load is present.

A feed-forward capacitor is placed in parallel with $R_{FBT}$ to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

Table 1 lists the values for $R_{FBT}$, $R_{FBB}$, $C_{FF}$ and $R_{ON}$.

### Table 1. Bill of Materials

<table>
<thead>
<tr>
<th>REF DES</th>
<th>DESCRIPTION</th>
<th>CASE SIZE</th>
<th>MANUFACTURER</th>
<th>MANUFACTURER P/N</th>
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<tr>
<td>U1</td>
<td>SIMPLE SWITCHER</td>
<td>PFM-7</td>
<td>Texas Instruments</td>
<td>LMZ12003 TZ</td>
</tr>
<tr>
<td>$C_{in1}$</td>
<td>1-µF, 50-V, X7R</td>
<td>1206</td>
<td>Taiyo Yuden</td>
<td>UMK316B7105KL-T</td>
</tr>
<tr>
<td>$C_{in2}$</td>
<td>10-µF, 50-V, X7R</td>
<td>1210</td>
<td>Taiyo Yuden</td>
<td>UMK325BJ106MM-T</td>
</tr>
<tr>
<td>$C_O$</td>
<td>1-µF, 50-V, X7R</td>
<td>1206</td>
<td>Taiyo Yuden</td>
<td>UMK316B7105KL-T</td>
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Typical Application (continued)

Table 1. Bill of Materials (continued)

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<th>DESCRIPTION</th>
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<th>MANUFACTURER</th>
<th>MANUFACTURER P/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{O2}</td>
<td>100-µF, 6.3-V, X7R</td>
<td>1210</td>
<td>Taiyo Yuden</td>
<td>JMK325BJ10CR7MM-T</td>
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<tr>
<td>R_{FBT}</td>
<td>1.37 kΩ</td>
<td>0603</td>
<td>Vishay Dale</td>
<td>CRCW06031K37FKEA</td>
</tr>
<tr>
<td>R_{FBB}</td>
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<td>0603</td>
<td>Vishay Dale</td>
<td>CRCW06031K07FKEA</td>
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<tr>
<td>R_{ON}</td>
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<td>0603</td>
<td>Vishay Dale</td>
<td>CRCW060332K4FKEA</td>
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<tr>
<td>R_{ENT}</td>
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<td>Vishay Dale</td>
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<td>0603</td>
<td>TDK</td>
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<tr>
<td>C_{SS}</td>
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<td>0603</td>
<td>TDK</td>
<td>C1608X7R1H223K</td>
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8.2.2.3 Soft-Start Capacitor Selection

Programmable soft-start permits the regulator to slowly ramp to its steady-state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turnon, after all UVLO conditions have been passed, an internal 8-µA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady-state operation is given by the formula:

\[ t_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}} = \frac{0.8 \text{ V} \times C_{SS}}{8 \text{ µA}} \]  

This equation can be rearranged as follows:

\[ C_{SS} = \frac{t_{SS} \times 8 \text{ µA}}{0.8 \text{ V}} \]  

Use of a 0.022-µF capacitor results in 2.2-ms soft-start duration. This is recommended as a minimum value.

As the soft-start input exceeds 0.8 V the output of the power stage will be in regulation. The soft-start capacitor continues charging until it reaches approximately 3.8 V on the SS pin. Voltage levels between 0.8 V and 3.8 V have no effect on other circuit operation. The following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200-µA current sink:

- The enable input being *pulled low*
- Thermal shutdown condition
- Overcurrent fault
- Internal V\textsubscript{CC} UVLO (Approx 4-V input to V\textsubscript{IN})

8.2.2.4 C\textsubscript{O} Selection

None of the required C\textsubscript{O} output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst case minimum ripple current rating of 0.5 × I\textsubscript{ERP-P}, as calculated in Equation 20. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Ceramic capacitors or other low ESR types are recommended. See AN-2024 for more detail.

**Equation 17** provides a good first pass approximation of C\textsubscript{O} for load transient requirements:

\[ C_{O} \geq \frac{I_{STEP} \times V_{FB} \times L \times V_{IN}}{(4 \times V_{O} \times (V_{IN} - V_{O}) \times V_{OUT-TRAN})} \]  

Solving for **Equation 7** yields the following:

\[ C_{O} \geq \frac{3 \text{ A} \times 0.8 \text{ V} \times 6.8 \text{ µH} \times 12 \text{ V}}{(4 \times 3.3 \text{ V} \times (12 \text{ V} - 3.3 \text{ V}) \times 33 \text{ mV})} \geq 52 \text{ µF} \]  

The LMZ12003 demonstration and evaluation boards are populated with a 100-uF 6.3-V X5R output capacitor. Locations for extra output capacitors are provided.
8.2.2.5 \( C_{IN} \) Selection

The LMZ12003 module contains an internal 0.47-\( \mu \)F input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance must be located in very close proximity to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst case input ripple current rating is dictated by Equation 8:

\[
I(C_{IN(RMS)}) \approx \frac{1}{2} \times I_O \times \sqrt{D / (1-D)}
\]

where

\[
D \approx \frac{V_O}{V_{IN}}
\]

As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when \( V_{IN} = 2 \times V_O \).

Recommended minimum input capacitance is 10-\( \mu \)F X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI recommends to pay attention to the voltage and temperature deratings of the capacitor selected.

**NOTE**

Ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this rating.

If the system design requires a certain minimum value of input ripple voltage \( \Delta V_{IN} \) be maintained then Equation 9 may be used.

\[
C_{IN} \geq I_O \times (1-D) / f_{SW-CCM} \times \Delta V_{IN}
\]

If \( \Delta V_{IN} \) is 1% of \( V_{IN} \) for a 20V input to 3.3-V output application this equals 200 mV and \( f_{SW} = 400 \) kHz.

\[
C_{IN} \geq 3 \text{ A} \times 3.3 \text{ V} / 20 \text{ V} \times (1 - 3.3 \text{ V} / 20 \text{ V}) / (400000 \times 0.200 \text{ V}) \geq 5.2 \mu\text{F}
\]

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

8.2.2.6 \( R_{ON} \) Resistor Selection

Many designs will begin with a desired switching frequency in mind. For that purpose Equation 10 can be used.

\[
f_{SW(CCM)} \approx \frac{V_O}{(1.3 \times 10^{-10} \times R_{ON})}
\]

This can be rearranged as

\[
R_{ON} \approx \frac{V_O}{(1.3 \times 10^{-10} \times f_{SW(CCM)})}
\]

The selection of \( R_{ON} \) and \( f_{SW(CCM)} \) must be confined by limitations in the ON-time and OFF-time for the COT Control Circuit Overview section.

The ON-time of the LMZ12003 timer is determined by the resistor \( R_{ON} \) and the input voltage \( V_{IN} \). It is calculated as follows:

\[
t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN}
\]

The inverse relationship of \( t_{ON} \) and \( V_{IN} \) gives a nearly constant switching frequency as VIN is varied. \( R_{ON} \) must be selected such that the ON-time at maximum \( V_{IN} \) is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for \( t_{ON} \). This limits the maximum operating frequency, which is governed by Equation 13:

\[
f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150 \text{ ns})
\]

This equation can be used to select \( R_{ON} \) if a certain operating frequency is desired so long as the minimum ON-time of 150 ns is observed. The limit for \( R_{ON} \) can be calculated as follows:

\[
R_{ON} \geq V_{IN(MAX)} \times 150 \text{ ns} / (1.3 \times 10^{-10})
\]

If \( R_{ON} \) calculated in Equation 11 is less than the minimum value determined in Equation 14 a lower frequency must be selected. Alternatively, \( V_{IN(MAX)} \) can also be limited in order to keep the frequency unchanged.

Additionally, consider the minimum OFF-time of 260 ns limits the maximum duty ratio. Larger \( R_{ON} \) (lower \( F_{SW} \)) should be selected in any application requiring large duty ratio.
8.2.2.7 Discontinuous Conduction and Continuous Conduction Mode Selection

Operating frequency in DCM can be calculated as follows:

\[ f_{SW(DCM)} \approx V_o \times (V_{IN} - 1) \times 6.8 \mu H \times 1.18 \times 10^{20} \times I_o / (V_{IN} - V_o) \times R_{ON}^2 \]  

(15)

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using Equation 7.

Figure 17 is a comparison pair of waveforms of the showing both CCM (upper) and DCM operating modes.

Figure 17. CCM and DCM Operating Modes

V_{IN} = 12 V, V_o = 3.3 V, I_o = 3 A/0.4 A 2 \mu s/\text{div}

The approximate formula for determining the DCM/CCM boundary is as follows:

\[ I_{DCB} \approx V_o \times (V_{IN} - V_o) / (2 \times 6.8 \mu H \times f_{SW(CCM)} \times V_{IN}) \]  

(16)

Figure 18 is a typical waveform showing the boundary condition.

Figure 18. Transition Mode Operation

V_{IN} = 12 V, V_o = 3.3 V, I_o = 0.5 A 2 \mu s/\text{div}

The inductor internal to the module is 6.8 \mu H. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

\[ I_{LR\,P-P} = V_o \times (V_{IN} - V_o) / (6.8 \mu H \times f_{SW} \times V_{IN}) \]

where

- \( V_{IN} \) is the maximum input voltage
- and \( f_{SW} \) is determined from Equation 10.

(17)

If the output current \( I_o \) is determined by assuming that \( I_o = I_L \), the higher and lower peak of \( I_{LR} \) can be determined. Be aware that the lower peak of \( I_{LR} \) must be positive if CCM operation is required.
### 8.2.3 Application Curves

#### Figure 19. Efficiency

$V_{\text{IN}} = 12 \, \text{V}, \, V_{\text{OUT}} = 5 \, \text{V}$

#### Figure 20. Thermal Derating Curve

$V_{\text{IN}} = 12 \, \text{V}, \, V_{\text{OUT}} = 5 \, \text{V}$

#### Figure 21. Radiated Emissions (EN 55022 Class B) from Evaluation Board
9 Power Supply Recommendations

The LMZ12003 device is designed to operate from an input voltage supply range between 4.5 V and 20 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ12003 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ12003, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-μF or 100-μF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops.

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt current paths during PCB layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor $C_{IN1}$ is placed a distance away for the LMZ12003. Therefore, physically place $C_{IN1}$ as close as possible to the LMZ12003 VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor must consist of a localized top side plane that connects to the GND exposed pad (EP).

2. Have a single point ground.

   The ground connections for the feedback, soft-start, and enable components must be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. Minimize trace length to the FB pin.

   Both feedback resistors, $R_{FBT}$ and $R_{FBB}$, and the feed forward capacitor $C_{FF}$, must be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The trace are from $R_{FBT}$, $R_{FBB}$, and $C_{FF}$ must be routed away from the body of the LMZ12003 to minimize noise.

4. Make input and output bus connections as wide as possible.

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. Provide adequate device heat-sinking.

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 x 6 via array with a minimum via diameter of 8 mils thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.
10.2 Layout Examples

**Figure 22. Critical Current Loops to Minimize**

**Figure 23. PCB Layout Guide**
10.3 Power Dissipation and Thermal Considerations

For the design case of $V_{IN} = 12\,V$, $V_O = 3.3\,V$, $I_O = 3\,A$, $T_{AMB(MAX)} = 85^\circ C$, and $T_{JUNCTION} = 125^\circ C$, the device must see a thermal resistance from case to ambient of less than:

$$R_{\theta CA} < \frac{(T_{J-MAX} - T_{AMB(MAX)})}{P_{IC-LOSS}} - R_{\theta JC}$$  \hspace{1cm} (18)

Given the typical thermal resistance from junction to case to be 1.9°C/W. Use the 85°C power dissipation curves in the Typical Characteristics section to estimate the $P_{IC-LOSS}$ for the application being designed. In this application it is 2.25 W.

$$R_{\theta CA} < \frac{(125 - 85)}{2.25 \,W} - 1.9 = 15.8$$  \hspace{1cm} (19)

To reach $R_{\theta CA} = 15.8$, the PCB is required to dissipate heat effectively. With no airflow and no external heat, a good estimate of the required board area covered by 1-oz. copper on both the top and bottom metal layers is:
Power Dissipation and Thermal Considerations (continued)

As a result, approximately 31 square cm of 1-oz. copper on top and bottom layers is required for the PCB design. The PCB copper heat sink must be connected to the exposed pad. Approximately thirty six, 8 mils thermal vias spaced 59 mils (1.5 mm) apart must connect the top copper to the bottom copper. For an example of a high thermal performance PCB layout, refer to the demo board application note AN-2024 SNVA422.

10.4 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- **Land Pattern** — Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads.
- **Stencil Aperture**
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- **Solder Paste** — Use a standard SAC Alloy such as SAC 305, type 3 or higher
- **Stencil Thickness** — 0.125 to 0.15 mm
- **Reflow** - Refer to solder paste supplier recommendation and optimized per board size and density
- **Refer to Design Summary LMZ1xxx and LMZ2xxx Power Modules Family (SNAA214) for reflow information.**
- **Maximum number of refows allowed is one**

![Image of Sample Reflow Profile]

**Figure 26. Sample Reflow Profile**

<table>
<thead>
<tr>
<th>PROBE</th>
<th>MAX TEMP (°C)</th>
<th>REACHED MAX TEMP</th>
<th>TIME ABOVE 235°C</th>
<th>REACHED 235°C</th>
<th>TIME ABOVE 245°C</th>
<th>REACHED 245°C</th>
<th>TIME ABOVE 260°C</th>
<th>REACHED 260°C</th>
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<tr>
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<td>242.5</td>
<td>6.58</td>
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<td>–</td>
<td>0.00</td>
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</tr>
</tbody>
</table>
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer
TI's publication of information regarding third-party products or services does not constitute an endorsement regarding the suitability of such products or services or a warranty, representation or endorsement of such products or services, either alone or in combination with any TI product or service.

11.1.2 Development Support
For developmental support, see the following:

11.2 Documentation Support

11.2.1 Related Documentation
For related documentation, see the following:
  • AN-2027 Inverting Application for the LMZ14203 SIMPLE SWITCHER Power Module, (SNVA425)
  • Absolute Maximum Ratings for Soldering, (SNOA549)
  • AN-2024 LMZ1420x / LMZ1200x Evaluation Board (SNVA422)
  • AN-2085 LMZ23605/03, LMZ22005/03 Evaluation Board (SNVA457)
  • AN-2054 Evaluation Board for LM10000 - PowerWise AVS System Controller (SNVA437)
  • AN-2020 Thermal Design By Insight, Not Hindsight (SNVA419)
  • AN-2026 Effect of PCB Design on Thermal Performance of SIMPLE SWITCHER Power Modules (SNVA424)
  • Design Summary LMZ1xxx and LMZ2xxx Power Modules Family (SNAA214)

11.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks
E2E is a trademark of Texas Instruments.
WEBENCH, SIMPLE SWITCHER are registered trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
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<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<td>TO-PMOD</td>
<td>NDW</td>
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<td>250</td>
<td>RoHS &amp; Green</td>
<td>CU SN</td>
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<td>-40 to 125</td>
<td>LMZ12003 TADJ</td>
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</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Mapping contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

![Reel Dimensions Diagram](image1)

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMZ12003TZ-ADJ/NOPB</td>
<td>TO-PMOD</td>
<td>NDW</td>
<td>7</td>
<td>250</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>14.22</td>
<td>5.0</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
<tr>
<td>LMZ12003TZX-ADJ/NOPB</td>
<td>TO-PMOD</td>
<td>NDW</td>
<td>7</td>
<td>500</td>
<td>330.0</td>
<td>24.4</td>
<td>10.6</td>
<td>14.22</td>
<td>5.0</td>
<td>16.0</td>
<td>24.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- User Direction of Feed
- Sprocket Holes
- Pocket Quadrants
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMZ12003TZ-ADJ/NOPB</td>
<td>TO-PMOD</td>
<td>NDW</td>
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<td>250</td>
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<td>367.0</td>
<td>45.0</td>
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<tr>
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<td>TO-PMOD</td>
<td>NDW</td>
<td>7</td>
<td>500</td>
<td>367.0</td>
<td>367.0</td>
<td>45.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
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