LPV821, 650nA, Precision, Nanopower, Zero-Drift Amplifier

1 Features
• Quiescent Current: 650 nA
• Low Offset Voltage: ±20 μV (Maximum)
• Zero Drift: 0.08 μV/°C (Maximum)
• 0.1-Hz to 10-Hz Noise: 3.9 μVpp
• Input Bias Current: ±7 pA
• Gain Bandwidth: 8 kHz
• Supply Voltage: 1.7 V to 3.6 V
• Rail-to-Rail Input/Output
• Industry Standard Package
  – Single in 5-pin SOT-23
• EMI Hardened

2 Applications
• Battery-Powered Instruments
• Gas Detection
• Current Sensing
  – Shunt Resistor
  – Current Transformer
• Temperature Measurements
  – High Impedance Thermistors
  – RTD’s, Thermocouples
• Strain Gauges
  – Electronic Scales
  – Pressure Sensors

3 Description
The LPV821 is a single-channel, nanopower, zero-drift operational amplifier for “Always ON” sensing applications in wireless and wired equipment where low input offset is required. With the combination of low initial offset, low offset drift, and 8 kHz of bandwidth from 650 nA of quiescent current, the LPV821 is the industry's lowest power zero-drift amplifier that can be used for end equipment that monitor current consumption, temperature, gas, or strain gauges.

The LPV821 zero-drift operational amplifier uses a proprietary auto-calibration technique to simultaneously provide low offset voltage (20 μV, maximum) and minimal drift over time and temperature. In addition to having low offset and ultra-low quiescent current, the LPV821 amplifier has pico-amp bias currents which reduce errors commonly introduced in applications monitoring sensors with high output impedance and amplifier configurations with megaohm feedback resistors.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPV821</td>
<td>SOT-23 (5)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
<tr>
<td>LPV821*</td>
<td>X2QFN (8)</td>
<td>1.50 mm × 1.50 mm</td>
</tr>
</tbody>
</table>

Precision Nano-Power Amplifier Family

<table>
<thead>
<tr>
<th>FAMILY</th>
<th>CHAN COUNT</th>
<th>Iq PER CHAN</th>
<th>VOS (MAX)</th>
<th>V SUPPLY</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPV821</td>
<td>1</td>
<td>650 nA</td>
<td>20 μV</td>
<td>1.7 to 3.6 V</td>
</tr>
<tr>
<td>LPV811</td>
<td>1</td>
<td>450 nA</td>
<td>370 μV</td>
<td>1.6 to 5.5 V</td>
</tr>
<tr>
<td>LPV812</td>
<td>2</td>
<td>425 nA</td>
<td>300 μV</td>
<td>1.6 to 5.5 V</td>
</tr>
<tr>
<td>OPA369</td>
<td>1.2</td>
<td>800 nA</td>
<td>750 μV</td>
<td>1.8 to 5.5 V</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) * Planned for near-future release

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.
4 Description Con’t
The LPV821 amplifier also features an input stage with rail-to-rail input common mode range and an output stage that swings within 15 mV of the rails, maintaining the widest dynamic range possible. The device is EMI hardened to reduce system sensitivity to unwanted RF signals from mobile phones, WiFi, radio transmitters, and tag readers.

The LPV821 zero-drift amplifier operates with a single supply voltage as low as 1.7V, ensuring continuous performance in low battery situations over the extended temperature range of -40ºC to 125ºC. The LPV821 (single) is available in industry standard 5-pin SOT-23.

5 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>August 2017</td>
<td>*</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

LPV821 5-Pin SOT-23
DBV Package
Top View

Pin Functions: LPV821 DBV

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>V–</td>
<td>P</td>
<td>Negative (lowest) power supply</td>
</tr>
<tr>
<td>+IN</td>
<td>I</td>
<td>Non-Inverting Input</td>
</tr>
<tr>
<td>–IN</td>
<td>I</td>
<td>Inverting Input</td>
</tr>
<tr>
<td>V+</td>
<td>P</td>
<td>Positive (highest) power supply</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings

See (1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage, ( V_S = (V^+ - V^-) )</td>
<td>-0.3</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>Input/Output Pin Voltage (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Input Voltage +IN - (-IN) (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>-10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Junction temperature</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Operating ambient temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, ( T_{stg} )</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.

(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)</td>
<td>±1000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)</td>
<td>±250</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, ( V_S = (V^+ - V^-) )</td>
<td>1.7</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Specified temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>Thermal Metric</th>
<th>LPV821</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-ambient thermal resistance</td>
<td>218.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-case (top) thermal resistance</td>
<td>101.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board thermal resistance</td>
<td>52.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-top characterization parameter</td>
<td>18.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board characterization parameter</td>
<td>52.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
### 7.5 Electrical Characteristics

\[ T_A = 25^\circ C, \ V_S = 1.8 \text{ V to 3.3 V, } V_{CM} = V_{OUT} = V_S/2, \text{ and } R_L \geq 10 \text{ M} \Omega \text{ to } V_S/2, \text{ unless otherwise noted.} \]

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OS} ) Input offset voltage ((1))</td>
<td>( V_S = 3.3 \text{ V} )</td>
<td>±1.5</td>
<td>±20</td>
<td></td>
<td>µV</td>
</tr>
<tr>
<td>( dV_{OS}/dT ) Input offset voltage drift</td>
<td>( T_A = -40^\circ C \text{ to } 125^\circ C, \ V_S = 3.3 \text{ V} )</td>
<td>±0.02</td>
<td>±0.08</td>
<td></td>
<td>µV/°C</td>
</tr>
<tr>
<td>PSRR Power-supply rejection ratio</td>
<td>( V_S = 1.8 \text{ V to 3.3 V} )</td>
<td>1</td>
<td>10</td>
<td></td>
<td>pV/V</td>
</tr>
</tbody>
</table>

**INPUT BIAS CURRENT**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_B ) Input bias current (+IN)</td>
<td>( T_A = 25^\circ C )</td>
<td>±7</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>( I_B ) Input bias current (-IN)</td>
<td>( T_A = 125^\circ C )</td>
<td>±7</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>( I_{OIS} ) Input offset current</td>
<td></td>
<td>±14</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
</tbody>
</table>

**NOISE**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( E_n ) Input voltage noise</td>
<td>( f = 0.1 \text{ Hz to } 10 \text{ Hz} )</td>
<td>3.9</td>
<td></td>
<td></td>
<td>µVpp</td>
</tr>
<tr>
<td>( e_n ) Input voltage noise density</td>
<td>( f = 100 \text{ Hz} )</td>
<td>215</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>( I_{in} ) Input current noise density</td>
<td>( f = 100 \text{ Hz} )</td>
<td>1</td>
<td></td>
<td></td>
<td>fA/√Hz</td>
</tr>
</tbody>
</table>

**INPUT VOLTAGE**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CM} ) Common-mode voltage range</td>
<td>( (V–) \leq V_{CM} \leq (V+) ), ( V_S = 3.3 \text{ V} )</td>
<td>90</td>
<td>125</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

**INPUT CAPACITANCE**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential</td>
<td></td>
<td>3.3</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Common-mode</td>
<td></td>
<td>3.7</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

**OPEN-LOOP GAIN**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_{OL} ) Open-loop voltage gain</td>
<td>( (V–) + 0.1 \text{ V} \leq V_O \leq (V+) – 0.1 \text{ V} ), ( R_L = 100 \text{ k} \Omega \text{ to } V_S/2 )</td>
<td>135</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

**FREQUENCY RESPONSE**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBW Gain-bandwidth product</td>
<td>( C_L = 20 \text{ pF}, R_L = 10 \text{ M} \Omega )</td>
<td>8</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>SR Slew rate</td>
<td>( G = +1, C_L = 20 \text{ pF} )</td>
<td>3.3</td>
<td></td>
<td></td>
<td>V/ms</td>
</tr>
</tbody>
</table>

**OUTPUT**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OH} ) Voltage output swing from positive rail</td>
<td>( R_L = 100 \text{ k} \Omega \text{ to } V^*/2, V_S = 3.3 \text{ V} )</td>
<td>15</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_{OL} ) Voltage output swing from negative rail</td>
<td>( R_L = 100 \text{ k} \Omega \text{ to } V^*/2, V_S = 3.3 \text{ V} )</td>
<td>15</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( I_{SC} ) Short-circuit current</td>
<td></td>
<td>21</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( C_L ) Capacitive load drive</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( Z_O ) Open-loop output impedance</td>
<td>( f = 100 \text{ Hz}, I_O = 0 \text{ A} )</td>
<td>80</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

**POWER SUPPLY**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_Q ) Quiescent current per channel</td>
<td>( V_{CM} = V_S/2, I_O = 0, V_S = 3.3 \text{ V} )</td>
<td>650</td>
<td>750</td>
<td></td>
<td>nA</td>
</tr>
</tbody>
</table>

(1) Max limit based on testing limitations at production. Device has demonstrated to perform better at time of characterization. See Plots
7.6 Typical Characteristics

At $T_A = 25^\circ C$, $V_S = 3.3\, V$, and $C_L = 0\, \mu F$, unless otherwise noted.
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = 3.3 \, V$, and $C_L = 0 \, pF$, unless otherwise noted.

![Graphs showing input bias current vs common mode voltage and temperature](image-url)
Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 3.3 \text{ V}$, and $C_L = 0 \text{ pF}$, unless otherwise noted.

Figure 13. CMRR vs Frequency

Figure 14. PSRR vs Frequency

Figure 15. EMIRR Performance

Figure 16. Per Channel Quiescent Current vs Supply Voltage

Figure 17. Open Loop Output Impedance

Figure 18. Voltage Noise Spectral Density vs Frequency
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = 3.3$ V, and $C_L = 0$ pF, unless otherwise noted.

---

V$_S$ = 1.8 V  
$T_A = -40, 25, 125^\circ C$

V$_S$ = 3.3 V  
$T_A = -40, 25, 125^\circ C$

Figure 19. Output Swing vs. Sinking Current, 1.8 V

Figure 20. Output Swing vs. Sinking Current, 3.3 V

---

V$_S$ = 1.8 V  
$T_A = -40, 25, 125^\circ C$

V$_S$ = 3.3 V  
$T_A = -40, 25, 125^\circ C$

Figure 21. Output Swing vs Sourcing Current, 1.8 V

Figure 22. Output Swing vs Sourcing Current, 3.3 V
8 Detailed Description

8.1 Overview
The LPV821 is a zero-drift, nanopower, rail-to-rail input and output operational amplifier. The device operates from 1.7 V to 3.7 V, is unity-gain stable, and is suitable for a wide range of general-purpose applications. The zero-drift architecture provides ultra low offset voltage and near-zero offset voltage drift.

8.2 Functional Block Diagram

8.3 Feature Description
The LPV821 is unity-gain stable and uses an auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

8.3.1 Operating Voltage
The LPV821 operational amplifier operates over a power-supply range of 1.7 V to 3.6V (±0.85 V to ± 1.8 V). Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section.

CAUTION
Supply voltages higher than 4 V (absolute maximum) can permanently damage the device.
Feature Description (continued)

8.3.2 Input

The LPV821 input common-mode voltage range extends to the supply rails. Typically, the input bias current is approximately 7 pA; however, input voltages that exceed the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with adding a resistor in series with the input, as shown in Figure 23.

8.3.3 Internal Offset Correction

The LPV821 operational amplifier combines an auto-calibration technique with a time-continuous 8-kHz operational amplifier in the signal path. The amplifier is zero-corrected every 1 ms using a proprietary technique. This design has no aliasing or flicker (1/f) noise.

8.4 Device Functional Modes

The LPV821 has a single functional mode. The device is powered on as long as the power supply voltage is between 1.7 V (±0.85 V) and 3.6 V (±1.8 V).

8.4.1 EMI Performance and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The LPV821 operational amplifier incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common mode and differential-mode filtering are provided by the input filter.

8.4.2 Driving Capacitive Load

The LPV821 is internally compensated for stable unity-gain operation, with a 8-kHz typical gain bandwidth. However, the unity-gain follower is the most sensitive configuration-to-capacitive load. The combination of a capacitive load placed directly on the output of an amplifier along with the output impedance of the amplifier creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response is under-damped, which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

In order to drive heavy (> 50 pF) capacitive loads, use an isolation resistor, $R_{ISO}$, as shown in Figure 24. The value of the $R_{ISO}$ to be used should be decided depending on the size of the $C_L$ and the level of performance desired. Values ranging from 5 kΩ to 100 kΩ are usually sufficient to ensure stability. By using the isolation resistor, the capacitive load is isolated from the output of the amplifier. The larger the value of $R_{ISO}$, the more stable the amplifier will be. If the value of $R_{ISO}$ is sufficiently large, the feedback loop is stable, independent of the value of $C_L$. However, larger values of $R_{ISO}$ (e.g. 50 kΩ) result in reduced output swing and reduced output current drive.
Device Functional Modes (continued)

![Resistive Isolation of Capacitive Load](image)

**Figure 24. Resistive Isolation of Capacitive Load**

## 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LPV821 is a unity-gain stable, precision operational amplifier with very low offset voltage drift; the device is also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1-μF capacitors are adequate.

### 9.2 Typical Applications

#### 9.2.1 Low-Side Current Measurement

This single-supply, low-side, current-sensing solution shown in Figure 25 detects load currents up to 1 A. This design uses the LPV821 because of its low offset voltage and rail-to-rail input and output. The LPV821 in the main signal path is configured as a difference amplifier and a second LPV821 provides a buffered bias voltage to allow transition of signal below and above the bias level for bi-direction current sensing. The low offset voltage and offset drift of the LPV821 facilitate excellent dc accuracy for the circuit.
Typical Applications (continued)

9.2.1.1 Design Requirements

The design requirements are as follows:
- Supply Voltage: 3.3 V DC
- Input: 1 A (Max)
- Output: 1.65V ± 1.54 V ; (110 mV to 3.19 V)

9.2.1.2 Detailed Design Procedure

Referring to Figure 25, the load current passing through the shunt resistor (Rshunt) develops the shunt voltage, Vshunt across the resistor. The shunt voltage is then amplified by the LPV821 by the ratio of R4 by R3. The gain of the difference amplifier is set by the ratio of R4 to R3. To minimize errors, set R2 = R4 and R1 = R3. The bias voltage is supplied by buffering a resistor divider using a second LPV821 nanopower op amp. The circuit equations are provided below.

\[ V_{\text{out}} = V_{\text{shunt}} \times \text{Gain}_{\text{Diff}} + V_{\text{bias}} \]  
\[ V_{\text{shunt}} = I_{\text{load}} \times R_{\text{shunt}} \]  
\[ \text{Gain}_{\text{Diff}} = \frac{R_4}{R_3} \]  
\[ V_{\text{bias}} = \left[ \frac{R_5}{R_5 + R_6} \right] \times V_{\text{CC}} \]  
\[ R_{\text{shunt}} = \left[ \frac{V_{\text{shunt}}(\text{max})}{I_{\text{load}}(\text{max})} \right] \]

Because \( V_{\text{shunt}} \) is a low-side measurement, a maximum value 100 mV was selected.

\[ R_{\text{shunt}} = \frac{V_{\text{shunt}}}{I_{\text{load}}} = \frac{100 \text{mV}}{1 \text{A}} = 100 \text{mΩ} \]

The tolerance of the shunt resistor, the ratio of R4 to R3 and the ratio of R2 to R1 are the main sources of gain error in the signal path. To optimize the cost, a shut resistor with a tolerance of 0.5% was chosen. The main sources of offset errors in the circuit are the voltage divider network comprise of R5, R6 and how closely the ratio of R4 / R3 matches the ration of R2 / R1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The shunt voltage is scaled down by a divider network made of R1 and R2 before reaching the LPV821 amplifier stage. The voltage present at the non-inverting node of the LPV821 should not exceed the common-mode range of the device. The extremely low offset voltage and drift of the LPV821 ensures minimized offset error in the measurement.
Typical Applications (continued)

In case a bi-direction current sensing is required, for symmetric load current of –1 A to 1 A, the voltage divider resistors R5 and R6 must be equal. To minimize power consumption, 100-kΩ resistors with a tolerance of 0.5% were selected.

To set the gain of the difference amplifier, the common-mode range and output swing of the LPV821 must be considered. The gain of the difference amplifier can now be calculated as shown below:

\[
\text{Gain} = \frac{\text{Vout (max)} - \text{Vout (min)}}{\text{R}_{\text{shunt}} \times (I_{\text{max}} - I_{\text{min}})} = \frac{3.2 \text{ V} - 100 \text{ mV}}{100 \text{ mΩ}} \times (1 \text{ A} - (-1 \text{ A})) = 15.5 \text{ V} / \text{V}
\]  

(7)

10 Power Supply Recommendations

The LPV821 is specified for operation from 1.7 V to 3.6 (±0.85 V to ±1.8 V); many specifications apply from –40°C to 125°C. The Typical Characteristics presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 4 V can permanently damage the device (see the Absolute Maximum Ratings).

TI recommends placing 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the Layout section.

11 Layout

11.1 Layout Guidelines

11.1.1 General Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The LPV821 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

11.2 Layout Example

Figure 26. SOT-23 Layout Example
12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

*TINA-TI SPICE-Based Analog Simulation Program

*DIP Adapter Evaluation Module

*TI Universal Operational Amplifier Evaluation Module

*TI FilterPro Filter Design Software

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
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</tr>
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(1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.
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