1 Features
- Inverts or Doubles Input Supply Voltage
- Narrow SO-8 Package
- 6.5-Ω Typical Output Resistance
- 88% Typical Conversion Efficiency at 100 mA
- Selectable Oscillator Frequency: 10 kHz/80 kHz

2 Applications
- Laptop Computers
- Cellular Phones
- Medical Instruments
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

3 Description
The MAX660 CMOS charge-pump voltage converter is a versatile unregulated switched-capacitor inverter or doubler. Operating from a wide 1.5-V to 5.5-V supply voltage, the MAX660 uses two low-cost capacitors to provide 100 mA of output current without the cost, size and EMI related to inductor-based converters. With an operating current of only 120 µA and operating efficiency greater than 90% at most loads, the MAX660 provides ideal performance for battery-powered systems. MAX660 devices can be operated directly in parallel to lower output impedance, thus providing more current at a given voltage.

The FC (frequency control) pin selects between a nominal 10-kHz or 80-kHz oscillator frequency. The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the MAX660 with an external clock up to 150 kHz. Through these methods, output ripple frequency and harmonics may be controlled.

Additionally, the MAX660 may be configured to divide a positive input voltage precisely in half. In this mode, input voltages as high as 11 V may be used.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX660</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2016) to Revision B Page

• Changed Figure 5 caption from “Efficiency vs Oscillator Frequency” to “Efficiency vs Load Current” ................. 7

Changes from Original (SNOS405) to Revision A Page

• Added additional info to DescriptionDevice Information and Pin Configuration and Functions sections, ESD Ratings
  and Thermal Information tables, Feature Description, Device Functional Modes, Application and Implementation,
  Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and
  Orderable Information sections ........................................... 1
• Deleted obsolete device number information from Device Comparison table ............................................. 3
• Deleted lead temperature spec from Abs Max as it is in POA ................................................................. 5
• Added additional thermal values; changed RθJA from “170°C/W” to “114.4°C/W” ........................................ 5
• Changed “PL” to “PM” and “PF” to PJ” - manufacturers changed their part number prefix ............................ 14
• Changed “Sprague” to “Vishay Sprague” per website ................................................................. 14
5 Device Comparison Tables

<table>
<thead>
<tr>
<th></th>
<th>LM2664</th>
<th>LM2665</th>
<th>MAX660</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>SOT-23 (6)</td>
<td>SOT-23 (6)</td>
<td>SOIC</td>
</tr>
<tr>
<td>Supply current (typical) (mA)</td>
<td>0.22</td>
<td>0.22</td>
<td>0.12 at 10 kHz, 1 at 80 kHz</td>
</tr>
<tr>
<td>Output (typical) (Ω)</td>
<td>12</td>
<td>12</td>
<td>6.5</td>
</tr>
<tr>
<td>Oscillator (kHz)</td>
<td>80</td>
<td>80</td>
<td>10, 80</td>
</tr>
<tr>
<td>Input (V)</td>
<td>1.8 to 5.5</td>
<td>1.8 to 5.5</td>
<td>1.8 to 5.5</td>
</tr>
<tr>
<td>Output mode(s)</td>
<td>Invert</td>
<td>Double</td>
<td>Invert, Double</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>MAX660</th>
<th>LM2662</th>
<th>LM2663</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>SOIC, VSSOP (8)</td>
<td>SOIC (8)</td>
<td>SOIC (8)</td>
</tr>
<tr>
<td>Supply current (typical) (mA)</td>
<td>0.12 at 10 kHz, 1 at 80 kHz</td>
<td>0.3 at 10 kHz, 1.3 at 70 kHz</td>
<td>1.3</td>
</tr>
<tr>
<td>Output (typical) (Ω)</td>
<td>6.5</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>Oscillator (kHz)</td>
<td>10, 80</td>
<td>10, 70</td>
<td>70</td>
</tr>
<tr>
<td>Input (V)</td>
<td>1.8 to 5.5</td>
<td>1.8 to 5.5</td>
<td>1.8 to 5.5</td>
</tr>
<tr>
<td>Output mode(s)</td>
<td>Invert, Double</td>
<td>Invert, Double</td>
<td>Invert, Double</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td>VOLTAGE INVERTER</td>
</tr>
<tr>
<td>CAP+</td>
<td>2</td>
<td>Power</td>
</tr>
<tr>
<td>CAP–</td>
<td>4</td>
<td>Power</td>
</tr>
<tr>
<td>FC</td>
<td>1</td>
<td>Input</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>Ground</td>
</tr>
<tr>
<td>LV</td>
<td>6</td>
<td>Input</td>
</tr>
<tr>
<td>OSC</td>
<td>7</td>
<td>Input</td>
</tr>
<tr>
<td>OUT</td>
<td>5</td>
<td>Power</td>
</tr>
<tr>
<td>V+</td>
<td>8</td>
<td>Power</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ to GND, or GND to OUT</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>(OUT – 0.3 V)</td>
<td>(V+ – 6 V)</td>
<td>mAh</td>
</tr>
<tr>
<td>(V+ 0.3 V)</td>
<td>(V+ – 6 V)</td>
<td>mAh</td>
</tr>
<tr>
<td>Operating junction temperature</td>
<td>–40</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, Tstg</td>
<td>–65</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(3) OUT may be shorted to GND for one second without damage. However, shorting OUT to V+ may damage the device and must be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V+, or device may be damaged.

(4) The maximum allowable power dissipation is calculated by using $P_{D\text{MAX}} = (T_{J\text{MAX}} - T_A) / R_{\theta JA}$, where $T_{J\text{MAX}}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $R_{\theta JA}$ is the junction-to-ambient thermal resistance of the specified package.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ (supply voltage)</td>
<td>3.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Inverter, LV = open</td>
<td>1.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Inverter, LV = GND</td>
<td>2.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Doubler, LV = out</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>MAX660</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction-to-ambient thermal resistance</td>
<td>114.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-case (top) thermal resistance</td>
<td>61.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board thermal resistance</td>
<td>55.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-top characterization parameter</td>
<td>9.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board characterization parameter</td>
<td>54.9</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
7.5 Electrical Characteristics

Unless otherwise specified: Limits apply for $T_J = 25^\circ C$, $V_+ = 5 \, V$, $FC = open$, $C1 = C2 = 150 \, \mu F$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_+$,(2)</td>
<td>$R_L = 1 , k\Omega$</td>
<td>3.5</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Inverter LV = open(3), $T_J = –40^\circ C$ to $85^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Inverter, LV = GND, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>1.5</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Doubler, LV = OUT, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>2.5</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>No load, $LV = open$</td>
<td>0.12</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$FC = open$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$FC = open$, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>0.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$FC = V_+$</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$FC = V_+$, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_L$</td>
<td>$T_A \leq 85^\circ C$, $OUT \leq –4 , V$</td>
<td>100</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$T_A &gt; 85^\circ C$, $OUT \leq –3.8 , V$</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{OUT}$</td>
<td>$I_L = 100 , mA$</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>$T_A \leq 85^\circ C$</td>
<td>6.5</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A &gt; 85^\circ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_J = –40^\circ C$ to $85^\circ C$</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A &gt; 85^\circ C$, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{OSC}$</td>
<td>$OSC = open$</td>
<td></td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>$FC = open$</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$FC = open$, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$FC = V_+$</td>
<td>80</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$FC = V_+$, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OSC}$</td>
<td>$FC = open$</td>
<td>±2</td>
<td></td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td>$FC = V_+$</td>
<td>±16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{EFF}$</td>
<td>$R_L (1 , k\Omega)$ between $V_+$ and $OUT$</td>
<td>98%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_L (1 , k\Omega)$ between $V_+$ and $OUT$, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>96%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_L (500 , \Omega)$ between GND and $OUT$</td>
<td>96%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_L (500 , \Omega)$ between GND and $OUT$, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>92%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_L = 100 , mA$ to GND</td>
<td>88%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DEFF}$</td>
<td>No load</td>
<td>99.96%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>No load, $T_J = –40^\circ C$ to $85^\circ C$</td>
<td>99%</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) In the test circuit, capacitors C1 and C2 are 0.2-Ω maximum ESR capacitors. Capacitors with higher ESR increase output resistance, reduce output voltage, and efficiency.

(2) Specified output resistance includes internal switch resistance and capacitor ESR.

(3) The minimum limit for this parameter is different from the limit of 3 V for the industry-standard 660 product. For inverter operation with supply voltage below 3.5 V, connect the LV pin to GND.
7.6 Typical Characteristics
Circuit of Voltage Inverter and Positive Voltage Doubler.

Figure 1. Supply Current vs Supply Voltage

Figure 2. Supply Current vs Oscillator Frequency

Figure 3. Output Source Resistance vs Supply Voltage

Figure 4. Output Source Resistance vs Temperature

Figure 5. Efficiency vs Load Current

Figure 6. Output Voltage Drop vs Load Current
Typical Characteristics (continued)

Circuit of Voltage Inverter and Positive Voltage Doubler.

Figure 7. Efficiency vs Oscillator Frequency

Figure 8. Output Voltage vs Oscillator Frequency

Figure 9. Oscillator Frequency Supply Voltage

Figure 10. Oscillator Frequency vs Supply Voltage

Figure 11. Oscillator Frequency vs Temperature

Figure 12. Oscillator Frequency vs Temperature
8 Parameter Measurement Information

8.1 MAX660 Test Circuit

![Diagram of MAX660 Test Circuit]

*C1 and C2 are 150 μF OS-CON Capacitors

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9 Detailed Description

9.1 Overview

The MAX660 contains four large CMOS switches which are switched in a sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 13 shows the voltage conversion scheme. When S1 and S3 are closed, C1 charges to the supply voltage V+. During this time interval switches S2 and S4 are open. In the second time interval, S1 and S3 are open and S2 and S4 are closed, C1 is charging C2. After a number of cycles, the voltage across C2 is pumped to V+. Because the anode of C2 is connected to ground, the output at the cathode of C2 equals \(-(V+)\) assuming no load on C2, no loss in the switches, and no ESR in the capacitors. In reality, the charge transfer efficiency depends on the switching frequency, the on-resistance of the switches, and the ESR of the capacitors.

Figure 13. Voltage Inverting Principle

9.2 Functional Block Diagram
9.3 Feature Description

The internal oscillator frequency can be selected using the frequency control (FC) pin. When FC is open, the oscillator frequency is 10 kHz; when FC is connected to V+, the frequency increases to 80 kHz. A higher oscillator frequency allows use of smaller capacitors for equivalent output resistance and ripple, but increases the typical supply current from 0.12 mA to 1 mA. The oscillator frequency can be lowered by adding an external capacitor between OSC and GND. (See Typical Characteristics.) Also, in the inverter mode, an external clock that swings within 100 mV of V+ and GND can be used to drive OSC. Any CMOS logic gate is suitable for driving OSC. LV must be grounded when driving OSC. The maximum external clock frequency is limited to 150 kHz.

The switching frequency of the converter (also called the charge-pump frequency) is half of the oscillator frequency.

NOTE

OSC cannot be driven by an external clock in the voltage-doubling mode.

<table>
<thead>
<tr>
<th>FC</th>
<th>OSC</th>
<th>OSCILLATOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open</td>
<td>Open</td>
<td>10 kHz</td>
</tr>
<tr>
<td>V+</td>
<td>Open</td>
<td>80 kHz</td>
</tr>
<tr>
<td>Open or V+</td>
<td>External capacitor</td>
<td>See Typical Characteristics</td>
</tr>
<tr>
<td>N/A</td>
<td>External clock (inverter mode only)</td>
<td>External clock frequency</td>
</tr>
</tbody>
</table>

9.4 Device Functional Modes

When V+ is applied to the MAX660, the device becomes enabled and operates in whichever configuration the device is placed (inverter, doubler, etc.).
10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The MAX660 CMOS charge-pump voltage converter is a versatile, unregulated switched-capacitor inverter or doubler. Operating from a wide 1.5-V to 5.5-V supply voltage, the MAX660 uses two low-cost capacitors to provide 100 mA of output current without the cost, size, and EMI related to inductor-based converters. With an operating current of only 120 µA and operating efficiency greater than 90% at most loads, the MAX660 provides ideal performance for battery-powered systems. MAX660 devices can be operated directly in parallel to lower output impedance, thus providing more current at a given voltage.

10.2 Typical Applications

10.2.1 Voltage Inverter

10.2.1.1 Design Requirements

For typical switched capacitor applications, use the parameters in Table 2:

Table 2. Design Parameters

<table>
<thead>
<tr>
<th>DESIGN PARAMETER</th>
<th>EXAMPLE VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>5.5 V (maximum)</td>
</tr>
<tr>
<td>Negative output voltage</td>
<td>−1.5 V to −5.5 V</td>
</tr>
<tr>
<td>Output current</td>
<td>100 mA</td>
</tr>
</tbody>
</table>

10.2.1.2 Detailed Design Procedure

The main application of MAX660 is to generate a negative supply voltage. The voltage inverter circuit uses only two external capacitors as shown in the Figure 14. The range of the input supply voltage is 1.5 V to 5.5 V. For a supply voltage less than 3.5 V, the LV pin must be connected to ground to bypass the internal regulator circuitry. This gives the best performance in low-voltage applications. If the supply voltage is greater than 3.5 V, LV may be connected to ground or left open. The choice of leaving LV open simplifies the direct substitution of the MAX660 for the LMC7660 switched capacitor voltage converter.

The output characteristics of this circuit can be approximated by an ideal voltage source in series with a resistor. The voltage source equals −(V+). The output resistance $R_{out}$ is a function of the ON resistance of the internal MOS switches, the oscillator frequency, and the capacitance and ESR of $C_1$ and $C_2$. A good approximation is:
\[ R_{\text{out}} = 2R_{\text{SW}} + \frac{2}{f_{\text{osc}} \times C_1} + 4 \text{ESR}_{C_1} + \text{ESR}_{C_2} \]

where

- \( R_{\text{SW}} \) is the sum of the ON resistance of the internal MOS switches shown in Figure 13.

High-value, low-ESR capacitors reduce the output resistance. Instead of increasing the capacitance, the oscillator frequency can be increased to reduce the \( \frac{2}{f_{\text{osc}} \times C_1} \) term. Once this term is trivial compared with \( R_{\text{SW}} \) and ESRs, further increase to oscillator frequency and capacitance become ineffective. The peak-to-peak output voltage ripple is determined by the oscillator frequency, and the capacitance and ESR of the output capacitor \( C_2 \):

\[ V_{\text{ripple}} = \frac{1}{f_{\text{osc}} \times C_2} + 2 \times I_{L} \times \text{ESR}_{C_2} \]

Again, using a low-ESR capacitor results in lower ripple.

### 10.2.1.2.1 Capacitor Selection

The output resistance and ripple voltage are dependent on the capacitance and ESR values of the external capacitors. The output voltage drop is the load current times the output resistance, and the power efficiency is shown in Equation 3:

\[ \eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{I_{Q(V+)}^2 R_L}{I_{Q(V+)}^2 R_L + I_{Q(V+)}^2 R_{\text{OUT}} + I_{Q(V+)} \times I_{L}} \]

where

- \( I_{Q(V+)} \) is the quiescent power loss of the device
- \( I_{Q(V+)}^2 R_{\text{OUT}} \) is the conversion loss associated with the switch on-resistance, the two external capacitors and their ESRs

Because the switching current charging and discharging \( C_1 \) is approximately twice that of the output current, the effect of the ESR of the pumping capacitor \( C_1 \) is multiplied by four in the output resistance. The output capacitor \( C_2 \) is charging and discharging at a current approximately equal to the output current; therefore, its ESR only counts once in the output resistance. However, the ESR of \( C_2 \) directly affects the output voltage ripple. Therefore, TI recommends low-ESR capacitors (Table 3) for both capacitors to maximize efficiency, reduce the output voltage drop and voltage ripple. For convenience, \( C_1 \) and \( C_2 \) are usually chosen to be the same. The output resistance varies with the oscillator frequency and the capacitors. In Figure 15, the output resistance vs oscillator frequency curves are drawn for three different tantalum capacitors. At very low frequency range, capacitance plays the most important role in determining the output resistance. Once the frequency is increased to some point (such as 20 kHz for the 150-μF capacitors), the output resistance is dominated by the ON resistance of the internal switches and the ESRs of the external capacitors. A low-value, smaller size capacitor usually has a higher ESR compared with a larger size capacitor of the same type. For lower ESR, use ceramic capacitors.

![Figure 15. Output Source Resistance vs Oscillator Frequency](image)
Table 3. Low-ESR Capacitor Manufacturers

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>CAPACITOR TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nichicon Corp.</td>
<td>PM, PJ series, through-hole aluminum electrolytic</td>
</tr>
<tr>
<td>AVX Corp.</td>
<td>TPS series, surface-mount tantalum</td>
</tr>
<tr>
<td>Vishay Sprague</td>
<td>593D, 594D, 595D series, surface-mount tantalum</td>
</tr>
<tr>
<td>Sanyo</td>
<td>OS-CON series, through-hole aluminum electrolytic</td>
</tr>
</tbody>
</table>

10.2.1.2.2 Paralleling Devices

Any number of MAX660 devices can be paralleled to reduce the output resistance. Each device must have its own pumping capacitor $C_1$, while only one output capacitor $C_{OUT}$ is required as shown in Figure 16. The composite output resistance is:

$$R_{OUT} = \frac{R_{OUT}}{\text{Number of Devices}}$$

(4)

![Figure 16. Lowering Output Resistance by Paralleling Devices](image)

10.2.1.2.3 Cascading Devices

Cascading the MAX660s is an easy way to produce a greater negative voltage (as shown in Figure 17). If $n$ is the integer representing the number of devices cascaded, the unloaded output voltage $V_{out}$ is $(-nV_{in})$. The effective output resistance is equal to the weighted sum of each individual device:

$$R_{out} = nR_{out_1} + \frac{n}{2}R_{out_2} + \cdots + R_{out_n}$$

(5)

A three-stage cascade circuit shown in Figure 18 generates $-3V_{in}$ from $V_{in}$.

Cascading is also possible when devices are operating in doubling mode. In Figure 19, two devices are cascaded to generate $3V_{IN}$.

An example of using the circuit in Figure 18 or Figure 19 is generating $+15V$ or $-15V$ from a $+5V$ input.

**NOTE**

The number of $n$ is practically limited because the increasing of $n$ significantly reduces the efficiency and increases the output resistance and output voltage ripple.
Figure 17. Increasing Output Voltage by Cascading Devices

Figure 18. Generating $-3V_{IN}$ From $+V_{IN}$

Figure 19. Generating $+3V_{IN}$ From $+V_{IN}$
10.2.1.2.4 Regulating Output Voltage

Output of the MAX660 can be regulated by use of a low-dropout regulator (such as LP2951). The whole converter is depicted in Figure 20. This converter can give a regulated output from $-1.5 \text{ V}$ to $-5.5 \text{ V}$ by choosing the proper resistor ratio:

$$V_{\text{out}} = V_{\text{ref}} \left( 1 + \frac{R_1}{R_2} \right)$$

(6)

The error flag on pin 5 of the LP2951 goes low when the regulated output at pin 4 drops by about 5%. The LP2951 can be shut down by taking pin 3 high.

Figure 20. Combining MAX660 With LP2951 to Make a Negative Regulator

As shown in Figure 21 by operating MAX660 in voltage doubling mode and adding a linear regulator (such as LP2981) at the output, the user can get +5-V output from an input as low as +3 V.

Figure 21. Generating +5 V From +3-V Input Voltage
10.2.1.3  Application Curves

Figure 22. Efficiency vs Load Current

Figure 23. Efficiency vs Oscillator Frequency

10.2.2  Positive Voltage Doubler

10.2.2.1  Design Requirements

The MAX660 can operate as a positive voltage doubler (as shown in the Figure 24). The doubling function is achieved by reversing some of the connections to the device. The input voltage is applied to the GND pin with an allowable voltage from 2.5 V to 5.5 V. The V+ pin is used as the output. The LV pin and OUT pin must be connected to ground. The OSC pin cannot be driven by an external clock in this operation mode. The unloaded output voltage is twice of the input voltage and is not reduced by the forward drop of the diode (D1).

10.2.2.2  Detailed Design Procedure

The Schottky diode D1 is only needed for start-up. The internal oscillator circuit uses the V+ pin and the LV pin (connected to ground in the voltage doubler circuit) as its power rails. Voltage across V+ and LV must be larger than 1.5 V to ensure the operation of the oscillator. During start-up, D1 is used to charge up the voltage at V+ pin to start the oscillator; also, it protects the device from turning on its own parasitic diode and potentially latching up. Therefore, the Schottky diode D1 must have enough current carrying capability to charge the output capacitor at start-up, as well as a low forward voltage to prevent the internal parasitic diode from turning on. A Schottky diode like 1N5817 can be used for most applications. If the input voltage ramp is less than 10V/ms, a smaller Schottky diode like MBR0520LT1 can be used to reduce the circuit size.
10.3 Split V+ in Half

Another interesting application shown in Figure 25 is to use the MAX660 as a precision voltage divider. Because the off-voltage across each switch equals VIN/2, the input voltage can be raised to 11 V.

![Diagram of V+ in Half](image)

**Figure 25. Splitting VIN in Half**

11 Power Supply Recommendations

The MAX660 is designed to operate from as an inverter over an input voltage supply range between 1.5 V and 5.5 V when the LV pin is grounded. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the MAX660 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.
12 Layout

12.1 Layout Guidelines

The high switching frequency and large switching currents of the MAX660 make the choice of layout important. The following steps should be used as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range:

- Place $C_{IN}$ on the top layer (same layer as the MAX60) and as close as possible to the device. Connecting the input capacitor through short, wide traces to both the $V+$ and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the $V+$ line.

- Place $C_{OUT}$ on the top layer (same layer as the MAX660) and as close as possible to the OUT and GND pin. The returns for both $C_{IN}$ and $C_{OUT}$ must come together at one point, as close as possible to the GND pin. Connecting $C_{OUT}$ through short, wide traces reduce the series inductance on the OUT and GND pins that can corrupt the $V_{OUT}$ and GND lines and cause excessive noise in the device and surrounding circuitry.

- Place $C_1$ on the top layer (same layer as the MAX660) and as close as possible to the device. Connect the flying capacitor through short, wide traces to both the CAP+ and CAP– pins.

12.2 Layout Example

![MAX660 Layout Example Diagram](image-url)
13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer
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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary
**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX660M</td>
<td>NRND</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td></td>
<td>MAX 660M</td>
<td></td>
</tr>
<tr>
<td>MAX660M/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>95</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>MAX 660M</td>
<td>Samples</td>
</tr>
<tr>
<td>MAX660MX/NOPB</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>MAX 660M</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W   (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX660MX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.5</td>
<td>5.4</td>
<td>2.0</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

---

* Dimensions are nominal.

**Legend:**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**Reel Dimensions**

**Tape Dimensions**

**Quadrant Assignments for Pin 1 Orientation in Tape**
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX660MX/NOPB</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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