36-V, SINGLE-SUPPLY, LOW-POWER OPERATIONAL AMPLIFIER

Check for Samples: OPA170-EP

FEATURES
- Supply Range: +2.7V to +36V, ±1.35V to ±18V
- Low Noise: 19nV/√Hz
- RFI Filtered Inputs
- Input Range Includes the Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- Gain Bandwidth: 1.2MHz
- Low Quiescent Current: 110µA per Amplifier
- High Common-Mode Rejection: 120dB
- Low Bias Current: 15pA (max)
  - microPackage:
    - Single in 5-Pin SOT553

DESCRIPTION
The OPA170 is a 36-V, single-supply, low-noise operational amplifier that features a micro package with the ability to operate on supplies ranging from +2.7V (±1.35V) to +36V (±18V). It offers good offset, drift, and bandwidth with low quiescent current.

Unlike most op amps, which are specified at only one supply voltage, the OPA170 is specified from +2.7V to +36V. Input signals beyond the supply rails do not cause phase reversal. The OPA170 is stable with capacitive loads up to 300pF. The input can operate 100mV below the negative rail and within 2V of the positive rail for normal operation. Note that these devices can operate with full rail-to-rail input 100mV beyond the positive rail, but with reduced performance within 2V of the positive rail.

The OPA170 is available in the SOT553-5 package and is specified from –40°C to +150°C.

APPLICATIONS
- Tracking Amplifier in Power Modules
- Merchant Power Supplies
- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS
- Controlled Baseline
- One Assembly or Test Site
- One Fabrication Site
- Available in Extended (–40°C to 150°C) Temperature Range (1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

(1) Additional temperature ranges available - contact factory

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION(1)

<table>
<thead>
<tr>
<th>$T_A$</th>
<th>PACKAGE</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
<th>VID NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>–40°C to 150°C</td>
<td>SOT553-5 - DRL</td>
<td>OPA170ASDRLTEP</td>
<td>SHN</td>
<td>V62/12627-01XE</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

### PIN CONFIGURATIONS

![PIN CONFIGURATIONS](image)

### ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>±20, +40 (single supply) V</td>
</tr>
<tr>
<td>Voltage</td>
<td>(V–) – 0.5 to (V+) + 0.5 V</td>
</tr>
<tr>
<td>Current</td>
<td>±10 mA</td>
</tr>
<tr>
<td>Output short circuit(2)</td>
<td>Continuous</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>–40 to +150 °C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>–65 to +150 °C</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>+150 °C</td>
</tr>
<tr>
<td>ESD ratings</td>
<td>Human body model (HBM) 4 kV, Charged device model (CDM) 750 V</td>
</tr>
</tbody>
</table>

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Short-circuit to ground, one amplifier per package.

### THERMAL INFORMATION

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA170 DRL (SOT553)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\theta_{JA}$</td>
<td>Junction-to-ambient thermal resistance</td>
<td>226.8 °C/W</td>
</tr>
<tr>
<td>$\theta_{JC(top)}$</td>
<td>Junction-to-case(top) thermal resistance</td>
<td>80.3 °C/W</td>
</tr>
<tr>
<td>$\theta_{JB}$</td>
<td>Junction-to-board thermal resistance</td>
<td>42.9 °C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>Junction-to-top characterization parameter</td>
<td>3.2</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>Junction-to-board characterization parameter</td>
<td>42.5</td>
</tr>
<tr>
<td>$\theta_{JC(bottom)}$</td>
<td>Junction-to-case(bottom) thermal resistance</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
**ELECTRICAL CHARACTERISTICS**

**Boldface limits apply over the specified temperature range, \( T_A = -40^\circ \text{C} \) to +150\(^\circ \text{C}.**

At \( T_A = +25^\circ \text{C}, V_{CM} = V_{OUT} = V_S/2, \) and \( R_L = 10k\Omega \) connected to \( V_S/2, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OFFSET VOLTAGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input offset voltage ( V_{OS} )</td>
<td></td>
<td>0.25</td>
<td>±1.8</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Over temperature ( T_A = -40^\circ \text{C} ) to +150(^\circ \text{C}.)</td>
<td></td>
<td>±2.5</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Drift ( \frac{dV_{OS}}{dT} )</td>
<td></td>
<td>±0.3</td>
<td></td>
<td>( \mu \text{V/}^\circ \text{C} )</td>
<td></td>
</tr>
<tr>
<td>vs power supply ( \text{PSRR} ) ( V_S = +4\text{V} ) to +36\text{V}</td>
<td></td>
<td>1</td>
<td>±5</td>
<td>( \mu \text{V/V} )</td>
<td></td>
</tr>
<tr>
<td>Channel separation, dc</td>
<td></td>
<td>5</td>
<td></td>
<td>( \mu \text{V/V} )</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT BIAS CURRENT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input bias current ( I_B )</td>
<td></td>
<td>±8</td>
<td>±15</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Over temperature ( T_A = -40^\circ \text{C} ) to +150(^\circ \text{C}.)</td>
<td></td>
<td>±8</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Input offset current ( I_{OS} )</td>
<td></td>
<td>±4</td>
<td>±15</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Over temperature ( T_A = -40^\circ \text{C} ) to +150(^\circ \text{C}.)</td>
<td></td>
<td>±8</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td><strong>NOISE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input voltage noise</td>
<td>( f = 0.1\text{Hz} ) to 10\text{Hz}</td>
<td>2</td>
<td></td>
<td>( \mu \text{V}_{\text{PP}} )</td>
<td></td>
</tr>
<tr>
<td>Input voltage noise density ( e_{n} )</td>
<td>( f = 100\text{Hz} )</td>
<td>22</td>
<td></td>
<td>nV/\sqrt{\text{Hz}}</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( f = 1\text{kHz} )</td>
<td>19</td>
<td></td>
<td>nV/\sqrt{\text{Hz}}</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT VOLTAGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-mode voltage range(1) ( (V_{–}) - 0.1\text{V} ) to ( (V_{+}) - 2\text{V} )</td>
<td>( V_S = \pm 2\text{V}, (V_{–}) = 0.1\text{V} &lt; V_{CM} &lt; (V_{+}) - 2\text{V} )</td>
<td>87</td>
<td>104</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Common-mode rejection ratio ( \text{CMRR} )</td>
<td>( V_S = \pm 18\text{V}, (V_{–}) - 0.1\text{V} &lt; V_{CM} &lt; (V_{+}) - 2\text{V} )</td>
<td>100</td>
<td>120</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT IMPEDANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential ( \text{DIFF} )</td>
<td></td>
<td>100</td>
<td>3</td>
<td>M( \Omega )</td>
<td></td>
</tr>
<tr>
<td>Common-mode ( \text{CM} )</td>
<td></td>
<td>6</td>
<td>3</td>
<td>10^{12} ( \Omega )</td>
<td></td>
</tr>
<tr>
<td><strong>OPEN-LOOP GAIN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open-loop voltage gain ( A_{OL} )</td>
<td>( V_S = +4\text{V} ) to +36\text{V}</td>
<td>107</td>
<td>130</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( (V_{–}) + 0.35\text{V} &lt; V_{O} &lt; (V_{+}) - 0.35\text{V} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FREQUENCY RESPONSE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain bandwidth product ( \text{GBP} )</td>
<td></td>
<td>1.2</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Slew rate ( \text{SR} )</td>
<td>( G = +1 )</td>
<td>0.4</td>
<td></td>
<td>V/\mu s</td>
<td></td>
</tr>
<tr>
<td>Settling time ( t_s ) ( \text{To 0.1%}, V_S = \pm 18\text{V}, G = +1, 10\text{V step} )</td>
<td>( G = +1, \text{To 0.01% (12 bit)}, V_S = \pm 18\text{V}, G = +1, 10\text{V step} )</td>
<td>20</td>
<td></td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
<tr>
<td>Overload recovery time ( t_{ov} )</td>
<td>( V_O \times \text{Gain} &gt; V_S )</td>
<td>28</td>
<td></td>
<td>( \mu \text{s} )</td>
<td></td>
</tr>
<tr>
<td>Total harmonic distortion + noise ( \text{THD+N} ) ( G = +1, \text{To 1kHz}, V_O = 3V_{\text{RMS}} )</td>
<td>( G = +1, V_O = 1V_{\text{RMS}} )</td>
<td>0.0002</td>
<td></td>
<td>%</td>
<td></td>
</tr>
</tbody>
</table>

(1) The input range can be extended beyond \( (V_{+}) - 2\text{V} \) up to \( V_{+} \). See the Typical Characteristics and Application Information sections for additional information.
ELECTRICAL CHARACTERISTICS (continued)

**Boldface** limits apply over the specified temperature range, $T_A = -40^\circ C$ to $+150^\circ C$.

At $T_A = +25^\circ C$, $V_{CM} = V_{OUT} = V_S/2$, and $R_L = 10\, k\Omega$ connected to $V_S/2$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage output swing from rail</td>
<td>$V_O$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive rail</td>
<td>$I_L = 0mA, V_S = +4V$ to $+36V$</td>
<td>10</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_L$ sourcing $1mA, V_S = +4V$ to $+36V$</td>
<td>130</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Negative rail</td>
<td>$I_L = 0mA, V_S = +4V$ to $+36V$</td>
<td>8</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_L$ sinking $1mA, V_S = +4V$ to $+36V$</td>
<td>72</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over temperature</td>
<td>$V_S = 5V, R_L = 10k\Omega$</td>
<td>$(V-) + 0.03$</td>
<td>V</td>
<td>$(V+) - 0.05$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_L = 10k\Omega, A_{OL} \geq 107dB$</td>
<td>$(V-) + 0.35$</td>
<td>V</td>
<td>$(V+) - 0.35$</td>
<td></td>
</tr>
<tr>
<td>Short-circuit current</td>
<td>$I_{SC}$</td>
<td>+17/-20</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitive load drive</td>
<td>$C_{LOAD}$</td>
<td>See Typical Characteristics</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open-loop output resistance</td>
<td>$R_O$</td>
<td>$f = 1MHz, I_O = 0A$</td>
<td>900</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Power supply</td>
<td>Specified voltage range</td>
<td>$V_S$</td>
<td>+2.7</td>
<td>+36</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Quiescent current per amplifier</td>
<td>$I_O$</td>
<td>$I_O = 0A$</td>
<td>110</td>
<td>145</td>
</tr>
<tr>
<td></td>
<td>Over temperature</td>
<td>$I_O = 0A$</td>
<td></td>
<td>160</td>
<td>μA</td>
</tr>
<tr>
<td>Temperature</td>
<td>Specified range</td>
<td></td>
<td>$-40$</td>
<td>+125</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Operating range</td>
<td></td>
<td>$-40$</td>
<td>+150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) See datasheet for absolute maximum and minimum recommended operating conditions.
(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
(3) Enhanced plastic product disclaimer applies.

Figure 1. OPA170-EP Operating Life Derating Chart
TYPICAL CHARACTERISTICS

$V_S = \pm 18V, V_{CM} = V_S/2, R_{LOAD} = 10k\Omega$ connected to $V_S/2$, and $C_L = 100pF$, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

Distribution Taken From 400 Amplifiers

OFFSET VOLTAGE DRIFT DISTRIBUTION

Distribution Taken From 104 Amplifiers

OFFSET VOLTAGE vs TEMPERATURE

5 Typical Units Shown
$V_S = \pm 18V$

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

5 Typical Units Shown
$V_{CM} = -18.1V$

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE (Upper Stage)

5 Typical Units Shown
$V_{CM} = +18.1V$

OFFSET VOLTAGE vs POWER SUPPLY

$V_{SUPPLY} = \pm 1.35V$ to $\pm 18V$

5 Typical Units Shown
TYPICAL CHARACTERISTICS (continued)

$V_S = \pm 18V$, $V_{CM} = V_S/2$, $R_{LOAD} = 10k\Omega$ connected to $V_S/2$, and $C_L = 100pF$, unless otherwise noted.

**Figure 8.**

**Figure 9.**

**Figure 10.**

**Figure 11.**

**Figure 12.**

**Figure 13.**
TYPICAL CHARACTERISTICS (continued)

\[ V_S = \pm 18V, \ V_{CM} = V_S/2, \ R_{LOAD} = 10k\Omega \ \text{connected to} \ V_S/2, \ \text{and} \ C_L = 100pF, \ \text{unless otherwise noted.} \]

**Figure 14.** 0.1Hz TO 10Hz NOISE

**Figure 15.** INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

**Figure 16.** THD+N RATIO vs FREQUENCY

**Figure 17.** THD+N vs OUTPUT AMPLITUDE

**Figure 18.**QUIESCENT CURRENT vs TEMPERATURE

**Figure 19.** QUIESCENT CURRENT vs SUPPLY VOLTAGE
V_S = ±18V, V_{CM} = V_S/2, R_{LOAD} = 10kΩ connected to V_S/2, and C_L = 100pF, unless otherwise noted.

**OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

![Graph showing open-loop gain and phase vs frequency.]

**CLOSED-LOOP GAIN vs FREQUENCY**

![Graph showing closed-loop gain vs frequency.]

**OPEN-LOOP GAIN vs TEMPERATURE**

![Graph showing open-loop gain vs temperature.]

**OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY**

![Graph showing open-loop output impedance vs frequency.]

**SMALL-SIGNAL OVERSHEEPT vs CAPACITIVE LOAD**

![Graph showing small-signal overshoot vs capacitive load.]

**TYPICAL CHARACTERISTICS (continued)**

![Graph showing typical characteristics.](http://www.ti.com)
TYPICAL CHARACTERISTICS (continued)

\[ V_S = \pm 18V, \ V_{CM} = V_S/2, \ R_{LOAD} = 10k\Omega \text{ connected to } V_S/2, \text{ and } C_L = 100pF, \text{ unless otherwise noted.} \]

**NO PHASE REVERSAL**

![Diagram](image1)

**POSITIVE OVERLOAD RECOVERY**

![Diagram](image2)

**NEGATIVE OVERLOAD RECOVERY**

![Diagram](image3)

**SMALL-SIGNAL STEP RESPONSE**

![Diagram](image4)

**LARGE-SIGNAL STEP RESPONSE**

![Diagram](image5)
TYPICAL CHARACTERISTICS (continued)

\[ V_S = \pm 18\text{V}, \ V_{CM} = V_S/2, \ R_{LOAD} = 10\text{k}\Omega \text{ connected to } V_S/2, \text{ and } C_L = 100\text{pF}, \text{ unless otherwise noted.} \]

![LARGE-SIGNAL STEP RESPONSE](image1)

![LARGE-SIGNAL SETTLING TIME](image2)

![MAXIMUM OUTPUT VOLTAGE vs FREQUENCY](image3)

![EMIRR IN+ vs FREQUENCY](image4)

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**Figure 32.**

**Figure 33.**

**Figure 34.**

**Figure 35.**

**Figure 36.**

**Figure 37.**

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Product Folder Links: **OPA170-EP**
APPLICATION INFORMATION

The OPA170 operational amplifier provides high overall performance. This device is ideal for many general-purpose applications. The excellent offset drift of only 2µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1µF capacitors are adequate.

OPERATING CHARACTERISTICS

The OPA170 is specified for operation from 2.7V to 36V (±1.35V to ±18V). Many of the specifications apply from −40°C to +150°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

GENERAL LAYOUT GUIDELINES

For best operational performance of the device, good printed circuit board (PCB) layout practices are recommended. Low-loss, 0.1µF bypass capacitors should be connected between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable to single-supply applications.

COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA170 extends 100mV below the negative rail and within 2V of the positive rail for normal operation. This device can operate with full rail-to-rail input 100mV beyond the positive rail, but with reduced performance within 2V of the positive rail. The typical performance in this range is summarized in Table 1.

PHASE-REVERSAL PROTECTION

The OPA170 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA170 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 38.

Table 1. Typical Performance Range

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Common-Mode Voltage</td>
<td>(V+) − 2</td>
<td>(V+) + 0.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Offset voltage</td>
<td>7</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>vs Temperature</td>
<td>12</td>
<td></td>
<td>μV/°C</td>
<td></td>
</tr>
<tr>
<td>Common-mode rejection</td>
<td>65</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Open-loop gain</td>
<td>60</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain-bandwidth product</td>
<td>0.3</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Slew rate</td>
<td>0.3</td>
<td></td>
<td>V/µs</td>
<td></td>
</tr>
</tbody>
</table>
CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPA170 have been optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, $R_{OUT}$ equal to 50Ω) in series with the output. Figure 39 and Figure 40 illustrate graphs of small-signal overshoot versus capacitive load for several values of $R_{OUT}$. Also, refer to Applications Bulletin AB-028, Feedback Plots Define Op Amp AC Performance (literature number SBOA015, available for download from the TI website), for details of analysis techniques and application circuits.

![Figure 39. Small-Signal Overshoot versus Capacitive Load (100mV Output Step, $G = +1$)](image)

![Figure 40. Small-Signal Overshoot versus Capacitive Load (100mV Output Step, $G = -1$)](image)

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA as stated in the Absolute Maximum Ratings. Figure 41 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

![Figure 41. Input Current Protection](image)

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.
If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation. However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.
# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA170ASDRLTEP</td>
<td>ACTIVE</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>5</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 150</td>
<td>DAQ</td>
<td>Samples</td>
</tr>
<tr>
<td>V62/12627-01XE</td>
<td>ACTIVE</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>5</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 150</td>
<td>DAQ</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

** OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp. -** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish -** Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA170-EP:

- Catalog: OPA170
- Automotive: OPA170-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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</thead>
<tbody>
<tr>
<td>OPA170ASDRLTEP</td>
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<td>DRL</td>
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<td>180.0</td>
<td>8.4</td>
<td>1.98</td>
<td>1.78</td>
<td>0.69</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
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</tbody>
</table>

*All dimensions are nominal.*

---

**TAPE DIMENSIONS**

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Sprocket Holes
- User Direction of Feed
- Pocket Quadrants

---

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## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA170ASDRLTEP</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>5</td>
<td>250</td>
<td>202.0</td>
<td>201.0</td>
<td>28.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.
Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 per end or side.
D. JEDEC package registration is pending.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0.127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
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