**OPA2182 36-V, 5-MHz, Low-Noise, Zero-Drift, MUX-Friendly, Precision Op Amp**

### 1 Features
- **Ultra-high precision:**
  - Zero-drift: 0.005 µV/°C
  - Ultra-low offset voltage: 3.5 µV (maximum)
- **Excellent dc precision:**
  - CMRR: 168 dB
  - Open-loop gain: 170 dB
- **Low noise:**
  - $e_n$ at 1 kHz: 5.7 nV/√Hz
  - 0.1-Hz to 10-Hz noise: 0.12 µV
- **Excellent dynamic performance:**
  - Gain bandwidth: 5 MHz
  - Slew rate: 10 V/µs
  - Fast settling: 10-V step, 0.01% in 1.7 µs
- **Robust design:**
  - MUX-friendly inputs
  - RFI/EMI filtered inputs
- **Wide supply:** ±2.25 V to ±18 V, 4.5 V to 36 V
- **Quiescent current:** 0.85 mA
- **Rail-to-rail output**
- **Input includes negative rail**

### 2 Applications
- Battery test
- DC power supply, ac source, electronic load
- Data acquisition (DAQ)
- Semiconductor test
- Weigh scale
- Analog input module
- Flow transmitter

### 3 Description
The OPA2182 high-precision operational amplifier is an ultra-low noise, fast-settling, zero-drift device that provides rail-to-rail output operation and features a unique MUX-friendly architecture and controlled startup system. These features and excellent ac performance, combined with only 0.45 µV of offset voltage and 0.005 µV/°C of drift over temperature, makes the OPA2182 a great choice for precision instrumentation, signal measurement, and active filtering applications.

The MUX-friendly input architecture prevents inrush current when applying large input differential voltages that improves settling performance in multichannel systems. Moreover, the controlled startup system rejects any inrush current upon ramping up the supply rails, all while providing robust ESD protection during shipment, handling, and assembly.

The device is specified from –40°C to +125°C.

### Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2182</td>
<td>SOIC (8)</td>
<td>4.90 mm x 3.90 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the package option addendum at the end of the data sheet.

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for pre-production products; subject to change without notice.
Table of Contents

1 Features ............................................................ 1
2 Applications ..................................................... 1
3 Description ....................................................... 1
4 Revision History ................................................ 2
5 Device Comparison Table .................................... 3
6 Pin Configuration and Functions .......................... 3
7 Specifications .................................................... 4
  7.1 Absolute Maximum Ratings .............................. 4
  7.2 ESD Ratings .................................................. 4
  7.3 Recommended Operating Conditions............... 4
  7.4 Thermal Information: OPA2182 ....................... 4
  7.5 Electrical Characteristics ............................... 5
  7.6 Typical Characteristics .................................. 7
8 Detailed Description ........................................... 9
  8.1 Overview .................................................... 9
  8.2 Functional Block Diagram ............................ 9
  8.3 Feature Description .................................... 9
4 Revision History .................................................... 10
9 Application and Implementation ........................ 11
  9.1 Application Information ................................ 11
  9.2 Typical Applications .................................... 11
10 Power Supply Recommendations ....................... 14
11 Layout ............................................................. 14
  11.1 Layout Guidelines ....................................... 14
  11.2 Layout Example .......................................... 15
12 Device and Documentation Support .................... 16
  12.1 Device Support .......................................... 16
  12.2 Documentation Support ............................... 16
  12.3 Receiving Notification of Documentation Updates 17
  12.4 Support Resources ..................................... 17
  12.5 Trademarks ............................................... 17
  12.6 Electrostatic Discharge Caution .................... 17
  12.7 Glossary .................................................. 17
13 Mechanical, Packaging, and Orderable Information 17

4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>December 2019</td>
<td>*</td>
<td>Initial release.</td>
</tr>
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</table>
5 Device Comparison Table

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>FEATURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2189</td>
<td>0.4-µV offset, 0.005-µV/°C drift, 5.2-nV/√Hz, Rail-to-Rail Output, 36-V, Zero-Drift, MUX-Friendly CMOS</td>
</tr>
<tr>
<td>OPA2188</td>
<td>6-µV offset, 0.03-µV/°C drift, 8.8-nV/√Hz, Rail-to-Rail Output, 36-V, Zero-Drift, MUX-Friendly CMOS</td>
</tr>
<tr>
<td>OPA2187</td>
<td>1-µV offset, 0.001-µV/°C drift, 100-µA quiescent current, Rail-to-Rail Output, 36-V, Zero-Drift CMOS</td>
</tr>
<tr>
<td>OPA2388</td>
<td>0.25-µV offset, 0.005-µV/°C drift, 7-nV/√Hz, 10-MHz, True Rail-to-Rail Input/Output, 5.5-V, Zero-Drift, Zero-Crossover CMOS</td>
</tr>
<tr>
<td>OPA2180</td>
<td>120-µV, 10-MHz, 5.1-nV/√Hz, 36-V JFET Input Industrial Op Amp</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td></td>
</tr>
<tr>
<td>–IN A</td>
<td>2</td>
<td>Inverting input channel A</td>
</tr>
<tr>
<td>+IN A</td>
<td>3</td>
<td>Noninverting input channel A</td>
</tr>
<tr>
<td>–IN B</td>
<td>6</td>
<td>Inverting input channel B</td>
</tr>
<tr>
<td>+IN B</td>
<td>5</td>
<td>Noninverting input channel B</td>
</tr>
<tr>
<td>OUT A</td>
<td>1</td>
<td>Output channel A</td>
</tr>
<tr>
<td>OUT B</td>
<td>7</td>
<td>Output channel B</td>
</tr>
<tr>
<td>V–</td>
<td>4</td>
<td>Negative supply</td>
</tr>
<tr>
<td>V+</td>
<td>8</td>
<td>Positive supply</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_S) Supply voltage</td>
<td>Single-supply, (V_S = (V+))</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Dual-supply, (V_S = (V+) - (V-))</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>(+\text{IN}, -\text{IN}) Voltage</td>
<td>Common-mode</td>
<td>((V+) - 0.5)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Differential</td>
<td>((V+) - (V-) + 0.2)</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>\pm 10</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Output short circuit(^{(2)})</td>
<td>Continuous</td>
<td>Continuous</td>
<td></td>
</tr>
<tr>
<td>(T_A) Operating temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>(T_J) Junction temperature</td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(T_{stg}) Storage temperature</td>
<td>-65</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>\pm 4000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>\pm 1000</td>
<td>V</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_S) Supply voltage</td>
<td>Single-supply, (V_S = (V+))</td>
<td>4.5</td>
<td>36</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Dual-supply, (V_S = (V+) - (V-))</td>
<td>\pm 2.25</td>
<td>\pm 18</td>
<td></td>
</tr>
<tr>
<td>(T_A) Operating temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

7.4 Thermal Information: OPA2182

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>OPA2182</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JUA}) Junction-to-ambient thermal resistance</td>
<td>115.7 (^{°})C/W</td>
</tr>
<tr>
<td>(R_{JUC(top)}) Junction-to-case (top) thermal resistance</td>
<td>51.1 (^{°})C/W</td>
</tr>
<tr>
<td>(R_{JUB}) Junction-to-board thermal resistance</td>
<td>60.8 (^{°})C/W</td>
</tr>
<tr>
<td>(\Psi_{JT}) Junction-to-top characterization parameter</td>
<td>9.8 (^{°})C/W</td>
</tr>
<tr>
<td>(\Psi_{JB}) Junction-to-board characterization parameter</td>
<td>59.7 (^{°})C/W</td>
</tr>
<tr>
<td>(R_{JUC(bot)}) Junction-to-case (bottom) thermal resistance</td>
<td>N/A (^{°})C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.5 Electrical Characteristics

at $T_A = 25^\circ$C, $V_{CM} = V_{OUT} = V_S / 2$, and $R_{LOAD} = 10 \, k\Omega$ connected to $V_S / 2$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Input offset voltage</td>
<td>±0.45</td>
<td>±3.5</td>
<td>μV</td>
<td></td>
</tr>
<tr>
<td>$dV_{OS}/dT$</td>
<td>Input offset voltage drift</td>
<td>$T_A = 0^\circ$C to 85°C</td>
<td>±0.005</td>
<td>μV/°C</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power-supply rejection ratio</td>
<td>$T_A = -40^\circ$C to +125°C</td>
<td>±0.005</td>
<td>±0.05</td>
<td>μV/V</td>
</tr>
<tr>
<td>INPUT BIAS CURRENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input bias current</td>
<td>$Z_{IN} = 100 , k\Omega \parallel 500 , pF$</td>
<td>±50</td>
<td>±350</td>
<td>pA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input offset current</td>
<td>$Z_{IN} = 100 , k\Omega \parallel 500 , pF$</td>
<td>±140</td>
<td>±700</td>
<td>pA</td>
</tr>
<tr>
<td>NOISE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$E_n$</td>
<td>Input voltage noise</td>
<td>$f = 0.1$ Hz to 10 Hz</td>
<td>20</td>
<td>nV RMS</td>
<td></td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input voltage noise density</td>
<td>$f = 10$ Hz</td>
<td>0.12</td>
<td>μV pp</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT IMPEDANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Common-mode voltage range</td>
<td>(V–) – 0.1 V ≤ $V_{CM}$ ≤ (V+) – 2.5 V</td>
<td>(V–) + 0.3 V &lt; $V_O$ &lt; (V+) – 0.3 V, $R_{LOAD}$ = 10 kΩ</td>
<td>150</td>
<td>170</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>(V–) + 0.3 V &lt; $V_O$ &lt; (V+) – 0.3 V, $R_{LOAD}$ = 10 kΩ, $T_A = -40^\circ$C to +125°C</td>
<td>140</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT VOLTAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td>Common-mode voltage range</td>
<td>(V–) – 0.1 V ≤ $V_{CM}$ ≤ (V+) – 2.5 V</td>
<td>$V_S = \pm 2.25$ V</td>
<td>120</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT IMPEDANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$z_d$</td>
<td>Differential input impedance</td>
<td>0.1</td>
<td></td>
<td>5.5</td>
<td>ΩΩ</td>
</tr>
<tr>
<td>$z_c$</td>
<td>Common-mode input impedance</td>
<td>60</td>
<td></td>
<td>1.7</td>
<td>ΩΩ</td>
</tr>
<tr>
<td>OPEN-LOOP GAIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{OL}$</td>
<td>Open-loop voltage gain</td>
<td>$V_S = \pm 18$ V</td>
<td>(V–) + 0.6 V &lt; $V_O$ &lt; (V+) – 0.6 V, $R_{LOAD}$ = 2 kΩ, $T_A = -40^\circ$C to +125°C</td>
<td>150</td>
<td>170</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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### Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_{LOAD} = 10 \text{k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RESPONSE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>UGB</td>
<td>$A_V = 1$</td>
<td>3.6</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>GBW</td>
<td>$A_V = 1000$</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Gain = 1, 10-V step</td>
<td>10</td>
<td></td>
<td></td>
<td>V/μs</td>
</tr>
<tr>
<td>THD+N</td>
<td>Gain = 1, $f = 1$ kHz, $V_O = 3.5$ V$_{RMS}$</td>
<td>0.00005%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Crosstalk</td>
<td>OPA2182, at dc</td>
<td>150</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>OPA2182, $f = 10$ kHz</td>
<td>120</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_S$</td>
<td>To 0.1$%$</td>
<td>1.3</td>
<td></td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>To 0.01$%$</td>
<td>1.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{OVR}$</td>
<td>$V_{IN} \times \text{gain} = V_S$</td>
<td>320</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_O$</td>
<td>Voltage output swing from rail</td>
<td>Positive rail</td>
<td>No load</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Negative rail</td>
<td>No load</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$R_{LOAD} = 10$ $\text{k}\Omega$</td>
<td>20</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$R_{LOAD} = 2$ $\text{k}\Omega$</td>
<td>80</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, both rails, $R_{LOAD} = 10$ $\text{k}\Omega$</td>
<td>20</td>
<td>120</td>
<td></td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Short-circuit current</td>
<td>±65</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$C_{LOAD}$</td>
<td>Capacitive load drive</td>
<td>TBD</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$Z_O$</td>
<td>Open-loop output impedance</td>
<td>$f = 1$ MHz</td>
<td>320</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current per amplifier</td>
<td>$V_S = \pm 2.25$ V to $\pm 18$ V</td>
<td>$T_A = 25^\circ\text{C}$</td>
<td>0.85</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$</td>
<td>1.1</td>
<td></td>
</tr>
</tbody>
</table>
7.6 Typical Characteristics

at $T_A = 25^\circ C$, $V_S = \pm 18 \text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10 \text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100 \text{ pF}$ (unless otherwise noted).
Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = \pm 18 V$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10 \, k\Omega$ connected to $V_S / 2$, and $C_L = 100 \, pF$ (unless otherwise noted)

Figure 7. Voltage Noise Spectral Density

Figure 8. Output Impedance vs Frequency
8 Detailed Description

8.1 Overview

The OPA2182 operational amplifier combines precision offset and drift with excellent overall performance, making it a great choice for many precision applications. The precision offset drift of only 0.005 µV/°C provides stability over the entire temperature range. In addition, this device offers excellent linear performance with high CMRR, PSRR, and $A_{OL}$. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. See the Layout Guidelines section for details and a layout example.

The OPA2182 is a zero-drift, MUX-friendly, rail-to-rail output operational amplifier. The device operates from 4.5 V to 36 V, is unity-gain stable, and a great choice for a wide range of general-purpose and precision applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise, zero flicker noise, and outstanding distortion performance when operating below the chopper frequency.

8.2 Functional Block Diagram

The functional block diagram shows a representation of the proprietary OPA2182 architecture.
8.3 Feature Description

The OPA2182 operational amplifier has several integrated features that help maintain a high level of precision throughout all operating conditions. These features include phase-reversal protection, input bias current clock feedthrough and MUX-friendly inputs.

8.3.1 Phase-Reversal Protection

The OPA2182 has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA2182 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 9.

![Figure 9. No Phase Reversal](image)

8.3.2 Input Bias Current Clock Feedthrough

Zero-drift amplifiers such as the OPA2182 use switching on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying; however, the pulses may be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter such as an RC network.

8.3.3 MUX-Friendly Inputs

The OPA2182 features a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature antiparallel diodes that protect input transistors from large $V_{GS}$ voltages that may exceed the semiconductor process maximum and permanently damage the device. Large $V_{GS}$ voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator. For more information, see the MUX-Friendly Precision Operational Amplifiers tech note.

The OPA2182 solves these problems with a switched-input technique that prevents large input bias currents when large differential voltages are applied. This input architecture solves many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials. The OPA2182 offers outstanding settling performance because of these design innovations, along with built-in slew rate boost and wide bandwidth. The OPA2182 can also be used as a comparator. Differential and common-mode Absolute Maximum Ratings still apply relative to the power supplies.

8.4 Device Functional Modes

The OPA2182 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5 V ($\pm$2.25 V). The maximum power supply voltage for the OPA2182 is 36 V ($\pm$18 V).
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The OPA2182 operational amplifier combines precision offset and drift with excellent overall performance, making the series a great choice for many precision applications. The precision offset drift of only 0.005 µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and $A_{\text{OL}}$ dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

The following application examples highlight only a few of the circuits where the OPA2182 can be used.

9.2 Typical Applications

9.2.1 Strain Gauge Analog Linearization

9.2.1.1 Design Requirements
A strain gauge is used to measure an alteration due to external force through the use of electrical resistance in a Wheatstone-bridge configuration. The Wheatstone bridge is used to measure very low values of resistances down in the mΩ range, with precision. An excitation voltage is applied to the bridge, and the output voltage across the middle of the bridge is measured. The total change in output voltage is relatively small, typically in the mV range. Therefore, an op amp is used to amplify the signal. The OPA2182 is designed to construct high-precision amplification.

Use the following parameters for this design example:
• Use the op amp linear output operating range, which is usually specified under the AOL test conditions. The common-mode voltage is equal to the input signal.
• Use an op amp that does not add significant noise to the system or else the small output voltage from the Wheatstone bridge will be lost.
• The input signal must be gained; therefore, use an op amp with low input offset voltage ($V_{\text{OS}}$)
• The input signal must be gained; therefore, use an op amp with enough open-loop gain to provide the required amplification
9.2.1.2 Detailed Design Procedure

The bridge sensor signal flow model is shown in Figure 11.

\[ V_{\text{bridge}}(P, V_{\text{exc}}) = V_{\text{exc}} \times K_p(P) \]  

(1)

\( K_p \) is the sensitivity of the bridge sensor, and is usually specified in mV/V. \( P \) represents the pressure relative to the range of the sensor, normalized to a scale from 0 to 1. Solving this equation with the variables given in the signal flow model and solving for \( V_{\text{out}} \) results in Equation 2.

\[ V_{\text{out}}(P) = \frac{V_{\text{OS}} + V_{\text{ref}} \times G \times K_{\text{lin}} \times K_p(P)}{1 - G \times K_{\text{lin}} \times K_p(P)} \]

(2)

This equation has three variables, \( V_{\text{OS}}, G \) and \( K_{\text{lin}} \), that require three equations to solve. To solve these equations, values of \( K_p \) at no load, midscale and full load conditions are needed for the sensor. With these values, the system can be linearized.

With known values for \( K_p, K_{\text{lin}} \) can be calculated as shown in Equation 3.

\[ K_{\text{lin}} = \frac{4 \times B_v \times V_{\text{ref}}}{(V_{\text{out\_high}} - V_{\text{out\_low}}) - 2 \times B_v \times (V_{\text{out\_high}} + V_{\text{out\_low}})} \]

(3)

In this equation, \( B_v \) represents the bridge nonlinearity which can be calculated as shown in Equation 4.

\[ B_v = \frac{K_p(0.5) - K_p(0)}{2 \times K_p(1) - K_p(0)} \]

(4)

\( B_v \) can be solved based on the sensor specifications, and this can then be used to solve for \( K_{\text{lin}} \). Next the system gain can be calculated using Equation 5 and Equation 6.

\[ V_{\text{out\_high}} = \frac{V_{\text{OS}} + V_{\text{ref}} \times G \times K_p(1)}{1 - G \times K_{\text{lin}} \times K_p(1)} \]

(5)

\[ V_{\text{out\_high}} = \frac{V_{\text{OS}} + V_{\text{ref}} \times G \times K_p(0)}{1 - G \times K_{\text{lin}} \times K_p(0)} \]

(6)
Typical Applications (continued)

Solving for \( V_{OS} \) in both equations and combining results in Equation 7.

\[
V_{\text{out\_high}}(1 - G \times K_{\text{lin}} \times K_P(1)) - V_{\text{ref}} \times G \times K_P(1) = V_{\text{out\_low}}(1 - G \times K_{\text{lin}} \times K_P(0)) - V_{\text{ref}} \times G \times K_P(0)
\]  
(7)

Solving for \( G \) gives Equation 8.

\[
G = \frac{V_{\text{out\_high}} - V_{\text{out\_low}}}{K_P(1) \times (K_{\text{lin}} \times V_{\text{out\_high}} + V_{\text{ref}}) - K_P(0) \times (K_{\text{lin}} \times V_{\text{out\_low}} + V_{\text{ref}})}
\]  
(8)

With both \( K_{\text{lin}} \) and \( G \) now calculated, \( V_{OS} \) can be solved as shown in Equation 9.

\[
V_{OS} = V_{\text{out\_low}}(1 - G \times K_{\text{lin}} \times K_P(0)) - V_{\text{ref}} \times G \times K_P(0)
\]  
(9)

For a sensor with a \( K_P \) of 0.0003 mV/V at no load, 0.0017 mV/V mid-scale and 0.00289 mV/V, the corresponding nonlinearity is approximately 4%. Solving for \( K_{\text{lin}} \), \( G \) and \( V_{OS} \) will give the values shown in Table 1.

<table>
<thead>
<tr>
<th>( K_{\text{lin}} )</th>
<th>0.173913</th>
</tr>
</thead>
<tbody>
<tr>
<td>( G )</td>
<td>323.8178</td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>-0.48573</td>
</tr>
</tbody>
</table>

### 9.2.1.3 Application Curves

Using the same \( K_P \) values used above, the bridge's nonlinearity is simulated as 4% peak, the output is a linear 0 to 5V out and the corrected system nonlinearity is approximately ±0.1%.
10 Power Supply Recommendations

The OPA2182 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. The Typical Characteristics presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION
Supply voltages larger than 40 V can permanently damage the device (see the Absolute Maximum Ratings).

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the Layout section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see The PCB is a component of op amp design.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As illustrated in Figure 15, keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

For the lowest offset voltage, avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors.

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.
11.2 Layout Example

Figure 15. Operational Amplifier Board Layout for Difference Amplifier Configuration
12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA-TI™ provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI™ offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI™ software be installed. Download the free TINA-TI™ software from the TINA-TI™ folder.

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12.1.1.2 TI Precision Designs

TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

• Texas Instruments, Zero-drift Amplifiers: Features and Benefits
• Texas Instruments, The PCB is a component of op amp design
• Texas Instruments, Operational amplifier gain stability, Part 3: AC gain-error analysis
• Texas Instruments, Operational amplifier gain stability, Part 2: DC gain-error analysis
• Texas Instruments, Using infinite-gain, MFB filter topology in fully differential active filters
• Texas Instruments, Op Amp Performance Analysis
• Texas Instruments, Single-Supply Operation of Operational Amplifiers
• Texas Instruments, Tuning in Amplifiers
• Texas Instruments, Shelf-Life Evaluation of Lead-Free Component Finishes
• Texas Instruments, Feedback Plots Define Op Amp AC Performance
• Texas Instruments, EMI Rejection Ratio of Operational Amplifiers
• Texas Instruments, Analog Linearization of Resistance Temperature Detectors
• Texas Instruments, TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter
12.3 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources
TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (3)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<td>D</td>
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<td>75</td>
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<td>POPA2182ID</td>
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<td>Call TI</td>
<td>Call TI</td>
<td>-40 to 125</td>
<td></td>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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