HIGH PRECISION, LOW NOISE OPERATIONAL AMPLIFIER

Check for Samples: OPA2227-EP

FEATURES
- Low Noise: 3 nV/√Hz
- Wide Bandwidth: 8 MHz, 2.3 V/μs
- Settling Time: 5 μs
- High CMRR: 138 dB (Typical)
- High Open-Loop Gain: 160 dB (Typical)
- Low Input Bias Current: 10 nA Maximum at 25°C
- Low Offset Voltage: 100 μV Maximum at 25°C
- Wide Supply Range: ±2.5 V to ±18 V

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS
- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military (–55°C to 125°C) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

APPLICATIONS
- Data Acquisition
- Telecom Equipment
- Geophysical Analysis
- Vibration Analysis
- Spectral Analysis
- Professional Audio Equipment
- Active Filters
- Power Supply Control

DESCRIPTION
The OPA2227 operational amplifier combines low noise and wide bandwidth with high precision to make it the ideal choice for applications requiring both ac and precision dc performance.

The OPA2227 is unity-gain stable and features high slew rate (2.3 V/μs) and wide bandwidth (8 MHz).

The OPA2227 operational amplifier is ideal for professional audio equipment. In addition, low quiescent current and low cost make them ideal for portable applications requiring high precision.

The OPA2227 operational amplifier is a pin-for-pin replacement for the industry standard OP-27 with substantial improvements across the board. The dual and quad versions are available for space savings and perchannel cost reduction.

The OPA2227 is available in an SOIC-8 package. Operation is specified from –55°C to 125°C.

(1) Additional temperature ranges available - contact factory
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE</th>
<th>TOP-SIDE MARKING</th>
<th>ORDERABLE PART NUMBER</th>
<th>VID NUMBER</th>
<th>TRANSPORT MEDIA</th>
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</thead>
<tbody>
<tr>
<td>-55°C to 125°C</td>
<td>SOIC-8 – D</td>
<td>2227EP</td>
<td>OPA2227MDREP</td>
<td>V62/12610-01XE</td>
<td>Tape and Reel, large</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>OPA2227MDEP</td>
<td>V62/12610-01XE-T</td>
<td>Tube</td>
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</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
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</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>±18</td>
<td>V</td>
</tr>
</tbody>
</table>
| Signal input terminals
  Voltage              | (V–) – 0.7 to (V+) + 0.7 | V |
| Current              | 20 mA |      |
| Output short-circuit (to ground)(2) | Continuous | |
| Operating temperature| -55 to 125 | °C |
| Storage temperature  | -65 to 150 | °C |
| Junction temperature | 150 | °C |
| Lead temperature (soldering, 10 s) | 300 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) One channel per package.

THERMAL INFORMATION

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA2227</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{JA} ) Junction-to-ambient thermal resistance(2)</td>
<td>91.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>( \theta_{JCtop} ) Junction-to-case (top) thermal resistance(3)</td>
<td>39.9</td>
<td></td>
</tr>
<tr>
<td>( \theta_{JB} ) Junction-to-board thermal resistance(4)</td>
<td>40.6</td>
<td></td>
</tr>
<tr>
<td>( \psi_{JT} ) Junction-to-top characterization parameter(5)</td>
<td>3.9</td>
<td></td>
</tr>
<tr>
<td>( \psi_{JB} ) Junction-to-board characterization parameter(6)</td>
<td>39.6</td>
<td></td>
</tr>
<tr>
<td>( \theta_{JCbot} ) Junction-to-case (bottom) thermal resistance(7)</td>
<td>N/A</td>
<td></td>
</tr>
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</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, \( \psi_{JT} \), estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining \( \theta_{JA} \) using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, \( \psi_{JB} \), estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining \( \theta_{JA} \) using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
# ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ$C, $V_S = \pm 5$ V to $\pm 15$ V, $R_L = 10$ kΩ (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td>Input offset voltage ($V_{OS}$) vs Temperature, $T_A = -55^\circ$C to 125°C</td>
<td>±5</td>
<td>±100</td>
<td>µV</td>
<td></td>
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<tr>
<td></td>
<td>vs Temperature ($dV_{OS}/dT$), $T_A = -55^\circ$C to 125°C</td>
<td>±10</td>
<td>±250</td>
<td>µV</td>
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<tr>
<td></td>
<td>vs Power supply (PSRR) $T_A = -55^\circ$C to 125°C</td>
<td>$V_S = \pm 2.5$ V to $\pm 18$ V</td>
<td>±0.5</td>
<td>±2.1</td>
<td>µV/V</td>
</tr>
<tr>
<td></td>
<td>vs Time Channel separation (dual)</td>
<td>dc</td>
<td>0.2</td>
<td>µV/mo</td>
<td></td>
</tr>
</tbody>
</table>

| INPUT BIAS CURRENT | Input bias current ($I_{Ib}$) $T_A = -55^\circ$C to 125°C | ±2.5 | ±10 | nA |
| | Input offset current ($I_{OS}$) $T_A = -55^\circ$C to 125°C | See Typical Characteristics |

| NOISE | Input voltage noise, $f = 0.1$ Hz to 10 Hz | 90 | nVP-p |
| | Input voltage noise density ($e_{in}$) $f = 10$ Hz | 15 | nVrms |
| | $f = 100$ Hz | 3.5 | nV/√Hz |
| | $f = 1$ kHz | 3 | nV/√Hz |
| | Current noise density ($i_{in}$), $f = 1$ kHz | 0.4 | pA/√Hz |

| INPUT VOLTAGE RANGE | Common-mode voltage range ($V_{CM}$) $T_A = -55^\circ$C to 125°C | ($V_-$) + 2 | ($V_+$) - 2 | V |
| | Common-mode rejection (CMRR) $T_A = -55^\circ$C to 125°C | $V_{CM} = (V_-) + 2$ V to $(V_+) - 2$ V | 120 | 138 | dB |
| | | $T_A = -55^\circ$C to 125°C | 108 | 138 | dB |

| INPUT IMPEDANCE | Differential Open-loop voltage gain ($A_{OL}$) | $10^7$ || 12 | Ω || pF |
| | Common-mode | $V_{CM} = (V_-) + 2$ V to $(V_+) - 2$ V | $10^9$ || 3 | Ω || pF |

| OPEN-LOOP GAIN | Open-loop voltage gain ($A_{OCL}$) $T_A = -55^\circ$C to 125°C | $V_O = (V_-) + 2$ V to $(V_+) - 2$ V, $R_L = 10$ kΩ | 132 | 160 | dB |
| | | $T_A = -55^\circ$C to 125°C | $V_O = (V_-) + 3.5$ V to $(V_+) - 3.5$ V, $R_L = 600$ Ω | 132 | 160 | dB |
| | | $T_A = -55^\circ$C to 125°C | $T_A = -55^\circ$C to 125°C | 112 | 160 | dB |

| FREQUENCY RESPONSE | Gain bandwidth product (GBW) | 8 | MHz |
| | Slew rate (SR) | 2.3 | V/µs |
| | Settling time: 0.1% | G = 1, 10-V Step, $C_L = 100$ pF | 5 | µs |
| | | 0.01% | G = 1, 10-V Step, $C_L = 100$ pF | 5.6 | µs |
| | Overload recovery time | $V_{IN} \times G = V_S$ | 1.3 | µs |
| | Total harmonic distortion + noise (THD+N) $f = 1$ kHz, $G = 1$, $V_O = 3.5$ Vrms | 0.00005 | % |

| OUTPUT | Voltage output $T_A = -55^\circ$C to 125°C | $R_L = 10$ kΩ | ($V_-$) + 2 | ($V_+$) - 2 | V |
| | $T_A = -55^\circ$C to 125°C | $R_L = 600$ Ω | ($V_-$) + 3.5 | ($V_+$) - 3.5 | V |
| | Short-circuit current ($I_{SC}$) | See Typical Characteristics |
| | Capacitive load drive ($C_{LOAD}$) | $I_{SC}$ | 45 | mA |

| POWER SUPPLY | Specified voltage range ($V_S$) | ±5 | ±15 | V |
| | Operating voltage range | ±2.5 | ±18 | V |
| | Quiescent current (per amplifier) ($I_Q$) | $I_Q = 0$ A | ±3.7 | ±3.95 |
ELECTRICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ C$, $V_S = \pm 5\, \text{V}$ to $\pm 15\, \text{V}$, $R_L = 10\, \text{k\Omega}$ (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>MIN</th>
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<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_A = -55^\circ C$ to $125^\circ C$</td>
<td>$I_O = 0, \text{A}$</td>
<td></td>
<td></td>
<td>$\pm 4.30$</td>
<td>mA</td>
</tr>
</tbody>
</table>

| TEMPERATURE RANGE | | | | |
| Specified temperature range | | $-55$ | $125$ | °C |
| Operating temperature range | | $-55$ | $125$ | °C |
| Storage temperature range | | $-65$ | $150$ | °C |

A. See datasheet for absolute maximum and minimum recommended operating conditions.
B. Silicon operating life design goal is 10 years at $105^\circ C$ junction temperature (does not include package interconnect life).

Figure 1. OPA2227-EP Wirebond Life Derating Chart
TYPICAL CHARACTERISTICS

At $T_A = 25^\circ C$, $R_L = 10 \, k\Omega$, $V_S = \pm 15 \, V$ (unless otherwise noted).

OPA2227-EP
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Dual and quad devices. $G = 1$, all channels.
Quad measured Channel A to D, or B to C; other combinations yield similar or improved rejection.
TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ C$, $R_L = 10 \, k\Omega$, $V_S = \pm 15 \, V$ (unless otherwise noted).

VOLTAGE NOISE DISTRIBUTION (10Hz)

WARM-UP OFFSET VOLTAGE DRIFT

A<sub>OL</sub>, CMRR, PSRR vs TEMPERATURE

INPUT BIAS CURRENT vs TEMPERATURE

INPUT OFFSET CURRENT vs TEMPERATURE

SHORT-CIRCUIT CURRENT vs TEMPERATURE
TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ C$, $R_L = 10 \, k\Omega$, $V_S = \pm 15 \, V$ (unless otherwise noted).

**QUIESCENT CURRENT vs TEMPERATURE**

**QUIESCENT CURRENT vs SUPPLY VOLTAGE**

**SLEW RATE vs TEMPERATURE**

**CHANGE IN INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE**

**SETTLING TIME vs CLOSED-LOOP GAIN**

Curve shows normalized change in bias current with respect to $V_{CM} = 0 \, V$. Typical $I_B$ may range from $-2 \, nA$ to $+2 \, nA$ at $V_S = \pm 10 \, V$.

$V_S = \pm 15 \, V$, 10V Step  
$C_L = 1500pF$  
$R_L = 2k\Omega$

$V_S = \pm 15V$, $10V$ Step  
$C_L = 1500pF$  
$R_L = 2k\Omega$

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Product Folder Links: OPA2227-EP
TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ C$, $R_L = 10 \, k\Omega$, $V_S = \pm 15 \, V$ (unless otherwise noted).

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT**

![Graph showing output voltage swing vs output current for different gains and temperatures.]

**MAXIMUM OUTPUT VOLTAGE vs FREQUENCY**

![Graph showing maximum output voltage vs frequency for different supply voltages.]

**SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE**

![Graph showing small-signal overshoot vs load capacitance for different gains.]

**SMALL-SIGNAL STEP RESPONSE**

- $G = +1$, $C_L = 1000\, \mu F$
- $G = +1$, $C_L = 5\, \mu F$

**LARGE-SIGNAL STEP RESPONSE**

- $G = -1$, $C_L = 1500\, \mu F$

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Product Folder Links: OPA2227-EP
APPLICATION INFORMATION

Basic Connection

The OPA2227 is a precision operational amplifier with very low noise. It is unity-gain stable with a slew rate of 2.3 V/μs and 8-MHz bandwidth. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

Offset Voltage and Drift

The OPA2227 has very low offset voltage and drift. To achieve highest dc precision, circuit layout and mechanical conditions should be optimized. Connections of dissimilar metals can generate thermal potentials at the op amp inputs which can degrade the offset voltage and drift. These thermocouple effects can exceed the inherent drift of the amplifier and ultimately degrade its performance. The thermal potentials can be made to cancel by assuring that they are equal at both input terminals. In addition:
- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as those created by cooling fans.

Operating Voltage

OPA2227 operational amplifier operates from ±2.5-V to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the OPA2227 is specified for real-world applications; a single set of specifications applies over the ±5-V to ±15-V supply range. Specifications are assured for applications between ±5-V and ±15-V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPA2227 can operate with as little as 5 V between the supplies and with up to 36 V between the supplies. For example, the positive supply could be set to 25 V with the negative supply at –5 V or vice-versa. In addition, key parameters are assured over the specified temperature range, –55°C to 125°C. Parameters which vary significantly with operating voltage or temperature are shown in the Typical Performance Curves.

Offset Voltage Adjustment

The OPA2227 is laser-trimmed for very low offset and drift so most applications will not require external adjustment.

Input Protection

Back-to-back diodes (see Figure 2) are used for input protection on the OPA2227. Exceeding the turn-on threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes due to the amplifier’s finite slew rate. Without external current-limiting resistors, the input devices can be destroyed. Sources of high input current can cause subtle damage to the amplifier. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may shift.

![Figure 2. Pulsed Operation](image)

When using the OPA2227 as a unity-gain buffer (follower), the input current should be limited to 20 mA. This can be accomplished by inserting a feedback resistor or a resistor in series with the source. Sufficient resistor size can be calculated:

\[ R_x = \frac{V_s}{20 \text{ mA}} \cdot R_{\text{SOURCE}} \]  

(1)
where \( R_X \) is either in series with the source or inserted in the feedback path. For example, for a 10-V pulse \((V_S = 10 \text{ V})\), total loop resistance must be 500 \( \Omega \). If the source impedance is large enough to sufficiently limit the current on its own, no additional resistors are needed. The size of any external resistors must be carefully chosen since they will increase noise. See the Noise Performance section of this data sheet for further information on noise calculation. Figure 2 shows an example implementing a current limiting feedback resistor.

**Input Bias Current Cancellation**

The input bias current of the OPA2227 is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between with input bias current and the cancellation current. The residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately equal. A resistor added to cancel the effect of the input bias current (as shown in Figure 3) may actually increase offset and noise and is therefore not recommended.

![Conventional Op Amp Configuration](image)

**Figure 3. Input Bias Current Cancellation**

**Noise Performance**

Figure 4 shows total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, therefore no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPA2227 has very low voltage noise, making it ideal for low source impedances (less than 20 k\( \Omega \)). A similar precision operational amplifier, the OPA277, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 k\( \Omega \) to 100 k\( \Omega \)). Above 100 k\( \Omega \), a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation is shown for the calculation of the total circuit noise. Note that \( e_n = \) voltage noise, \( i_n = \) current noise, \( R_S = \) source impedance, \( k = \) Boltzmann’s constant = 1.38 x 10\(^{-23}\) J/K and \( T \) is temperature in K. For more details on calculating noise, see “Basic Noise Calculations.”

![Noise Performance of the OPA2227 in Unity-Gain Buffer Configuration](image)
Basic Noise Calculations

Design of low noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is shown plotted in Figure 4. Since the source impedance is usually fixed, select the operational amplifier and the feedback resistors to minimize their contribution to the total noise.

Figure 4 shows total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Consequently, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 5 shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.
Noise in Noninverting Gain Configuration

\[
E_o^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + \left(\frac{R_2}{R_1}\right)^2 e_3^2 + \left(\frac{R_2}{R_1}\right)^2 e_4^2
\]

Where \( e_5 = \sqrt{4kTR_5} \times \left(1 + \frac{R_2}{R_1}\right) \) = thermal noise of \( R_5 \)

\( e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right) \) = thermal noise of \( R_1 \)

\( e_2 = \sqrt{4kTR_2} \) = thermal noise of \( R_2 \)

Noise in Inverting Gain Configuration

\[
E_o^2 = \left(1 + \frac{R_2}{R_1 + R_5}\right)^2 e_n^2 + e_1^2 + e_2^2 + \left(\frac{R_2}{R_1 + R_5}\right)^2 e_3^2
\]

Where \( e_5 = \sqrt{4kTR_5} \times \left(\frac{R_2}{R_1 + R_5}\right) \) = thermal noise of \( R_5 \)

\( e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_5}\right) \) = thermal noise of \( R_1 \)

\( e_2 = \sqrt{4kTR_2} \) = thermal noise of \( R_2 \)

For op amps at 1kHz, \( e_n = 3nV/\sqrt{Hz} \) and \( i_n = 0.4pA/\sqrt{Hz} \).

Figure 5. Noise Calculation in Gain Configurations
Figure 6 shows the 0.1-Hz to 10-Hz bandpass filter used to test the noise of the OPA2227. The filter circuit was designed using Texas Instruments’ FilterPro software (available at www.ti.com). Figure 7 shows the configuration of the OPA2227 for noise testing.

Figure 6. 0.1-Hz to 10-Hz Bandpass Filter Used to Test Wideband Noise of the OPA2227

Figure 7. Noise Test Circuit
NOTE: Use metal film resistors and plastic film capacitor. Circuit must be well shielded to achieve low noise.

Responsivity $2.5 \times 10^8 \approx 4\text{ V/W}$

Output Noise $30\mu\text{Vrms}, 0.1\text{Hz to 10Hz}$

OPA2227

$100\Omega$ $100k\Omega$

$0.1\mu F$

Figure 8. Three-Pole, 20-kHz Low Pass, 0.5-dB Chebyshev Filter

Figure 9. Long-Wavelength Infrared Detector Amplifier
This application uses two op amps in parallel for higher output current drive.

Figure 10. Headphone Amplifier
Figure 11. Three-Band ActiveTone Control (Bass, Midrange and Treble)
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings (4)</th>
<th>Samples</th>
</tr>
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<tbody>
<tr>
<td>OPA2227MDREP</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-55 to 125</td>
<td>2227EP</td>
<td></td>
</tr>
<tr>
<td>V62/12610-01XE</td>
<td>ACTIVE</td>
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<td>2227EP</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF OPA2227-EP**:
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
# Tape and Reel Information

**Device**: OPA2227MDREP  
**Package Type**: SOIC  
**Drawing**: D  
**Pins**: 8  
**SPQ**: 2500  
**Reel Diameter (mm)**: 330.0  
**Reel Width W1 (mm)**: 12.4  
**A0 (mm)**: 6.4  
**B0 (mm)**: 5.2  
**K0 (mm)**: 2.1  
**P1 (mm)**: 8.0  
**W (mm)**: 12.0  
**Pin1 Quadrant**: Q1

### Reel Dimensions
- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

### Quadrant Assignments for Pin 1 Orientation in Tape

<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
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<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
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<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
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</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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