Low-Noise, High-Speed, 16-Bit Accurate, CMOS OPERATIONAL AMPLIFIER

FEATURES
- High Bandwidth: 150MHz
- 16-Bit Settling in 150ns
- Low Noise: 3nV/√Hz
- Low Distortion: 0.003%
- Low Power: 9.5mA (typ) on 5.5V
- Shutdown to 5µA
- Unity-Gain Stable
- Excellent Output Swing: (V+) - 100mV to (V-) + 100mV
- Single Supply: +2.7V to +5.5V
- Tiny Packages: MSOP and SOT23

APPLICATIONS
- 16-Bit ADC Input Drivers
- Low-Noise Preamplifiers
- IF/RF Amplifiers
- Active Filtering

DESCRIPTION
The OPA300 and OPA301 series high-speed, voltage-feedback, CMOS operational amplifiers are designed for 16-bit resolution systems. The OPA300/OPA301 series are unity-gain stable and feature excellent settling and harmonic distortion specifications. Low power applications benefit from low quiescent current. The OPA300 and OPA2300 feature a digital shutdown (Enable) function to provide additional power savings during idle periods. Optimized for single-supply operation, the OPA300/OPA301 series offer superior output swing and excellent common-mode range.

The OPA300 and OPA301 series op amps have 150MHz of unity-gain bandwidth, low 3nV/√Hz voltage noise, and 0.1% settling within 30ns. Single-supply operation from 2.7V (±1.35V) to 5.5V (±2.75V) and an available shutdown function that reduces supply current to 5µA are useful for portable low-power applications. The OPA300 and OPA301 are available in SO-8 and SOT-23 packages. The OPA2300 is available in MSOP-10, and the OPA2301 is available in SO-8 and MSOP-8. All versions are specified over the industrial temperature range of −40°C to +125°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.
PACKAGE/ORDERING INFORMATION(1)

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE-LEAD</th>
<th>PACKAGE DESIGNATOR</th>
<th>PACKAGE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA300</td>
<td>SO-8</td>
<td>D</td>
<td>300A</td>
</tr>
<tr>
<td>OPA300</td>
<td>SOT23-6</td>
<td>DBV</td>
<td>A52</td>
</tr>
<tr>
<td>OPA301</td>
<td>SO-8</td>
<td>D</td>
<td>301A</td>
</tr>
<tr>
<td>OPA301</td>
<td>SOT23-5</td>
<td>DBV</td>
<td>A52</td>
</tr>
<tr>
<td>OPA2300</td>
<td>MSOP−10</td>
<td>DGS</td>
<td>C01</td>
</tr>
<tr>
<td>OPA2301</td>
<td>SO−8</td>
<td>DBV</td>
<td>A52</td>
</tr>
<tr>
<td>OPA2301</td>
<td>MSOP−8</td>
<td>DGK</td>
<td>OAWM</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS over operating free-air temperature range unless otherwise noted(1)

- Power Supply V+ ........................................7V
- Signal Input Terminals(2), Voltage 0.5V to (V+) + 0.5V Current .....................................±10mA
- Open Short-Circuit Current(3) ..........................Continuous
- Operating Temperature Range ..........................−55°C to +125°C
- Storage Temperature Range .............................−60°C to +150°C
- Junction Temperature .....................................+150°C

ESD Ratings
- Human Body Model (HBM) .................................4kV
- Charged-Device Model (CDM) ............................500V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

(3) Short-circuit to ground; one amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS

Top View

NOTE: (1) Not connected. (2) SOT23-6 pin 1 oriented as shown with reference to package marking.
**ELECTRICAL CHARACTERISTICS: \( V_S = 2.7V \) to 5.5V**

**Boldface limits apply over the temperature range, \( T_A = -40^\circ C \) to +125\(^\circ C \).**

All specifications at \( T_A = +25^\circ C \), \( R_L = 2k\Omega \) connected to \( V_S/2 \), \( V_{OUT} = V_S/2 \), and \( V_{CM} = V_S/2 \), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td>( V_S = 5V )</td>
<td>1</td>
<td>5</td>
<td>7</td>
<td>mV</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>( V_S = 5V )</td>
<td>1</td>
<td>7</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>Over Temperature</td>
<td>2.5</td>
<td>( \mu V/\circ C )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drift</td>
<td>( V_S = 2.7V ) to 5.5V, ( V_{CM} &lt; (V+) –0.9V )</td>
<td>50</td>
<td>200</td>
<td>( \mu V/V )</td>
<td></td>
</tr>
<tr>
<td>vs. Power Supply</td>
<td>140</td>
<td>100</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel Separation, dc</td>
<td>( f = 5MHz )</td>
<td>( V_S/2 ), ( V_{OUT} = V_S/2 ), and ( V_{CM} = V_S/2 ), unless otherwise noted.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>( V_{CM} = (V−) –0.2V &lt; V_{CM} &lt; (V+) –0.9V )</td>
<td>66</td>
<td>80</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Voltage Range</td>
<td>( V_{CM} = (V+) –0.2V &lt; V_{CM} &lt; (V+) –0.9V )</td>
<td>66</td>
<td>80</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>( V_{CM} = (V+) –0.2V &lt; V_{CM} &lt; (V+) –0.9V )</td>
<td>66</td>
<td>80</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>INPUT BIAS CURRENT</td>
<td>( I_B )</td>
<td>±0.1</td>
<td>±5</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>( I_O )</td>
<td>±0.5</td>
<td>±5</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>INPUT IMPEDANCE</td>
<td>Differential</td>
<td>( 10^{13}</td>
<td></td>
<td>3 )</td>
<td>( \Omega</td>
</tr>
<tr>
<td>Common-Mode</td>
<td>( 10^{13}</td>
<td></td>
<td>6 )</td>
<td>( \Omega</td>
<td></td>
</tr>
<tr>
<td>NOISE</td>
<td>Input Voltage Noise, ( f = 0.1Hz ) to 1MHz</td>
<td>40</td>
<td>( \mu V_{pp} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Noise Density, ( f &gt; 1MHz )</td>
<td>3</td>
<td>( nV/\sqrt{Hz} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current Noise Density, ( f &lt; 1kHz )</td>
<td>1.5</td>
<td>( fA/\sqrt{Hz} )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Gain Error</td>
<td>( NTSC, R_L = 150\Omega )</td>
<td>0.01</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Phase Error</td>
<td>( NTSC, R_L = 150\Omega )</td>
<td>0.1</td>
<td>°</td>
<td></td>
<td></td>
</tr>
<tr>
<td>OPEN-LOOP GAIN</td>
<td>Over Temperature</td>
<td>( V_S = 5V, R_L = 2k\Omega, 0.1V &lt; V_O &lt; 4.9V )</td>
<td>95</td>
<td>106</td>
<td>dB</td>
</tr>
<tr>
<td>Open-Loop Voltage Gain</td>
<td>( V_S = 5V, R_L = 2k\Omega, 0.1V &lt; V_O &lt; 4.9V )</td>
<td>95</td>
<td>106</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Over Temperature</td>
<td>( V_S = 5V, R_L = 100\Omega, 0.5V &lt; V_O &lt; 4.5V )</td>
<td>90</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td>Voltage Output Swing from Rail</td>
<td>( R_L = 2k\Omega, A_{OL} &gt; 95dB )</td>
<td>75</td>
<td>100</td>
<td>mV</td>
</tr>
<tr>
<td>Short-Circuit Current</td>
<td>( R_L = 100\Omega, A_{OL} &gt; 95dB )</td>
<td>300</td>
<td>500</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( I_{SC} )</td>
<td>70</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open-Loop Output Impedance</td>
<td>( I_{O} = 0, f = 1MHz )</td>
<td>20</td>
<td>( \Omega )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitive Load Drive</td>
<td>See Typical Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FREQUENCY RESPONSE</td>
<td>Gain-Bandwidth Product</td>
<td>( GBW )</td>
<td>150</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>( SR )</td>
<td>80</td>
<td>( V_{bs} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling Time, 0.01%</td>
<td>( TS )</td>
<td>90</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overload Recovery Time</td>
<td>( T_O )</td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion + Noise</td>
<td>( THD+N )</td>
<td>( V_S = 5V, V_O = 3V_{pp}, G = +1, f = 1kHz )</td>
<td>0.003</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td>Specified Voltage Range</td>
<td>( V_S )</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td>( V_S )</td>
<td>2.7 to 5.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent Current (per amplifier)</td>
<td>( I_Q )</td>
<td>9.5</td>
<td>12</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Over Temperature</td>
<td>( I_Q )</td>
<td>13</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHUTDOWN</td>
<td>( I_{OFF} )</td>
<td>40</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{ON} )</td>
<td>5</td>
<td>( \mu s )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_T ) (shutdown)</td>
<td>( V_T = (V-) –0.2V )</td>
<td>( V_T = (V+) +0.2V )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{Q} ) (amplifier is active)</td>
<td>( V_{Q} = (V-) +2.5V )</td>
<td>( V_{Q} = (V+) +0.8V )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{QSD} ) (per amplifier)</td>
<td>3</td>
<td>10</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEMPERATURE RANGE</td>
<td>Specified Range</td>
<td>( -40^\circ C )( +125^\circ C )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Range</td>
<td>( -55^\circ C )( +125^\circ C )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Range</td>
<td>( -60^\circ C )( +150^\circ C )</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance</td>
<td>( \theta_{JA} )</td>
<td>( SO-8, MSOP-8, MSOP-10 )</td>
<td>150</td>
<td>( ^\circ C/W )</td>
<td></td>
</tr>
<tr>
<td>SOT23-5, SOT23-6</td>
<td>200</td>
<td>( ^\circ C/W )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
TYPICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ \text{C}$, $V_S = 5\text{V}$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.

**Noninverting Gain**

**Small-Signal Frequency Response**

- Frequency (Hz): 1M, 10M, 100M, 1G
- Normalized Gain (dB): $G = 2$, $G = 1$, $G = 5$, $G = 10$
- $V_O = 0.1V_{pp}$
- $R_F = 310\Omega$ for $G > 1$

**Large-Signal Step Response**

- Time (50ns/div)
- Output Voltage (500mV/div)

**Large-Signal Enable/Disable Response**

- Time (100ns/div)
- Enable Pin, Amplifier Output

**Inverting Gain**

**Small-Signal Frequency Response**

- Frequency (Hz): 1M, 10M, 100M, 1G
- Normalized Gain (dB): $G = -2$, $G = -1$, $G = -5$, $G = -10$
- $V_O = 0.1V_{pp}$
- $R_F = 310\Omega$ for $G > 1$

**0.1dB Gain Flatness for Various $R_F$**

- Frequency (MHz): 1, 10, 100
- Normalized Gain (dB): $R_F = 825\Omega$, $R_F = 450\Omega$, $R_F = 205\Omega$

**Small-Signal Step Response**

- Time (5ns/div)
- Output Voltage (10mV/div)
TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ$C, $V_S = 5V$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.

---

**HARMONIC DISTORTION vs OUTPUT VOLTAGE**

- $R_L = 200\Omega$
- $V_O = 2V_{pp}$
- $f = 1MHz$
- $R_F = 310\Omega$
- Gain = 2

---

**HARMONIC DISTORTION vs INVERTING GAIN**

- $V_O = 2V_{pp}$
- $R_L = 200\Omega$
- $f = 1MHz$
- $R_F = 310\Omega$
- Gain = 2

---

**HARMONIC DISTORTION vs LOAD RESISTANCE**

- $V_O = 2V_{pp}$
- $f = 1MHz$
- $R_F = 310\Omega$

---

**HARMONIC DISTORTION vs FREQUENCY**

- $V_O = 2V_{pp}$
- $R_L = 200\Omega$
- Gain = 2

---

**HARMONIC DISTORTION vs NONINVERTING GAIN**

- $V_O = 2V_{pp}$
- $R_L = 200\Omega$
- Gain = 2

---

**INPUT VOLTAGE AND CURRENT NOISE**

**SPECTRAL DENSITY vs FREQUENCY**

- Voltage Noise (nV/√Hz)
- Current Noise (fA/√Hz)
TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ C$, $V_S = 5V$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.

- **Frequency Response for Various $R_L$**
  - Gain = 1
  - $V_O = 0.1V_{pp}$
  - $R_{LOAD} = 1k\Omega$
  - $R_{LOAD} = 150\Omega$
  - $R_{LOAD} = 50\Omega$

- **Frequency Response vs Capacitive Load**
  - $C_{LOAD} = 1pF, R_S = 75\Omega$
  - $C_{LOAD} = 5pF, R_S = 55\Omega$
  - $C_{LOAD} = 10pF, R_S = 40\Omega$
  - $C_{LOAD} = 47pF, R_S = 30\Omega$
  - $C_{LOAD} = 100pF, R_S = 20\Omega$

- **Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency**
  - PSRR $V-$$V+$
  - CMRR

- **Composite Video Differential Gain and Phase**
  - $dP$ vs Number of $150\Omega$ Loads

- **Output Voltage Swing vs Output Current**
  - $V_S = 5V$
  - $25^\circ C, 125^\circ C, 85^\circ C, 55^\circ C, 25^\circ C$
TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT**

$V_S = 2.7\text{V}$

**QUIESCENT CURRENT vs TEMPERATURE**

**INPUT BIAS CURRENT vs TEMPERATURE**

**POWER-SUPPLY REJECTION RATIO and COMMON-MODE REJECTION RATIO vs TEMPERATURE**

**INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE**

**SHORT-CIRCUIT CURRENT vs TEMPERATURE**
TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ C$, $V_S = 5V$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.
TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ C$, $V_S = 5V$, and $R_L = 150\Omega$ connected to $V_S/2$ unless otherwise noted.
APPLICATIONS INFORMATION

The OPA300 and OPA301 series of single-supply CMOS op amps are designed to interface with high-speed 16-bit analog-to-digital converters (ADCs). Featuring wide 150MHz bandwidth, fast 150ns settling time to 16 bits, and high open loop gain, this series offers excellent performance in a small SO-8 and tiny SOT23 packages.

THEORY OF OPERATION

The OPA300 and OPA301 series op amps use a classic two-stage topology, shown in Figure 1. The differential input pair is biased to maximize slew rate without compromising stability or bandwidth. The folded cascode adds the signal from the input pair and presents a differential signal to the class AB output stage. The class AB output stage allows rail-to-rail output swing, with high-impedance loads (> 2kΩ), typically 100mV from the supply rails. With 10Ω loads, a useful output swing can be achieved and still maintain high open-loop gain. See the typical characteristic Output Voltage Swing vs Output Current.

OPERATING VOLTAGE

OPA300/OPA301 series op amp parameters are fully specified from +2.7V to +5.5V. Supply voltages higher than 5.5V (absolute maximum) can cause permanent damage to the amplifier. Many specifications apply from -40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

PCB LAYOUT

As with most high-speed operational amplifiers, board layout requires special attention to maximize AC and DC performance. Extensive use of ground planes, short lead lengths, and high-quality bypass capacitors will minimize leakage that can compromise signal quality. Guard rings applied with potential as near to the input pins as possible help minimize board leakage.

INPUT AND ESD PROTECTION

All OPA300/OPA301 series op amps' pins are static-protected with internal ESD protection diodes tied to the supplies, as shown in Figure 2. These diodes will provide overdrive protection if the current is externally limited to 10mA, as stated in the Absolute Maximum Ratings. Any input current beyond the Absolute Maximum Ratings, or long-term operation at maximum ratings, will shorten the lifespan of the amplifier.

ENABE FUNCTION

The shutdown function of the OPA300 and OPA2300 is referenced to the negative supply voltage of the operational amplifier. A logic level HIGH enables the op amp. A valid logic HIGH is defined as 2.5V above the negative supply applied to the enable pin. A valid logic LOW is defined as < 0.8V above the negative supply pin. If dual or split power supplies are used, care should be taken to ensure logic input signals are properly referred to the negative supply voltage. If this pin is not connected to a valid high or low voltage, the internal circuitry will pull the node high and enable the part to function.

The logic input is a high-impedance CMOS input. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10µs; disable time is 1µs. When disabled, the output assumes a high-impedance state. This allows the OPA300 to be operated as a gated amplifier, or to have its output multiplexed onto a common analog output bus.
DRIVING CAPACITIVE LOADS
When using high-speed operational amplifiers, it is extremely important to consider the effects of capacitive loading on amplifier stability. Capacitive loading will interact with the output impedance of the operational amplifier, and depending on the capacitor value, may significantly decrease the gain bandwidth, as well as introduce peaking. To reduce the effects of capacitive loading and allow for additional capacitive load drive, place a series resistor between the output and the load. This will reduce available bandwidth, but permit stable operation with capacitive loading. Figure 3 illustrates the recommended relationship between the resistor and capacitor values.

Amplifiers configured in unity gain are most susceptible to stability issues. The typical characteristic, Frequency Response vs Capacitive Load, describes the relationship between capacitive load and stability for the OPA300/OPA301 series. In unity gain, the OPA300/OPA301 series is capable of driving a few picofarads of capacitive load without compromising stability. Board level parasitic capacitance can often fall into the range of a picofarad or more, and should be minimized through good circuit-board layout practices to avoid compromising the stability of the OPA300/OPA301. For more information on detecting parasitics during testing, see the Application Note Measuring Board Parasitics in High-Speed Analog Design (SBOA094), available at the TI web site www.ti.com.

Figure 3. Recommended Rs and CL Combinations

Figure 4. The OPA30x Drives the 16-Bit ADS8401

Table 1. OPA30x Performance Results Driving a 1.25MSPS ADS8401

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>RESULTS (f = 10kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>THD</td>
<td>−99.3dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>101.2dB</td>
</tr>
<tr>
<td>THD+N</td>
<td>84.2dB</td>
</tr>
<tr>
<td>SNR</td>
<td>84.3dB</td>
</tr>
</tbody>
</table>

DRIVING A 16-BIT ADC
The OPA300/OPA301 series feature excellent THD+noise, even at frequencies greater than 1MHz, with a 16-bit settling time of 150ns. Figure 4 shows a total single supply solution for high-speed data acquisition. The OPA300/OPA301 directly drives the ADS8401, a 1.25 mega sample per second (MSPS) 16-bit data converter. The OPA300/OPA301 is configured in an inverting gain of 1, with a 5V single supply. Results of the OPA300/OPA301 performance are summarized in Table 1.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2300AIDGSR</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>C01</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2300AIDGSRG4</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>C01</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2300AIDGST</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>C01</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2301AID</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 2301A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2301AIDG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 2301A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2301AIDGKR</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OAWM</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2301AIDGKT</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OAWM</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2301AIDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 2301A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA300AID</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 300A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA300AIDBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>A52</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA300AIDBVT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>A52</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA301AID</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 301A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA301AIDBVR</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>AUP</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA301AIDBVT</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>AUP</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA301AIDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 301A</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE**: Product device recommended for new designs.

**LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2300AIDGSR</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA2300AIDGST</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>2500</td>
<td>180.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA2301AIDGKR</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA2301AIDGTK</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>180.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA2301AIDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA300AIDBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>OPA300AIDBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>2500</td>
<td>178.0</td>
<td>9.0</td>
<td>3.23</td>
<td>3.17</td>
<td>1.37</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>OPA301AIDBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>178.0</td>
<td>9.0</td>
<td>3.3</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>OPA301AIDBVT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>2500</td>
<td>178.0</td>
<td>9.0</td>
<td>3.3</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
<tr>
<td>OPA301AIDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2300AIDGSR</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA2300AIDGST</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA2301AIDGKR</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA2301AIDGKT</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA2301AIDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA300AIDBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>445.0</td>
<td>220.0</td>
<td>345.0</td>
</tr>
<tr>
<td>OPA300AIDBVBT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>445.0</td>
<td>220.0</td>
<td>345.0</td>
</tr>
<tr>
<td>OPA301AIDBVR</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>3000</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>OPA301AIDBVBT</td>
<td>SOT-23</td>
<td>DBV</td>
<td>5</td>
<td>250</td>
<td>180.0</td>
<td>180.0</td>
<td>18.0</td>
</tr>
<tr>
<td>OPA301AIDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
△ Falls within JEDEC MO-178 Variation AB, except minimum lead width.
DBV (R-PDSC-G6)  PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS–012 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC–7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
DGS (S-PDSO-G10)  PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY TECHNOLOGY, PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated