1.8-V MICROPPOWER CMOS OPERATIONAL AMPLIFIER
ZERO-DRIFT SERIES
Check for Samples: OPA2333-HT

FEATURES

• Low Offset Voltage: 26 μV (Max)
• 0.01-Hz to 10-Hz Noise: 1.5 μVpp
• Quiescent Current: 50 μA
• Single-Supply Operation
• Supply Voltage: 1.8 V to 5.5 V
• Rail-to-Rail Input/Output

APPLICATIONS

• Down-Hole Drilling
• High Temperature Environments

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

• Controlled Baseline
• One Assembly/Test Site
• One Fabrication Site
• Available in Extreme (−55°C/210°C) Temperature Range (1)
• Extended Product Life Cycle
• Extended Product-Change Notification
• Product Traceability
• Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

(1) Custom temperature ranges available

DESCRIPTION/ORDERING INFORMATION (2)

The OPA2333 series of CMOS operational amplifiers uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage and near-zero drift over time and temperature. These miniature, high-precision, low-quiescent-current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 150 mV of the rails. Single or dual supplies as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V) may be used. They are optimized for low-voltage single-supply operation.

The OPA2333 family offers excellent common-mode rejection ratio (CMRR) without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

(2) Refer to Electrical Characteristics for performance degradation over temperature.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>~55°C to 210°C</td>
<td>KGD</td>
<td>OPA2333SKGD1</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>JD</td>
<td>OPA2333SJD</td>
<td>OPA2333SJD</td>
</tr>
<tr>
<td></td>
<td>HKJ</td>
<td>OPA2333SHKJ</td>
<td>OPA2333SHKJ</td>
</tr>
<tr>
<td></td>
<td>HKQ</td>
<td>OPA2333SHKQ</td>
<td>OPA2333SHKQ</td>
</tr>
<tr>
<td>~55°C to 175°C</td>
<td>D</td>
<td>OPA2333HD</td>
<td>O2333H</td>
</tr>
</tbody>
</table>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

### BARE DIE INFORMATION

<table>
<thead>
<tr>
<th>DIE THICKNESS</th>
<th>BACKSIDE FINISH</th>
<th>BACKSIDE POTENTIAL</th>
<th>BOND PAD METALLIZATION COMPOSITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 mils.</td>
<td>Silicon with backgrind</td>
<td>V-</td>
<td>Al-Si-Cu (0.5%)</td>
</tr>
</tbody>
</table>

### Table 2. BOND PAD COORDINATES

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>PAD NUMBER</th>
<th>a</th>
<th>b</th>
<th>c</th>
<th>d</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT A</td>
<td>1</td>
<td>21.20</td>
<td>1288.50</td>
<td>97.20</td>
<td>1364.50</td>
</tr>
<tr>
<td>~IN A</td>
<td>2</td>
<td>21.20</td>
<td>923.65</td>
<td>97.20</td>
<td>999.65</td>
</tr>
<tr>
<td>+IN A</td>
<td>3</td>
<td>21.20</td>
<td>533.05</td>
<td>97.20</td>
<td>609.05</td>
</tr>
<tr>
<td>V-</td>
<td>4</td>
<td>31.30</td>
<td>172.20</td>
<td>107.30</td>
<td>248.20</td>
</tr>
<tr>
<td>+IN B</td>
<td>5</td>
<td>864.80</td>
<td>162.25</td>
<td>940.80</td>
<td>238.25</td>
</tr>
<tr>
<td>~IN B</td>
<td>6</td>
<td>864.80</td>
<td>552.65</td>
<td>940.80</td>
<td>628.65</td>
</tr>
<tr>
<td>OUT B</td>
<td>7</td>
<td>864.80</td>
<td>897.10</td>
<td>940.80</td>
<td>973.10</td>
</tr>
<tr>
<td>V+</td>
<td>8</td>
<td>854.70</td>
<td>1280.45</td>
<td>930.70</td>
<td>1356.45</td>
</tr>
</tbody>
</table>
# THERMAL CHARACTERISTICS FOR JD PACKAGE

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{JA} ) Junction-to-ambient thermal resistance(^{(1)} )</td>
<td>High-K board(^{(2)} ), no airflow</td>
<td>64.9</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>( \theta_{JA} ) Junction-to-ambient thermal resistance (^{(1)} )</td>
<td>No airflow</td>
<td>83.4</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>( \theta_{JB} ) Junction-to-board thermal resistance</td>
<td>High-K board without underfill</td>
<td>27.9</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>( \theta_{JC} ) Junction-to-case thermal resistance</td>
<td></td>
<td>6.49</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>

\(^{(1)}\) The intent of \( \theta_{JA} \) specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

\(^{(2)}\) JED51-7, high effective thermal conductivity test board for leaded surface mount packages

# THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{JC} ) Junction-to-case thermal resistance</td>
<td>5.7</td>
<td></td>
<td>13.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

# THERMAL CHARACTERISTICS FOR D PACKAGE

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \theta_{JC} ) Junction-to-case thermal resistance (to bottom of case)</td>
<td>39.4</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>

# ABSOLUTE MAXIMUM RATINGS\(^{(1)}\)

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>7 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal input terminals, voltage(^{(2)})</td>
<td>−0.3</td>
<td>(V+) + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>Output short circuit(^{(3)})</td>
<td>Continuous</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>JD, HKJ, HKQ packages</td>
<td>−55</td>
<td>210</td>
</tr>
<tr>
<td>D package</td>
<td>−55</td>
<td>175</td>
<td></td>
</tr>
<tr>
<td>Junction temperature</td>
<td>JD, HKJ, HKQ packages</td>
<td>210</td>
<td></td>
</tr>
<tr>
<td>D package</td>
<td>175</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ESD rating</td>
<td>Human-Body Model (HBM)</td>
<td>4000</td>
<td></td>
</tr>
<tr>
<td>Charged-Device Model (CDM)</td>
<td>1000</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.

\(^{(3)}\) Short circuit to ground, one amplifier per package.
**ELECTRICAL CHARACTERISTICS: \( V_S = 1.8 \) V to 5.5 V**

Boldface limits apply over the specified temperature range, \( T_A = -55^\circ\text{C} \) to 210°C. At \( T_A = 25^\circ\text{C} \), \( R_L = 10 \) kΩ connected to \( V_S/2 \), \( V_{CM} = V_S/2 \), and \( V_{OUT} = V_S/2 \) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A = -55^\circ\text{C} ) to 125°C</th>
<th>( T_A = 175^\circ\text{C}(1) )</th>
<th>( T_A = 210^\circ\text{C}(2) )</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Voltage</td>
<td>( V_{OS} ) ( V_S = 5 ) V</td>
<td>2</td>
<td>10</td>
<td></td>
<td>( \mu V )</td>
</tr>
<tr>
<td>over temperature ( \text{d}V_{OS}/\text{d}T )</td>
<td></td>
<td>0.02</td>
<td>0.05</td>
<td>0.05</td>
<td>( \mu V/\text{C} )</td>
</tr>
<tr>
<td>vs power supply ( V_S = 1.8 ) V to 5.5 V</td>
<td>1</td>
<td>6</td>
<td>1.2</td>
<td>8</td>
<td>1.7</td>
</tr>
<tr>
<td>Offset Current ( I_{OS} ) ( V_S = 5 ) V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise ( V_{n} ) ( f = 0.01 ) Hz to</td>
<td>0.3</td>
<td>1.0</td>
<td>1.0</td>
<td>( \mu V_{PP} )</td>
<td></td>
</tr>
<tr>
<td>1 Hz ( V_{n} ) ( f = 0.1 ) Hz to 10 Hz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio ( V_{CM} ) ( (V-) - 0.1 ) V ( V_{CM} )</td>
<td>102</td>
<td>130</td>
<td>101</td>
<td>91</td>
<td>dB</td>
</tr>
<tr>
<td>Differential ( C_L ) ( \text{ capacitance } )</td>
<td>2</td>
<td>4.25</td>
<td>4.25</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Common ( A_{CL} ) ( (V-) &lt; 100 \text{ mV} &lt; (V+) \text{ mV} ) ( R_L = 10 ) kΩ</td>
<td>104</td>
<td>130</td>
<td>93</td>
<td>110</td>
<td>85</td>
</tr>
<tr>
<td>Gain-bandwidth product ( GBW ) ( C_L = 100 ) pF</td>
<td>350</td>
<td>350</td>
<td>350</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Slew rate ( SR ) ( G = 1 ) ( V/\mu s )</td>
<td>0.16</td>
<td>0.25</td>
<td>0.25</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) Minimum and maximum parameters are characterized for operation at \( T_A = 175^\circ\text{C} \), but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

(2) Minimum and maximum parameters are characterized for operation at \( T_A = 210^\circ\text{C} \), but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

(3) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 \( \mu V \).

(4) The OPA2333-HT is not intended to be used as a comparator due to its limited differential input range capability.
ELECTRICAL CHARACTERISTICS: $V_S = 1.8 \text{ V to } 5.5 \text{ V (continued)}$

Boldface limits apply over the specified temperature range, $T_A = –55^\circ\text{C to } 210^\circ\text{C}$. At $T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$ (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$T_A = –55^\circ\text{C to } 125^\circ\text{C}$</th>
<th>$T_A = 175^\circ\text{C}$</th>
<th>$T_A = 210^\circ\text{C}$</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTPUT</td>
<td>Voltage output over temperature</td>
<td>$R_L = 10 \text{ k}\Omega$</td>
<td>30</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Short-circuit current</td>
<td></td>
<td></td>
<td></td>
<td>$\pm 5$</td>
</tr>
<tr>
<td></td>
<td>Capacitive load drive</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Open-loop output impedance(5)</td>
<td>$f = 350 \text{ kHz}$, $I_O = 0$</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td>Specified voltage range</td>
<td>$V_S$</td>
<td>1.8</td>
<td>5.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Quiescent current per amplifier over temperature</td>
<td>$I_Q = 0$</td>
<td>17</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Turn-on time</td>
<td>$V_S = 5 \text{ V}$</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEMPERATURE RANGE</td>
<td>Specified range</td>
<td>-55 to 210</td>
<td>-55 to 175</td>
<td>-55 to 210</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Operating range</td>
<td>-55 to 210</td>
<td>-55 to 175</td>
<td>-55 to 210</td>
<td>°C</td>
</tr>
</tbody>
</table>

(5) See Typical Characteristics.
(1) See datasheet for absolute maximum and minimum recommended operating conditions.
(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.
(4) This device is qualified for 1000 hours of continuous operation at maximum rated temperature.

Figure 1. OPA2333SKGD1/OPA2333HD Operating Life Derating Chart
TYPICAL CHARACTERISTICS

At $T_A = 25^\circ C$, $V_S = 5$ V, and $C_L = 0$ pF (unless otherwise noted).

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

OFFSET VOLTAGE SWING vs OUTPUT CURRENT

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

COMMON-MODE REJECTION RATIO vs FREQUENCY

POWER-SUPPLY REJECTION RANGE vs FREQUENCY

OPEN-LOOP GAIN vs FREQUENCY

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

At $T_A = 25^\circ C$, $V_S = 5$ V, and $C_L = 0$ pF (unless otherwise noted).

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

OFFSET VOLTAGE SWING vs OUTPUT CURRENT

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

COMMON-MODE REJECTION RATIO vs FREQUENCY

POWER-SUPPLY REJECTION RANGE vs FREQUENCY

OPEN-LOOP GAIN vs FREQUENCY

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT
SMALL-SIGNAL STEP RESPONSE
Output Voltage (50mV/div)
Time (5 µs/div)
G = +1
R_L = 10k Ω

POSITIVE OVER-VOLTAGE RECOVERY
2V/div
0
1V/div
0
Time (50 µs/div)
Input
Output
1 0k Ω
1 k Ω
O PA2333
+2.5V
−2.5V

QUIESCENT CURRENT vs TEMPERATURE
IB (pA)
0
100
80
60
40
20
0
− 20
− 40
− 60
− 80
− 100
1
Common–Mode Voltage (V)
54321
− IB
+I B
V_S = 5V

INPUT BIAS CURRENT vs TEMPERATURE
IB (pA)
− 50
200
150
100
50
0
− 50
− 100
− 150
− 200
− 25
Temperature (°C)
1251007550250
V_S = 5.5V
V_S = 1.8V

LARGE–SIGNAL STEP RESPONSE
Output Voltage (1V/div)
Time (50µs/div)
G = 1
R_L = 10k Ω

Product Folder Links: OPA2333-HT
TYPICAL CHARACTERISTICS (continued)

NEGATIVE OVER-VOLTAGE RECOVERY

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

SETTLING TIME vs CLOSED-LOOP GAIN

0.1Hz TO 10Hz NOISE
APPLICATION INFORMATION (1)

The OPA2333 is unity-gain stable and free from unexpected output phase reversal. It uses a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by ensuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals)
- Thermally isolate components from power supplies or other heat sources
- Shield op amp and input circuitry from air currents, such as cooling fans

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

Operating Voltage

The OPA2333 op amp operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Input Voltage

The OPA2333 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA2333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is about 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor (see Figure 2).

![Figure 2. Input Current Protection](image)

Internal Offset Correction

The OPA2333 op amp uses an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. This amplifier is zero corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

(1) At T_{A} = 25°C (unless otherwise noted).
Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA2333 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve (see Figure 3).

![Figure 3. V\text{OUT} Range to Ground](image)

The OPA2333 has an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA2333 has been characterized to perform with this technique; however, the recommended resistor value is approximately 20 kΩ. Note that this configuration will increase the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

General Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in their susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA2333 has been specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous-generation devices. Strong RF fields may still cause varying offset levels.
A. REF3140 has not been characterized or tested at 210°C.

**Figure 4. Temperature Measurement**

**Figure 5** shows the basic configuration for a bridge amplifier.

**Figure 5. Single Op-Amp Bridge Amplifier**

A low-side current shunt monitor is shown in **Figure 6**. $R_N$ are operational resistors used to isolate the ADS1100 from the noise of the digital I²C bus. Since the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 may be omitted.
Two zener biasing methods are shown.

NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 6. Low-Side Current Monitor

Figure 7. High-Side Current Monitor
\[ V_O = (1 + \frac{2R_2}{R_1}) \left( V_2 - V_1 \right) \]

A. INA152 has not been characterized or tested at 210°C.

**Figure 8. Thermistor Measurement**

**Figure 9. Precision Instrumentation Amplifier**
# REVISION HISTORY

## Changes from Revision G (September 2012) to Revision H

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed Operating Life Derating Chart</td>
<td>7</td>
</tr>
</tbody>
</table>
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2333HD</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-4-260C-72 HR</td>
<td>-55 to 175</td>
<td>O2333H</td>
<td></td>
</tr>
<tr>
<td>OPA2333SHKJ</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>HKJ</td>
<td>8</td>
<td>1</td>
<td>TBD</td>
<td>Call TI</td>
<td>N / A for Pkg Type</td>
<td>-55 to 210</td>
<td>OPA2333S</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2333SHKQ</td>
<td>ACTIVE</td>
<td>CFP</td>
<td>HKQ</td>
<td>8</td>
<td>1</td>
<td>TBD</td>
<td>AU</td>
<td>N / A for Pkg Type</td>
<td>-55 to 210</td>
<td>OPA2333S</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2333SJD</td>
<td>ACTIVE</td>
<td>CDIP SB</td>
<td>JD</td>
<td>8</td>
<td>1</td>
<td>TBD</td>
<td>POST-PLATE</td>
<td>N / A for Pkg Type</td>
<td>-55 to 210</td>
<td>OPA2333SJD</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2333SKGD1</td>
<td>ACTIVE</td>
<td>XCEPT</td>
<td>KGD</td>
<td>0</td>
<td>100</td>
<td>TBD</td>
<td>Call TI</td>
<td>Call TI</td>
<td>-55 to 210</td>
<td></td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. – The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF OPA2333-HT :**

- Catalog: OPA2333
- Automotive: OPA2333-Q1

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package can be hermetically sealed with a metal lid.  
D. The terminals will be gold plated.  
E. Lid is not connected to any lead.
MECHANICAL DATA

JD (R-CDIP-T**)  CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

20 PINS SHOWN

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

DIM    8    14   16   18   20   24
A MAX   0.405 (10.29) 0.757 (19.23) 0.810 (20.57) 0.910 (23.11) 1.010 (25.65) 1.100 (27.94)
MECHANICAL DATA

D (R-PDSO-G8) PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
WARNING: Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
WARNING: Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Audio</td>
<td>Automotive and Transportation</td>
</tr>
<tr>
<td>Amplifiers</td>
<td>Communications and Telecom</td>
</tr>
<tr>
<td>Data Converters</td>
<td>Computers and Peripherals</td>
</tr>
<tr>
<td>DLP® Products</td>
<td>Consumer Electronics</td>
</tr>
<tr>
<td>DSP</td>
<td>Energy and Lighting</td>
</tr>
<tr>
<td>Clocks and Timers</td>
<td>Industrial</td>
</tr>
<tr>
<td>Interface</td>
<td>Medical</td>
</tr>
<tr>
<td>Logic</td>
<td>Security</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Space, Avionics and Defense</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Video and Imaging</td>
</tr>
<tr>
<td>RFID</td>
<td></td>
</tr>
<tr>
<td>OMAP Applications Processors</td>
<td>TI E2E Community</td>
</tr>
<tr>
<td>Wireless Connectivity</td>
<td>e2e.ti.com</td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated