Low-Power, Dual Current-Feedback OPERATIONAL AMPLIFIER

FEATURES
- Minimal Bandwidth Change Versus Gain
- 170MHz Bandwidth at G = +2
- > 120MHz Bandwidth to Gain > +10
- Low Distortion: < −82dBc at 5MHz
- High Output Current: 120mA
- Single +5V to +12V Supply Operation
- Dual ±2.5 to ±6.0V Supply Operation
- Low Supply Current: 3.4mA Total

APPLICATIONS
- Short-Loop ADSL CO Driver
- Low-Power Broadcast Video Drivers
- Differential Equalizing Filters
- Differential SAW Filter Post Amplifier
- Multichannel Summing Amplifiers
- Professional Cameras
- ADC Input Drivers

DESCRIPTION
The OPA2684 provides a new level of performance in low-power, wideband, current-feedback (CFB) amplifiers. This CFBPLUS amplifier is among the first to use an internally closed-loop input buffer stage that enhances performance significantly over earlier low-power CFB amplifiers. While retaining the benefits of very low power operation, this new architecture provides many of the benefits of a more ideal CFB amplifier. The closed-loop input stage buffer gives a very low and linearized impedance path at the inverting input to sense the feedback error current. This improved inverting input impedance retains exceptional bandwidth to much higher gains and improves harmonic distortion over earlier solutions limited by inverting input linearity. Beyond simple high-gain applications, the OPA2684 CFBPLUS amplifier permits the gain setting element to be set with considerable freedom from amplifier bandwidth interaction. This allows frequency response peaking elements to be added, multiple input inverting summing circuits to have greater bandwidth, and low-power line drivers to meet the demanding requirements of studio cameras and broadcast video.

The output capability of the OPA2684 also sets a new mark in performance for low-power, current-feedback amplifiers. Delivering a full ±4Vp-p swing on ±5V supplies, the OPA2684 also has the output current to support > ±3Vp-p into 50Ω loads. This minimal output headroom requirement is complemented by a similar 1.2V input stage headroom giving exceptional capability for single +5V operation.

The OPA2684’s low 3.4mA supply current is precisely trimmed at +25°C. This trim, along with low shift over temperature and supply voltage, gives a very robust design over a wide range of operating conditions.

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**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>±6.5V DC</td>
</tr>
<tr>
<td>Internal Power Dissipation</td>
<td>±1.2V</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>±V S</td>
</tr>
<tr>
<td>Storage Temperature Range: ID, IDBV</td>
<td>-65°C to +125°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+300°C</td>
</tr>
<tr>
<td>Junction Temperature (T J)</td>
<td>+175°C</td>
</tr>
<tr>
<td>ESD Rating: Human Body Model (HBM)</td>
<td>2000V</td>
</tr>
<tr>
<td>ESD Rating: Charged Device Model (CDM)</td>
<td>1500V</td>
</tr>
</tbody>
</table>

**NOTE:** (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

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**OPA2684 RELATED PRODUCTS**

<table>
<thead>
<tr>
<th>SINGLES</th>
<th>DUALS</th>
<th>TRIPLES</th>
<th>QUADS</th>
<th>FEATURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA684</td>
<td>OPA2683</td>
<td>OPA3684</td>
<td>OPA2684</td>
<td>Low-Power CFB PLUS</td>
</tr>
<tr>
<td>OPA691</td>
<td>OPA2691</td>
<td>OPA3691</td>
<td>—</td>
<td>High Slew Rate CFB</td>
</tr>
<tr>
<td>OPA885</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>&gt; 500MHz CFB</td>
</tr>
</tbody>
</table>

**PACKAGE/ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>PACKAGE-LEAD</th>
<th>PACKAGE DESIGNATOR</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
<th>PACKAGE MARKING</th>
<th>ORDERING NUMBER</th>
<th>TRANSPORT MEDIA, QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2684</td>
<td>SO-8</td>
<td>D</td>
<td>-40°C to +85°C</td>
<td>OPA2684</td>
<td>OPA2684ID</td>
<td>Rails, 100 Tape and Reel, 2500</td>
</tr>
<tr>
<td>OPA2684</td>
<td>SOT23-8</td>
<td>DCN</td>
<td>-40°C to +85°C</td>
<td>OPA2684IDCN</td>
<td>OPA2684IDCNR</td>
<td>Tape and Reel, 250 Tape and Reel, 3000</td>
</tr>
</tbody>
</table>

**NOTE:** (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

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**PIN CONFIGURATION**

**Top View**

```
   1  2  3  4  5  6  7  8
Out A  +V S  -In B  +In A  -In A  +V S  Out B  -In B  -V S
```

**SOT**

```
   1  2  3  4  5  6  7  8
Out A  -In A  +In A  -In B  -V S  +V S  Out B  -V S
```

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**ELECTROSTATIC DISCHARGE SENSITIVITY**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
ELECTRICAL CHARACTERISTICS: \( V_S = \pm 5V \)

**Boldface** limits are tested at +25°C. 
\( R_F = 800\Omega, \ R_L = 100\Omega, \) and \( G = +2 \). (see Figure 1 for AC performance only), unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>TYP</th>
<th>MIN/MAX OVER TEMPERATURE</th>
<th>TEST LEVEL</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( +25^\circ \text{C} )</td>
<td>( +25^\circ \text{C}(1) )</td>
<td>( -40^\circ \text{C} ) to ( 70^\circ \text{C}(2) )</td>
<td>( \text{UNITS} )</td>
</tr>
<tr>
<td>AC PERFORMANCE (see Figure 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Small-Signal Bandwidth ( (V_O = 0.5Vp-p) )</td>
<td>( G = +1, \ R_F = 800\Omega )</td>
<td>250</td>
<td></td>
<td>MHz typ C</td>
</tr>
<tr>
<td></td>
<td>( G = +2, \ R_F = 800\Omega )</td>
<td>170</td>
<td>120 118 117</td>
<td>MHz min B</td>
</tr>
<tr>
<td></td>
<td>( G = +5, \ R_F = 800\Omega )</td>
<td>138</td>
<td></td>
<td>MHz typ C</td>
</tr>
<tr>
<td></td>
<td>( G = +10, \ R_F = 800\Omega )</td>
<td>120</td>
<td></td>
<td>MHz typ C</td>
</tr>
<tr>
<td>Bandwidth for 0.1dB Gain Flatness</td>
<td>( G = +20, \ R_F = 800\Omega )</td>
<td>95</td>
<td></td>
<td>MHz typ C</td>
</tr>
<tr>
<td></td>
<td>( G = +2, \ V_O = 0.5Vp-p, \ R_L = 800\Omega )</td>
<td>19</td>
<td>16 14 14</td>
<td>MHz min B</td>
</tr>
<tr>
<td>Peaking at a Gain of +1</td>
<td>( R_F = 800\Omega, \ V_O = 0.5Vp-p )</td>
<td>1.4</td>
<td>4.8 5.9 6.3</td>
<td>dB max B</td>
</tr>
<tr>
<td>Large-Signal Bandwidth</td>
<td>( G = +2, \ V_O )</td>
<td>90</td>
<td></td>
<td>MHz typ C</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>( G = -1, \ V_O = 4\text{ Step} )</td>
<td>780</td>
<td>675 650 575</td>
<td>( \mu \text{V/\mu} \text{sec} ) min B</td>
</tr>
<tr>
<td></td>
<td>( G = +2, \ V_O = 4\text{ Step} )</td>
<td>750</td>
<td>680 660 656</td>
<td>( \mu \text{V/\mu} \text{sec} ) min B</td>
</tr>
<tr>
<td>Rise-and-Fall Time</td>
<td>( G = +2, \ V_O = 0.5\text{ Step} )</td>
<td>3</td>
<td></td>
<td>ns typ C</td>
</tr>
<tr>
<td></td>
<td>( G = +2, \ V_O = 4\text{ Step} )</td>
<td>3.8</td>
<td></td>
<td>ns typ C</td>
</tr>
<tr>
<td>Harmonic Distortion</td>
<td>( G = +2, f = )</td>
<td>25</td>
<td>355</td>
<td>160 155 153</td>
</tr>
<tr>
<td>2nd-Harmonic</td>
<td>( R_L = 100\Omega )</td>
<td></td>
<td>-67</td>
<td>-59 -59 -58</td>
</tr>
<tr>
<td></td>
<td>( R_L &gt; 1k\Omega )</td>
<td></td>
<td>-82</td>
<td>-66 -65 -65</td>
</tr>
<tr>
<td>3rd-Harmonic</td>
<td>( R_L = 100\Omega )</td>
<td></td>
<td>-70</td>
<td>-66 -65 -65</td>
</tr>
<tr>
<td></td>
<td>( R_L &gt; 1k\Omega )</td>
<td></td>
<td>-84</td>
<td>-82 -81 -81</td>
</tr>
<tr>
<td>Input Voltage Noise</td>
<td>( f &gt; 1\text{MHz} )</td>
<td></td>
<td>3.7</td>
<td>4.1 4.2 4.4</td>
</tr>
<tr>
<td>Inverting Input Current Noise</td>
<td>( f &gt; 1\text{MHz} )</td>
<td></td>
<td>9.4</td>
<td>11 12 12.5</td>
</tr>
<tr>
<td>Average Noninverting Input Bias Current</td>
<td>( f &gt; 1\text{MHz} )</td>
<td></td>
<td>17</td>
<td>18 18.5 19</td>
</tr>
<tr>
<td>Average Noninverting Input Bias Current Drift</td>
<td>( f = 1\text{MHz} )</td>
<td></td>
<td>0.04</td>
<td></td>
</tr>
<tr>
<td>Differential Phase</td>
<td>( G = +2, \ V_O = 1.4\text{Vp}, \ R_L = 150\Omega )</td>
<td></td>
<td>0.02</td>
<td></td>
</tr>
<tr>
<td>Channel-to-Channel Isolation</td>
<td>( f = 5\text{MHz} )</td>
<td></td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>DC PERFORMANCE(3)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open-Loop Transimpedance Gain ( (Z_{OL}) )</td>
<td>( V_O = 0\text{V}, \ R_L = 1\text{k\Omega} )</td>
<td>355</td>
<td>160 155 153</td>
<td>\text{kA} min A</td>
</tr>
<tr>
<td>Input Offset Voltage</td>
<td>( V_{CM} = 0\text{V} )</td>
<td></td>
<td>±1.5</td>
<td>±3.8 ±4.4 ±4.6</td>
</tr>
<tr>
<td>Average Offset Voltage Drift</td>
<td>( V_{CM} = 0\text{V} )</td>
<td></td>
<td>±12</td>
<td>±12</td>
</tr>
<tr>
<td>Noninverting Input Bias Current</td>
<td>( V_{CM} = 0\text{V} )</td>
<td></td>
<td>±5.0</td>
<td>±11</td>
</tr>
<tr>
<td>Average Noninverting Input Bias Current Drift</td>
<td>( V_{CM} = 0\text{V} )</td>
<td></td>
<td>±25</td>
<td>±25</td>
</tr>
<tr>
<td>Inverting Input Bias Current</td>
<td>( V_{CM} = 0\text{V} )</td>
<td></td>
<td>±5.0</td>
<td>±17</td>
</tr>
<tr>
<td>Average Inverting Input Bias Current Drift</td>
<td>( V_{CM} = 0\text{V} )</td>
<td></td>
<td>±35</td>
<td>±35</td>
</tr>
<tr>
<td>INPUT Common-Mode Input Range(5) ( (\text{CMIR}) )</td>
<td>( V_{CM} = 0\text{V} )</td>
<td></td>
<td>±3.75</td>
<td>±3.65 ±3.65 ±3.65</td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio ( (\text{CMRR}) )</td>
<td>( V_{CM} = 0\text{V} )</td>
<td></td>
<td>60</td>
<td>53 52 52</td>
</tr>
<tr>
<td>Noninverting Input Impedance</td>
<td>( 50 | 2 )</td>
<td></td>
<td>4.0</td>
<td></td>
</tr>
<tr>
<td>Inverting Input Resistance ( (R_L) )</td>
<td>Open-Loop, DC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OUTPUT Voltage Output Swing</td>
<td>1k\Omega Load</td>
<td></td>
<td>±4.1</td>
<td>±3.9 ±3.9 ±3.8</td>
</tr>
<tr>
<td>Current Output, Sourcing</td>
<td>( V_O = 0 )</td>
<td></td>
<td>160</td>
<td>130 125 120</td>
</tr>
<tr>
<td>Minimum Operating Voltage Range</td>
<td>( V_O = 0 )</td>
<td></td>
<td>±1.4</td>
<td>±6 ±6 ±6</td>
</tr>
<tr>
<td>Maximum Operating Voltage Range</td>
<td>( V_O = 0 )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Closed-Loop Output Impedance</td>
<td>( G = +2, f = 100kHz )</td>
<td></td>
<td>0.006</td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY Specified Operating Voltage</td>
<td></td>
<td></td>
<td>±5</td>
<td></td>
</tr>
<tr>
<td>Maximum Operating Voltage Range</td>
<td></td>
<td></td>
<td>±6</td>
<td>±6 ±6 ±6</td>
</tr>
<tr>
<td>Minimum Operating Voltage Range</td>
<td></td>
<td></td>
<td>±1.4</td>
<td></td>
</tr>
<tr>
<td>Max Quiescent Current</td>
<td>( V_O = 5\text{V/\text{per channel}} )</td>
<td></td>
<td>1.7</td>
<td>1.8 1.85 1.85</td>
</tr>
<tr>
<td>Min Quiescent Current</td>
<td>( V_S = 5\text{V/\text{per channel}} )</td>
<td></td>
<td>1.7</td>
<td>1.6 1.55 1.45</td>
</tr>
<tr>
<td>Power-Supply Rejection Ratio ( (\text{PSRR}) )</td>
<td>Input Referred</td>
<td></td>
<td>60</td>
<td>54 53 53</td>
</tr>
<tr>
<td>TEMPERATURE RANGE Specification: ID, IDCN</td>
<td>Junction-to-Ambient</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, ( \theta_{JA} )</td>
<td>D SO-8</td>
<td>125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D C SOT23-8</td>
<td>150</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

(1) Junction temperature = ambient for +25°C tested specifications.

(2) Junction temperature = ambient at low temperature limit, junction temperature = ambient +2°C at high temperature limit for over temperature tested specifications.

(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

(4) Current is considered positive out-of-node. \( V_{CM} \) is the input common-mode voltage.

(5) Tested < 3dB below minimum specified CMR at ± CMIR limits.
**ELECTRICAL CHARACTERISTICS: \( V_S = +5V \)**

**Boldface limits are tested at +25°C.**

\( R_F = 1k \Omega, \ R_L = 100\Omega, \) and \( G = +2. \) (see Figure 3 for AC performance only), unless otherwise noted.

### DC PERFORMANCE

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>TYP</th>
<th>MIN/MAX OVER TEMPERATURE</th>
<th>UNITS</th>
<th>TEST LEVEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small-Signal Bandwidth ( (V_S = +5V) )</td>
<td>( G = +1, \ R_F = 1k\Omega )</td>
<td>140</td>
<td>140</td>
<td>MHz</td>
<td>typ C</td>
</tr>
<tr>
<td>Bandwidth for 0.1dB Gain Flatness</td>
<td>( G = +2, \ R_F &lt; 0.5V-p-p, \ R_F &gt; 1.0\Omega )</td>
<td>110</td>
<td>86</td>
<td>MHz</td>
<td>min B</td>
</tr>
<tr>
<td>Bandwidth peaking at Gain of +1</td>
<td>( G = +5, \ R_F = 1.0\Omega )</td>
<td>100</td>
<td>100</td>
<td>MHz</td>
<td>min C</td>
</tr>
<tr>
<td>Large-Signal Bandwidth</td>
<td>( G = +10, \ R_F = 1.0\Omega )</td>
<td>90</td>
<td>90</td>
<td>MHz</td>
<td>typ C</td>
</tr>
<tr>
<td>slew Rate</td>
<td>( G = +20, \ R_F = 1.0\Omega )</td>
<td>75</td>
<td>75</td>
<td>MHz</td>
<td>typ C</td>
</tr>
<tr>
<td>Harmonic Distortion</td>
<td>( G = 2, V_O = 2Vp-p )</td>
<td>21</td>
<td>21</td>
<td>dB</td>
<td>max B</td>
</tr>
<tr>
<td>2nd-Harmonic</td>
<td>( R_L = 100\Omega, V_O = 1.4Vp, R_L = 150\Omega )</td>
<td>12</td>
<td>12</td>
<td>dB</td>
<td>max C</td>
</tr>
<tr>
<td>3rd-Harmonic</td>
<td>( R_L = 100\Omega, \ V_O = 1.4Vp, R_L = 150\Omega )</td>
<td>11</td>
<td>11</td>
<td>dB</td>
<td>max C</td>
</tr>
<tr>
<td>Input Voltage Noise</td>
<td>( f &gt; 1MHz )</td>
<td>3.7</td>
<td>3.7</td>
<td>nV/√Hz</td>
<td>max B</td>
</tr>
<tr>
<td>Differential Gain</td>
<td>( G = +2, V_O = 2Vp-p )</td>
<td>70</td>
<td>70</td>
<td>%</td>
<td>typ C</td>
</tr>
<tr>
<td>Differential Phase</td>
<td>( G = +2, V_O = 1.4Vp, R_L = 150\Omega )</td>
<td>0.04</td>
<td>0.04</td>
<td>%</td>
<td>typ C</td>
</tr>
<tr>
<td>Channel-to-Channel Isolation</td>
<td>( G = +2, \ R_F = 2Vp-p )</td>
<td>4.8</td>
<td>4.8</td>
<td>%</td>
<td>typ C</td>
</tr>
</tbody>
</table>

### AC PERFORMANCE

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>TYP</th>
<th>MIN/MAX OVER TEMPERATURE</th>
<th>UNITS</th>
<th>TEST LEVEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Small-Signal Bandwidth ( (V_S = +5V) )</td>
<td>( G = +1, \ R_F = 1k\Omega )</td>
<td>140</td>
<td>140</td>
<td>MHz</td>
<td>typ C</td>
</tr>
<tr>
<td>Bandwidth for 0.1dB Gain Flatness</td>
<td>( G = +2, \ R_F &lt; 0.5V-p-p, \ R_F &gt; 1.0\Omega )</td>
<td>110</td>
<td>86</td>
<td>MHz</td>
<td>min B</td>
</tr>
<tr>
<td>Bandwidth peaking at Gain of +1</td>
<td>( G = +5, \ R_F = 1.0\Omega )</td>
<td>100</td>
<td>100</td>
<td>MHz</td>
<td>min C</td>
</tr>
<tr>
<td>Large-Signal Bandwidth</td>
<td>( G = +10, \ R_F = 1.0\Omega )</td>
<td>90</td>
<td>90</td>
<td>MHz</td>
<td>typ C</td>
</tr>
<tr>
<td>slew Rate</td>
<td>( G = +20, \ R_F = 1.0\Omega )</td>
<td>75</td>
<td>75</td>
<td>MHz</td>
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<tr>
<td>Harmonic Distortion</td>
<td>( G = 2, V_O = 2Vp-p )</td>
<td>21</td>
<td>21</td>
<td>dB</td>
<td>max B</td>
</tr>
<tr>
<td>2nd-Harmonic</td>
<td>( R_L = 100\Omega, V_O = 1.4Vp, R_L = 150\Omega )</td>
<td>12</td>
<td>12</td>
<td>dB</td>
<td>max C</td>
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<tr>
<td>3rd-Harmonic</td>
<td>( R_L = 100\Omega, \ V_O = 1.4Vp, R_L = 150\Omega )</td>
<td>11</td>
<td>11</td>
<td>dB</td>
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<tr>
<td>Input Voltage Noise</td>
<td>( f &gt; 1MHz )</td>
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<td>Differential Gain</td>
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<td>Differential Phase</td>
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<td>0.04</td>
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<td>Channel-to-Channel Isolation</td>
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<td>4.8</td>
<td>4.8</td>
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### POWER SUPPLY

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<th>UNITS</th>
<th>TEST LEVEL</th>
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<tbody>
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<td>( V_S = +5V )</td>
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<tr>
<td>Max Single-Supply Operating Voltage Range</td>
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<td>V</td>
<td>max A</td>
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<tr>
<td>Min Single-Supply Operating Voltage Range</td>
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<td>V</td>
<td>min A</td>
</tr>
<tr>
<td>Max Quiescent Current</td>
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<td>max A</td>
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<tr>
<td>Power-Supply Rejection Ratio (+PSRR)</td>
<td>( V_S = +5V )</td>
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### TEMPERATURE RANGE

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<th>Specification: ID, IDBV</th>
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<td>Thermal Resistance, ( r_{JA} ) Junction-to-Ambient</td>
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TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

At $T_A = +25^\circ C$, $G = +2$, $R_F = 800\,\Omega$, and $R_L = 100\,\Omega$, unless otherwise noted.
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25^\circ C$, $G = +2$, $R_P = 800\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

### HARMONIC DISTORTION vs LOAD RESISTANCE

- $V_O = 2Vp-p$
- $f = 5MHz$
- $G = +2$

2nd-Harmonic
3rd-Harmonic

See Figure 1

### HARMONIC DISTORTION vs FreQUENCY

- $V_O = 2Vp-p$
- $R_L = 100\Omega$

2nd-Harmonic
3rd-Harmonic

See Figure 1

### HARMONIC DISTORTION vs OUTPUT VOLTAGE

- $f = 5MHz$
- $R_L = 100\Omega$

2nd-Harmonic
3rd-Harmonic

### 5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

- $V_O = 2Vp-p$
- $R_L = 100\Omega$

2nd-Harmonic
3rd-Harmonic

### HARMONIC DISTORTION vs NONINVERTING GAIN

- $f = 5MHz$
- $R_L = 100\Omega$

2nd-Harmonic
3rd-Harmonic

See Figure 1

### HARMONIC DISTORTION vs INVERTING GAIN

- $f = 5MHz$
- $R_L = 100\Omega$

2nd-Harmonic
3rd-Harmonic

See Figure 2
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25^\circ C$, $G = +2$, $R_F = 800\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

2-TONE, 3RD-ORDER INTERMODULATION DISTORTION

R$_S$ vs C$_{LOAD}$

SMALL-SIGNAL BANDWIDTH vs C$_{LOAD}$

CMRR and PSRR vs FREQUENCY

OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE

INVERTING CURRENT NOISE

9.4pA/√Hz

3.7nV/√Hz

20MHz

10MHz

5MHz

1MHz

-50

-60

-70

-80

-90

3rd-Order Spurious Level (dBc)

-14

-5

-3

-1

0

1

2

3

4

5

6

7

8

Power at Load ($P_O$ each tone, dBm)

OPEN-LOOP TRANSIMPEDANCE GAIN (dB)

$20\log (Z_{OL})$

OPEN-LOOP PHASE (°)

$\angle Z_{OL}$

CMRR

PSRR

Power-Supply Rejection Ratio (dB)

Common-Mode Rejection Ratio (dB)

$1k\Omega$ is Optional

0.5dB Peaking

Normalized Gain (dB)

0

3

6

9

6

5

4

3

2

1

0

$10^2$

$10^3$

$10^4$

$10^5$

$10^6$

$10^7$

$10^8$

Frequency (Hz)

$V_I$

$C_L$

$800\Omega$

$V_O$

$50\Omega$

$75pF$

$20pF$

$100pF$

$50pF$

$200pF$

$12pF$

$5pF$

$100pF$

$50pF$

$200pF$

$12pF$

$5pF$

$100pF$

$50pF$

$200pF$

$12pF$

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$50pF$

$200pF$

$12pF$

$5pF$

$100pF$

$50pF$

$200pF$

$12pF$

$5pF$
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25^\circ C$, $G = +2$, $R_F = 800\,\Omega$, and $R_L = 100\,\Omega$, unless otherwise noted.
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25^\circ\text{C}$, $G = \pm 2$, $R_F = 800\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

![Noninverting Overdrive Recovery Diagram]

![Inverting Overdrive Recovery Diagram]

![Input and Output Range vs Supply Voltage Diagram]
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25°C$, $G = +2$, $R_P = 800Ω$, $R_L = 100Ω$, unless otherwise noted.

DIFFERENTIAL PERFORMANCE TEST CIRCUIT

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

DIFFERENTIAL DISTORTION vs FREQUENCY

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25°C$, $G = +2$, $R_P = 800Ω$, $R_L = 100Ω$, unless otherwise noted.

DIFFERENTIAL PERFORMANCE TEST CIRCUIT

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

DIFFERENTIAL DISTORTION vs FREQUENCY

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25°C$, $G = +2$, $R_P = 800Ω$, $R_L = 100Ω$, unless otherwise noted.

DIFFERENTIAL PERFORMANCE TEST CIRCUIT

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

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DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

DIFFERENTIAL DISTORTION vs FREQUENCY

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25°C$, $G = +2$, $R_P = 800Ω$, $R_L = 100Ω$, unless otherwise noted.

DIFFERENTIAL PERFORMANCE TEST CIRCUIT

DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE

DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE

DIFFERENTIAL DISTORTION vs LOAD RESISTANCE

DIFFERENTIAL DISTORTION vs FREQUENCY

DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

At $T_A = +25°C$, $G = +2$, $R_P = 800Ω$, $R_L = 100Ω$, unless otherwise noted.
Typical Characteristics: \( V_S = +5V \)

At \( T_A = +25^\circ C \), \( V_S = 5V \), \( G = +2 \), \( R_F = 1.0k\Omega \), and \( R_L = 100\Omega \), unless otherwise noted.

**Noninverting Small-Signal Frequency Response**

- \( R_F = 1k\Omega \)
- \( G = 100 \)
- \( G = 10 \)
- \( G = 2 \)
- \( G = 1 \)
- \( G = 3 \)

See Figure 3

**Inverting Small-Signal Frequency Response**

- \( R_F = 1.0k\Omega \)
- \( G = 1 \)
- \( G = 2 \)
- \( G = 5 \)
- \( G = 50 \)

See Figure 4

**Noninverting Large-Signal Frequency Response**

- \( 0.2V_{p-p} \)
- \( 1V_{p-p} \)
- \( 2V_{p-p} \)

See Figure 3

**Inverting Large-Signal Frequency Response**

- \( V_O = 0.2V_{p-p} \)
- \( V_O = 1V_{p-p} \)
- \( V_O = 2V_{p-p} \)

See Figure 4

**Noninverting Pulse Response**

- Large-Signal Right Scale
- Small-Signal Left Scale

See Figure 3

**Inverting Pulse Response**

- Small-Signal Left Scale
- Large-Signal Right Scale

See Figure 4
TYPICAL CHARACTERISTICS: \( V_S = +5V \) (Cont.)

At \( T_A = +25^\circ C, V_S = 5V, G = +2\), \( R_F = 1.0k\Omega \), and \( R_L = 100\Omega \), unless otherwise noted.
TYPICAL CHARACTERISTICS: $V_S = +5V$ (Cont.)

At $T_A = +25^\circ C$, $V_S = 5V$, $G = +2$, $R_F = 1.0\Omega$, and $R_L = 100\Omega$, unless otherwise noted.

**DIFFERENTIAL PERFORMANCE TEST CIRCUIT**

**DIFFERENTIAL SMALL-SIGNAL FREQUENCY RESPONSE**

**DIFFERENTIAL LARGE-SIGNAL FREQUENCY RESPONSE**

**DIFFERENTIAL DISTORTION vs LOAD RESISTANCE**

**DIFFERENTIAL DISTORTION vs FREQUENCY**

**DIFFERENTIAL DISTORTION vs OUTPUT VOLTAGE**
Applications Information

Low-Power, Current-Feedback Operation

The dual channel OPA2684 gives a new level of performance in low-power, current-feedback op amps. Using a new input stage buffer architecture, the OPA2684 CFBPLUS amplifier holds nearly constant AC performance over a wide gain range. This closed-loop internal buffer gives a very low and linearized impedance at the inverting node, isolating the amplifier’s AC performance from gain element variations. This allows both the bandwidth and distortion to remain nearly constant over gain, moving closer to the ideal current-feedback performance of gain bandwidth independence.

This low-power amplifier also delivers exceptional output performance of gain bandwidth independence. This allows both the bandwidth and distortion to remain nearly constant over gain, moving closer to the ideal current-feedback performance of gain bandwidth independence.

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This low-power amplifier also delivers exceptional output performance of gain bandwidth independence. This allows both the bandwidth and distortion to remain nearly constant over gain, moving closer to the ideal current-feedback performance of gain bandwidth independence.

As the desired gain increases for the inverting configuration, RG is adjusted to achieve the desired gain, while RM is also adjusted to hold a 50Ω input match. A point will be reached where RG will equal 50Ω, R M is removed, and the input match is set by RG only. With RG fixed to achieve an input match to 50Ω, increasing RF will increase the gain. This will, however, reduce the achievable bandwidth as the feedback resistor increases from its recommended value of 800Ω. If the source does not require an input match to 50Ω, either adjust RM to get the desired load, or remove it and let the RG resistor alone provide the input load.

These circuits show ±5V operation. The same circuit can be applied with bipolar supplies from ±2.5V to ±6V. Internal supply independent biasing gives nearly the same performance for the OPA2684 over this wide range of supplies. Generally, the optimum feedback resistor value (for nominally flat frequency response at G = +2) will increase in value as the total supply voltage across the OPA2684 is reduced from ±5V.

See Figure 3 for the AC-coupled, single +5V supply, gain of +2V/V circuit configuration used as a basis only for the +5V Electrical and Typical Characteristics for each channel. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 10kΩ resistors) to the noninverting input. The input signal is then AC-coupled.
into this midpoint voltage bias. The input voltage can swing to within 1.25V of either supply pin, giving a 2.5Vp-p input signal range centered between the supply pins. The input impedance of Figure 3 is set to give a 50Ω input match. If the source does not require a 50Ω match, remove this and drive directly into the blocking capacitor. The source will then see the 5kΩ load of the biasing network. The gain resistor (RG) is AC-coupled, giving the circuit a DC gain of +1, which puts the noninverting input DC bias voltage (2.5V) on the output as well. The feedback resistor value has been adjusted from the bipolar ±5V supply condition to re-optimize for a flat frequency response in +5V only, gain of +2, operation. On a single +5V supply, the output voltage can swing to within 1.0V of either supply pin while delivering more than 70mA output current giving 3V output swing into 100Ω (8dBm maximum at a matched 50Ω load). The circuit of Figure 3 shows a blocking capacitor driving into a 50Ω output resistor then into a 50Ω load. Alternatively, the blocking capacitor could be removed if the load is tied to a supply midpoint or to ground if the DC current required by the load is acceptable.

The circuits of Figure 3 and 4 show single-supply operation at +5V. These same circuits may be used up to single supplies of +12V with minimal change in the performance of the OPA2684.

DIFFERENTIAL INTERFACE APPLICATIONS

Dual op amps are particularly suitable to differential input to differential output applications. Typically, these fall into either Analog-to-Digital Converter (ADC) input interface or line driver applications. Two basic approaches to differential I/O are noninverting or inverting configurations. Since the output is differential, the signal polarity is somewhat meaningless—the noninverting and inverting terminology applies here to where the input is brought into the OPA2684. Each has its advantages and disadvantages. Figure 5 shows a basic starting point for noninverting differential I/O applications.
This approach provides for a source termination impedance that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs without interacting with the gain setting. The differential signal gain for the circuit of Figure 5 is:

$$A_D = 1 + 2 \cdot \frac{R_F}{R_G}$$

Since the OPA2684 is a CFB PLUS amplifier, its bandwidth is principally controlled with the feedback resistor value. Figure 5 shows the recommended value of 800Ω. The differential gain, however, may be adjusted with considerable freedom using just the $R_G$ resistor. In fact, $R_G$ may be a reactive network providing a very isolated shaping to the differential frequency response. Since the inverting inputs of the OPA2684 are very low impedance closed-loop buffer outputs, the $R_G$ element does not interact with the amplifier’s bandwidth, wide ranges of resistor values and/or filter elements may be inserted here with minimal amplifier bandwidth interaction.

Various combinations of single-supply or AC-coupled gain can also be delivered using the basic circuit of Figure 5. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of 1 since an equal DC voltage at each inverting node creates no current through $R_G$. This circuit does show a common-mode gain of 1 from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is problem, the output interface may also be used to reject that common-mode. For instance, most modern differential input ADC’s reject common-mode signals very well while a line driver application through a transformer will also attenuate the common-mode signal through to the line.

Figure 6 shows a differential I/O stage configured as an inverting amplifier. In this case, the gain resistors ($R_G$) become part of the input resistance for the source. This provides a better noise performance than the noninverting configuration but does limit the flexibility in setting the input impedance separately from the gain.

The two noninverting inputs provide an easy common-mode control input. This is particularly easy if the source is AC-coupled through either blocking caps or a transformer. In either case, the common-mode input voltages on the two noninverting inputs again have a gain of 1 to the output pins giving particularly easy common-mode control for single-supply operation. The OPA2684 used in this configuration does constrain the feedback to the 800Ω region for best frequency response. With $R_F$ fixed, the input resistors may be adjusted to the desired gain but will also be changing the input impedance as well. The high frequency common-mode gain for this circuit from input to output will be the same as for the signal gain. Again, if the source might include an undesired common-mode signal, that could be rejected at the input using blocking caps (for low frequency and DC common-mode) or a transformer coupling.

**DC-COUPLED SINGLE TO DIFFERENTIAL CONVERSION**

The previous differential output circuits were set up to receive a differential input as well. A simple way to provide a DC-coupled single to differential conversion using a dual op amp is shown in Figure 7. Here, the output of the first stage is simply inverted by the second to provide an inverting version of a single amplifier design. This approach works well for lower frequencies but will start to depart from ideal differential outputs as the propagation delay and distortion of the inverting stage adds significantly to that present at the noninverting output pin.

The circuit of Figure 7 is set up for a single-ended gain of 6 to the output of the first amplifier then an inverting gain of $-1$ through the second stage to provide a total differential gain of 12. See Figure 8 for the SSBW for the circuit of Figure 7. Large-signal distortion at 12Vp-p output into the 100Ω differential load is $\leq 80$dBc.
DIFFERENTIAL ACTIVE FILTER

The OPA2684 can provide a very capable gain block for low-power active filters. The dual design lends itself very well to differential active filters. Where the filter topology is looking for a simple gain function to implement the filter, the noninverting configuration is preferred to isolate the filter elements from the gain elements in the design. Figure 9 shows an example of a very low power 10MHz 3rd-order Butterworth low-pass Sallen-Key filter. Often, these filters are designed at an amplifier gain of 1 to minimize amplifier bandwidth interaction with the desired filter shape. Since the OPA2684 shows minimal bandwidth change with gain, this would not be a constraint in this design. The example of

Figure 9 designs the filter for a differential gain of 5 using the OPA2684. The resistor values have been adjusted slightly to account for the amplifier bandwidth effects.

While this circuit is bipolar, using ±5V supplies, it can easily be adapted to single-supply operation. This is typically done by providing a supply midpoint reference at the noninverting inputs then adding DC blocking caps at each input and in series with the amplifier gain resistor, RG. This will add two real zeroes in the response transforming the circuit into a bandpass. Figure 10 shows the frequency response for the filter of Figure 9.

FIGURE 8. Small-Signal Bandwidth for Figure 7.


FIGURE 10. Frequency Response for 10MHz, 3rd-Order Butterworth Low-Pass Filter.

**SINGLE-SUPPLY, HIGH GAIN DIFFERENTIAL ADC DRIVER**

Where a very low power differential I/O interface to a moderate performance ADC is required, the circuit of Figure 11 may be considered. The circuit builds on the inverting differential I/O configuration of Figure 6 by adding the input transformer and the output low-pass filter. The input transformer provides a single-to-differential conversion where the input signal is still very low power—it also provides a gain of 2 and removes any common-mode signal from the inputs. This single +5V design sets a midpoint bias from the supply at each of the noninverting inputs.

This circuit also includes optional 500Ω pull-down resistors at the output. With a 2.5V DC common-mode operating point (set by $V_{CM}$), this will add 5mA to ground in the output stage. This essentially powers up the NPN side of the output stage significantly reducing distortion. It is important for good 2nd-order distortion to connect the grounds of these two resistors at the same point to minimize ground plane current for the differential output signal. Figure 12 shows the measured 2nd- and 3rd-harmonic distortion for the circuit of Figure 11 with and without the pull-down resistors.

Less than −65dBc distortion is possible through 5MHz without the pull-down current while this extends to 10MHz using the two 500Ω pull-down resistors.

**SYNTHETIC IMPEDANCE DSL LINE DRIVER**

The need for very low power DSL line drivers is well supported by the OPA2684 with its high (> 100mA) output current, low (< 1.2V) headroom, and low supply current (3.4mA). To further improve power efficiency, simple differential line drivers are often modified to produce a portion of the output impedance through positive feedback. This reduces the voltage swing loss in the remaining discrete matching resistor leaving more of the available voltage swing at the input of the transformer. This typically will allow the transformer turns ratio to be reduced, reducing the peak output current required. All of this together can reduce the power dissipated in the line driver while delivering a low distortion DSL signal to the line.

[FIGURE 12. Measured Harmonic Distortion for the Circuit of Figure 11.]

See Figure 13 for an example design for a +12V single-supply SHDSL4 line driver where only 27% of the output impedance is implemented with the physical (18.2Ω) output resistors with the remaining 73% implemented with positive feedback. This synthetic output impedance circuit feeds back the transformer input voltage to the opposite inverting nodes.

FIGURE 13. Synthetic Output Impedance xDSL Driver.

This example takes a 2Vp-p maximum differential input to a 12.67Vp-p maximum differential voltage on a 135Ω line using a 1:1 transformer. For a nominal line at maximum target power, each output swings a maximum 8Vp-p delivering a peak 47mA current, on a 12V supply this leaves 2V headroom on each output with a total amplifier power dissipation of 163mW. Figure 14 shows the distortion for a full scale (12.67Vp-p on the line) and 1/2 scale sinusoid signal from 100kHz to 1MHz.

FIGURE 14. Harmonic Distortion for Figure 13.

**DESIGN-IN TOOLS**

**DEMONSTRATION FIXTURES**

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2684 in its two package styles. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

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<td>DEM-OPA-SO-2A</td>
<td>SBOU003</td>
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<td>OPA2684IDCN</td>
<td>SOT23-8</td>
<td>DEM-OPA-SOT-2A</td>
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</tbody>
</table>

**TABLE I. Demonstration Fixtures by Package.**

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2684 product folder.

**MACROMODELS**

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for higher speed designs where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2684 is available in the product folder on the TI web site (www.ti.com). This is the single channel model for the OPA684—simply use two of these to implement an OPA2684 simulation. These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

**OPERATING SUGGESTIONS**

**SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH**

Any current-feedback op amp like the OPA2684 can hold high bandwidth over signal-gain settings with the proper adjustment of the external resistor values. A low-power part like the OPA4684 typically shows a larger change in bandwidth due to the significant contribution of the inverting input impedance to loop-gain changes as the signal gain is changed. Figure 15 shows a simplified analysis circuit for any current-feedback amplifier.

**FIGURE 15. Current-Feedback Transfer Function Analysis Circuit.**
The key elements of this current-feedback op amp model are:

- $\alpha \Rightarrow$ Buffer gain from the noninverting input to the inverting input
- $R_I \Rightarrow$ Buffer output impedance
- $i_{ERR} \Rightarrow$ Feedback error current signal
- $Z(s) \Rightarrow$ Frequency dependent open-loop transimpedance gain from $i_{ERR}$ to $V_O$

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For the buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log(1 - \alpha)$. The closed-loop input stage buffer used in the OPA2684 gives a buffer gain more closely approaching 1.00 and this shows up in a slightly higher CMRR than previous current-feedback op amps.

$R_I$, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA2684 reduces this element to approximately 4.0Ω using the loop gain of the closed-loop input stage buffer. This significant reduction in output impedance, on very low power, contributes significantly to extending the bandwidth at higher gains.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 15 gives Equation 1:

$$\frac{V_O}{V_I} = \frac{\alpha}{1 + \frac{R_F}{R_G} \left(1 + \frac{R_F + R_I}{R_G}\right)} = \frac{\alpha \text{NG}}{1 + \frac{R_F + R_I \text{NG}}{Z(s)}} \left[\text{NG} = \left(1 + \frac{R_F}{R_G}\right)^\prime\right]$$

This is written in a loop-gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If $Z(s)$ were infinite over all frequencies, the denominator of Equation 1 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 1 determines the frequency response. Equation 2 shows this as the loop-gain equation.

$$\frac{Z(s)}{R_F + R_I \text{NG}} = \text{Loop Gain}$$

If $20 \cdot \log(R_F + \text{NG} \cdot R_I)$ were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, $Z(s)$ rolls off to equal the denominator of Equation 2, at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier’s closed-loop frequency response given by Equation 1 will start to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 2 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA2684 is internally compensated to give a maximally flat frequency response for $R_F = 800\Omega$ at NG = 2 on ±5V supplies. That optimum value goes to 1.0kΩ on a single +5V supply. Normally, with a current-feedback amplifier, it is possible to adjust the feedback resistor to hold this bandwidth up as the gain is increased. The CFBPLUS architecture has reduced the contribution of the inverting input impedance to provide exceptional bandwidth to higher gains without adjusting the feedback resistor value. The Typical Characteristics show the small-signal bandwidth over gain with a fixed feedback resistor.

Putting a closed-loop buffer between the noninverting and inverting inputs does bring some added considerations. Since the voltage at the inverting output node is now the output of a locally closed-loop buffer, parasitic external capacitance on this node can cause frequency response peaking for the transfer function from the noninverting input voltage to the inverting node voltage. While it is always important to keep the inverting node capacitance low for any current-feedback op amp, it is critically important for the OPA2684. External layout capacitance in excess of 2pF will start to peak the frequency response. This peaking can be easily reduced by then increasing the feedback resistor value—but it is preferable, from a noise and dynamic range standpoint, to keep that capacitance low, allowing a close to nominal 800Ω feedback resistor for flat frequency response. Very high parasitic capacitance values on the inverting node (> 5pF) can possibly cause input stage oscillation that cannot be filtered by a feedback element adjustment.

An added consideration is that at very high gains, 2nd-order effects in the inverting output impedance cause the overall response to peak up. If desired, it is possible to retain a flat frequency response at higher gains by adjusting the feedback resistor to higher values as the gain is increased. Since the exact value of feedback that will give a flat frequency response at high gains depends strongly in inverting and output node parasitic capacitance values, it is best to experiment in the specific board with increasing values until the desired flatness (or pulse response shape) is obtained. In general, increasing $R_F$ (and adjusting $R_G$ then to the desired gain) will move towards flattening the response, while decreasing it will extend the bandwidth at the cost of some peaking. The OPA684 data sheet gives an example of this optimization of $R_F$ versus Gain.

**OUTPUT CURRENT AND VOLTAGE**

The OPA2684 provides output voltage and current capabilities that can support the needs of driving doubly-terminated 50Ω lines. For a 1000Ω load at the gain of +2, (see Figure 1), the total load is the parallel combination of the 100Ω load and
the 1.6kΩ total feedback network impedance. This 94Ω load will require no more than 40mA output current to support the ±3.8V minimum output voltage swing specified for 100Ω loads. This is well under the specified minimum +120/–90mA specifications over the full temperature range.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the Output Voltage and Current Limitations plot in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2684’s output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, their junction temperatures will increase, decreasing their VBE’s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8 pin packages) can destroy the amplifier. If additional short-circuit protection is required, consider a small-series resistor in the power-supply leads. This will, under heavy output loads, reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short-circuit, while decreasing the available output voltage swing only 0.25V for up to 50mA desired load currents. Always place the 0.1µF power-supply decoupling capacitors after these supply current limiting resistors directly on the supply pins.

**DRIVING CAPACITIVE LOADS**

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC, including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high-open-loop gain amplifier like the OPA2684 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier’s open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended $R_S$ vs $C_{LOAD}$ and the resulting frequency response at the load. The 1kΩ resistor shown in parallel with the load capacitor is a measurement path and may be omitted. The required series resistor value may be reduced by increasing the feedback resistor value from its nominal recommended value. This will increase the phase margin for the loop gain, allowing a lower series resistor to be effective in reducing the peaking due capacitive load. SPICE simulation can be effectively used to optimize this approach. Parasitic capacitive loads greater than 5pF can begin to degrade the performance of the OPA2684. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2684 output pin (see Board Layout Guidelines).

**DISTORTION PERFORMANCE**

The OPA2684 provides very low distortion in a low-power part. The CFBPLUS architecture also gives two significant areas of distortion improvement. First, in operating regions where the 2nd-harmonic distortion due to output stage nonlinearities is very low (frequencies < 1MHz, low output swings into light loads) the linearization at the inverting node provided by the CFBPLUS design gives 2nd-harmonic distortions that extend into the –90dBc region. Previous current-feedback amplifiers have been limited to approximately –85dBc due to the nonlinearities at the inverting input. The second area of distortion improvement comes in a distortion performance that is largely gain independent. To the extent that the distortion at a particular output power is output stage dependent, 3rd-harmonics particularly, and to a lesser extend 2nd-harmonic distortion, is constant as the gain is increased. This is due to the constant loop gain versus signal gain provided by the CFBPLUS design. As shown in the Typical Characteristics, while the 3rd-harmonic is constant with gain, the 2nd-harmonic degrades at higher gains. This is largely due to board parasitic issues. Slightly imbalanced load return currents will couple into the gain resistor to cause a portion of the 2nd-harmonic distortion. At high gains, this imbalance has more gain to the output giving increased 2nd-harmonic distortion.

Relative to alternative amplifiers with < 2mA supply current, the OPA2684 holds much lower distortion at higher frequencies (> 5MHz) and to higher gains. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a
lower 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 1) this is the sum of \( R_F + R_G \), while in the inverting configuration it is just \( R_F \). Also, providing an additional supply decoupling capacitor (0.1\( \mu \)F) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. A low-power part like the OPA2684 includes quiescent boost circuits to provide the full-power bandwidth shown in the Typical Characteristics. These act to increase the bias in a very linear fashion only when high slew rate or output power are required. This also acts to actually reduce the distortion slightly at higher output power levels. The Typical Characteristics show the 2nd-harmonic holding constant from 500mVp-p to 5Vp-p outputs while the 3rd-harmonics actually decrease with increasing output power.

The OPA2684 has an extremely low 3rd-order harmonic distortion, particularly for light loads and at lower frequencies. This also gives low 2-tone, 3rd-order intermodulation distortion as shown in the Typical Characteristics. Since the OPA2684 includes internal power boost circuits to retain good full-power performance at high frequencies and outputs, it does not show a classical 2-tone, 3rd-order intermodulation intercept characteristic. Instead, it holds relatively low and constant 3rd-order intermodulation spurious levels over power. The Typical Characteristics show this spurious level as a dBC below the carrier at fixed center frequencies swept over single-tone power at a matched 50Ω load. These spurious levels drop significantly (> 12dB) for lighter loads than the 100Ω used in that plot. Converter inputs for instance will see ≤ 82dBc 3rd-order spurious to 10MHz for full-scale inputs. For even lower 3rd-order intermodulation distortion to much higher frequencies, consider the OPA2691.

**NOISE PERFORMANCE**

Wideband current-feedback op amps generally have a higher output noise than comparable voltage-feedback op amps. The OPA2684 offers an excellent balance between voltage and current noise terms to achieve low output noise in a low power amplifier. The inverting current noise (17pA/\( \sqrt{\text{Hz}} \)) is lower most other current-feedback op amps while the input voltage noise (3.7nV/\( \sqrt{\text{Hz}} \)) is lower than any unity-gain stable, comparable slew rate, voltage-feedback op amp. This low input voltage noise was achieved at the price of higher noninverting input current noise (9.4pA/\( \sqrt{\text{Hz}} \)). As long as the AC source impedance looking out of the noninverting node is less than 200Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 16 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/\( \sqrt{\text{Hz}} \) or pA/\( \sqrt{\text{Hz}} \).

![Figure 16. Op Amp Noise Analysis Model.](image-url)

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 3 shows the general form for the output noise voltage using the terms shown in Figure 16.

\[
E_O = \sqrt{E_{NI}^2 + (IBN R_S)^2 + 4kT R_S NG^2 + (IBF R_F)^2 + 4kT R_F NG}
\]

Dividing this expression by the noise gain (\( NG = (1 + R_F/R_G) \)) will give the equivalent input referred spot noise voltage at the noninverting input as shown in Equation 4.

\[
E_N = \sqrt{E_{NI}^2 + (IBN R_S)^2 + 4kT R_S + \left(\frac{IBF R_F}{NG}\right)^2 + 4kT R_F NG}
\]

Evaluating these two equations for the OPA2684 circuit and component values (see Figure 1) will give a total output spot noise voltage of 16.3nV/\( \sqrt{\text{Hz}} \) and a total equivalent input spot noise voltage of 8.2 nV/\( \sqrt{\text{Hz}} \). This total input referred spot noise voltage is higher than the 3.7nV/\( \sqrt{\text{Hz}} \) specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. As the gain is increased, this fixed output noise power term contributes less to the total output noise and the total input referred voltage noise given by Equation 4 will approach just the 3.7nV/\( \sqrt{\text{Hz}} \) of the op amp itself. For example, going to a gain of +20 in the circuit of Figure 1, adjusting only the gain resistor to 42.1Ω, will give a total input referred noise of 3.9nV/\( \sqrt{\text{Hz}} \). A more complete description of op amp noise analysis can be found in TI application note AB-103, “Noise Analysis for High-Speed Op Amps” (SBOA066), located at www.ti.com.

**DC ACCURACY AND OFFSET CONTROL**

A current-feedback op amp like the OPA2684 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high slew rate voltage-feedback amplifiers. The two input bias currents,
THERMAL ANALYSIS

The OPA2684 will not require external heatsinking for most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by T_A + P_D * θ_JA. The total internal power dissipation (P_D) is the sum of quiescent power (P_DQ) and additional power dissipated in the output stage (P_DL) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_DL will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition P_DL = V_S^2/(4 * R_L) where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an absolute worst-case example, compute the maximum T_J using an OPA2684IDCN (SOT23-8 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C with both outputs driving a grounded 100Ω load to 2.5V_DC.

P_D = 10V * 3.9mA + 2 * (5Ω^2 / (4 * (100Ω || 1.6kΩ))) = 172mW

Maximum T_J = +85°C + (0.172W * 150°C/W) = 111°C

This maximum operating junction temperature is well below most system level targets. Most applications will be lower than this since an absolute worst-case output stage power in both channels simultaneously was assumed in this calculation.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2684 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken anywhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.01µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA2684. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing its value will reduce the peaking at higher gains, while decreasing it will give a more peaked frequency response at lower gains. The 800Ω feedback resistor used in the Electrical Characteristics at a gain of +2 on ±5V supplies is a good starting point for design. Note that an 800Ω feedback resistor, rather than a direct short, is required for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.
d) Connections to other wideband devices on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set Rs from the plot of recommended Rs vs CLOAD. Low parasitic capacitive loads (< 5pF) may not need an Rs since the OPA2684 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact a higher impedance environment will improve distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2684 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2684 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Rs vs CLOAD. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2684 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2684 onto the board.

INPUT AND ESD PROTECTION

The OPA2684 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table where an absolute maximum 13V across the supply pins is reported. All device pins have limited ESD protection using internal diodes to the power supplies as shown in Figure 17.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2684), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

FIGURE 17. Internal ESD Protection.
## Revision History

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<tr>
<td>7/08</td>
<td>D</td>
<td>2</td>
<td>Abs Max Ratings</td>
<td>Changed Storage Temperature Range from −40°C to +125°C to −65°C to +125°C.</td>
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<td></td>
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<td>3, 4</td>
<td>Electrical Characteristics, Power Supply</td>
<td>Added minimum supply voltage. Changed min and max quiescent current values from total to per channel.</td>
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<tr>
<td>5/06</td>
<td>C</td>
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## PACKAGING INFORMATION

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(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO-178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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