OPAx355 200-MHz CMOS Operational Amplifiers With Shutdown

1 Features
- Unity-Gain Bandwidth: 450 MHz
- Wide Bandwidth: 200 MHz GBW
- Low Noise: 5.8 nV/√Hz
- Excellent Video Performance
  - Differential Gain: 0.02%
  - Differential Phase: 0.05°
  - 0.1-dB Gain Flatness: 75 MHz
- Input Range Includes Ground
- Rail-to-Rail Output (within 100 mV)
- Low Input Bias Current: 3 pA
- Low Shutdown Current: 3.4 µA
- Enable and Disable Time: 100 ns and 30 ns
- Thermal Shutdown
- Single-Supply Operating Range: 2.5 V to 5.5 V
- MicroSIZE Packages

2 Applications
- Video Processing
- Ultrasound
- Optical Networking, Tunable Lasers
- Photodiode Transimpedance Amplifiers
- Active Filters
- High-Speed Integrators
- Analog-to-Digital Converter (ADC) Input Buffers
- Digital-to-Analog Converter (DAC) Output Amplifiers
- Barcode Scanners
- Communications

3 Description
The OPA355 series of high-speed, voltage-feedback CMOS operational amplifiers are designed for video and other applications requiring wide bandwidth. The OPA355 series is unity-gain stable and can drive large output currents. In addition, the OPAx355 series has a digital shutdown (enable) function. This feature provides power saving during idle periods and places the output in a high-impedance state to support output multiplexing. The differential gain is 0.02% and the differential phase is 0.05°. The quiescent current is 8.3 mA per channel.

The OPAx355 series is optimized for operation on single supply or dual supplies as low as 2.5 V (±1.25 V) and up to 5.5 V (±2.75 V). The common-mode input range for the OPAx355 series extends 100 mV below ground and up to 1.5 V from V+. The output swing is within 100 mV of the rails, supporting wide dynamic range.

The OPAx355 series is available in single (SOT-23-6 and SO-8), dual (VSSOP-10), and triple (TSSOP-14 and SO-14) versions. Multichannel versions feature completely independent circuitry for lowest crosstalk and freedom from interaction. All packages are specified from –40°C to +125°C.

### Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA355</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>SOT-23 (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
<tr>
<td>OPA2355</td>
<td>VSSOP (10)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
<tr>
<td>OPA3355</td>
<td>SOIC (14)</td>
<td>8.65 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (14)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
Table of Contents

1 Features ................................................................. 1
2 Applications .......................................................... 1
3 Description .......................................................... 1
4 Revision History ....................................................... 2
5 Device Comparison Table ........................................... 3
6 Pin Configuration and Functions ............................... 4
7 Specifications ......................................................... 7
   7.1 Absolute Maximum Ratings ................................. 7
   7.2 ESD Ratings .................................................. 7
   7.3 Recommended Operating Conditions ..................... 7
   7.4 Thermal Information: OPA355 .............................. 8
   7.5 Thermal Information: OPA2355 .............................. 8
   7.6 Thermal Information: OPA3355 .............................. 8
   7.7 Electrical Characteristics: V_S ............................. 9
      = 2.7 V to 5.5 V (Single-Supply) ......................... 
   7.8 Typical Characteristics ...................................... 11
8 Detailed Description ............................................... 16
   8.1 Overview ...................................................... 16
   8.2 Functional Block Diagram .................................... 16
8.3 Feature Description ............................................... 16
8.4 Device Functional Modes ....................................... 17
9 Application and Implementation ............................. 18
   9.1 Application Information ..................................... 18
   9.2 Typical Applications ......................................... 18
   9.3 Video ........................................................ 22
   9.4 Wideband Video Multiplexing .............................. 23
10 Power Supply Recommendations ............................ 25
11 Layout ................................................................. 25
   11.1 Layout Guidelines .......................................... 25
   11.2 Layout Example ............................................ 25
12 Device and Documentation Support ......................... 26
   12.1 Related Links ................................................ 26
   12.2 Receiving Notification of Documentation Updates ....... 26
   12.3 Community Resources ..................................... 26
   12.4 Trademarks .................................................. 26
   12.5 Electrostatic Discharge Caution ......................... 26
   12.6 Glossary .................................................... 26
13 Mechanical, Packaging, and Orderable Information ....... 27

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (January 2004) to Revision E

- Updated data sheet to latest TIS documentation and translation standards ............................................... 1
- Changed pin type typo from MSOP to VSSOP in Description section ................................................. 1
- Added Device Information table ............................................................................................................. 1
- Deleted the Absolute Maximum Ratings table note: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less. .................. 7
- Added ESD Ratings table ......................................................................................................................... 7
- Added Recommended Operating Conditions table ..................................................................................... 7
- Added Thermal Information tables ......................................................................................................... 8
- Changed pin type typo from MSOP to VSSOP in Electrical Characteristics section .............................. 10
- Deleted the test conditions statement from Typical Characteristics graphs and moved the conditions to tablenotes below the graphs ................................................................. 11
- Added Detailed Description section ......................................................................................................... 16
- Added Functional Block Diagram graphic ............................................................................................... 16
- Deleted Input and ESD Protection section ............................................................................................... 16
- Added Application and Implementation section ....................................................................................... 18
- Deleted Internal ESD Protection application ........................................................................................... 18
- Added Power Supply Recommendations section .................................................................................... 25
- Added Layout Guidelines section ........................................................................................................... 25
## 5 Device Comparison Table

<table>
<thead>
<tr>
<th>OPAx355 RELATED PRODUCTS</th>
<th>FEATURES</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA356</td>
<td>200-MHz, Rail-to-Rail Output, CMOS, No Shutdown</td>
</tr>
<tr>
<td>OPAx350</td>
<td>38-MHz, Rail-to-Rail Input and Output, CMOS</td>
</tr>
<tr>
<td>OPAx631</td>
<td>75-MHz, Rail-to-Rail Output</td>
</tr>
<tr>
<td>OPAx634</td>
<td>150-MHz, Rail-to-Rail Output</td>
</tr>
<tr>
<td>THS412x</td>
<td>Differential Input and Output, 3.3-V Supply</td>
</tr>
</tbody>
</table>
6 Pin Configuration and Functions

OPA355 DBV Package
6-Pin SOT-23
Top View

OPA355 D Package
8-Pin SOIC
Top View

(1) Pin 1 of the SOT-23-6 is determined by orienting the package marking as indicated in the diagram.

(2) NC - no internal connection

Pin Functions: OPA355

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>SOT-23</td>
<td>SOIC</td>
</tr>
<tr>
<td>ENABLE</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>IN−</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>1.5</td>
</tr>
<tr>
<td>OUT</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>V+</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>V−</td>
<td>2</td>
<td>4</td>
</tr>
</tbody>
</table>
## Pin Functions: OPA2355

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td></td>
</tr>
</tbody>
</table>
| ENABLE A       | 5   | — Amplifier power down, channel A.  
                      |     | Low = disabled, high = normal operation (pin must be driven) |
| ENABLE B       | 6   | — Amplifier power down, channel B.  
                      |     | Low = disabled, high = normal operation (pin must be driven) |
| +IN A          | 3   | I Noninverting input pin, channel A            |
| +IN B          | 7   | I Noninverting input pin, channel B            |
| –IN A          | 2   | I Inverting input pin, channel A              |
| –IN B          | 8   | I Inverting input pin, channel B              |
| OUT A          | 1   | O Output pin, channel A                       |
| OUT B          | 9   | O Output pin, channel B                       |
| V+             | 10  | — Positive power supply                        |
| V−             | 4   | — Negative power supply                        |
Pin Functions: OPA3355

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENABLE A</td>
<td>1</td>
<td>—</td>
<td>Amplifier power down, channel A. Low = disabled, high = normal operation (pin must be driven)</td>
</tr>
<tr>
<td>ENABLE B</td>
<td>2</td>
<td>—</td>
<td>Amplifier power down, channel B. Low = disabled, high = normal operation (pin must be driven)</td>
</tr>
<tr>
<td>ENABLE C</td>
<td>3</td>
<td>—</td>
<td>Amplifier power down, channel C. Low = disabled, high = normal operation (pin must be driven)</td>
</tr>
<tr>
<td>+IN A</td>
<td>5</td>
<td>I</td>
<td>Noninverting input pin, channel A</td>
</tr>
<tr>
<td>+IN B</td>
<td>10</td>
<td>I</td>
<td>Noninverting input pin, channel B</td>
</tr>
<tr>
<td>+IN C</td>
<td>12</td>
<td>I</td>
<td>Noninverting input pin, channel C</td>
</tr>
<tr>
<td>−IN A</td>
<td>6</td>
<td>I</td>
<td>Inverting input pin, channel A</td>
</tr>
<tr>
<td>−IN B</td>
<td>9</td>
<td>I</td>
<td>Inverting input pin, channel B</td>
</tr>
<tr>
<td>−IN C</td>
<td>13</td>
<td>I</td>
<td>Inverting input pin, channel C</td>
</tr>
<tr>
<td>OUT A</td>
<td>7</td>
<td>O</td>
<td>Output, channel A</td>
</tr>
<tr>
<td>OUT B</td>
<td>8</td>
<td>O</td>
<td>Output channel B</td>
</tr>
<tr>
<td>OUT C</td>
<td>14</td>
<td>O</td>
<td>Output, channel C</td>
</tr>
<tr>
<td>V+</td>
<td>4</td>
<td>—</td>
<td>Positive power supply</td>
</tr>
<tr>
<td>V−</td>
<td>11</td>
<td>—</td>
<td>Negative power supply</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V+ to V–</td>
<td></td>
<td>7.5</td>
<td>V</td>
</tr>
<tr>
<td>Signal input terminals</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage</td>
<td>(V–) – 0.5</td>
<td>(V+) + 0.5</td>
<td>V</td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Output short circuit(2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating temperature</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction temperature</td>
<td></td>
<td>160</td>
<td>°C</td>
</tr>
<tr>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>300</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature range, Tstg</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses above Absolute Maximum Ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDAJEDEC JS-001(1)</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(2)</td>
<td>±250</td>
<td></td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

7.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vtotal supply voltage</td>
<td>2.7</td>
<td></td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Tambient temperature</td>
<td>–40</td>
<td>25</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>
### 7.4 Thermal Information: OPA355

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA355</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D (SOIC)</td>
<td>DBV (SOT-23)</td>
</tr>
<tr>
<td></td>
<td>8 PINS</td>
<td>6 PINS</td>
</tr>
<tr>
<td>$R_{JA}$ Junction-to-ambient thermal resistance</td>
<td>136.3</td>
<td>166.1  °C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>76.7</td>
<td>104.3  °C/W</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>79.8</td>
<td>38.7   °C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>26.3</td>
<td>23.4   °C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>79</td>
<td>38.5   °C/W</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>—</td>
<td>—      °C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 7.5 Thermal Information: OPA2355

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA2355</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DGS (VSSOP)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 PINS</td>
<td></td>
</tr>
<tr>
<td>$R_{JA}$ Junction-to-ambient thermal resistance</td>
<td>171.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>58</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>92.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>6.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>91.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>—</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

### 7.6 Thermal Information: OPA3355

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA3355</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>D (SOIC)</td>
<td>PW (TSSOP)</td>
</tr>
<tr>
<td></td>
<td>14 PINS</td>
<td>14 PINS</td>
</tr>
<tr>
<td>$R_{JA}$ Junction-to-ambient thermal resistance</td>
<td>85.3</td>
<td>113.3 °C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>41.4</td>
<td>38     °C/W</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>41.5</td>
<td>58.1   °C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>8.3</td>
<td>2.8    °C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>41.2</td>
<td>57.3   °C/W</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>—</td>
<td>—      °C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.7 Electrical Characteristics: \( V_S = 2.7 \text{ V to 5.5 V (Single-Supply)} \)

at \( T_A = 25^\circ \text{C}, R_F = 604 \Omega, R_L = 150 \Omega \), and connected to \( V_S / 2 \), (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OS} )</td>
<td>Input offset voltage</td>
<td>( V_S = 5 \text{ V} )</td>
<td>±2</td>
<td>±9</td>
<td>mV</td>
</tr>
<tr>
<td>( T_A = -40^\circ \text{C to } +125^\circ \text{C} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( dV_{OS}/dT )</td>
<td>Input offset voltage vs temperature</td>
<td>( T_A = -40^\circ \text{C to } +125^\circ \text{C} )</td>
<td>±7</td>
<td></td>
<td>µV/°C</td>
</tr>
<tr>
<td>Input offset voltage vs power supply</td>
<td></td>
<td></td>
<td>±80</td>
<td>±350</td>
<td>µV/V</td>
</tr>
</tbody>
</table>

INPUT BIAS CURRENT

\( I_B \) | Input bias current | 3 | ±50 | pA |
\( I_{OS} \) | Input offset current | ±1 | ±50 | pA |

NOISE

Input noise voltage density | \( f = 1 \text{ MHz} \) | 5.8 | | nV/√Hz |
Current noise density | \( f = 1 \text{ MHz} \) | 50 | | fA/√Hz |

INPUT VOLTAGE RANGE

\( V_{CM} \) | Common-mode voltage range | \( (V^-) - 0.1 \) | 66 | 80 | V |
\( (V^+) - 1.5 \) | | | | | |
\( V_S = 5.5 \text{ V} \), \( -0.1 \text{ V} < V_{CM} < 4 \text{ V} \) |
\( V_S = 5.5 \text{ V} \), \( -0.1 \text{ V} < V_{CM} < 4 \text{ V} \) |
| \( T_A = -40^\circ \text{C to } +125^\circ \text{C} \) | | | | | |
| CMRR | Common-mode rejection ratio | \( V_S = 5.5 \text{ V} \), \( -0.1 \text{ V} < V_{CM} < 4 \text{ V} \) | 66 | | dB |
| \( T_A = -40^\circ \text{C to } +125^\circ \text{C} \) | | | | | |

INPUT IMPEDANCE

Differential | | | | | |
| Common-mode | | | | | |

OPEN-LOOP GAIN

Open-loop gain | | 84 | 92 | dB |
\( V_S = 5 \text{ V} \), \( 0.3 \text{ V} < V_O < 4.7 \text{ V} \) |
\( \text{OPA355: } V_S = 5 \text{ V} \), \( 0.3 \text{ V} < V_O < 4.7 \text{ V} \) |
\( T_A = -40^\circ \text{C to } +125^\circ \text{C} \) |
\( \text{OPA2355, OPA355: } V_S = 5 \text{ V} \), \( 0.4 \text{ V} < V_O < 4.6 \text{ V} \) |

FREQUENCY RESPONSE

\( f_{-3dB} \) | Small-signal bandwidth | \( G = 1, V_O = 100 \text{ mVp-p}, R_F = 0 \Omega \) | 450 | | MHz |
\( G = 2, V_O = 100 \text{ mVp-p}, R_L = 50 \Omega \) | 100 | | MHz |
\( G = 2, V_O = 100 \text{ mVp-p}, R_L = 150 \Omega \) | 170 | | MHz |
\( G = 2, V_O = 100 \text{ mVp-p}, R_L = 1 \text{ k} \Omega \) | 200 | | MHz |

\( GBW \) | Gain-bandwidth product | \( G = 10, R_L = 1 \text{ k} \Omega \) | 200 | | MHz |

\( f_{0.1dB} \) | Bandwidth for 0.1-dB gain flatness | \( G = 2, V_O = 100 \text{ mVp-p}, R_F = 560 \Omega \) | 75 | | MHz |

SR | Slew rate | \( V_S = 5 \text{ V}, G = 2, 4-V \text{ output step} \) | 300 / -360 | | V/µs |
Rise and fall time | \( G = 2, V_O = 200 \text{ Vp-p}, 10\% \text{ to } 90\% \) | 2.4 | | ns |
\( G = 2, V_O = 2 \text{ Vp-p}, 10\% \text{ to } 90\% \) | 8 | | ns |

Settling time | \( 0.1\%:\ V_S = 5 \text{ V}, G = 2, 2-V \text{ output step} \) | 30 | | ns |
\( 0.01\%:\ V_S = 5 \text{ V}, G = 2, 2-V \text{ output step} \) | 120 | | ns |

Overload recovery time | \( V_{IN} \times \text{gain} = V_S \) | 8 | | ns |

HARMONIC DISTORTION

Second harmonic | | | | | |
Third harmonic | | | | | |
Differential gain error | NTSC, \( R_L = 150 \Omega \) | 0.02 | | % |

Copyright © 2001–2018, Texas Instruments Incorporated
## Electrical Characteristics: \( V_S = 2.7 \text{ V} \) to 5.5 V (Single-Supply) (continued)

at \( T_A = 25^\circ\text{C} \), \( R_F = 604 \, \Omega \), \( R_L = 150 \, \Omega \), and connected to \( V_S / 2 \), (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential phase error</td>
<td>NTSC, ( R_L = 150 , \Omega )</td>
<td>0.05</td>
<td></td>
<td></td>
<td>°</td>
</tr>
<tr>
<td>Channel-to-channel crosstalk</td>
<td>OPA2355: ( f = 5 , \text{MHz} )</td>
<td>–90</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OPA3355: ( f = 5 , \text{MHz} )</td>
<td>–70</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### OUTPUT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage output swing from rail</td>
<td>( V_S = 5 , \text{V}, , R_L = 150 , \Omega, , A_{OL} &gt; 84 , \text{dB} )</td>
<td>0.2</td>
<td>0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_S = 5 , \text{V}, , R_L = 1 , \text{k} , \Omega )</td>
<td>0.1</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Continuous output current (1)</td>
<td></td>
<td>±60</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak output current (1)</td>
<td>( V_S = 5 , \text{V} )</td>
<td>±100</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_S = 3 , \text{V} )</td>
<td>±80</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Closed-loop output impedance (1)</td>
<td>( f &lt; 100 , \text{kHz} )</td>
<td>0.02</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

### POWER SUPPLY

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_S ) Specified voltage range</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Operating voltage range</td>
<td>2.5 to 5.5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( I_Q ) Quiescent current (per amplifier)</td>
<td>( V_S = 5 , \text{V}, , \text{enabled}, , I_O = 0 )</td>
<td>8.3</td>
<td>11</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>( T_A = -40^\circ\text{C} ) to ( +125^\circ\text{C} )</td>
<td>14</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

### SHUTDOWN

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disabled (logic-LOW threshold)</td>
<td>0.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Enabled (logic-HIGH threshold)</td>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable time</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Disable time</td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown current (per amplifier)</td>
<td>3.4</td>
<td>6</td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

### THERMAL SHUTDOWN

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction temperature</td>
<td>160</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Reset from shutdown</td>
<td>140</td>
<td></td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

### TEMPERATURE RANGE

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specified range</td>
<td>–40</td>
<td>125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating range</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage range</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>( \theta_J ) Thermal resistance</td>
<td>SOT-23-6, VSSOP-10</td>
<td>150</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SO-8</td>
<td>125</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SO-14, TSSOP-14</td>
<td>100</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

(1) See Output Voltage Swing vs Output Current.
7.8 Typical Characteristics

\( T_A = 25^\circ C, \, V_S = 5 \, V, \, G = 2, \, R_F = 604 \, \Omega, \) and \( R_L = 150 \, \Omega \) connected to \( V_S / 2, \) (unless otherwise noted)

---

**Figure 1. Noninverting Small-Signal Frequency Response**

**Figure 2. Inverting Small-Signal Frequency Response**

**Figure 3. Noninverting Small-Signal Step Response**

**Figure 4. Noninverting Large-Signal Step Response**

**Figure 5. Large-Signal Disable and Enable Response**

**Figure 6. 0.1-dB Gain Flatness for Various \( R_F \) Values**
Typical Characteristics (continued)

\[ T_A = 25^\circ C, V_S = 5\ V, G = 2, R_F = 604\ \Omega, \text{ and } R_L = 150\ \Omega \text{ connected to } V_S / 2, \text{ (unless otherwise noted)} \]

Figure 7. Harmonic Distortion vs Output Voltage

Figure 8. Harmonic Distortion vs Noninverting Gain

Figure 9. Harmonic Distortion vs Inverting Gain

Figure 10. Harmonic Distortion vs Frequency

Figure 11. Harmonic Distortion vs Load Resistance

Figure 12. Input Voltage and Current Noise Spectral Density vs Frequency
Typical Characteristics (continued)

\( T_A = 25^\circ \text{C}, \ V_S = 5 \text{ V}, \ G = 2, \ R_C = 604 \ \Omega, \) and \( R_L = 150 \ \Omega \) connected to \( V_S / 2, \) (unless otherwise noted)

\begin{figure} [h]
\centering
\includegraphics[width=0.4\textwidth]{figure13}
\caption{Frequency Response for Various \( R_L \) Values}
\end{figure}

\begin{figure} [h]
\centering
\includegraphics[width=0.4\textwidth]{figure14}
\caption{Frequency Response for Various \( C_L \) Values}
\end{figure}

\begin{figure} [h]
\centering
\includegraphics[width=0.4\textwidth]{figure15}
\caption{Recommended \( R_S \) Values vs Capacitive Load}
\end{figure}

\begin{figure} [h]
\centering
\includegraphics[width=0.4\textwidth]{figure16}
\caption{Frequency Response vs Capacitive Load}
\end{figure}

\begin{figure} [h]
\centering
\includegraphics[width=0.4\textwidth]{figure17}
\caption{Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency}
\end{figure}

\begin{figure} [h]
\centering
\includegraphics[width=0.4\textwidth]{figure18}
\caption{Open-Loop Gain and Phase}
\end{figure}
## Typical Characteristics (continued)

$T_A = 25°C$, $V_S = 5$ V, $G = 2$, $R_C = 604$ $\Omega$, and $R_L = 150$ $\Omega$ connected to $V_S / 2$, (unless otherwise noted)

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Shutdown Current (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>65</td>
<td>85</td>
</tr>
<tr>
<td>105</td>
<td>55</td>
</tr>
<tr>
<td>25</td>
<td>45</td>
</tr>
<tr>
<td>135</td>
<td>125 – 55</td>
</tr>
<tr>
<td>45</td>
<td>– 35</td>
</tr>
<tr>
<td>25</td>
<td>– 15</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.5</td>
</tr>
<tr>
<td>4.0</td>
</tr>
<tr>
<td>3.5</td>
</tr>
<tr>
<td>3.0</td>
</tr>
<tr>
<td>2.5</td>
</tr>
<tr>
<td>2.0</td>
</tr>
<tr>
<td>1.5</td>
</tr>
<tr>
<td>1.0</td>
</tr>
<tr>
<td>0.5</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

$V = 5$ V

$V = 3$ V

$V = 5.5$ V

$V = 2.5$ V

---

### Figure 19. Composite Video Differential Gain and Phase

![Composite Video Differential Gain and Phase](image)

### Figure 20. Input Bias Current vs Temperature

![Input Bias Current vs Temperature](image)

Continuous currents above 60 mA are not recommended

$V_S = 3$ V

### Figure 21. Output Voltage Swing vs Output Current

![Output Voltage Swing vs Output Current](image)

Continuous currents above 60 mA are not recommended

$V_S = 5$ V

### Figure 22. Supply Current vs Temperature

![Supply Current vs Temperature](image)

### Figure 23. Output Voltage Swing vs Output Current

![Output Voltage Swing vs Output Current](image)

### Figure 24. Shutdown Current vs Temperature

![Shutdown Current vs Temperature](image)
Typical Characteristics (continued)

\( T_A = 25^\circ C, \ V_S = 5 \text{ V}, \ G = 2, \ R_C = 604 \ \Omega, \) and \( R_L = 150 \ \Omega \) connected to \( V_S / 2, \) (unless otherwise noted)

![Graphs and charts showing typical characteristics of OPA355, OPA2355, OPA3355 amplifiers.](image-url)

Figure 25. Closed-Loop Output Impedance vs Frequency

Figure 26. Maximum Output Voltage vs Frequency

Figure 27. Output Settling Time to 0.1%

Figure 28. Open-Loop Gain vs Temperature

Figure 29. Offset Voltage Production Distribution

Figure 30. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature
8 Detailed Description

8.1 Overview

The OPA355 series is a CMOS, high-speed, voltage-feedback, operational amplifier designed for video and other general-purpose applications. The series is available as a single, dual, or triple op amp. The family features a 200-MHz gain bandwidth and 360 V/µs slew rate, but the series is unity-gain stable and can operate as a 1 V/V voltage follower.

The input common-mode range includes ground, allowing the OPAx355 family to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Operating Voltage

The OPAx355 family is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 to ±2.75 V). However, the supply voltage ranges from 2.5 to 5.5 V (±1.25 to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

8.3.2 Enable Function

The OPAx355 series is enabled by applying a TTL high-voltage level to the enable pin. Conversely, a TTL low-voltage level disables the amplifier, which reduces the supply current from 8.3 mA to 3.4 µA per amplifier. This pin voltage is referenced to a single-supply ground. When using a split-supply, such as ±2.5 V, the enable and disable voltage levels are referenced to V–. For portable battery-operated applications, this feature greatly reduces the average current and as a result, extends battery life.

The enable input is modeled as a CMOS input gate with a 100-kΩ pullup resistor to V+. The enable pin assumes a logic high and the amplifier turns on if the enable pin is left open.
Feature Description (continued)

The enable time is 100 ns and the disable time is 30 ns, which allows the OPAx355 series to operate as a gated amplifier, or to have the output multiplexed onto a common output bus. When disabled, the output assumes a high-impedance state.

8.3.3 Output Drive

The output stage supplies a high short-circuit current (typically over 200 mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPAx355 series from dangerously-high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

NOTE

Running a continuous DC current in excess of ±60 mA is not recommended. See the Output Voltage Swing vs Output Current graphs (Figure 21 and Figure 22) in the Typical Characteristics section.

8.4 Device Functional Modes

The OPAx355 family is powered on when the supply is connected. The series operates as a single supply operational amplifier or dual supply amplifier depending on the application. The series is used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (example: V– set to –3.5 V and V+ set to 1.5 V).
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The OPAx355 series is a CMOS, high-speed, voltage-feedback, operational amplifier (op amp) designed for general-purpose applications.

The amplifiers feature a 200-MHz gain bandwidth and 300-V/μs slew rate, but the devices are unity-gain stable and operate as a 1-V/V voltage follower.

The input common-mode voltage range of the series includes ground, which allows the OPAx355 to be used in virtually any single-supply application up to a supply voltage of 5.5 V.

9.2 Typical Applications

9.2.1 Transimpedance Amplifier
Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx355 series a preferred wideband photodiode transimpedance amplifier family. Low voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequencies.

The key elements to a transimpedance design, as shown in Figure 31, are the expected diode capacitance \( C_{[D]} \), which must include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF), the desired transimpedance gain \( R_{[FB]} \), and the gain-bandwidth (GBW) for the OPAx355 family (20 MHz). With these three variables set, the feedback capacitor value \( C_{[FB]} \) controls the frequency response. \( C_{[FB]} \) includes the stray capacitance of \( R_{[FB]} \), which is 0.2 pF for a typical surface-mount resistor.

\[ C_{[FB]} \leq 1 \text{ pF} \]

\( R_{[FB]} = 10 \text{ MQ} \)

\( V_{(V+)}, V_{(V-)} \)

\( V_{O} \)

(1) \( C_{[FB]} \) is optional to prevent gain peaking. \( C_{[FB]} \) includes the stray capacitance of \( R_{[FB]} \).

Figure 31. Dual-Supply Transimpedance Amplifier

9.2.1.1 Design Requirements

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage ( V_{(V+)} )</td>
<td>2.5 V</td>
</tr>
<tr>
<td>Supply voltage ( V_{(V-)} )</td>
<td>–2.5 V</td>
</tr>
</tbody>
</table>
9.2.1.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole to:

\[
\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{2 \times \pi \times R_{(FB)} \times C_{(D)}}{\text{GBW}}} \tag{1}
\]

Use Equation 2 to calculate the bandwidth.

\[
f_{(-3 \, \text{dB})} = \sqrt{\frac{\text{GBW}}{2 \times \pi \times R_{(FB)} \times C_{(D)}}} \tag{2}
\]

For other transimpedance bandwidths, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), or OPA656 and OPA657 (400-MHz GBW).

For single-supply applications, the +INx input is biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail. Figure 32 shows this configuration. This bias voltage appears across the photodiode, providing a reverse bias for faster operation.

For additional information, see Compensate Transimpedance Amplifiers Intuitively.

9.2.1.2.1 Optimizing The Transimpedance Circuit

To achieve the best performance, select components according to the following guidelines:

1. For lowest noise, select \( R_{(FB)} \) to create the total required gain. Using a lower value for \( R_{(FB)} \) and adding gain after the transimpedance amplifier generally results in poorer noise performance. \( R_{(FB)} \) produces noise that increases with the square root of \( R_{(FB)} \), whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.

2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequencies). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.

3. Noise increases with increased bandwidth. Only use the required circuit bandwidth. Use a capacitor across \( R_{(FB)} \) to limit bandwidth, even if a capacitor is not required for stability.

4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. Control leakage by using a circuit board guard trace that encircles the summing junction and
drives at the same voltage.

For additional information, see *Noise Analysis of FET Transimpedance Amplifiers* and *Noise Analysis for High-Speed Op Amps*.

### 9.2.1.3 Application Curve

![Graph showing AC Transfer Function](image)

–3 dB bandwidth is 4.56 MHz

**Figure 33. AC Transfer Function**

### 9.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by an amplifier. The input bias current of this amplifier loads the sensor output and causes a voltage drop across the source resistance. Figure 34 shows ($V_{(+INx)} = V_S - (I_{(BIAS)} \times R_{(S)})$). The last term ($I_{(BIAS)} \times R_{(S)}$) shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, use an op amp with low input bias current with high-impedance sensors. This low current keeps the $I_{(BIAS)} \times R_{(S)}$ error contribution less than the input voltage noise of the amplifier so that input voltage noise is not the dominant noise factor. The OPAx355 op amps feature low input bias current (typically 200 fA), and as a result, a preferred choice for these applications.

![Diagram showing Noise as a Result of $I_{(BIAS)}$](image)

**Figure 34. Noise as a Result of $I_{(BIAS)}$**
9.2.3 Driving ADCs

The OPAx355 op amps are designed to drive sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPAx355 series to drive ADCs without degrading differential linearity and THD.

The OPAx355 series buffers the ADC switched input capacitance and resulting charge injection while providing signal gain. Figure 35 shows the OPAx355 series configured to drive the ADS8326.


Figure 35. Driving the ADS8326

(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a −0.3-V supply to allow output swing to true ground potential.

9.2.4 Active Filter

The OPAx355 series is designed for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 36 shows a 500 kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is −40 dB/dec. The Butterworth response is preferred for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (see Figure 37).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.
9.3 Video

The OPAx355 output stage is capable of driving a standard back-terminated 75-Ω video cable. By back-terminating a transmission line, the line does not exhibit a capacitive load to the driver. A properly back-terminated 75-Ω cable does not appear as capacitance; the cable presents only a 150-Ω resistive load to the OPAx355 output.

The OPAx355 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level by offsetting and AC-coupling the signal, as shown in Figure 38.
Video (continued)

9.4 Wideband Video Multiplexing

One common application for video speed amplifiers which include an enable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple wired-OR video multiplexer can be easily implemented using the OPA357; see Figure 39.

Figure 38. RGB Cable Driver
Wideband Video Multiplexing (continued)

Figure 39. Multiplexed Output
10 Power Supply Recommendations

The OPAx355 is specified for operation from 2.7 to 5.5 V (±1.35 to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the Typical Characteristics section.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the Layout Guidelines section.

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, VS – VO. Minimize power dissipation by using the lowest possible power-supply voltage required to ensure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. Power Amplifier Stress and Power Handling Limitations explains how to calculate or measure power dissipation with unusual signals and loads, and is available on www.ti.com.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature to trigger the thermal protection at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

11 Layout

11.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be used for the OPAx355 amplifiers. Generous use of ground planes, short direct-signal traces, and a preferred bypass capacitor located at the V+ pin ensures clean and stable operation. Large areas of copper help dissipate heat generated within the amplifiers in normal operation.

Sockets are not recommended for use with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-μF or larger tantalum capacitor in parallel is beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

11.2 Layout Example

![Layout Example Diagram]

Figure 40. Layout Example
12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 1. Related Links

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>ORDER NOW</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA355</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>OPA2355</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>OPA3355</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

FilterPro is a trademark of Texas Instruments Incorporated.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2355DGSA/250</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>D55</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA2355DGSA/250G4</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAUAG</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>D55</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA3355EA/250</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA3355EA</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA3355EA/250G4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA3355EA</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA3355UA</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA3355UA</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA355NA/250</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>C55</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA355NA/250G4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>C55</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA355NA/3K</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>C55</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA355NA/3KG4</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>C55</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA355UA</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA355UA</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA355UA/2K5</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA355UA</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA355UA/2K5G4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA355UA</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA355UAG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA355UA</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

Addendum-Page 1
RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA355:

- Automotive: OPA355-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
### TAPE AND REEL INFORMATION

**Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Reel Diameter (mm)** | **Reel Width W1 (mm)** | **A0 (mm)** | **B0 (mm)** | **K0 (mm)** | **P1 (mm)** | **W (mm)** | **Pin1 Quadrant**
---|---|---|---|---|---|---|---|---|---|---|---|---|
OPA2355DGSA/250 | VSSOP | DGS | 10 | 250 | 180.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1
OPA3355EA/250 | TSSOP | PW | 14 | 250 | 180.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1
OPA3355EA/2K5 | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1
OPA355NA/250 | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3
OPA355NA/3K | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3
OPA355UA/2K5 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1

*All dimensions are nominal.

**Legend for TAPE DIMENSIONS**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

---

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Pin 1 orientation in the tape is indicated by the User Direction of Feed. The Pocket Quadrants are marked with Q1 to Q4.

---

**Tape and Reel Information**

- **Device**: OPA2355DGSA/250, OPA3355EA/250, OPA3355EA/2K5, OPA355NA/250, OPA355NA/3K, OPA355UA/2K5
- **Package Type**: VSSOP, TSSOP, SOT-23, SOIC
- **Drawing**: DGS, PW, DBV
- **Pins**: 10, 14, 6, 6, 8
- **SPQ**: 250, 250, 3000, 2500
- **Reel Diameter (mm)**: 180.0, 180.0, 330.0, 178.0, 178.0, 330.0
- **Reel Width W1 (mm)**: 12.4, 12.4, 12.4, 9.0, 9.0, 12.4
- **A0 (mm)**: 5.3, 6.9, 5.6, 3.23, 3.23, 6.4
- **B0 (mm)**: 3.4, 6.9, 5.6, 3.17, 3.17, 5.2
- **K0 (mm)**: 1.4, 1.6, 1.6, 1.37, 1.37, 2.1
- **P1 (mm)**: 8.0, 8.0, 8.0, 4.0, 4.0, 8.0
- **W (mm)**: 12.0, 12.0, 12.0, 8.0, 8.0, 12.0
- **Pin1 Quadrant**: Q1, Q1, Q1, Q3, Q3, Q1

*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA2355DGSA/250</td>
<td>VSSOP</td>
<td>DGS</td>
<td>10</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA3355EA/250</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA3355EA/2K5</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA355NA/250</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>250</td>
<td>445.0</td>
<td>220.0</td>
<td>345.0</td>
</tr>
<tr>
<td>OPA355NA/3K</td>
<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>3000</td>
<td>445.0</td>
<td>220.0</td>
<td>345.0</td>
</tr>
<tr>
<td>OPA355UA/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
DBV (R–PDSO–G6)  PLASTIC SMALL–OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0,15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
   △ Falls within JEDEC MO–178 Variation AB, except minimum lead width.

4073253–5/N  12/14
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
NOTES:  A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
   ▶ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
   ▶ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AB.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:  
A. All linear dimensions are in millimeters. 
B. This drawing is subject to change without notice. 
C. Publication IPC-7351 is recommended for alternate designs. 
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations. 
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AA.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation BA.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and/or implied warranties, for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers’ applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ACCURACY OR COMPLETENESS, TITLE, ANY PATENT RIGHT OF OR TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHTS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NONINFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI. TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALLFAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY PATENT RIGHT OF OR TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, INDIRECT, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designers may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designers will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated