OPA365, OPA2365

OPAx365 50-MHz, Zero-Crossover, Low-Distortion, High CMRR, RRI/O, Single-Supply Operational Amplifier

1 Features
- Gain Bandwidth: 50 MHz
- Zero-Crossover Distortion Topology:
  - Excellent THD+N: 0.0004%
  - CMRR: 100 dB (Minimum)
  - Rail-to-Rail Input and Output
    - Input 100 mV Beyond Supply Rail
- Low Noise: 4.5 nV/√Hz at 100 kHz
- Slew Rate: 25 V/µs
- Fast Settling: 0.3 µs to 0.01%
- Precision:
  - Low Offset: 100 µV
  - Low Input Bias Current: 0.2 pA
- 2.2-V to 5.5-V Operation

2 Applications
- Signal Conditioning
- Data Acquisition
- Process Control
- Active Filters
- Test Equipment
- Audio
- Wideband Amplifiers

3 Description
The OPA365 zero-crossover series, rail-to-rail, high-performance, CMOS operational amplifiers are optimized for very low voltage, single-supply applications. Rail-to-rail input or output, low-noise (4.5 nV/√Hz) and high-speed operation (50-MHz Gain Bandwidth) make these devices ideal for driving sampling analog-to-digital converters (ADCs). Applications include audio, signal conditioning, and sensor amplification. The OPA365 family of op amps are also well-suited for cell phone power amplifier control loops.

Special features include an excellent common-mode rejection ratio (CMRR), no input stage crossover distortion, high input impedance, and rail-to-rail input and output swing. The input common-mode range includes both the negative and positive supplies. The output voltage swing is within 10 mV of the rails.

The OPA365 (single version) is available in the micro-size SOT23-5 (SOT-5) and SOIC-8 packages. The OPA2365 (dual version) is offered in the SOIC-8 package. All versions are specified for operation from −40°C to +125°C. Single and dual versions have identical specifications for maximum design flexibility.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA365, OPA2365</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>SOT-23 (5)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Fast Settling Peak Detector

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

Changes from Revision D (June 2009) to Revision E

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation
  section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and
  Mechanical, Packaging, and Orderable Information section. ................................................................. 1
• Added current package designators to last paragraph of Description section ............................................. 1
5 Pin Configuration and Functions

Pin Functions: OPA365

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>SOIC</td>
<td>SOT</td>
</tr>
<tr>
<td>–IN</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>+IN</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>V–</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>V+</td>
<td>7</td>
<td>5</td>
</tr>
<tr>
<td>VOUT</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>NC</td>
<td>1, 5, 8</td>
<td>—</td>
</tr>
</tbody>
</table>

Pin Functions: OPA2365

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>SOIC</td>
<td>I/O</td>
</tr>
<tr>
<td>–IN A</td>
<td>2</td>
<td>I</td>
</tr>
<tr>
<td>+IN A</td>
<td>3</td>
<td>I</td>
</tr>
<tr>
<td>–IN B</td>
<td>6</td>
<td>I</td>
</tr>
<tr>
<td>+IN B</td>
<td>5</td>
<td>I</td>
</tr>
<tr>
<td>V–</td>
<td>4</td>
<td>—</td>
</tr>
<tr>
<td>V+</td>
<td>8</td>
<td>—</td>
</tr>
<tr>
<td>VOUT A</td>
<td>1</td>
<td>O</td>
</tr>
<tr>
<td>VOUT B</td>
<td>7</td>
<td>O</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply voltage</td>
<td>5.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Signal input terminals, voltage(^{(2)})</td>
<td>–0.5</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>Current</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal input terminals, current(^{(2)})</td>
<td>–10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Output short-circuit(^{(3)})</td>
<td>Continuous</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating, (T_A)</td>
<td>–40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction, (T_J)</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage, (T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{ESD}}) Electrostatic discharge</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±4000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±1000</td>
<td></td>
</tr>
<tr>
<td>Machine model</td>
<td>±400</td>
<td></td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage, ((V+) – (V–))</td>
<td>2.2</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Specified temperature</td>
<td>–40</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating temperature</td>
<td>–40</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information: OP365

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>OPA365</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5 PINS</td>
</tr>
<tr>
<td>(R_{\text{JA}}) Junction-to-ambient thermal resistance</td>
<td>206.9</td>
</tr>
<tr>
<td>(R_{\text{JC(top)}}) Junction-to-case (top) thermal resistance</td>
<td>69.4</td>
</tr>
<tr>
<td>(R_{\text{JB}}) Junction-to-board thermal resistance</td>
<td>34.2</td>
</tr>
<tr>
<td>(\psi_{\text{JT}}) Junction-to-top characterization parameter</td>
<td>1.8</td>
</tr>
<tr>
<td>(\psi_{\text{JB}}) Junction-to-board characterization parameter</td>
<td>33.9</td>
</tr>
<tr>
<td>(R_{\text{JC(bot)}}) Junction-to-case (bottom) thermal resistance</td>
<td>n/a</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Thermal Information: OPA2365

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>OPA2365</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$</td>
<td>115.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$</td>
<td>60.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JB}$</td>
<td>56.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>9.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>56.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(bot)}$</td>
<td>n/a</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

At $T_A = 25°C$, $R_L = 10 \, kΩ$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Input offset voltage</td>
<td>100</td>
<td>200</td>
<td>µV</td>
<td></td>
</tr>
<tr>
<td>$dV_{OS}/dT$</td>
<td>Input offset voltage versus drift</td>
<td>At $T_A = -40°C$ to $+125°C$</td>
<td>1</td>
<td>µV/°C</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Input offset voltage versus power supply $V_S = 2.2 , V$ to $5.5 , V$, at $T_A = -40°C$ to $+125°C$</td>
<td>10</td>
<td>µV/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel separation, DC</td>
<td></td>
<td>0.2</td>
<td></td>
<td>µV/V</td>
<td></td>
</tr>
<tr>
<td>INPUT BIAS CURRENT</td>
<td></td>
<td></td>
<td>±0.2</td>
<td>±10</td>
<td>pA</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input bias current</td>
<td>Over temperature at $T_A = -40°C$ to $+125°C$</td>
<td>See Typical Characteristics</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input offset current</td>
<td></td>
<td>±0.2</td>
<td>±10</td>
<td>pA</td>
</tr>
<tr>
<td>NOISE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input voltage noise</td>
<td>$f = 0.1 , Hz$ to $10 , Hz$</td>
<td>5</td>
<td>µV/√H</td>
<td></td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input voltage noise density</td>
<td>$f = 100 , kHz$</td>
<td>4.5</td>
<td>nV/√Hz</td>
<td></td>
</tr>
<tr>
<td>$I_n$</td>
<td>Input current noise density</td>
<td>$f = 10 , kHz$</td>
<td>4</td>
<td>fA/√Hz</td>
<td></td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Common-mode voltage range</td>
<td>$(V-) = 0.1 , V$ to $(V+) + 0.1 , V$, at $T_A = -40°C$ to $+125°C$</td>
<td>100</td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>$(V-) - 0.1 , V \leq V_{CM} \leq (V+) + 0.1 , V$, at $T_A = -40°C$ to $+125°C$</td>
<td>100</td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td>INPUT CAPACITANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential</td>
<td></td>
<td>6</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Common-mode</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>OPEN-LOOP GAIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{OL}$</td>
<td>Open-loop voltage gain</td>
<td>$R_L = 10 , kΩ$, $100 , mV &lt; V_O &lt; (V+) - 100 , mV$, at $T_A = -40°C$ to $+125°C$</td>
<td>100</td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td>$R_L = 600 , Ω$, $200 , mV &lt; V_O &lt; (V+) - 200 , mV$, at $T_A = -40°C$ to $+125°C$</td>
<td>100</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_L = 600 , Ω$, $200 , mV &lt; V_O &lt; (V+) - 200 , mV$, at $T_A = -40°C$ to $+125°C$</td>
<td>94</td>
<td></td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FREQUENCY RESPONSE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-bandwidth product</td>
<td>$V_S = 5 , V$</td>
<td>50</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew rate $V_S = 5 , V$, $G = 1$</td>
<td>25</td>
<td>V/µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Settling time $0.1%$</td>
<td>$V_S = 5 , V$, 4-V step, $G = +1$</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Settling time $0.01%$</td>
<td>$V_S = 5 , V$, 4-V step, $G = +1$</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

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Product Folder Links: OPA365 OPA2365
### Electrical Characteristics (continued)

At $T_A = 25^\circ C$, $R_L = 10 \, \text{k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overload recovery time</td>
<td>$V_S = 5 , \text{V}, V_{IN} \times \text{Gain} &gt; V_S$</td>
<td>&lt; 0.1</td>
<td></td>
<td></td>
<td>$\mu\text{s}$</td>
</tr>
<tr>
<td>THD+N</td>
<td>Total harmonic distortion + noise $^{(1)}$</td>
<td>$V_S = 5 , \text{V}, R_L = 600 , \Omega, V_O = 4 , V_{PP}, G = 1, f = 1 , \text{kHz}$</td>
<td></td>
<td>0.0004%</td>
<td></td>
</tr>
</tbody>
</table>

#### OUTPUT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage output swing from rail</td>
<td>$R_L = 10 , \text{k}\Omega, V_S = 5.5 , \text{V}, \text{at } T_A = -40^\circ \text{C} \text{ to } +125^\circ \text{C}$</td>
<td>10</td>
<td>20</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Short-circuit current</td>
<td></td>
<td>±65</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$C_L$</td>
<td>Capacitive load drive</td>
<td></td>
<td></td>
<td>See Typical Characteristics</td>
<td></td>
</tr>
<tr>
<td>Open-loop output impedance</td>
<td>$f = 1 , \text{MHz}, I_O = 0 , \text{mA}$</td>
<td>30</td>
<td></td>
<td>$\Omega$</td>
<td></td>
</tr>
</tbody>
</table>

#### POWER SUPPLY

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_S$</td>
<td>Specified voltage range</td>
<td></td>
<td>2.2</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current per amplifier</td>
<td>$I_O = 0 , \text{mA}$</td>
<td></td>
<td>4.6</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Over temperature</td>
<td>At $T_A = -40^\circ \text{C} \text{ to } +125^\circ \text{C}$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$^{(1)}$ 3rd-order filter; bandwidth 80 kHz at −3 dB.
6.7 Typical Characteristics

At \( T_A = 25^\circ C \), \( V_S = 5 \) V, and \( C_L = 0 \) pF, unless otherwise noted.

![Figure 1. Open-Loop Gain and Phase vs Frequency](image)

![Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency](image)

![Figure 3. Offset Voltage Production Distribution](image)

![Figure 4. Offset Voltage Drift Production Distribution](image)

![Figure 5. Input Bias Current vs Temperature](image)

![Figure 6. Input Bias Current vs Common-Mode Voltage](image)
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = 5 \text{ V}$, and $C_L = 0 \text{ pF}$, unless otherwise noted.

**Figure 7. OPA365 Output Voltage vs Output Current**

**Figure 8. OPA2365 Output Voltage vs Output Current**

**Figure 9. Short-Circuit Current vs Temperature**

**Figure 10. Quiescent Current vs Supply Voltage**

**Figure 11. Quiescent Current vs Temperature**

**Figure 12. 0.1-Hz to 10-Hz Input Voltage Noise**
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = 5 \text{ V}$, and $C_L = 0 \text{ pF}$, unless otherwise noted.

![Graph 1](image1.png)

**Figure 13. Total Harmonic Distortion + Noise vs Frequency**

![Graph 2](image2.png)

**Figure 14. Input Voltage Noise Spectral Density**

![Graph 3](image3.png)

**Figure 15. Overshoot vs Capacitive Load**

![Graph 4](image4.png)

**Figure 16. Small-Signal Step Response**

![Graph 5](image5.png)

**Figure 17. Large-Signal Step Response**

![Graph 6](image6.png)

**Figure 18. Small-Signal Step Response**
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = 5$ V, and $C_L = 0$ pF, unless otherwise noted.

![Figure 19. Large-Signal Step Response](image-url)
7 Detailed Description

7.1 Overview

The OPAx365 series of operational amplifiers feature rail-to-rail, high performance that make these devices an excellent choice for driving ADCs. Other typical applications include signal conditioning, cell phone power amplifier control loops, audio, and sensor amplification. The OPA365 is a wideband amplifier that may be operated with either a single supply or dual supplies.

Furthermore, the OPA365 amplifier parameters are fully specified from 2.2 V to 5.5 V. Many of the specifications apply from −40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 Rail-to-Rail Input

The OPA365 product family features true rail-to-rail input operation, with supply voltages as low as ±1.1 V (2.2 V). A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary stage operational amplifiers. This topology also allows the OPA365 to provide superior common-mode performance over the entire input range, which extends 100 mV beyond both power-supply rails, as shown in Figure 20. When driving ADCs, the highly linear $V_{CM}$ range of the OPA365 assures that the op amp or ADC system linearity performance is not compromised.

![Figure 20. OPA365 Linear Offset Over the Entire Common-Mode Range](image)

A simplified schematic illustrating the rail-to-rail input circuitry is shown in the Functional Block Diagram.

7.3.2 Input and ESD Protection

The OPA365 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, provided that the current is limited to 10 mA as stated in the Absolute Maximum Ratings. Figure 21 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to the minimum in noise-sensitive applications.

![Figure 21. Input Current Protection](image)

7.3.3 Capacitive Loads

The OPA365 may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA365 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (+1 – V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.
Feature Description (continued)

When operating in the unity-gain configuration, the OPA365 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors ($C_L > 1 \mu F$) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See Figure 15.

One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor, typically 10 $\Omega$ to 20 $\Omega$, in series with the output; see Figure 22. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider may be insignificant. For instance, with a load resistance, $R_L = 10 \text{k} \Omega$, and $R_S = 20 \Omega$, the gain error is only about 0.2%. However, when $R_L$ is decreased to 600 $\Omega$, which the OPA365 is able to drive, the error increases to 7.5%.

![Figure 22. Improving Capacitive Load Drive](image)

7.3.4 Achieving an Output Level of Zero Volts (0 V)

Certain single-supply applications require the op amp output to swing from 0 V to a positive full-scale voltage and have high accuracy. An example is an op amp employed to drive a single-supply ADC having an input range from 0 V to 5 V. Rail-to-rail output amplifiers with very light output loading may achieve an output level within millivolts of 0 V (or $+V_S$ at the high end), but not 0 V. Furthermore, the deviation from 0 V only becomes greater as the load current required increases. This increased deviation is a result of limitations of the CMOS output stage.

When a pulldown resistor is connected from the amplifier output to a negative voltage source, the OPA365 can achieve an output level of 0 V, and even a few millivolts below 0 V. Below this limit, nonlinearity and limiting conditions become evident. Figure 23 illustrates a circuit using this technique.

A pulldown current of approximately 500 $\mu A$ is required when OPA365 is connected as a unity-gain buffer. A practical termination voltage ($V_{NEG}$) is $-5 \text{ V}$, but other convenient negative voltages also may be used. The pull-down resistor $R_L$ is calculated from $R_L = [(V_O - V_{NEG}) / (500 \text{ } \mu A)]$.

Using a minimum output voltage ($V_O$) of 0 V, $R_L = [0 \text{ V} - (-5 \text{ V})] / (500 \text{ } \mu A)] = 10 \text{ k} \Omega$. Keep in mind that lower termination voltages result in smaller pulldown resistors that load the output during positive output voltage excursions.

**NOTE**

This technique does not work with all op amps and should only be applied to op amps such as the OPA365 that have been specifically designed to operate in this manner. Also, operating the OPA365 output at 0 V changes the output stage operating conditions, resulting in somewhat lower open-loop gain and bandwidth.

Keep these precautions in mind when driving a capacitive load because these conditions can affect circuit transient response and stability.
Feature Description (continued)

7.3.5 Active Filtering

The OPA365 is well-suited for active filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 24 shows a 500-kHz, second-order, low-pass filter utilizing the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is $-40\,\text{dB/dec}$. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

• adding an inverting amplifier;
• adding an additional second-order MFB stage; or
• using a noninverting filter topology such as the Sallen-Key.

The Sallen-Key topology is shown in Figure 25.
Feature Description (continued)

7.4 Device Functional Modes

The OPA365 family has a single functional mode and are operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the OPA365 family is 5.5 V (±2.75 V).

Figure 25. Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

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8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Amplifier Configurations

As with other single-supply op amps, the OPA365 may be operated with either a single supply or dual supplies. A typical dual-supply connection is shown in Figure 26, which is accompanied by a single-supply connection. The OPA365 is configured as a basic inverting amplifier with a gain of $-10 \, \text{V/V}$. The dual-supply connection has an output voltage centered on zero, while the single-supply connection has an output centered on the common-mode voltage $V_{CM}$. For the circuit shown, this voltage is 1.5 V, but may be any value within the common-mode input voltage range. The OPA365 $V_{CM}$ range extends 100 mV beyond the power-supply rails.

![Figure 26. Basic Circuit Connections](image)

Figure 26. Basic Circuit Connections

Figure 27 shows a single-supply, electret microphone application where $V_{CM}$ is provided by a resistive divider. The divider also provides the bias voltage for the electret element.
Application Information (continued)

8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA365 is ideally suited to construct high-speed, high-precision active filters. Figure 28 illustrates a second-order low-pass filter commonly encountered in signal processing applications.

8.2.1 Design Requirements

Use the following parameters for this design example:
- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 28. Use Equation 1 to calculate the voltage transfer function.

\[
\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2) \left(1/R_1 + 1/R_3 + 1/R_4 \right) + 1/R_3 R_4 C_2 C_5}
\]  

(1)

This circuit produces a signal inversion. For this circuit the gain at DC and the low-pass cutoff frequency can be calculated using Equation 2.

\[
\text{Gain} = \frac{R_4}{R_1}
\]

\[
f_c = \frac{1}{2\pi} \sqrt{\frac{1}{R_3 R_4 C_2 C_5}}
\]  

(2)
Typical Application (continued)

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners. Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows you to design, optimize, and simulate complete multi-stage active filter solutions within minutes.

8.2.3 Application Curve

Figure 29. OPA365 Second-Order 25 kHz, Chebyshev, Low-Pass Filter

8.3 System Examples

8.3.1 Driving an Analog-to-Digital Converter

Very wide common-mode input range, rail-to-rail input and output voltage capability, and high speed make the OPA365 an ideal driver for modern ADCs. Also, because it is free of the input offset transition characteristics inherent to some rail-to-rail CMOS op amps, the OPA365 provides low THD and excellent linearity throughout the input voltage swing range.

Figure 30 shows the OPA365 driving an ADS8326, 16-bit, 250-kSPS converter. The amplifier is connected as a unity-gain, noninverting buffer and has an output swing to 0 V, making it directly compatible with the ADC minus full-scale input level. The 0-V level is achieved by powering the OPA365 V− pin with a small negative voltage established by the diode forward voltage drop. A small, signal-switching diode or Schottky diode provides a suitable negative supply voltage of −0.3 V to −0.7 V. The supply rail-to-rail is equal to V+, plus the small negative voltage.
System Examples (continued)

One method for driving an ADC that negates the need for an output swing down to 0 V uses a slightly compressed ADC full-scale input range (FSR). For example, the 16-bit ADS8361 (shown in Figure 31) has a maximum FSR of 0 V to 5 V, when powered by a 5-V supply and VREF of 2.5 V. The idea is to match the ADC input range with the op amp full linear output swing range; for example, an output range of 0.1 V to 4.9 V. The reference output from the ADS8361 ADC is divided down from 2.5 V to 2.4 V using a resistive divider. The ADC FSR then becomes 4.8 V_{PP} centered on a common-mode voltage of 2.5 V. Current from the ADS8361 reference pin is limited to approximately ±10 μA. Here, 5 μA was used to bias the divider. The resistors must be precise to maintain the ADC gain accuracy. An additional benefit of this method is the elimination of the negative supply voltage; it requires no additional power-supply current.

An RC network, consisting of R1 and C1, is included between the op amp and the ADS8361. It not only provides a high-frequency filter function, but more importantly serves as a charge reservoir used for charging the converter internal hold capacitance. This capability assures that the op amp output linearity is maintained as the ADC input characteristics change throughout the conversion cycle. Depending on the particular application and ADC, some optimization of the R1 and C1 values may be required for best transient performance.

---

(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground due to op amp output swing limitation. If a negative power supply is available, this simple circuit creates a −0.3-V supply to allow output swing to true ground potential.

Figure 30. Driving the ADS8326
Figure 31. Driving the ADS8361

Figure 32 illustrates the OPA2365 dual op amp providing signal conditioning within an ADS1258 bridge sensor circuit. It follows the ADS1258 16:1 multiplexer and is connected as a differential in or differential out amplifier. The voltage gain for this stage is approximately 10 V/V. Driving the ADS1258 internal ADC in differential mode, rather than in a single-ended, exploits the full linearity performance capability of the converter. For best common-mode rejection, the two $R_2$ resistors should be closely matched.

Note that in Figure 32, the amplifiers, bridges, ADS1258, and internal reference are powered by the same single 5-V supply. This ratiometric connection helps cancel excitation voltage drift effects and noise. For best performance, the 5-V supply must be as free as possible of noise and transients.

When the ADS1258 data rate is set to maximum and the chop feature enabled, this circuit yields 12 bits of noise-free resolution with a 50-mV full-scale input.

The chop feature is used to reduce the ADS1258 offset and offset drift to very low levels. A 2.2-nF capacitor is required across the ADC inputs to bypass the sampling currents. The 47-Ω resistors provide isolation for the OPA2365 outputs from the relatively large, 2.2-nF capacitive load. For more information regarding the ADS1258, see the product data sheet available for download at www.ti.com.
System Examples (continued)

Figure 32. Conditioning Input Signals to the ADS1258 on a Single Supply

9 Power Supply Recommendations

The OPA365 family is specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from −40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - The OPA365 is capable of high-output current (in excess of 65 mA). Applications with low impedance
Layout Guidelines (continued)

loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1-µF solid tantalum capacitors may improve dynamic performance in these applications.

- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to Circuit Board Layout Techniques (SLOA089).

- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.

- Place the external components as close to the device as possible. As shown in Figure 33, keeping RF and RG close to the inverting input minimizes parasitic capacitance.

- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

- Cleaning the PCB following board assembly is recommended for best performance.

- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

Figure 33. Layout Recommendation

Figure 34. Schematic Representation
11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)
TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE
These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 DIP Adapter EVM
The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (MSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Op Amp EVM
The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

NOTE
These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 TI Precision Designs
TI Precision Designs are analog solutions created by TI’s precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.5 WEBENCH® Filter Designer
WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI’s vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.
11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPAx365, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- User guide: FilterPro™ MFB and Sallen-Key Low-Pass Filter Design Program User Guide (SBFA001)
- Application report: Low Power Input and Reference Driver Circuit for ADS8318 and ADS8319 (SBOA118)
- Application bulletin AB-045: Op Amp Performance Analysis (SBOA054)
- Application bulletin AB-067: Single-Supply Operation of Operational Amplifiers (SBOA059)
- Application bulletin AB-105: Tuning in Amplifiers (SBOA067)
- Reference book: The Best of Baker's Best – Amplifiers eBook (SLYC124)

11.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** Ti's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** Ti's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
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TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
### PACKAGING INFORMATION

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<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>O365A</td>
<td>Samples</td>
</tr>
</tbody>
</table>

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(1) The marketing status values are defined as follows:

- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD**: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA2365, OPA365:

- Automotive: OPA2365-Q1, OPA365-Q1
- Enhanced Product: OPA365-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

![Reel Dimensions Diagram](image)

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
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</table>

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram](image)

*All dimensions are nominal.

<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
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<td>330.0</td>
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<td>12.0</td>
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</table>

*All dimensions are nominal*
MECHANICAL DATA

DBV (R-PDSO-G5)  PLASTIC SMALL-OUTLINE PACKAGE

Diagram showing the dimensions and features of the package.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.
DBV (R-PDSC-G5)  PLASTIC SMALL OUTLINE

Example Board Layout

1.90

2.7

0.95

Solder Mask Opening

1.05

0.07

All Around

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1.00

1.90

0.55

2.7

0.95

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

4209593–3/C 08/11

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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\triangle\] Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
\[\triangle\] Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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