FET-Input, Low Distortion
OPERATIONAL AMPLIFIER

FEATURES
- LOW DISTORTION: 0.0003% at 1kHz
- LOW NOISE: 10nV/√Hz
- HIGH SLEW RATE: 25V/µs
- WIDE GAIN-BANDWIDTH: 20MHz
- UNITY-GAIN STABLE
- WIDE SUPPLY RANGE: $V_S = \pm 4.5$ to $\pm 24V$
- DRIVES 600$\Omega$ LOAD
- DUAL VERSION AVAILABLE (OPA2604)

APPLICATIONS
- PROFESSIONAL AUDIO EQUIPMENT
- PCM DAC I/V CONVERTERS
- SPECTRAL ANALYSIS EQUIPMENT
- ACTIVE FILTERS
- TRANSDUCER AMPLIFIERS
- DATA ACQUISITION

DESCRIPTION
The OPA604 is a FET-input operational amplifier designed for enhanced AC performance. Very low distortion, low noise and wide bandwidth provide superior performance in high quality audio and other applications requiring excellent dynamic performance.

New circuit techniques and special laser trimming of dynamic circuit performance yield very low harmonic distortion. The result is an op amp with exceptional sound quality. The low-noise FET input of the OPA604 provides wide dynamic range, even with high source impedance. Offset voltage is laser-trimmed to minimize the need for interstage coupling capacitors.

The OPA604 is available in 8-pin plastic mini-DIP and SO-8 surface-mount packages, specified for the $-25^\circ$C to $+85^\circ$C temperature range.
ABSOLUTE MAXIMUM RATINGS

- Power Supply Voltage: ±25V
- Input Voltage: (V–)–1V to (V+)–1V
- Output Short Circuit to Ground: Continuous
- Operating Temperature: –40°C to +100°C
- Storage Temperature: –40°C to +125°C
- Junction Temperature: +150°C
- Lead Temperature (soldering, 10s): +300°C
- Lead Temperature (soldering, 3s): +260°C

ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see to the Package Option Addendum at the end of this data sheet.
# ELECTRICAL CHARACTERISTICS

\( T_A = +25°C, V_g = ±15V, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<td>OFFSET VOLTAGE</td>
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<tr>
<td>Input Offset Voltage</td>
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<td>±5</td>
<td>mV</td>
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<tr>
<td>Average Drift</td>
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<td>±8</td>
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<td>µV/°C</td>
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<td>Power Supply Rejection</td>
<td>( V_g = ±5 ) to ±24V</td>
<td>80</td>
<td>100</td>
<td>dB</td>
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<td>INPUT BIAS CURRENT(1)</td>
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<td></td>
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<td>pA</td>
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<td>pA</td>
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<td>NOISE</td>
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<td>Noise Density: f = 10Hz</td>
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<td>25</td>
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<td>f = 100Hz</td>
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<td>15</td>
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<td>nV/√Hz</td>
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<td>10</td>
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<tr>
<td>Voltage Noise, BW = 20Hz to 20kHz</td>
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<td>1.5</td>
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<td>( \mu V_{pp} )</td>
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<tr>
<td>Input Bias Current Noise</td>
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<td>4</td>
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<tr>
<td>Common-Mode Input Range</td>
<td>( V_{CM} = ±12V )</td>
<td>±12</td>
<td>±13</td>
<td>V</td>
<td></td>
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<tr>
<td>Common-Mode Rejection</td>
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<td>100</td>
<td>dB</td>
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<td>INPUT IMPEDANCE</td>
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<td>Common-Mode</td>
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<td></td>
<td>8 | 10^12</td>
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<td>OPEN-LOOP GAIN</td>
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<tr>
<td>Open-Loop Voltage Gain</td>
<td>( V_o = ±10V, R_L = 1kΩ )</td>
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<td>80</td>
<td>100</td>
<td>dB</td>
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<td>FREQUENCY RESPONSE</td>
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<tr>
<td>Gain-Bandwidth Product</td>
<td>( G = 100 )</td>
<td>20</td>
<td>25</td>
<td>MHz</td>
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<tr>
<td>Slew Rate</td>
<td>( 20V_{pp}, R_L = 1kΩ )</td>
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<td>15</td>
<td></td>
<td>V/µs</td>
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<td>Settling Time: 0.01%</td>
<td>( G = -1, 10V ) Step</td>
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<td>1.5</td>
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<td>µs</td>
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<td>0.1%</td>
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<td>1</td>
<td></td>
<td>µs</td>
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<td>Total Harmonic Distortion + Noise (THD+N)</td>
<td>( G = 1, f = 1kHz )</td>
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<td></td>
<td>%</td>
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<tr>
<td>OUTPUT</td>
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<td>Current Output</td>
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<td>Short Circuit Current</td>
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<tr>
<td>Output Resistance, Open-Loop</td>
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<td>POWER SUPPLY</td>
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<tr>
<td>Specified Operating Voltage</td>
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<td>V</td>
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<td>Operating Voltage Range</td>
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<td>V</td>
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<td>Current</td>
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<td>±5.3</td>
<td>±7</td>
<td>mA</td>
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<td>Storage</td>
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<td>Thermal Resistance(2), ( \theta_{JA} )</td>
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<td>°C</td>
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<td></td>
<td></td>
<td>±40</td>
<td>+125</td>
<td>°C</td>
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</tbody>
</table>
| NOTES: (1) Typical performance, measured fully warmed-up. (2) Soldered to circuit board—see text.
TYPICAL CHARACTERISTICS

$T_a = +25^\circ C, V_c = \pm 15V$, unless otherwise noted.

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY**

- THD + N (%) vs Frequency (Hz)
- Measurement BW = 80kHz
- See "Distortion Measurements" for description of test method.

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE**

- THD + N (%) vs Output Voltage ($V_{pp}$)
- Measurement BW = 80kHz
- See "Distortion Measurements" for description of test method.

**OPEN-LOOP GAIN/PHASE vs FREQUENCY**

- Voltage Gain (dB)
- Phase Shift (Degrees)
- Frequency (Hz)

**INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY**

- Voltage Noise (nV/Hz)
- Current Noise (fA/Hz)
- Frequency (Hz)

**INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE**

- Input Bias Current (pA)
- Input Offset Current (pA)
- Ambient Temperature (°C)

**INPUT BIAS AND INPUT OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE**

- Input Bias Current (pA)
- Input Offset Current (pA)
- Common-Mode Voltage (V)
TYPICAL CHARACTERISTICS (Cont.)

$T_a = +25^\circ C$, $V_s = \pm 15V$, unless otherwise noted.

**INPUT BIAS CURRENT vs TIME FROM POWER TURN-ON**

**COMMON-MODE REJECTION vs COMMON-MODE VOLTAGE**

**POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY**

**A_{OL}, PSR, AND CMR vs SUPPLY VOLTAGE**

**GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE**

**GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE**
TYPICAL CHARACTERISTICS (Cont.)

$T_a = +25^\circ C$, $V_s = \pm 15V$, unless otherwise noted.

### Settling Time vs Closed-Loop Gain

- $V_O = 10V$ Step
- $R_L = 1k\Omega$
- $C_L = 50\mu F$

### Maximum Output Voltage Swing vs Frequency

- $V_s = \pm 15V$

### Supply Current vs Temperature

- $V_s = \pm 15V$
- $V_s = \pm 24V$
- $V_s = \pm 5V$

### Short-Circuit Current vs Temperature

- $I_{SC+}$ and $I_{SC-}$

### Small-Signal Transient Response

### Large-Signal Transient Response
APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT
The OPA604 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3\(\mu\text{V/°C}\) for each 100\(\mu\text{V}\) of adjusted offset. The OPA604 can replace many other amplifiers by leaving the external null circuit unconnected.

The OPA604 is unity-gain stable, making it easy to use in a wide range of circuitry. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins. In most cases, a 1\(\mu\text{F}\) tantalum capacitor at each power supply pin is adequate.

Op amp distortion can be considered an internal error source which can be referred to the input. Figure 2 shows a circuit which causes the op amp distortion to be 101 times greater than normally produced by the op amp. The addition of \(R_3\) to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101. This extends the measurement limit, including the effects of the signal-source purity, by a factor of 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without \(R_3\).

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with the Audio Precision System One, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS
The dynamic characteristics of the OPA604 have been optimized for commonly encountered gains, loads and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Load capacitance reacts with the op amp’s open-loop output resistance to form an additional pole in the feedback loop. Figure 3 shows various circuits which preserve phase margin with capacitive load. For details of analysis techniques and applications circuits, refer to application bulletin AB-028 (SBOA015) located at www.ti.com.
For the unity-gain buffer, Figure 3a, stability is preserved by adding a phase-lead network, $R_C$ and $C_C$. Voltage drop across $R_C$ will reduce output voltage swing with heavy loads. An alternate circuit, Figure 3b, does not limit the output with low load impedance. It provides a small amount of positive feedback to reduce the net feedback factor. Input impedance of this circuit falls at high frequency as op amp gain rolloff reduces the bootstrap action on the compensation network.

Figures 3c and 3d show compensation techniques for noninverting amplifiers. Like the follower circuits, the circuit in Figure 3d eliminates voltage drop due to load current, but at the penalty of somewhat reduced input impedance at high frequency.

Figures 3e and 3f show input lead compensation networks for inverting and difference amplifier configurations.

**NOISE PERFORMANCE**

Op amp noise is described by two parameters—noise voltage and noise current. The voltage noise determines the noise performance with low source impedance. Low noise bipolar-input op amps such as the OPA27 and OPA37 provide very low voltage noise. But if source impedance is greater than a few thousand ohms, the current noise of bipolar-input op amps react with the source impedance and will dominate. At a few thousand ohms source impedance and above, the OPA604 will generally provide lower noise.

**POWER DISSIPATION**

The OPA604 is capable of driving a 600Ω load with powersupply voltages up to ±24V. Internal power dissipation is increased when operating at high power supply voltage. The typical characteristic curve, Power Dissipation vs Power Supply Voltage, shows quiescent dissipation (no signal or no load) as well as dissipation with a worst case continuous sine wave. Continuous high-level music signals typically produce dissipation significantly less than worst-case sine waves.

Copper leadframe construction used in the OPA604 improves heat dissipation compared to conventional plastic packages. To achieve best heat dissipation, solder the device directly to the circuit board and use wide circuit board traces.

**OUTPUT CURRENT LIMIT**

Output current is limited by internal circuitry to approximately ±40mA at 25°C. The limit current decreases with increasing temperature as shown in the typical curves.

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**FIGURE 2. Distortion Test Circuit.**

![Distortion Test Circuit](image-url)

---

**TABLE 1**

<table>
<thead>
<tr>
<th>SIG. GAIN</th>
<th>DIST. GAIN</th>
<th>$R_1$</th>
<th>$R_2$</th>
<th>$R_3$</th>
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<tr>
<td>1</td>
<td>101</td>
<td>∞</td>
<td>5kΩ</td>
<td>50Ω</td>
</tr>
<tr>
<td>10</td>
<td>101</td>
<td>500Ω</td>
<td>5kΩ</td>
<td>500Ω</td>
</tr>
<tr>
<td>100</td>
<td>101</td>
<td>50Ω</td>
<td>5kΩ</td>
<td>∞</td>
</tr>
</tbody>
</table>

NOTE: (1) Measurement BW = 80kHz
FIGURE 3. Driving Large Capacitive Loads.

NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.
FIGURE 4. Three-Pole Low-Pass Filter.

FIGURE 5. Three-Pole Generalized Immittance Converter (GIC) Low-Pass Filter.

FIGURE 7. High Impedance Amplifier.

FIGURE 8. Digital Audio DAC I-V Amplifier.

SOUND QUALITY

The following discussion is provided, recognizing that not all measured performance behavior explains or correlates with listening tests by audio experts. The design of the OPA604 included consideration of both objective performance measurements, as well as an awareness of widely held theory on the success and failure of previous op amp designs.

SOUND QUALITY

The sound quality of an op amp is often the crucial selection criteria—even when a data sheet claims exceptional distortion performance. By its nature, sound quality is subjective. Furthermore, results of listening tests can vary depending on application and circuit configuration. Even experienced listeners in controlled tests often reach different conclusions.

Many audio experts believe that the sound quality of a high performance FET op amp is superior to that of bipolar op amps. A possible reason for this is that bipolar designs generate greater odd-order harmonics than FETs. To the human ear, odd-order harmonics have long been identified as sounding more unpleasant than even-order harmonics. FETs, like vacuum tubes, have a square-law I-V transfer function which is more linear than the exponential transfer function of a bipolar transistor. As a direct result of this square-law characteristic, FETs produce predominantly even-order harmonics. Figure 10 shows the transfer function of a bipolar transistor and FET. Fourier transformation of both transfer functions reveals the lower odd-order harmonics of the FET amplifier stage.

THE OPA604 DESIGN

The OPA604 uses FETs throughout the signal path, including the input stage, input-stage load, and the important phase-splitting section of the output stage. Bipolar transistors are used where their attributes, such as current capability are important, and where their transfer characteristics have minimal impact.

The topology consists of a single folded-cascode gain stage followed by a unity-gain output stage. Differential input transistors J1 and J2 are special large-geometry, P-channel JFETs. Input stage current is a relatively high 800 µA, providing high transconductance and reducing voltage noise. Laser trimming of stage currents and careful attention to symmetry yields a nearly symmetrical slew rate of ±25V/µs.

The JFET input stage holds input bias current to approximately 50pA, providing high transconductance and reducing voltage noise. Laser trimming of stage currents and careful attention to symmetry yields a nearly symmetrical slew rate of ±25V/µs.

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FIGURE 10. I-V and Spectral Response of NPN and JFET.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (1)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (2)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<tr>
<td>OPA604AP</td>
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<td>Samples</td>
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<td>D</td>
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<td>Level-3-260C-168 HR</td>
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<td>OPA604AU</td>
<td>Samples</td>
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</tbody>
</table>

**Notes:**
1. The marketing status values are defined as follows:
   - **ACTIVE:** Product device recommended for new designs.
   - **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
   - **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
   - **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
   - **OBsolete:** TI has discontinued the production of the device.

2. **Eco Plan** - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

3. **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

4. There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

5. Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# TAPE AND REEL INFORMATION

## TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

## REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width (W1)**

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA604AU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA604AU/2K5</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.

4. This dimension does not include interlead flash.

5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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