1 Features

- Input Voltage Noise Density: 4 nV/√Hz at 1 kHz
- Input Voltage Noise: 0.1 Hz to 10 Hz: 250 nV_{PP}
- Input Bias Current: 10 pA (Maximum)
- Input Offset Voltage: 150 µV (Maximum)
- Input Offset Drift: 2 µV/°C (Maximum)
- Gain Bandwidth: 22 MHz
- Slew Rate: 28 V/µs
- Quiescent Current: 4.8 mA/Ch
- Wide Supply Range: ±4 V to ±18 V
- Packages: 8-Pin SOIC and 8-Pin VSSOP

2 Applications

- ADC Drivers
- DAC Output Buffers
- Test Equipment
- Medical Equipment
- PLL Filters
- Seismic Applications
- Transimpedance Amplifiers
- Integrators
- Active Filters

3 Description

The OPA827 series of JFET operational amplifiers combine outstanding DC precision with excellent AC performance. These amplifiers offer low offset voltage (150 µV, maximum), very low drift over temperature (0.5 µV/°C, typical), low-bias current (3 pA, typical), and very low 0.1-Hz to 10-Hz noise (250 nV_{PP}, typical). The device operates over a wide supply voltage range, ±4 V to ±18 V on a low supply current (4.8 mA/Ch, typical).

Excellent AC characteristics, such as a 22-MHz gain bandwidth product (GBW), a slew rate of 28 V/µs, and precision DC characteristics make the OPA827 series well-suited for a wide range of applications including 16-bit to 18-bit mixed signal systems, transimpedance (I/V-conversion) amplifiers, filters, precision ±10-V front ends, and professional audio applications.

The OPA827 is available in both 8-pin SOIC and 8-pin VSSOP surface-mount packages, and is specified from −40°C to 125°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA827</td>
<td>SOIC (8)</td>
<td>4.90 mm × 3.91 mm</td>
</tr>
<tr>
<td></td>
<td>VSSOP (8)</td>
<td>3.00 mm × 3.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
Table of Contents

1 Features ................................................................. 1
2 Applications ............................................................. 1
3 Description ............................................................... 1
4 Revision History ......................................................... 2
5 Pin Configuration and Functions ...................................... 4
6 Specifications .......................................................... 5
   6.1 Absolute Maximum Ratings .................................. 5
   6.2 ESD Ratings ..................................................... 5
   6.3 Recommended Operating Conditions ......................... 5
   6.4 Thermal Information ........................................... 5
   6.5 Electrical Characteristics ....................................... 6
   6.6 Typical Characteristics ......................................... 8
7 Detailed Description .................................................... 15
   7.1 Overview ......................................................... 15
   7.2 Functional Block Diagram ....................................... 15
   7.3 Feature Description ............................................. 15
   7.4 Device Functional Modes ....................................... 20
8 Application and Implementation ..................................... 21
   8.1 Application Information ....................................... 21
   8.2 Typical Application ............................................ 21
   8.3 System Examples .............................................. 22
9 Power Supply Recommendations .................................... 24
10 Layout ......................................................................... 25
   10.1 Layout Guidelines ............................................. 25
   10.2 Layout Example ................................................ 25
11 Device and Documentation Support .................................. 26
   11.1 Device Support ............................................... 26
   11.2 Documentation Support ...................................... 26
   11.3 Receiving Notification of Documentation Updates .......... 26
   11.4 Community Resource ......................................... 26
   11.5 Trademarks ..................................................... 26
   11.6 Electrostatic Discharge Caution ............................. 26
   11.7 Glossary ........................................................ 26
12 Mechanical, Packaging, and Orderable Information ............... 27

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (May 2012) to Revision I

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section .......................................................... 1
- Deleted Package/Ordering Information table, see POA at the end of the data sheet.......................................................... 4
- Changed values in the Thermal Information table to align with JEDEC standards.......................................................... 5

Changes from Revision G (February 2012) to Revision H

- Updated Figure 3.......................................................... 8
- Updated Figure 4.......................................................... 8

Changes from Revision F (March 2009) to Revision G

- Changed Input bias current and Input offset drift Features bullets .......................................................... 1
- Changed product status from Mixed Status to Production Data .......................................................... 1
- Changed description of amplifier drift and bias current in first paragraph of Description section .......................................................... 1
- Deleted high grade (OPA827I) option and footnote 2 from Package/Ordering Information table .......................................................... 4
- Deleted high grade (OPA827I) option from Electrical Characteristics table .......................................................... 6
- Changed Offset Voltage, Input Offset Voltage Drift parameter typical and maximum specifications in Electrical Characteristics table .......................................................... 6
- Changed Input Bias Current section specifications in Electrical Characteristics table .......................................................... 6
- Changed -40°C to +85°C Input Bias Current parameter unit .......................................................... 6
- Added Frequency Response, Slew Rate parameter minimum specification to Electrical Characteristics table .......................................................... 6
- Added Output, Short-Circuit Current parameter minimum specification to Electrical Characteristics table .......................................................... 7
- Updated Figure 7.......................................................... 8
- Updated Figure 8.......................................................... 8
• Updated Figure 9.............................................................................................................................................................. 8
• Updated Figure 11............................................................................................................................................................ 8
• Updated Figure 12............................................................................................................................................................ 8
• Updated Figure 14............................................................................................................................................................ 9
5 Pin Configuration and Functions

(1) NC denotes no internal connection.

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO.</td>
<td>NAME</td>
<td></td>
</tr>
<tr>
<td>+IN</td>
<td>3</td>
<td>I</td>
</tr>
<tr>
<td>–IN</td>
<td>2</td>
<td>I</td>
</tr>
<tr>
<td>NC</td>
<td>1, 5, 8</td>
<td>—</td>
</tr>
<tr>
<td>OUT</td>
<td>6</td>
<td>O</td>
</tr>
<tr>
<td>V+</td>
<td>7</td>
<td>—</td>
</tr>
<tr>
<td>V–</td>
<td>4</td>
<td>—</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, $V_S = (V+) - (V-)$</td>
<td>40</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input voltage (2)</td>
<td>$(V-) - 0.5$</td>
<td>$(V+) + 0.5$</td>
<td>V</td>
</tr>
<tr>
<td>Input current (2)</td>
<td>±10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Differential input voltage</td>
<td></td>
<td>±1$V_S$</td>
<td>V</td>
</tr>
<tr>
<td>Output short-circuit (2)</td>
<td></td>
<td>Continuous</td>
<td></td>
</tr>
<tr>
<td>Operating temperature, $T_A$</td>
<td>−55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction temperature, $T_J$</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, $T_{stg}$</td>
<td>−65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current-limited to 10 mA or less.

(3) Short-circuit to $V_S/2$ (ground in symmetrical dual-supply setups).

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(ESD)}$ Electrostatic discharge</td>
<td>±4000</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)</td>
<td>±1000</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_S$ Supply voltage</td>
<td>±4</td>
<td></td>
<td>±18</td>
<td>V</td>
</tr>
<tr>
<td>$T_A$ Specified temperature</td>
<td>−40</td>
<td></td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>OPA827</th>
<th>D (SOIC)</th>
<th>DGK (VSSOP)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JUA}$ Junction-to-ambient thermal resistance</td>
<td>160</td>
<td>180</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$R_{JUC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>75</td>
<td>55</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$R_{JUB}$ Junction-to-board thermal resistance</td>
<td>60</td>
<td>130</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>9</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>50</td>
<td>120</td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>$R_{JUC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>—</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
6.5 Electrical Characteristics

at $V_S = \pm 4\, \text{V}$ to $\pm 18\, \text{V}$, $T_A = 25^\circ\, \text{C}$, $R_L = 10\, \text{k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OFFSET VOLTAGE</strong></td>
<td>$V_{OS}$</td>
<td></td>
<td></td>
<td></td>
<td>µV</td>
</tr>
<tr>
<td>Input offset voltage</td>
<td>$V_S = \pm 15, \text{V}$, $V_{CM} = 0, \text{V}$</td>
<td>75</td>
<td>150</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$dV_{OS}/dT$</td>
<td>$T_A = -40^\circ, \text{C}$ to $125^\circ, \text{C}$</td>
<td>0.1</td>
<td>2</td>
<td>µV/°C</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>$T_A = -40^\circ, \text{C}$ to $125^\circ, \text{C}$</td>
<td>0.2</td>
<td>1</td>
<td>µV/V</td>
<td></td>
</tr>
<tr>
<td><strong>INPUT BIAS CURRENT</strong></td>
<td></td>
<td>±3</td>
<td>±10</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>$I_B$</td>
<td>$T_A = -40^\circ, \text{C}$ to $85^\circ, \text{C}$</td>
<td></td>
<td>±500</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>$T_A = -40^\circ, \text{C}$ to $125^\circ, \text{C}$</td>
<td>±3</td>
<td>±10</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td><strong>NOISE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$e_n$</td>
<td>$f = 0.1, \text{Hz}$ to $10, \text{Hz}$, $V_S = \pm 18, \text{V}$, $V_{CM} = 0, \text{V}$</td>
<td>250</td>
<td>nVpp</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Noise Density</td>
<td>$f = 1, \text{kHz}$, $V_S = \pm 18, \text{V}$, $V_{CM} = 0, \text{V}$</td>
<td>4</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_n$</td>
<td>$f = 10, \text{kHz}$, $V_S = \pm 18, \text{V}$, $V_{CM} = 0, \text{V}$</td>
<td>3.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>INPUT VOLTAGE RANGE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Common-mode voltage range</td>
<td>$(V-) + 3$ ≤ $V_{CM} ≤ (V+) - 3$, $V_S &lt; 10, \text{V}$</td>
<td>104</td>
<td>114</td>
<td>V</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>$V_S = \pm 18, \text{V}$, $V_{CM} = 0, \text{V}$</td>
<td>114</td>
<td>126</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$(V-) + 3$ ≤ $V_{CM} ≤ (V+) - 3$, $V_S ≥ 10, \text{V}$</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$(V-) + 3$ ≤ $V_{CM} ≤ (V+) - 3$, $V_S ≥ 10, \text{V}$</td>
<td></td>
<td>110</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>INPUT IMPEDANCE</strong></td>
<td>$10^{13}$</td>
<td></td>
<td>pF</td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>Differential</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OPEN-LOOP GAIN</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{OL}$</td>
<td>Open-loop voltage gain</td>
<td>$(V-) + 3$ ≤ $V_S ≤ (V+) - 3$, $R_L = 1, \text{k}\Omega$</td>
<td>120</td>
<td>126</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$T_A = -40^\circ, \text{C}$ to $125^\circ, \text{C}$</td>
<td></td>
<td>114</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>FREQUENCY RESPONSE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-bandwidth product</td>
<td>$G = +1$</td>
<td>22</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>SR</td>
<td>Slew rate</td>
<td>$G = -1$</td>
<td>20</td>
<td>28</td>
<td>V/µs</td>
</tr>
<tr>
<td>$f_S$</td>
<td>Settling time</td>
<td>$\pm 0.01%$, 10-V step, $G = -1$, $C_L = 100, \text{pF}$</td>
<td>550</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$G = -1$, 0.00075% (16-bit), 10-V step, $C_L = 100, \text{pF}$</td>
<td>850</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overload recovery time</td>
<td>Gain = $-10$</td>
<td></td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>THD+N</td>
<td>Total Harmonic Distortion + Noise</td>
<td>$G = +1$, $f = 1, \text{kHz}$</td>
<td>0.00004%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_O = 3, V_{RMS}$, $R_L = 600, \Omega$</td>
<td>−128</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Electrical Characteristics (continued)

at $V_S = \pm 4$ V to $\pm 18$ V, $T_A = 25^\circ$C, $R_L = 10$ kΩ connected to midsupply, and $V_{CM} = V_{OUT} = $ midsupply (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUTPUT</td>
<td>Voltage output swing</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_L = 1$ kΩ, $A_{OL} &gt; 120$ dB</td>
<td>(V–) + 3</td>
<td>(V+) – 3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_L = 1$ kΩ, $A_{OL} &gt; 114$ dB</td>
<td>(V–) + 3</td>
<td>(V+) – 3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A = -40^\circ$C to $125^\circ$C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>Output current</td>
<td></td>
<td></td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$[V_S - V_{OUT}] &lt; 3$ V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Short-circuit current</td>
<td>±55</td>
<td>±65</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$C_{LOAD}$</td>
<td>Capacitive load drive</td>
<td></td>
<td></td>
<td>See Typical Characteristics</td>
<td></td>
</tr>
<tr>
<td>$Z_O$</td>
<td>Open-loop output impedance</td>
<td></td>
<td></td>
<td>See Typical Characteristics</td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td>Specified voltage</td>
<td>±4</td>
<td>±18</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_Q$</td>
<td>Quiescent current (per amplifier)</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$I_{OUT} = 0$ A</td>
<td>4.8</td>
<td>5.2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_A = -40^\circ$C to $125^\circ$C</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
6.6 Typical Characteristics

At $T_A = 25^\circ C$, $V_S = \pm 15\, V$, $R_L = 10\, k\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

---

**Figure 1. Input Voltage Noise Density vs Frequency**

**Figure 2. Integrated Input Voltage Noise vs Bandwidth**

**Figure 3. Total Harmonic Distortion + Noise Ratio vs Frequency**

**Figure 4. Total Harmonic Distortion + Noise Ratio vs Amplitude**

**Figure 5. 0.1-Hz to 10-Hz Noise**

**Figure 6. Offset Voltage Production Distribution**
Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $R_L = 10\ \Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

---

**Figure 7. Offset Voltage Drift Production Distribution**

---

**Figure 8. Offset Voltage vs Common-Mode Voltage**

---

**Figure 9. Offset Voltage vs Common-Mode Voltage**

---

**Figure 10. $V_{OS}$ Warmup**

---

**Figure 11. Offset Voltage vs Temperature**

---

**Figure 12. Input Bias Current and Offset Current vs Supply Voltage**
Typical Characteristics (continued)

At $T_A = 25°C$, $V_S = \pm 18\, \text{V}$, $R_L = 10\, \text{k}Ω$ connected to midsupply, and $V_{\text{CM}} = V_{\text{OUT}} = \text{midsupply}$, unless otherwise noted.

---

**Figure 13. Input Bias Current vs Common-Mode Voltage**

---

**Figure 14. Input Bias Current vs Temperature**

---

**Figure 15. Normalized Quiescent Current vs Time**

---

**Figure 16. Quiescent Current vs Temperature**

---

**Figure 17. Quiescent Current vs Supply Voltage**

---

**Figure 18. Output Voltage Swing vs Output Current**
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = \pm 18 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{ midsupply}$, unless otherwise noted.

---

Figure 19. Output Voltage Swing vs Output Current

Figure 20. Power-Supply Rejection Ratio vs Frequency

Figure 21. Common-Mode Rejection Ratio vs Frequency

Figure 22. Power-Supply Rejection Ratio vs Temperature

Figure 23. Common-Mode Rejection Ratio vs Temperature

Figure 24. Open-Loop Gain and Phase vs Frequency
Typical Characteristics (continued)

At $T_A = 25^\circ C$, $V_S = \pm 18$ V, $R_L = 10$ k$\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} =$ midsupply, unless otherwise noted.

![Figure 25. Closed-Loop Gain vs Frequency](image)

![Figure 26. Open-Loop Gain vs Temperature](image)

![Figure 27. Open-Loop Output Impedance vs Frequency](image)

![Figure 28. Small-Signal Overshoot vs Capacitive Load](image)

![Figure 29. No Phase Reversal](image)

![Figure 30. Positive Overload Recovery](image)
Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\,\text{V}$, $R_L = 10\,\text{k}\Omega$ connected to midsupply, and $V_{CM} = V_{OUT} =$ midsupply, unless otherwise noted.

**Figure 31. Negative Overload Recovery**

**Figure 32. Small-Signal Step Response**

**Figure 33. Small-Signal Step Response**

**Figure 34. Large-Signal Step Response**

**Figure 35. Large-Signal Step Response**

**Figure 36. Large-Signal Positive Settling Time**
Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 18\text{ V}$, $R_L = 10\kOmega$ connected to midsupply, and $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

Figure 37. Large-Signal Positive Settling Time

Figure 38. Large-Signal Negative Settling Time

Figure 39. Large-Signal Negative Settling Time

Figure 40. Short-Circuit Current vs Temperature
7 Detailed Description

7.1 Overview

The OPA827 is a unity-gain stable, precision operational amplifier with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate.

7.2 Functional Block Diagram

![Functional Block Diagram]

7.3 Feature Description

The OPA827 is a precision JFET amplifier with low input offset voltage, low input offset voltage drift and low noise. High impedance inputs make the OPA827 ideal for high source impedance applications and transimpedance applications.

7.3.1 Operating Voltage

The OPA827 series of op amps can be used with single or dual supplies from an operating range of $V_S = 8 \text{ V (±4 V)}$ and up to $V_S = 36 \text{ V (±18 V)}$. This device does not require symmetrical supplies; it only requires a minimum supply voltage of 8 V. Supply voltages higher than 40 V (±20 V) can permanently damage the device; see Absolute Maximum Ratings. Key parameters are specified over the operating temperature range, $T_A = –40°C$ to 125°C. Key parameters that vary over the supply voltage or temperature range are shown in Typical Characteristics of this data sheet.

7.3.2 Noise Performance

Figure 41 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA827 (GBW = 22 MHz) and OPA211 (GBW = 80 MHz) are both shown in this example with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA827 family has both low voltage noise and lower current noise because of the FET input of the op amp. Very low current noise allows for excellent noise performance with source impedances greater than 10 kΩ. OPA211 has lower voltage noise and higher current noise. The low voltage noise makes the OPA211 a better choice for low source impedances (less than 2 kΩ). For high source impedance, current noise may dominate, and makes the OPA827 series amplifier the better choice.
Feature Description (continued)

The equation in Figure 41 shows the calculation of the total circuit noise, with these parameters:

- $e_n =$ voltage noise
- $i_n =$ current noise
- $R_S =$ source impedance
- $k =$ Boltzmann's constant $= 1.38 \times 10^{-23}$ J/K
- $T =$ temperature in kelvins

For more details on calculating noise, see Basic Noise Calculations.

![Figure 41. Noise Performance of the OPA827 and OPA211 in Unity-Gain Buffer Configuration](image)

7.3.3 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on the overall noise performance of the op amp. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 41. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 42 illustrates both noninverting (A) and inverting (B) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components.

The feedback resistor values can generally be chosen to make these noise sources negligible.

**NOTE**

Low-impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations shown in both configurations in Figure 42.
Feature Description (continued)

A) Noise in Noninverting Gain Configuration

\[ E_0^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_1^2 + e_2^2 + (i_n R_3)^2 + e_3^2 + (i_n R_2)^2 \left(1 + \frac{R_2}{R_1}\right)^2 \]

Where \( e_2 = \sqrt{4kT R_s} \cdot \left(1 + \frac{R_2}{R_1}\right) \) = thermal noise of \( R_s \)

\( e_1 = \sqrt{4kT R_1} \cdot \left(\frac{R_2}{R_1}\right) \) = thermal noise of \( R_1 \)

\( e_2 = \sqrt{4kT R_2} \) = thermal noise of \( R_2 \)

B) Noise in Inverting Gain Configuration

\[ E_0^2 = \left(1 + \frac{R_2}{R_1 + R_s}\right)^2 e_1^2 + e_2^2 + (i_n R_3)^2 + e_3^2 \]

Where \( e_2 = \sqrt{4kT R_s} \cdot \left(\frac{R_2}{R_1 + R_s}\right) \) = thermal noise of \( R_s \)

\( e_1 = \sqrt{4kT R_1} \cdot \left(\frac{R_2}{R_1 + R_s}\right) \) = thermal noise of \( R_1 \)

\( e_2 = \sqrt{4kT R_2} \) = thermal noise of \( R_2 \)

For the OPA827 series op amps at 1kHz, \( e_n = 4nV/\sqrt{Hz} \) and \( i_n = 2.2fA/\sqrt{Hz} \).

7.3.4 Total Harmonic Distortion Measurements

The OPA827 series op amps have excellent distortion characteristics. THD + Noise is below 0.0001% \((G = +1, V_O = 3 V_{RMS})\) throughout the audio frequency range, 20 Hz to 20 kHz, with a 600-\(\Omega\) load (see Figure 3).

The distortion produced by the OPA827 series is below the measurement limit of many commercially available testers. However, a special test circuit (illustrated in Figure 43) can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. Figure 43 shows a circuit that causes the op amp distortion to be 101 times greater than that distortion normally produced by the op amp. The addition of \(R_3\) to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101.

NOTE

the input signal and load applied to the op amp are the same as with conventional feedback without \(R_3\). The value of \(R_3\) must be kept small to minimize its effect on the distortion measurements.
Feature Description (continued)

The validity of this technique can be verified by duplicating measurements at high gain and high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion and noise analyzer, which greatly simplifies such repetitive measurements. This measurement technique, however, can be performed with manual distortion measurement instruments.

![Distortion Test Circuit](image)

Figure 43. Distortion Test Circuit

7.3.5 Capacitive Load and Stability

The combination of gain bandwidth product (GBW) and near constant open-loop output impedance (Z\textsubscript{O}) over frequency gives the OPA827 the ability to drive large capacitive loads. Figure 44 shows the OPA827 connected in a buffer configuration (G = +1) while driving a 2.2-\(\mu\)F ceramic capacitor (with an ESR value of approximately 0 \(\Omega\)). The small overshoot and fast settling time are results of good phase margin. This feature provides superior performance compared to the competition. Figure 44 and Figure 45 were taken without any resistive load in parallel to shorten the ringing time.

In Figure 45, the OPA827 is driving a 2.2-\(\mu\)F tantalum capacitor. A relatively small ESR that is internal to the capacitor additionally improves phase margin and provides an output waveform with no ringing and minimal overshoot. Figure 45 shows a stable system that can be used in almost any application.

Capacitive load drive depends on the gain and overshoot requirements of the application. Capacitive loads limit the bandwidth of the amplifier. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see Figure 28).

7.3.6 Phase-Reversal Protection

The OPA827 family has internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA827 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see Figure 29).
Feature Description (continued)

7.3.7 Transimpedance Amplifier

The gain bandwidth, low voltage noise, and current noise of the OPA827 series make them ideal wide bandwidth transimpedance amplifiers in a photo-conductive application. High transimpedance gains with feedback resistors greater than 100 kΩ benefit from the low input current noise (2.2 fA/Hz) of the JFET input. Low voltage noise is important because photodiode capacitance causes the effective noise gain in the circuit to increase at high frequencies. Total input capacitance of the circuit limits the overall gain bandwidth of the amplifier and is addressed below. Figure 46 shows a photodiode transimpedance application.

7.3.7.1 Key Transimpedance Points

- The total input capacitance (C_{TOT}) consists of the photodiode junction capacitance, and both the common-mode and differential input capacitance of the operational amplifier.
- The desired transimpedance gain, V_{OUT} = I_D R_F.
- The Unity Gain Bandwidth Product (UGBW) (22 MHz for the OPA827).

With these three variables set, the feedback capacitor value (C_F) can be calculated to ensure stability. C_{STRAY} is the parasitic capacitance of the PCB and passive components, which is approximately 0.5 pF.

To ensure 45° phase margin, the minimal amount of feedback capacitance can be calculated using Equation 1.

\[
C_F \left( \frac{1}{4\pi R_F \text{UGBW}} \right) \left( 1 + \sqrt{1 + (8\pi C_{TOT} R_F \text{UGBW})} \right)
\]  

(1)
Feature Description (continued)

Bandwidth \( f_{3\text{dB}} \) can be calculated using Equation 2.

\[
f_{3\text{dB}} = \frac{\text{UGBW}}{2\pi R_F(C_{\text{TOT}})} \text{ Hz}
\]

(2)

These equations result in maximum transimpedance bandwidth. For additional information, refer to Compensate Transimpedance Amplifiers Intuitively, available for download at www.ti.com.

![Figure 46. Transimpedance Amplifier](image)

**NOTES:**
1. \( C_T \) is optional to prevent gain peaking.
2. \( C_{\text{STRAY}} \) is the stray capacitance of \( R_F \)
   (typically, 2pF for a surface-mount resistor).

![Figure 47. Equivalent Schematic (Single-Channel)](image)

### 7.4 Device Functional Modes

The OPA827 has a single functional mode and is operational when the power-supply voltage is greater than 4 V (±2 V). The maximum power supply voltage for the OPA827 is 36 V (±18 V).
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The OPA827 is a unity-gain stable, operational amplifier with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1-µF capacitors are adequate. Designers can easily take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision data converters.

8.2 Typical Application

8.2.1 Design Requirements
Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA827 is ideally suited to construct high-speed, high-precision active filters. Figure 48 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:
• Gain = 5 V/V (inverting gain)
• Low-pass cutoff frequency = 25 kHz
• Second-order Chebyshev filter response with 3-dB gain peaking in the pass band

8.2.2 Detailed Design Procedure
The infinite-gain multiple-feedback circuit for a low-pass network function is shown in. Use Equation 3 to calculate the voltage transfer function.

\[
\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_3 R_5 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5}
\]  

(3)

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by Equation 4.

\[
\text{Gain} = \frac{R_4}{R_1}
\]

\[
f_C = \frac{1}{2\pi \sqrt{(1/R_3 R_4 C_2 C_5)}}
\]  

(4)
Typical Application (continued)

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. WEBENCH® Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH Design Center, WEBENCH Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.2.3 Application Curve

8.3 System Examples

The OPA827 is well-suited for phase-lock loop (PLL) applications because of the low voltage offset, low noise, and wide gain bandwidth. Figure 50 illustrates an example of the OPA827 in this application. The first amplifier (OPA827) provides the loop low-pass, active filter function, while the second amplifier (OPA211) serves as a scaling amplifier. This second stage amplifies the DC error voltage to the appropriate level before it is applied to the voltage-controlled oscillator (VCO).

Operational amplifiers used in PLL applications are often required to have low voltage offset. As with other DC levels generated in the loop, a voltage offset applied to the VCO is interpreted as a phase error. An operational amplifier with inherently low voltage offset helps reduce this source of error. Also, any noise produced by the operational amplifiers modulates the voltage applied to the VCO and limits the spectral purity of the oscillator output. The VCO generates noise-related, random phase variations of its own, but this characteristic becomes worse when the input voltage source noise is included. This noise appears as random sideband energy that can limit system performance. The very low flicker noise (1/f) and current noise (In) of the OPA827 help to minimize the operational amplifier contribution to the phase noise.
8.3.1 OPA827 Used as an I/V Converter

The OPA827 series of operation amplifiers have low current noise and offset voltage that make these devices a great choice for an I/V converter. DAC8811 is a single-channel, current output, 16-bit digital-to-analog converter (DAC). The \( I_{\text{OUT}} \) terminal of the DAC is held at a virtual GND potential by the use of the OPA827 as an external I/V converter op amp. The R-2R ladder is connected to an external reference input (\( V_{\text{REF}} \)) that determines the DAC full-scale current. The external reference voltage can vary in a range of \(-15 \text{ V} \) to \(15 \text{ V} \), thus providing bipolar \( I_{\text{OUT}} \) current operation. By using the OPA827 as an external I/V converter in conjunction with the internal DAC8811 \( R_{\text{FB}} \) resistor, output voltage ranges of \(-V_{\text{REF}} \) to \(+V_{\text{REF}} \) can be generated.

When using an external I/V converter and the DAC8811 \( R_{\text{FB}} \) resistor, the DAC output voltage is given by Equation 5.

\[
V_{\text{OUT}} = \frac{-V_{\text{REF}} \times \text{CODE}}{65536}
\]  

(5)

NOTE

The DAC output impedance as seen looking into the \( I_{\text{OUT}} \) terminal changes versus code. The low offset voltage of the OPA827 minimizes the error propagated from the DAC.

For a current-to-voltage design (see Figure 51), the DAC8811 \( I_{\text{OUT}} \) pin and the inverting node of the OPA827 must be as short as possible and adhere to good PCB layout design. For each code change on the output of the DAC, there is a step function. If the parasitic capacitance is excessive at the inverting node, then gain peaking is possible. For circuit stability, two compensation capacitors, \( C_1 \) and \( C_2 \) (4 pF to 20 pF typical) can be added to the design.

Some applications require full four-quadrant multiplying capabilities or a bipolar output swing. As shown in Figure 51, the OPA827 is added as a summing amp and has a gain of 2x that widens the output span to 20 V. A four-quadrant multiplying circuit is implemented by using a 10-V offset of the reference voltage to bias the OPA827.
9 Power Supply Recommendations

The OPA827 is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the Absolute Maximum Ratings.

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the Absolute Maximum Ratings.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Layout.
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.

- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.

- Place the external components as close to the device as possible. As illustrated in Figure 52, keeping RF and RG close to the inverting input minimizes parasitic capacitance.

- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

- For best performance, TI recommends cleaning the PCB following board assembly.

- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example

![Figure 52. Operational Amplifier Board Layout for Noninverting Configuration](image)

Run the input traces as far away from the supply lines as possible.

Place components close to device and to each other to reduce parasitic errors.

Use low-ESR, ceramic bypass capacitor.

Ground (GND) plane on another layer.

Use low-ESR, ceramic bypass capacitor.
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI’S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT
CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES
OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER
ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

For development support see the following:
• WEBENCH® Filter Designer
• OPA211
• DAC8811

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:
Compensate Transimpedance Amplifiers Intuitively (SBOA055)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper
right corner, click on Alert me to register and receive a weekly digest of any product information that has
changed. For change details, review the revision history included in any revised document.

11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective
contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of
Use.

TI E2E™ Online Community  TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration
among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help
solve problems with fellow engineers.

Design Support  TI's Design Support Quickly find helpful E2E forums along with design support tools and
contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam
during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
**PACKAGING INFORMATION**

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA827AID</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 827 A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA827AIDG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 827 A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA827AIDGKR</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>NSP</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA827AIDGKT</td>
<td>ACTIVE</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>NSP</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA827AIDR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 827 A</td>
<td>Samples</td>
</tr>
<tr>
<td>OPA827AIDRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>OPA 827 A</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
# TAPE AND REEL INFORMATION

## TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA827AIDGKR</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA827AIDGKT</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>180.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>OPA827AIDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
</tbody>
</table>
**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA827AIDGKR</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA827AIDGKT</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>250</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
<tr>
<td>OPA827AIDR</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
   ▶ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
   ▶ Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

4073329/E 05/06
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that TI is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer’s risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Audio</td>
<td>Automotive and Transportation</td>
</tr>
<tr>
<td>Amplifiers</td>
<td>Communications and Telecom</td>
</tr>
<tr>
<td>Data Converters</td>
<td>Computers and Peripherals</td>
</tr>
<tr>
<td>DLP® Products</td>
<td>Consumer Electronics</td>
</tr>
<tr>
<td>DSP</td>
<td>Energy and Lighting</td>
</tr>
<tr>
<td>Clocks and Timers</td>
<td>Industrial</td>
</tr>
<tr>
<td>Interface</td>
<td>Medical</td>
</tr>
<tr>
<td>Logic</td>
<td>Security</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Space, Avionics and Defense</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Video and Imaging</td>
</tr>
<tr>
<td>RFID</td>
<td><a href="http://www.ti-rfid.com">www.ti-rfid.com</a></td>
</tr>
<tr>
<td>OMAP Applications Processors</td>
<td><a href="http://www.ti.com/omap">www.ti.com/omap</a></td>
</tr>
<tr>
<td>Wireless Connectivity</td>
<td>TI E2E Community</td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2016, Texas Instruments Incorporated