PGA400-Q1 Pressure-Sensor Signal Conditioner

1 Features

- Analog features
  - Analog front-end for resistive bridge sensors
  - Self-oscillating demodulator for capacitive sensors
  - On-chip temperature sensor
  - Programmable gain
  - 16-bit, 1-MHz sigma-delta analog-to-digital converter for signal channel
  - 10-bit sigma-delta analog-to-digital converter for temperature channel
  - Two 12-bit digital-to-analog outputs
- Digital features
  - Microcontroller core
    - 10-MHz 8051 WARP core
      - 2 clocks per instruction cycle
    - On-chip oscillator
  - Memory
    - 8KB of OTP memory
    - 89 bytes of EEPROM
    - 256 bytes data SRAM
- Peripheral features
  - Serial peripheral interface (SPI)
  - Inter-integrated circuit (I^2C)
  - One-wire interface (OWI)
  - Two input capture ports
  - Two output compare ports
  - Software watchdog timer
  - Oscillator watchdog
  - Power management control
  - Analog low-voltage detect
- General features
  - AEC-Q100 qualified with the following results:
    - Device temperature grade 1: –40°C to +125°C ambient operating temperature
    - Device HBM ESD classification level 2
    - Device HBM ESD classification level C3B
  - Power supply: 4.5-V to 5.5-V operational, –5.5-V to 16-V absolute maximum

2 Applications

- Pressure sensor-signal conditioning
- Level sensor-signal conditioning
- Humidity sensor-signal conditioning

3 Description

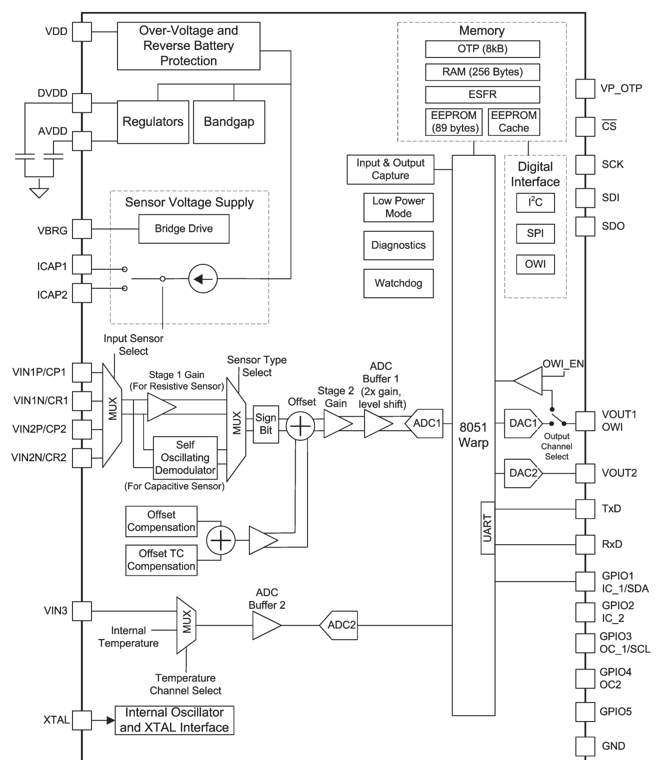
The PGA400-Q1 is an interface device for piezoresistive, strain gauge, and capacitive-sense elements. The device incorporates the analog front end (AFE) that directly connects to the sense element and has voltage regulators and an oscillator. The device also includes a sigma-delta analog-to-digital converter (ADC), 8051 WARP core microprocessor, and OTP memory. Sensor compensation algorithms can be implemented in software. The PGA400-Q1 also includes two digital-to-analog converter (DAC) outputs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA400QRHHRQ1	VQFN (36)	6.00 mm × 6.00 mm
PGA400QYZRQ1	WCSP (36)	3.65 mm × 3.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

4 Device and Documentation Support

4.1 Documentation Support

4.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PGA400-Q1 EVM* user guide
- Texas Instruments, *PGA400-Q1* errata
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application report

4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

4.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

4.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA400QRHHRQ1	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	PGA400Q RHH-Q100	Samples
PGA400QYZSRQ1	ACTIVE	DSBGA	YZS	36	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	PGA400	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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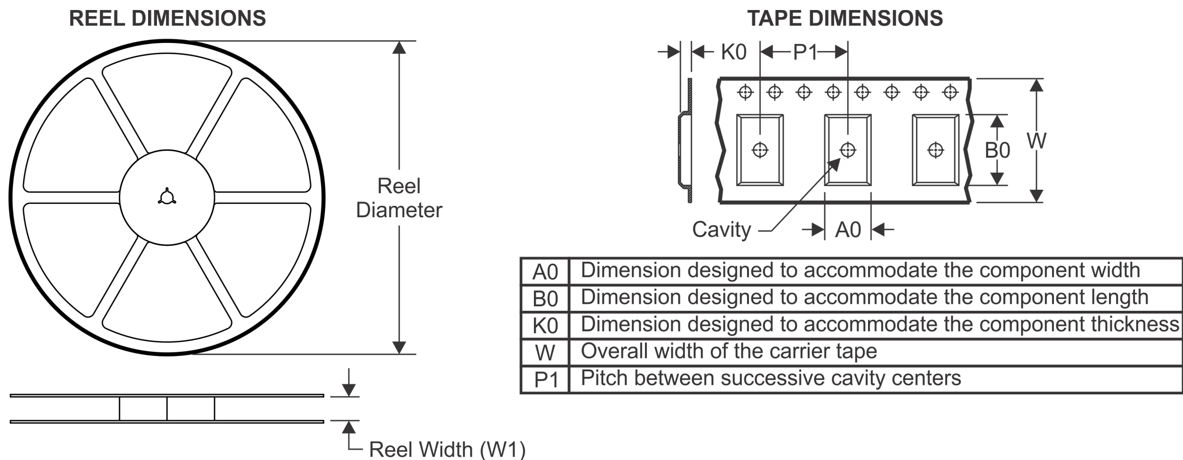
OTHER QUALIFIED VERSIONS OF PGA400-Q1 :

- Enhanced Product: PGA400-EP

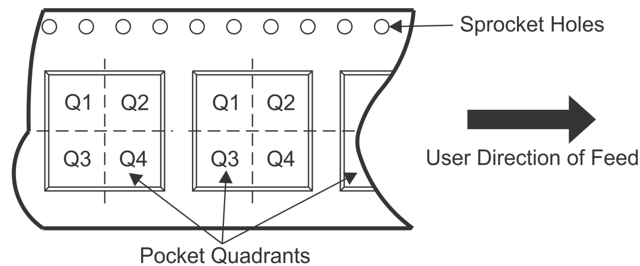
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



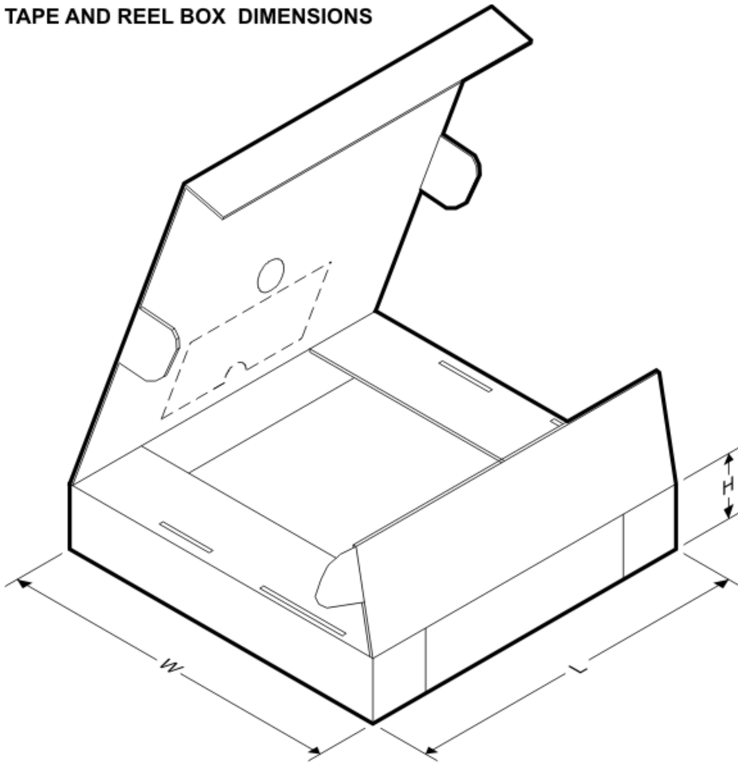
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA400QRHHRQ1	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
PGA400QYZSRQ1	DSBGA	YZS	36	1500	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1

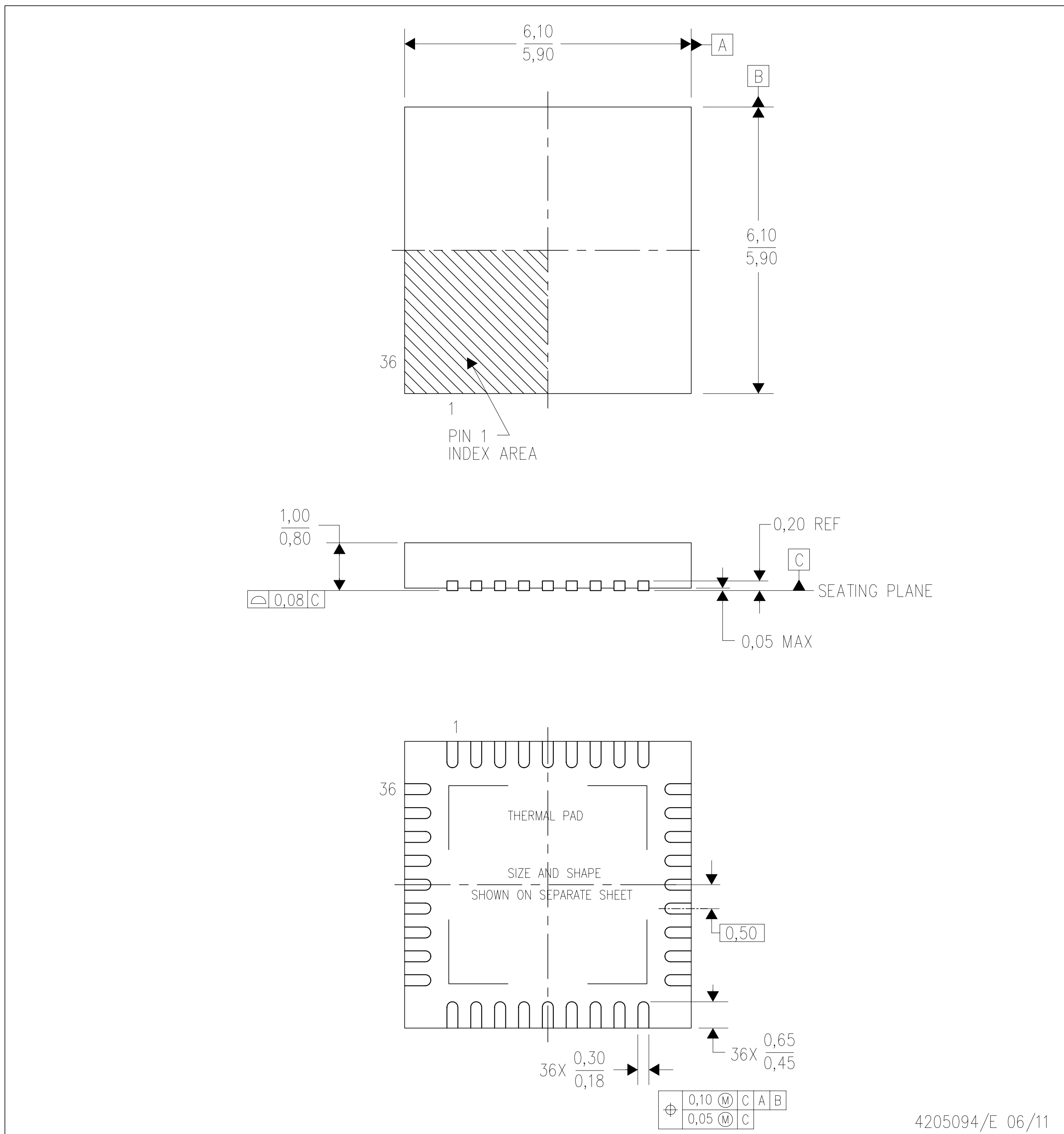
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA400QRHHRQ1	VQFN	RHH	36	2500	367.0	367.0	38.0
PGA400QYZSRQ1	DSBGA	YZS	36	1500	210.0	185.0	35.0

RHH (S-PVQFN-N36) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

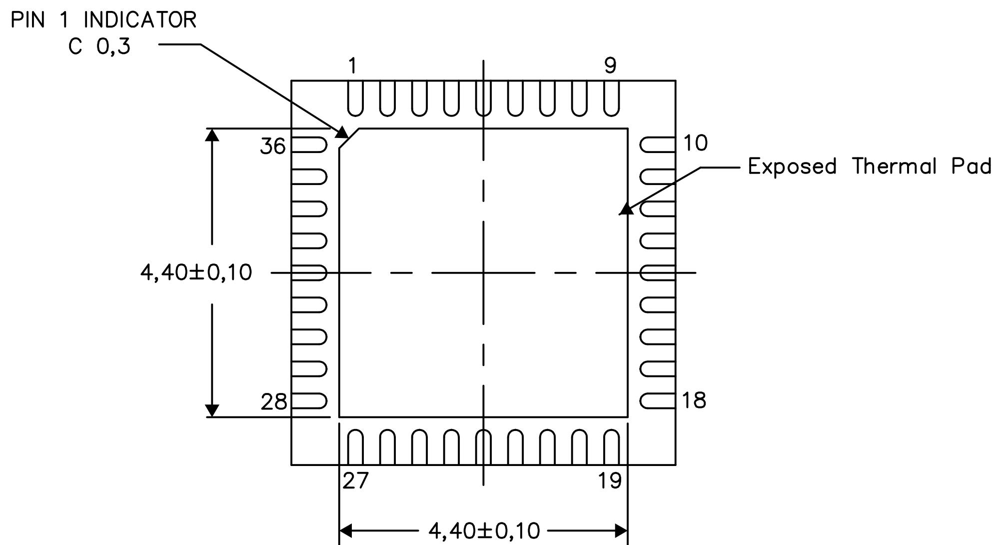
RHH (S-PVQFN-N36) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



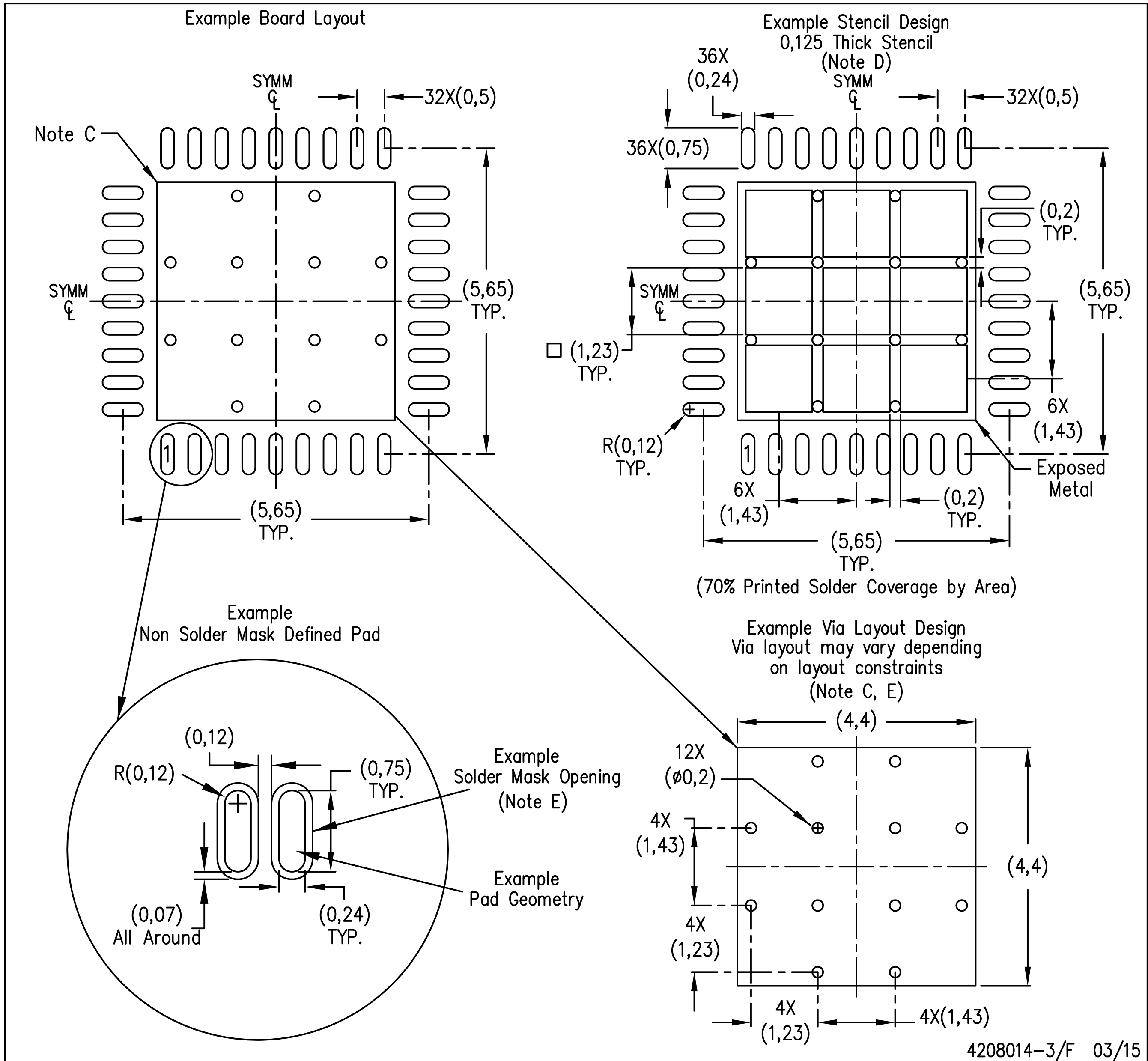
Bottom View

Exposed Thermal Pad Dimensions

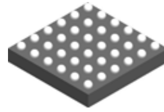
4206362-5/M 11/13

NOTE: All linear dimensions are in millimeters

RHH (S-PVQFN-N36) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.



B
E
A
BALL A1
CORNER
D
0.625 MAX
C
SEATING PLANE
0.225
0.175
BALL TYP
0.05 C
2.5
TYP
SYMM
2.5
TYP
F
E
D
C
B
A
1 2 3 4 5 6
SYMM
0.5 TYP
36X ∅ 0.3
0.2
0.015 Ⓜ C A B
0.5 TYP

D: Max = 3.693 mm, Min =3.632 mm
E: Max = 3.693 mm, Min =3.632 mm

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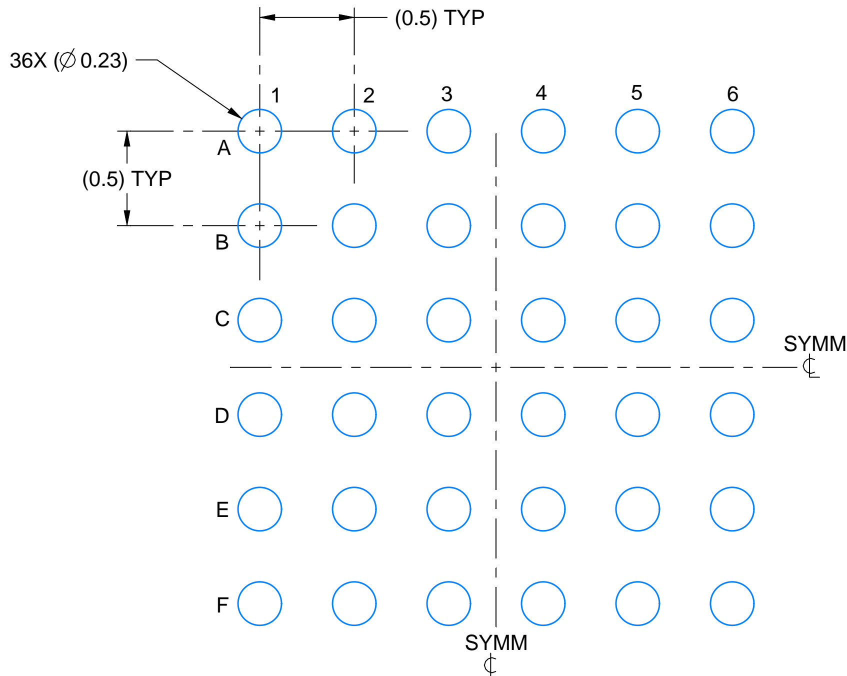
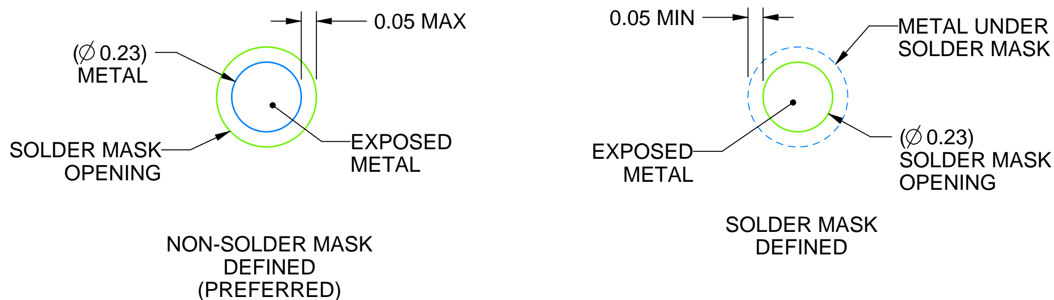
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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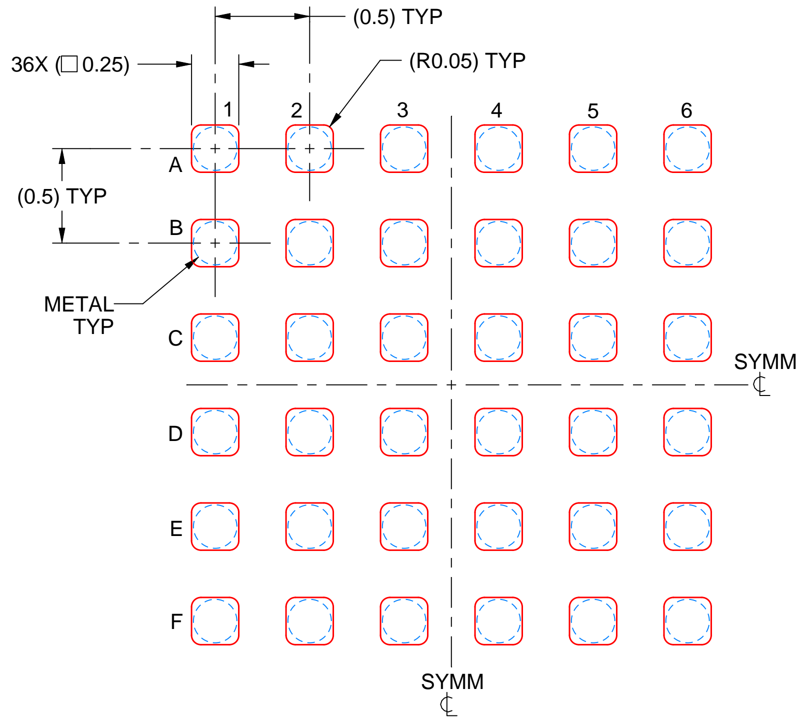
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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