PGA900 Programmable Resistive Sensing Conditioner With Digital and Analog Outputs

1 Features

- High accuracy, low noise, low power, small size resistive sensing signal conditioner
- User-programmable temperature and nonlinearity compensation
- On-chip ARM® Cortex® M0 microprocessor allows users to develop and implement calibration software
- One-wire interface enables the communication through power supply pin without using additional lines
- On-chip power management accepts wide power supply voltage from 3.3 V to 30 V
- Operating temperature range: –40°C to +150°C
- Memory:
  - 8-kB software memory
  - 128 bytes EEPROM
  - 1-kB data SRAM
- Accommodates sensor sensitivities from 1 mV/V to 135 mV/V
- Two individual analog-front end (AFE) chains, each including:
  - Low-noise programmable gain amplifier
  - 24-bit sigma-delta analog-to-digital converter
- Built-in internal temperature sensor with option to use external temperature sensor
- 14-bit DAC with programmable gain amplifier
- Output options:
  - Ratiometric and absolute voltage output
  - 4- to 20-mA current loop interface
  - One-wire interface (OWI) over power line
  - PWM output
  - Serial peripheral interface (SPI)
  - Inter-integrated circuit (I^2C)
- Depletion MOSFET gate driver
- Diagnostic functions

2 Applications

- Pressure sensor transmitters and transducers
- Liquid level meters and flow meters
- Weight scales, load meters, and strain gauges
- Thermocouples, thermistors, and 2-wire resistance thermometers (RTD)
- Resistive field transmitters

3 Description

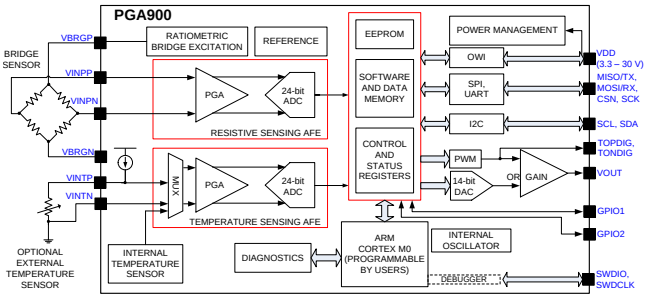
The PGA900 is a signal conditioner for resistive sensing applications. It can accommodate various sensing element types. The PGA900 conditions its input signals by amplification and digitization through two analog front end channels. With the user programmed software in the on-chip ARM Cortex M0 processor, the PGA900 can perform linearization, temperature compensation, and other user defined compensation algorithms. The conditioned signal can be output as ratiometric voltage, absolute voltage, 4- to 20-mA current loop or PWM. The data and configuration registers can also be accessed through SPI, I^2C, UART, and two GPIO ports. In addition, the unique OWI allows communication and configuration through the power supply pin without using additional lines. The PGA900 operating voltage is from 3.3 V to 30 V and it can operate in temperatures from –40°C to +150°C.

Device Information(1)

NUMBER	PACKAGE	BODY SIZE (NOM)
PGA900	VQFN (36)	6.00 mm × 6.00 mm
	DSBGA (36)	3.66 mm × 3.66 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

PGA900 Simplified Block Diagram



4 Device and Documentation Support

4.1 Documentation Support

4.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PGA900 as a Capacitive Load Driver* application note
- Texas Instruments, *PGA900 as a 4- to 20-mA Current Loop Transmitter* application note
- Texas Instruments, *Understanding Open Loop Gain of the PGA900 DAC Gain Amplifier* application note
- Texas Instruments, *Connecting PGA900 Instrumentation Amplifier to Resistive Bridge Sensor* application note
- Texas Instruments, *Understanding Open Loop Output Impedance of the PGA900 DAC Gain Amplifier* application note
- Texas Instruments, *System Noise Analysis of a Resistive Bridge Pressure Sensor Connected to the PGA900* application note
- Texas Instruments, *PGAxxxEVM-034* user's guide
- Texas Instruments, *PGA900 Software* user's guide
- Texas Instruments, *PGA900 Pressure and Temperature Sensor Signal Conditioner* user's guide

4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

4.4 Trademarks

E2E is a trademark of Texas Instruments.
ARM, Cortex are registered trademarks of ARM Ltd.
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4.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

4.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA900ARHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PGA900A RHH	Samples
PGA900ARHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PGA900A RHH	Samples
PGA900AYZSR	ACTIVE	DSBGA	YZS	36	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 150	PGA900A YZS	Samples
PGA900AYZST	ACTIVE	DSBGA	YZS	36	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 150	PGA900A YZS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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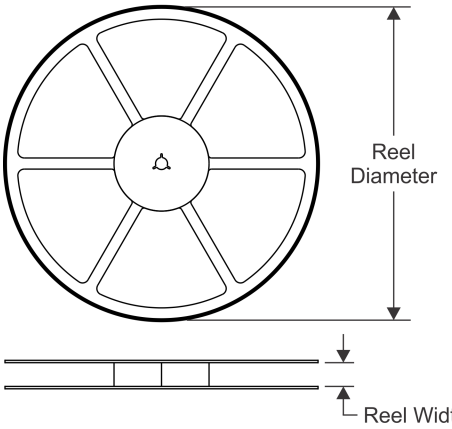
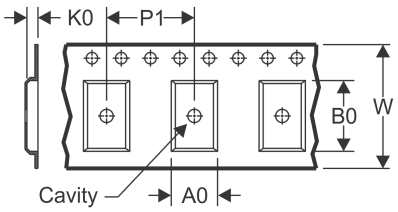
TAPE AND REEL INFORMATION

REEL DIMENSIONS

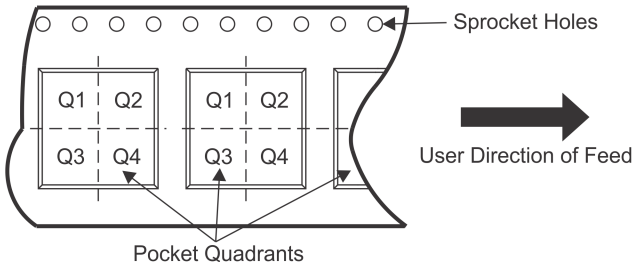


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

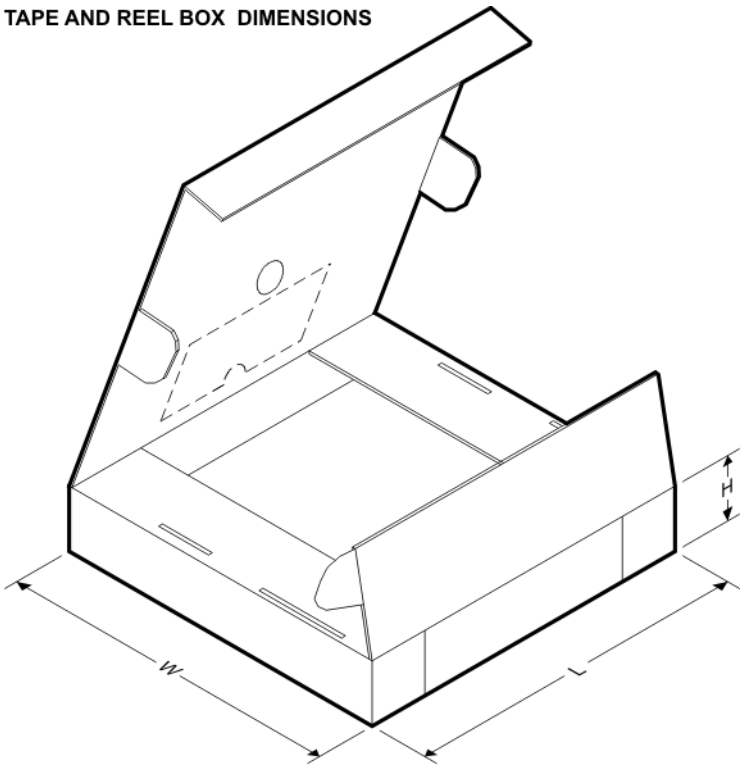
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA900ARHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
PGA900ARHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
PGA900AYZST	DSBGA	YZS	36	250	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1

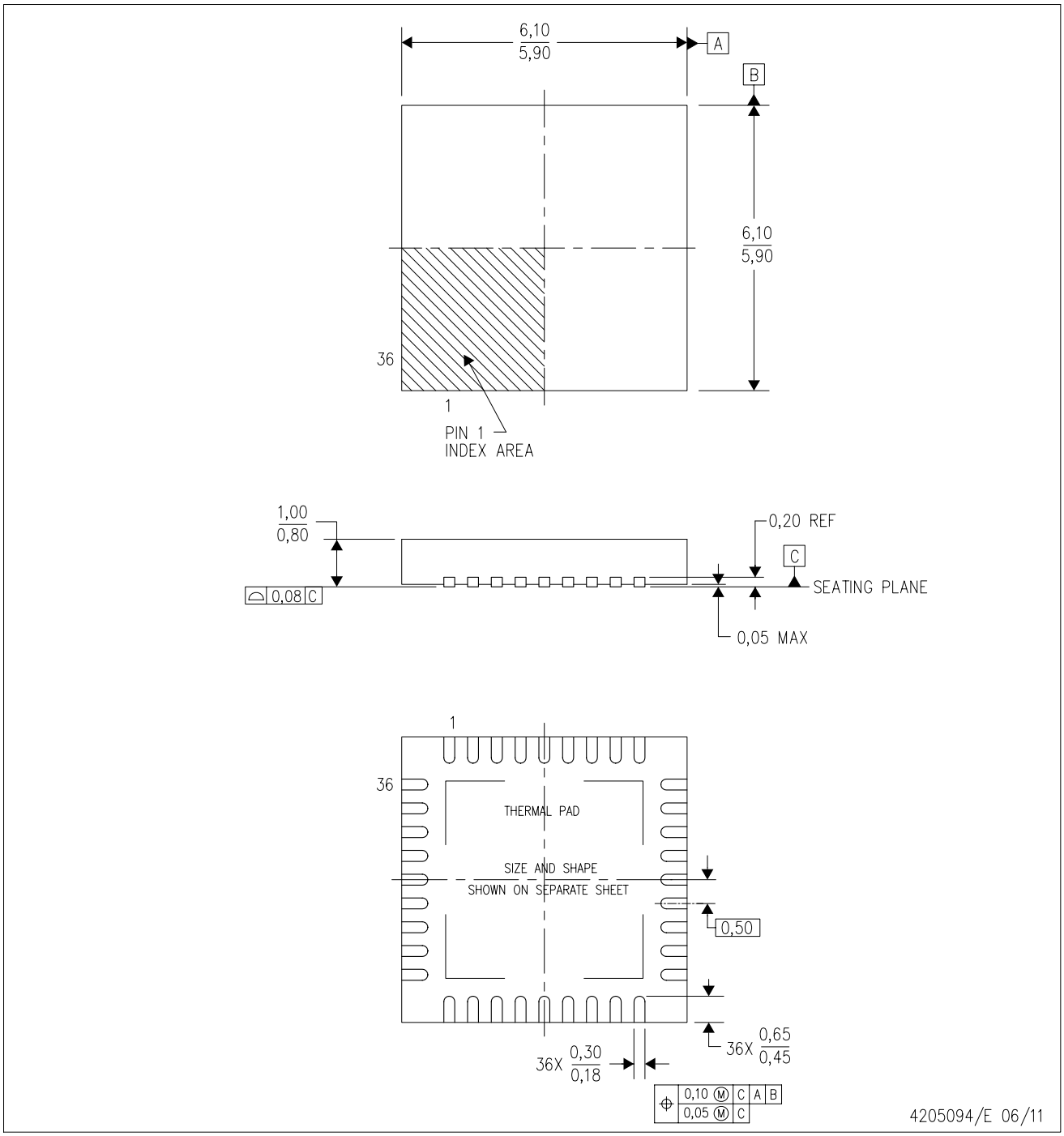
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA900ARHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
PGA900ARHHT	VQFN	RHH	36	250	210.0	185.0	35.0
PGA900AYZST	DSBGA	YZS	36	250	210.0	185.0	35.0

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

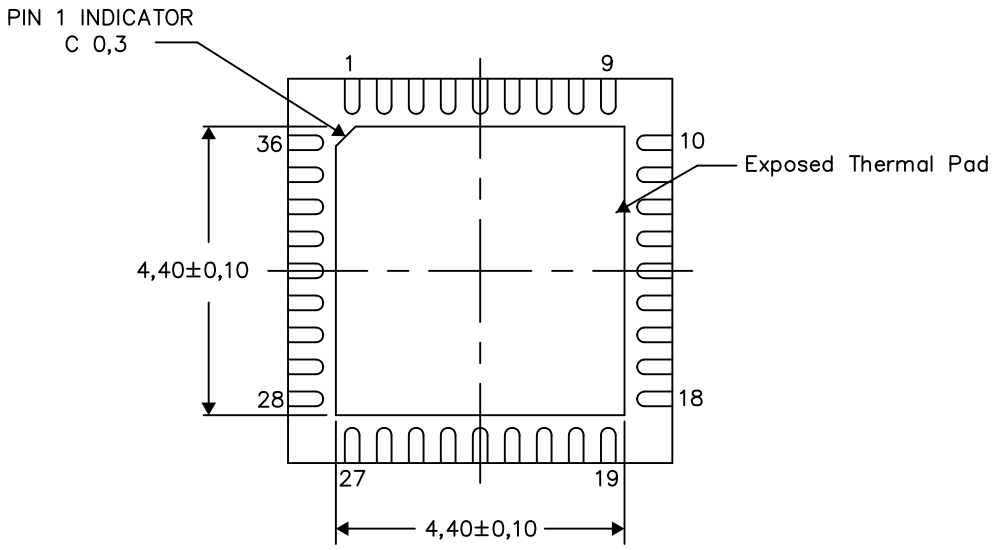
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



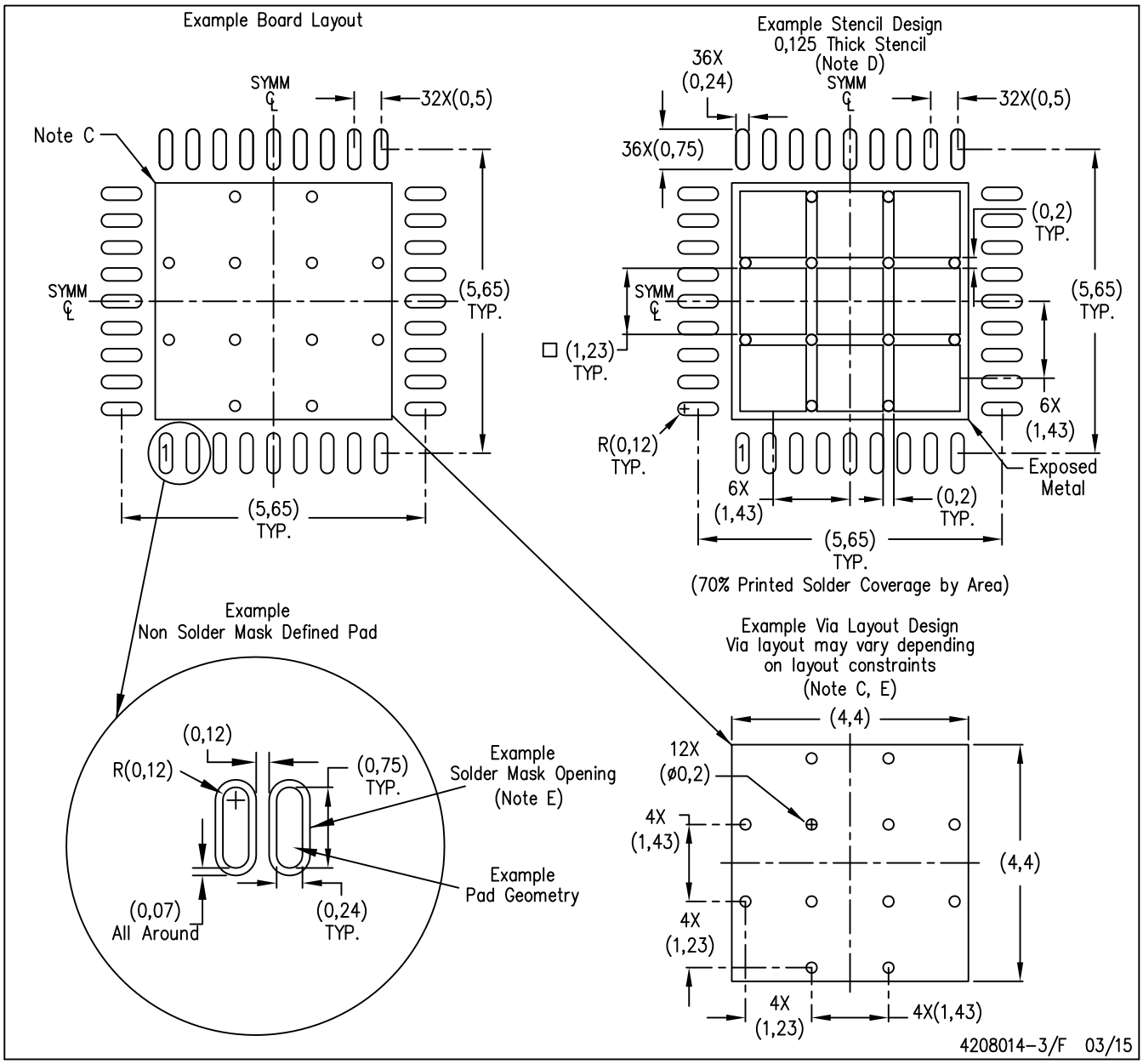
Bottom View

Exposed Thermal Pad Dimensions

4206362–5/M 11/13

NOTE: All linear dimensions are in millimeters

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



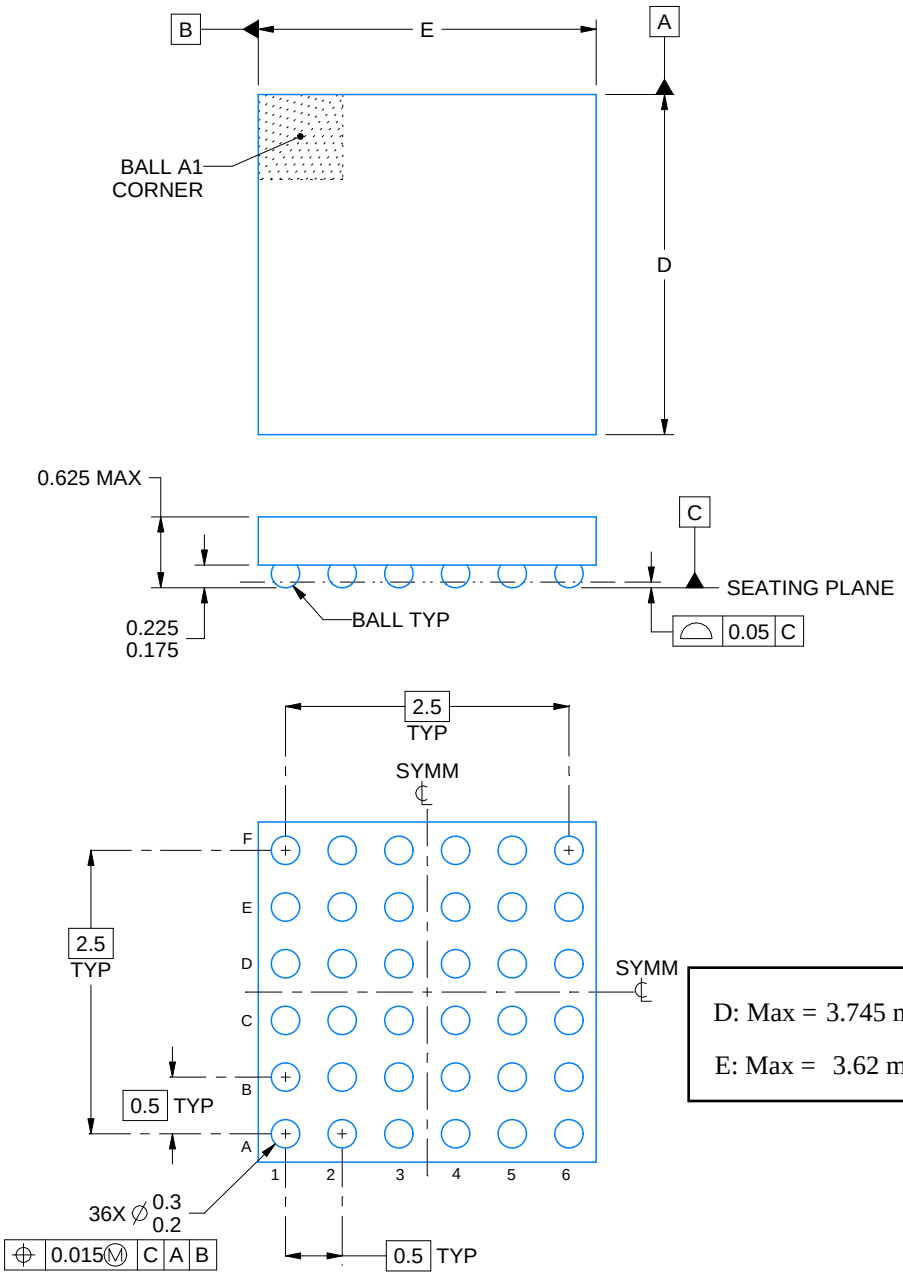
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

PACKAGE OUTLINE

YZS0036

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

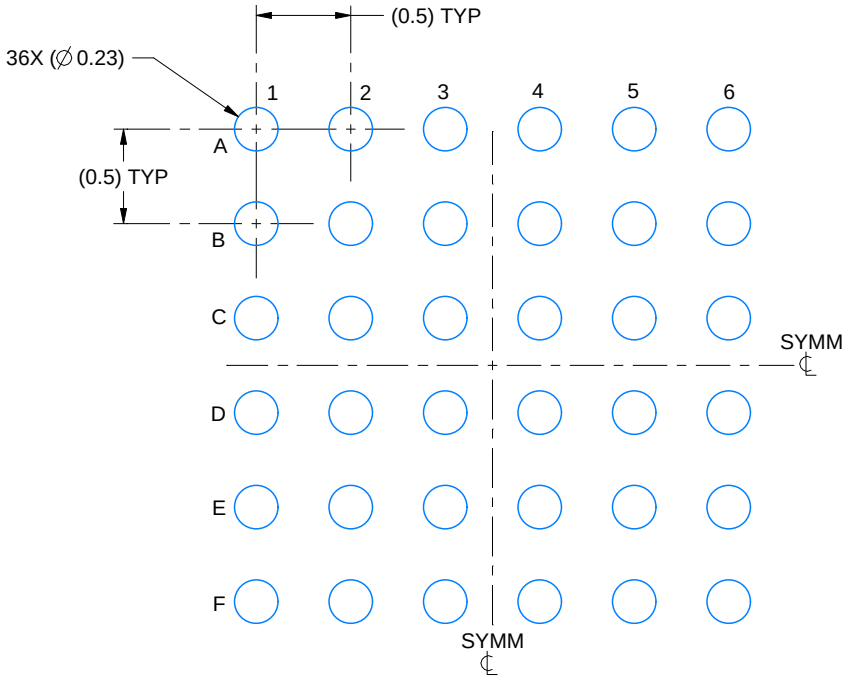
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

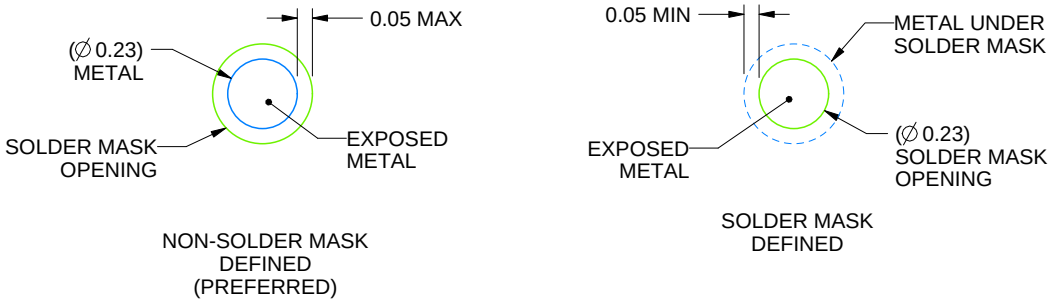
YZS0036

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS
NOT TO SCALE

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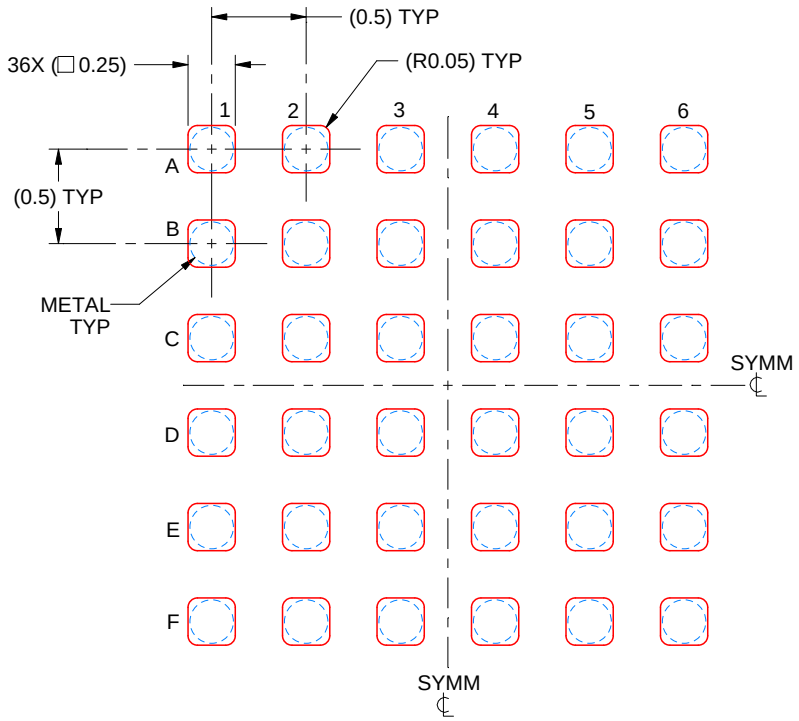
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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