FEATURES

- OUTPUT VOLTAGE: +5V ±0.2% max
- EXCELLENT TEMPERATURE STABILITY: 10ppm/°C max (−40°C to +85°C)
- LOW NOISE: 10μVpp max (0.1Hz to 10Hz)
- EXCELLENT LINE REGULATION: 0.01%/V max
- EXCELLENT LOAD REGULATION: 0.008%/mA max
- LOW SUPPLY CURRENT: 1.4mA max
- SHORT-CIRCUIT PROTECTED
- WIDE SUPPLY RANGE: 8V to 40V
- INDUSTRIAL TEMPERATURE RANGE: −40°C to +85°C
- PACKAGE OPTIONS: DIP-8, SO-8

APPLICATIONS

- PRECISION REGULATORS
- CONSTANT CURRENT SOURCE/SINK
- DIGITAL VOLTMETERS
- V/F CONVERTERS
- A/D AND D/A CONVERTERS
- PRECISION CALIBRATION STANDARD
- TEST EQUIPMENT

DESCRIPTION

The REF02 is a precision 5V voltage reference. The drift is laser trimmed to 10ppm/°C max over the extended industrial and military temperature range. The REF02 provides a stable 5V output that can be externally adjusted over a ±6% range with minimal effect on temperature stability. The REF02 operates from a single supply with an input range of 8V to 40V with a very low current drain of 1mA, and excellent temperature stability due to an improved design. Excellent line and load regulation, low noise, low power, and low cost make the REF02 the best choice whenever a 5V voltage reference is required. Available package options are DIP-8 and SO-8. The REF02 is an ideal choice for portable instrumentation, temperature transducers, Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters, and digital voltmeters.
**SPECIFICATIONS**

**ELECTRICAL**

At $T_A = +25^\circ C$ and $V_{IN} = +15$V power supply, unless otherwise noted.

| PARAMETER | CONDITIONS | REF02A | | | REF02B | | | UNITS |
|-----------|------------|--------|---|---|---|---|---|
| **OUTPUT VOLTAGE** | $I_{LOAD} = 0$mA | 4.985 | 5.0 | 5.015 | 4.990 | * | 5.010 | V |
| Change with Temperature$^{(1, 2)}$ ($\Delta V_{OT}$) | $-40^\circ C$ to $+85^\circ C$ | 0.05 | 0.19 | * | 0.05 | 0.13 | % |
| **OUTPUT VOLTAGE DRIFT**$^{(3)}$ | $-40^\circ C$ to $+85^\circ C$ ($TCV_O$) | 4 | 15 | 4 | 10 | ± ppm/°C |
| **LONG-TERM STABILITY** | 2000h Test | 100 | 15 | 100 | 50 | ± ppm |
| First 1000h | 50 | | | | ± ppm |
| Second 1000h | | | | | |
| **OUTPUT ADJUSTMENT RANGE** | $R_{POT} = 10k\Omega$ | ±3 | ±6 | * | * | % |
| **CHANGE IN $V_O$ TEMP COEFFICIENT WITH OUTPUT ADJUSTMENT** | $(-55^\circ C$ to $+125^\circ C)$ | | | | |
| $R_{POT} = 10k\Omega$ | 0.7 | | | | ppm/% |
| **OUTPUT VOLTAGE NOISE** | $0.1Hz$ to $10Hz$ | 4 | 10 | * | * | µVpp |
| **LINE REGULATION**$^{(4)}$ | $V_{IN} = 8$V to $33$V | 0.006 | 0.010 | * | * | %/V |
| $V_{IN} = 8.5$V to $33$V | 0.008 | 0.012 | * | * | %/V |
| **LOAD REGULATION**$^{(4)}$ | $I_L = 0$mA to $+10$mA | 0.005 | 0.010 | * | 0.008 | %/mA |
| $I_L = 0$mA to $+10$mA | 0.007 | 0.012 | * | 0.010 | %/mA |
| **TURN-ON SETTLING TIME** | To ±0.1% of Final Value | 5 | | | * | µs |
| **QUIESCENT CURRENT** | No Load | 1.0 | 1.4 | * | * | mA |
| **LOAD CURRENT (SOURCE)** | | 10 | 21 | * | * | mA |
| **LOAD CURRENT (SINK)** | $-0.3$ | $-0.5$ | * | * | mA |
| **SHORT-CIRCUIT CURRENT** | $V_{OUT} = 0$ | 30 | | | * | mA |
| **POWER DISSIPATION** | No Load | 15 | 21 | * | * | mW |
| **TEMPERATURE VOLTAGE OUTPUT**$^{(7)}$ | | 630 | | * | mV |
| **TEMPERATURE COEFFICIENT** | of Temperature Pin Voltage | | | | 2.1 | mV/°C |
| $(-55^\circ C$ to $+125^\circ C)$ | | | | | |
| **TEMPERATURE RANGE** | Specification | REF02A, B, C | $-40$ | $+85$ | * | * | °C |

NOTES: (1) $\Delta V_{OT}$ is defined as the absolute difference between the maximum output and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_O = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

(2) $\Delta V_{OT}$ specification applies trimmed to $+5.000$V or untrimmed.

(3) $TCV_O$ is defined as $\Delta V_{OT}$ divided by the temperature range.

(4) Line and load regulation specifications include the effect of self heating.

(5) Sample tested.

(6) 10kΩ potentiometer connected between $V_{OUT}$ and ground with wiper connected to Trim pin. See figure on page 1.

(7) Pin 3 is insensitive to capacitive loading. The temperature voltage will be modified by 7mV for each µA of loading.
ABSOLUTE MAXIMUM RATINGS

Input Voltage ................................................................. +40V
Operating Temperature
P, U ........................................................................... –40°C to +85°C
Storage Temperature Range
P, U ........................................................................... –65°C to +125°C
Output Short Circuit Duration (to Ground or V IN ) ................. Indefinite
Junction Temperature .................................................... –65°C to +150°C
θ JA P ......................................................................... 120°C/W
θ JA U ......................................................................... 80°C/W
Lead Temperature (soldering, 60s) ........................................ +300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>V OUT at 25°C</th>
<th>MAX DRIFT (ppm/°C)</th>
<th>PACKAGE</th>
<th>PACKAGE DRAWING DESIGNATOR</th>
<th>SPECIFICATION TEMPERATURE RANGE</th>
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<tbody>
<tr>
<td>REF02AU</td>
<td>5V±15mV</td>
<td>±15</td>
<td>SO-8</td>
<td>D</td>
<td>–40°C to +85°C</td>
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<tr>
<td>REF02BU</td>
<td>5V±10mV</td>
<td>±10</td>
<td>SO-8</td>
<td>D</td>
<td>–40°C to +85°C</td>
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<tr>
<td>REF02AP</td>
<td>5V±15mV</td>
<td>±15</td>
<td>DIP-8</td>
<td>P</td>
<td>–40°C to +85°C</td>
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<tr>
<td>REF02BP</td>
<td>5V±10mV</td>
<td>±10</td>
<td>DIP-8</td>
<td>P</td>
<td>–40°C to +85°C</td>
</tr>
</tbody>
</table>

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.
TYPICAL PERFORMANCE CURVES

AT $T_A = +25^\circ C$, unless otherwise noted.

OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz to frequency indicated)

OUTPUT CHANGE DUE TO THERMAL SHOCK

MAXIMUM LOAD CURRENT vs INPUT VOLTAGE

LINE REGULATION vs FREQUENCY

LINE REGULATION vs SUPPLY VOLTAGE
TYPICAL PERFORMANCE CURVES (Cont.)

At $T_A = +25^\circ$C, unless otherwise noted.

NORMALIZED LOAD REGULATION ($\Delta I_L = 10mA$) vs TEMPERATURE

NORMALIZED LINE REGULATION vs TEMPERATURE

REFERENCE $V_{OUT}$

MAXIMUM LOAD CURRENT vs TEMPERATURE

QUIESCENT CURRENT vs TEMPERATURE

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE

$V_{IN} = 15V$

$V_{IN} = 15V$
At $T_A = +25^\circ C$, unless otherwise noted.
OUTPUT ADJUSTMENT

The REF02 trim terminal can be used to adjust the voltage over a 5V ±150mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V, including 5.12V\(^{(1)}\) for binary applications (see circuit on page 1).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7ppm/°C for 100mV of output adjustment.

NOTE: (1) 20mV LSB for 8-bit applications.

REFERENCE STACKING PROVIDES OUTSTANDING LINE REGULATION

By stacking two REF01s and one REF02, a systems designer can achieve 5V, 15V, and 25V outputs. One very important advantage of this circuit is the near-perfect line regulation at 5V and 15V outputs. This circuit can accept a 27V to 55V change to the input with less than the noise voltage as a change to the output voltage. \(R_B\), a load bypass resistor, supplies current \(I_{SV}\) for the 15V regulator.

Any number of REF01s and REF02s can be stacked in this configuration. For example, if ten devices are stacked in this configuration, ten 5V or five 10V outputs are achieved. The line voltage may range from 100V to 130V. Care should be exercised to insure that the total load currents do not exceed the maximum usable current, which is typically 21mA.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
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<tbody>
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<td>REF02BU</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.
RoHS: TI defines “RoHS” to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, “RoHS” products are suitable for use in specified lead-free processes. TI may reference these types of products as “Pb-Free”.

RoHS Exempt: TI defines “RoHS Exempt” to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines “Green” to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

MSL, Peak Temp.: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish: Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### REEL DIMENSIONS

- **Reel Diameter**
- **Reel Width** (W₁)

### PACKAGING INFORMATION

#### REF02AU/2K5
- **Device**: REF02AU/2K5
- **Package Type**: SOIC
- **Package Number**: D
- **Number of Pins**: 8
- **SPQ**: 2500
- **Reel Diameter**: 330.0 mm
- **Reel Width**: 12.4 mm
- **A₀**: 6.4 mm
- **B₀**: 5.2 mm
- **K₀**: 2.1 mm
- **P₁**: 8.0 mm
- **W**: 12.0 mm
- **Pin1 Quadrant**: Q1

#### REF02BU/2K5
- **Device**: REF02BU/2K5
- **Package Type**: SOIC
- **Package Number**: D
- **Number of Pins**: 8
- **SPQ**: 2500
- **Reel Diameter**: 330.0 mm
- **Reel Width**: 12.4 mm
- **A₀**: 6.4 mm
- **B₀**: 5.2 mm
- **K₀**: 2.1 mm
- **P₁**: 8.0 mm
- **W**: 12.0 mm
- **Pin1 Quadrant**: Q1

*All dimensions are nominal.*
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>SPQ</th>
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<th>Width (mm)</th>
<th>Height (mm)</th>
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</table>
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
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