• Perform Fixed-Rate or Variable-Rate Frequency Division
• For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
• Typical Maximum Clock Frequency . . . 32 Megahertz

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These six-bit serial binary counters feature buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 64, ie:

\[ f_{out} = \frac{M \cdot f_{in}}{64} \]

where: \( M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0 \)

When the rate input is binary 0 (all rate inputs low), \( Z \) remains high. In order to cascade devices to perform 12-bit rate multiplication, the enable output is connected to the enable and strobe inputs of the next stage, the \( Z \) output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the \( Y \) output.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the \( Y \) output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the \( Y \) output.

logic symbol†

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Schematics of inputs and outputs

Equivalent of each input:

\[ V_{cc} \]

\[ R_{eq} \]

Input:

Clock input: \( R_{eq} = 2 \text{ k}\Omega \text{ NOM} \)

Other inputs: \( R_{eq} = 4 \text{ k}\Omega \text{ NOM} \)

Typical of all outputs:

\[ V_{cc} \]

\[ 100 \Omega \text{ NOM} \]

Output:

State and/or rate function table (See Note A)

<table>
<thead>
<tr>
<th>Clear</th>
<th>Enable</th>
<th>Strobe</th>
<th>Binary Rate</th>
<th>Number of Clock Pulses</th>
<th>Unity/Cascade</th>
<th>Logic Level or Number of Pulses</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Y</td>
<td>Z</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L L L L L L</td>
<td>64</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L L L L H H</td>
<td>64</td>
<td>H</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L L L L H L</td>
<td>64</td>
<td>H</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L L L L L L</td>
<td>64</td>
<td>H</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L L H L L L</td>
<td>64</td>
<td>H</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L H L L L L</td>
<td>64</td>
<td>H</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L H L L L L</td>
<td>64</td>
<td>H</td>
<td>32</td>
<td>32</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L H L L L L</td>
<td>64</td>
<td>H</td>
<td>63</td>
<td>63</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H H H H H H</td>
<td>64</td>
<td>L</td>
<td>H</td>
<td>63</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L H L L L L</td>
<td>64</td>
<td>H</td>
<td>40</td>
<td>40</td>
</tr>
</tbody>
</table>

Notes:

A. \( H \) = high level, \( L \) = low level, \( X \) = irrelevant. All remaining entries are numeric counts.

B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of \( Y \) and \( Z \). A low unity/cascade will cause output \( Y \) to remain high.

C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.

D. Unity/cascade is used to inhibit output \( Y \).

E. \[ f_{out} = \frac{M \cdot f_{in}}{64} = \frac{(8 + 32) f_{in}}{64} = \frac{40 f_{in}}{64} = 0.625 f_{in} \]
 logic diagram (positive logic)
SN5497, SN7497
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

SDLS130 – DECEMBER 1972 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) .................................................. 7 V
Input voltage ............................................................................. 5.5 V
Operating free-air temperature range: SN5497 (see Note 2) ............. -55°C to 125°C
SN7497 .................................................................................. 0°C to 70°C
Storage temperature range ......................................................... -65°C to 150°C

recommended operating conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN5497</th>
<th>SN7497</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>NOM</td>
</tr>
<tr>
<td>Supply voltage, VCC</td>
<td>4.5</td>
<td>5</td>
</tr>
<tr>
<td>HIGH-level output current, IOH</td>
<td>-400</td>
<td></td>
</tr>
<tr>
<td>LOW-level output current, IOL</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>Clock frequency, fck</td>
<td>0</td>
<td>25</td>
</tr>
<tr>
<td>Width of clock pulse, tmck</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>Width of clear pulse, tmclk</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>Enable setup time, tsu: Before positive-going transition of clock pulse</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>Before negative-going transition of previous clock pulse</td>
<td>0</td>
<td>tmck-10</td>
</tr>
<tr>
<td>Enable hold time, th: After positive-going transition of clock pulse</td>
<td>0</td>
<td>tmck-10</td>
</tr>
<tr>
<td>After negative-going transition of previous clock pulse</td>
<td>20</td>
<td>tpd-10</td>
</tr>
<tr>
<td>Operating free-air temperature, TA (See Note 2)</td>
<td>-55</td>
<td>125</td>
</tr>
</tbody>
</table>

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS †</th>
<th>MIN</th>
<th>TYP ‡</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>High-level input voltage</td>
<td>VCC = MIN, I1 = -12 mA</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Low-level input voltage</td>
<td>VCC = MIN, IOL = 16 mA</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>HIGH-level output voltage</td>
<td>VCC = MIN, I0H = 2 V, IoH = -400 μA</td>
<td>3.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>LOW-level output voltage</td>
<td>VCC = MIN, IOL = 16 mA</td>
<td>0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IT</td>
<td>Input current at maximum input voltage</td>
<td>VCC = MAX, VI = 5.5 V</td>
<td>1</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I1H</td>
<td>High-level input current</td>
<td>clock input other inputs</td>
<td>VCC = MAX, VI = 2.4 V</td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>I1L</td>
<td>Low-level input current</td>
<td>clock input other inputs</td>
<td>VCC = MAX, VI = 0.4 V</td>
<td>-3.2</td>
<td>mA</td>
</tr>
<tr>
<td>IOS</td>
<td>Short circuit output current §</td>
<td>VCC = MAX</td>
<td>-55</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>ICCP</td>
<td>Supply current, outputs high</td>
<td>VCC = MAX</td>
<td>See Note 3</td>
<td>58</td>
<td>mA</td>
</tr>
<tr>
<td>ICCP</td>
<td>Supply current, outputs low</td>
<td>VCC = MAX</td>
<td>See Note 4</td>
<td>80</td>
<td>mA</td>
</tr>
</tbody>
</table>

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at VCC = 5 V, TA = 25°C.
§Not more than one output should be shorted at a time.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN5497 in the W package operating at free-air temperatures above 110°C requires a heat sink that provides a thermal resistance from case to free-air, RθCA, of not more than 1.5°C/W.
3. ICCP is measured with outputs open and all inputs grounded.
4. ICCP is measured with outputs open and all inputs at 4.5 V.
switching characteristics, $V_{CC} = 5 \, V$, $T_A = 25^\circ C$, $N = 10$

<table>
<thead>
<tr>
<th>PARAMETER\textsuperscript{\textdagger}</th>
<th>FROM INPUT</th>
<th>TO OUTPUT</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{max}}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PLH}}$</td>
<td>Enable</td>
<td>Enable</td>
<td>$C_L = 15 , \text{pF}$, $R_L = 400 , \Omega$, See Figure 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PHL}}$</td>
<td>Strobe</td>
<td>Z</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PLH}}$</td>
<td>Clock</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PHL}}$</td>
<td>Clock</td>
<td>Z</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PLH}}$</td>
<td>Rate</td>
<td>Z</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PLH}}$</td>
<td>Unity/Cascade</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PHL}}$</td>
<td>Strobe</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PHL}}$</td>
<td>Clock</td>
<td>Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PLH}}$</td>
<td>Clear</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_{\text{PHL}}$</td>
<td>Any Rate Input</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\textsuperscript{\textdagger}$f_{\text{max}}$ = maximum clock frequency.

$T_{\text{PLH}}$ = propagation delay time, low-to-high-level output.

$T_{\text{PHL}}$ = propagation delay time, high-to-low-level output.

**TYPICAL APPLICATION DATA**

This application demonstrates how the '97 can be cascaded to perform 18-bit rate multiplication. This scheme is expandable to n-bits by extending the pattern illustrated.

As illustrated, two of the 6-bit multipliers can be cascaded by connecting the Z output of unit A to the unity cascade input of unit B, in which case, a two-input NOR gate is used to cascade the remaining multipliers. Alternatively, all three Y outputs can be cascaded with a 3-input NOR gate. The three unused unity cascade inputs can be conveniently terminated by connecting each to its Z output.
1. Unity/Cascade and pin 2 (rate input), other inputs are low. Clear the counter and apply clock and enable pulse as illustrated.

2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulse (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transition enabled.

NOTES:  
A. The input pulse generator has the following characteristics: $t_{w\text{ (clock)}} = 20\, \text{ns}$, $\tau_{\text{THL}} < 10\, \text{ns}$, $\tau_{\text{TLH}} < 10\, \text{ns}$, PRR = 1 MHz, $Z_{\text{out}} = 50\, \Omega$.
B. $C_{\text{L}}$ includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES
PARAMETER MEASUREMENT INFORMATION

OUTPUT OF DEVICE UNDER TEST

VCC
400 Ω
See Note C

CL = 15 pF
(See Note B)

All three outputs are loaded during testing.

LOAD CIRCUIT

CLOCK OR STROBE

1.5 V
1.5 V
0 V

1.5 V
1.5 V
VOL

OUTPUT Z

tpHL

VOH

OUTPUT Y

tpHL

VOH

1.5 V
VOL

1.5 V
1.5 V
VOL

Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum.

PROPAGATION DELAY TIMES, CLOCK TO Z AND Y, AND STROBE INPUT TO Z AND Y

PROGRESSION DELAY TIMES, RATE INPUT TO Z

RATE INPUT

3 V

1.5 V
1.5 V
0 V

VOL

OUTPUT Z

1.5 V
1.5 V

3 V

1.5 V
0 V

VOH

PROGRESSION DELAY TIMES, UNITY/CASCADE INPUT TO Z

UNITY/CASCADE INPUT

3 V

1.5 V
1.5 V
0 V

VOL

OUTPUT Z

1.5 V
1.5 V

1.5 V
0 V

VOH

PROGRESSION DELAY TIMES, UNITY/CASCADE INPUT TO Y

Output Z is high.

PROGRESSION DELAY TIMES, ENABLE INPUT TO ENABLE OUTPUT

ENABLE INPUT

3 V

1.5 V
1.5 V
0 V

VOL

ENABLE OUTPUT

1.5 V
1.5 V

VOL

Flip-flops are at the maximum count. Other inputs are low.

NOTES:
A. The input pulse generator has the following characteristics: "tW(clock) = 20 ns, tPLH < 10 ns, tTHL < 10 ns, PRR = 1 MHz, Zout = 50 Ω."
B. CL includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES (CONTINUED)
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN5497J</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>SN5497J</td>
<td>Samples</td>
</tr>
<tr>
<td>SN7497N</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>SN7497N</td>
<td>Samples</td>
</tr>
<tr>
<td>SN7497N</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>SN7497N</td>
<td>Samples</td>
</tr>
<tr>
<td>SNJ5497J</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>SNJ5497J</td>
<td>Samples</td>
</tr>
<tr>
<td>SNJ5497J</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>SNJ5497J</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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OTHER QUALIFIED VERSIONS OF SN5497, SN7497:

- Catalog: SN7497
- Military: SN5497

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
CERAMIC DUAL IN-LINE PACKAGE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.
N (R—PDIP—T**)  PLASTIC DUAL—IN—LINE PACKAGE

16 PINS SHOWN

<table>
<thead>
<tr>
<th>DIM</th>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
<td></td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
<td></td>
</tr>
<tr>
<td>MS—001 VARIATION</td>
<td>AA</td>
<td>BB</td>
<td>AC</td>
<td>AD</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS—001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

14/18 Pin Only
20 Pin vendor option

0.010 (0.25) NOM
0.015 (0.38)
0.021 (0.53)
0.015 (0.38)
0.010 (0.25) @

0.430 (10.92) MAX
0.325 (8.26)
0.300 (7.62)
0.200 (5.08) MAX
Seating Plane
0.125 (3.18) MIN

0.200 (5.08)
0.020 (0.51) MIN
0.030 (0.76)
0.045 (1.14)

0.260 (6.60)
0.240 (6.10)

0.100 (2.54)
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