State-of-the-Art EPIC-II™ BiCMOS Design Significantly Reduces Power Dissipation

ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17

Typical \( V_{OLP} \) (Output Ground Bounce) < 1 V at \( V_{CC} = 5 \text{ V} \), \( T_A = 25^\circ \text{C} \)

High-Drive Outputs (\(-32\text{-mA} I_{OH}, 64\text{-mA} I_{OL}\))

Parity Error Flag With Parity Generator/Checker

Register for Storage of the Parity Error Flag

Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

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description

The 'ABT833 8-bit to 9-bit parity transceivers are designed for communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the open-collector parity-error (ERR) output indicates whether or not an error in the B data has occurred. The output-enable (OEA and OEB) inputs can be used to disable the device so that the buses are effectively isolated. The 'ABT833 provide true data at their outputs.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with the ERR flag. ERR is clocked into the register on the rising edge of the clock (CLK) input. The error flag register is cleared with a low pulse on the clear (CLR) input. When both OEA and OEB are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

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To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT833 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT833 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT AND I/O</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>OEB</td>
<td>OEA</td>
<td>CLR</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>No↑</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>Odd</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>Even</td>
</tr>
</tbody>
</table>

NA = not applicable, NC = no change, X = don’t care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume ERR was previously high.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

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**logic symbol¶**

¶ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.
logic diagram (positive logic)

Pin numbers shown are for the DW, JT, and NT packages.

ERROR-FLAG FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>INTERNAL TO DEVICE</th>
<th>OUTPUT PRE-STATE</th>
<th>OUTPUT ERR</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLR</td>
<td>CLK</td>
<td>POINT P</td>
<td>ERR_{n-1}†</td>
<td>ERR</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
<td>X</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
<td>L</td>
<td>X</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
</tr>
</tbody>
</table>

† The state of ERR before any changes at CLR, CLK, or point P
error-flag waveforms

![Waveform diagram]

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, \( V_{CC} \)  
Input voltage range, \( V_I \) (except I/O ports) (see Note 1)  
Voltage range applied to any output in the high or power-off state, \( V_O \)  
Current into any output in the low state, \( I_O \): SN54ABT833  
SN74ABT833  
Input clamp current, \( I_{IK} \) (\( V_I < 0 \))  
Output clamp current, \( I_{OK} \) (\( V_O < 0 \))  
Package thermal impedance, \( \theta_{JA} \) (see Note 2): DW package  
NT package  
Storage temperature range, \( T_{stg} \)

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:  
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.
**recommended operating conditions (see Note 3)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SN54ABT833</th>
<th>SN74ABT833</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC}) Supply voltage</td>
<td>4.5</td>
<td>5.5</td>
<td>4.5</td>
</tr>
<tr>
<td>(V_{IH}) High-level input voltage</td>
<td>2</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL}) Low-level input voltage</td>
<td>0.8</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>(V_I) Input voltage</td>
<td>0</td>
<td>(V_{CC})</td>
<td>0</td>
</tr>
<tr>
<td>(V_{OH}) High-level output voltage</td>
<td>ERR</td>
<td>5.5</td>
<td>5.5</td>
</tr>
<tr>
<td>(I_{OH}) High-level output current</td>
<td>Except ERR</td>
<td>–24</td>
<td>–32</td>
</tr>
<tr>
<td>(I_{OL}) Low-level output current</td>
<td>48</td>
<td>64</td>
<td>mA</td>
</tr>
<tr>
<td>(\Delta t/\Delta v) Input transition rise or fall rate</td>
<td>Outputs enabled</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>(T_A) Operating free-air temperature</td>
<td>–55</td>
<td>125</td>
<td>–40</td>
</tr>
</tbody>
</table>

**NOTE 3:** Unused pins (input or I/O) must be held high or low to prevent them from floating.
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A = 25^\circ C )</th>
<th>SN54ABT833</th>
<th>SN74ABT833</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IK} )</td>
<td>( V_{CC} = 4.5 \text{ V}, \ II = -18 \text{ mA} )</td>
<td>MIN</td>
<td>TYP†</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>( V_{I} )</td>
<td>( V_{CC} = 4.5 \text{ V}, \ IOH = -3 \text{ mA} )</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CC} = 5 \text{ V}, \ IOH = -3 \text{ mA} )</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{CC} = 4.5 \text{ V}, \ IOH = -24 \text{ mA} )</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{CC} = 4.5 \text{ V}, \ IOH = -32 \text{ mA} )</td>
<td>2*</td>
<td>2*</td>
<td>2*</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>( V_{CC} = 4.5 \text{ V}, \ IOH = 24 \text{ mA} )</td>
<td>0.55</td>
<td>0.55</td>
<td>0.55</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>( V_{CC} = 6.5 \text{ V}, \ IOH = 64 \text{ mA} )</td>
<td>0.55*</td>
<td>0.55*</td>
<td>0.55*</td>
<td>V</td>
</tr>
<tr>
<td>( V_{\text{hys}} )</td>
<td></td>
<td>100</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( IOH )</td>
<td>( V_{CC} = 4.5 \text{ V}, \ IOH = 5.5 \text{ V} )</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_I )</td>
<td>Control inputs</td>
<td>( V_{CC} = 5.5 \text{ V}, \ V_I = V_{CC} \text{ or GND} )</td>
<td>±1</td>
<td>±1</td>
<td>±1</td>
</tr>
<tr>
<td>( I_I )</td>
<td>A or B ports</td>
<td>( V_{CC} = 0 ), ( V_I = \text{GND} )</td>
<td>±100</td>
<td>±100</td>
<td>±100</td>
</tr>
<tr>
<td>( I_{OZH})</td>
<td>( V_{CC} = 5.5 \text{ V}, \ VO = 2.7 \text{ V} )</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{OZL})</td>
<td>( V_{CC} = 5.5 \text{ V}, \ VO = 0.5 \text{ V} )</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{\text{off}} )</td>
<td>( V_{CC} = 0 ), ( V_I \text{ or } VO \leq 4.5 \text{ V} )</td>
<td>±100</td>
<td>±100</td>
<td>±100</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{\text{CEX}} )</td>
<td>( V_{CC} = 5.5 \text{ V}, \ VO = 5.5 \text{ V} )</td>
<td>Outputs high</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>( I_{\text{Q}})</td>
<td>( V_{CC} = 5.5 \text{ V}, \ VO = 2.5 \text{ V} )</td>
<td>Outputs high</td>
<td>1</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>( I_{\text{Q}})</td>
<td>Outputs low</td>
<td>24</td>
<td>38†</td>
<td>38†</td>
<td>38†</td>
</tr>
<tr>
<td>( I_{\text{Q}})</td>
<td>Outputs disabled</td>
<td>0.5</td>
<td>250</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>A or B ports</td>
<td>( V_{CC} = 5.5 \text{ V}, \ VO = 5.5 \text{ V} )</td>
<td>Outputs enabled</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Other inputs at ( V_{CC} \text{ or GND} )</td>
<td>Outputs enabled</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>( I_{CL} )</td>
<td>Control inputs</td>
<td>( V_I = 2.5 \text{ V or } 0.5 \text{ V} )</td>
<td>10.5</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

* On products compliant to MIL-PRF-38535, this parameter does not apply.
† All typical values are at \( V_{CC} = 5 \text{ V} \).
‡ The parameters \( I_{OZH} \) and \( I_{OZL} \) include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ These limits may vary among suppliers.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than \( V_{CC} \) or GND.
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>UNIT</th>
<th>V CC = 5 V, T A = 25°C</th>
<th>SN54ABT833</th>
<th>SN74ABT833</th>
</tr>
</thead>
<tbody>
<tr>
<td>t w</td>
<td>ns</td>
<td>3 3 3</td>
<td>SN54ABT833</td>
<td>SN74ABT833</td>
</tr>
<tr>
<td>t w SETUP</td>
<td>ns</td>
<td>3 3 3</td>
<td>SN54ABT833</td>
<td>SN74ABT833</td>
</tr>
<tr>
<td>t h</td>
<td>ns</td>
<td>0 0 0</td>
<td>SN54ABT833</td>
<td>SN74ABT833</td>
</tr>
</tbody>
</table>

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>V CC = 5 V, T A = 25°C</th>
<th>SN54ABT833</th>
<th>SN74ABT833</th>
</tr>
</thead>
<tbody>
<tr>
<td>t PHL</td>
<td>A or B</td>
<td>B or A</td>
<td>1.2 2.8 4.8</td>
<td>1.2 5.4</td>
<td>1.2 5.3</td>
</tr>
<tr>
<td>t PHL</td>
<td>A</td>
<td>PARITY</td>
<td>2.1 5.5 9.5</td>
<td>2.1 11.3</td>
<td>2.1 11.2</td>
</tr>
<tr>
<td>t PLH</td>
<td>OE</td>
<td>PARITY</td>
<td>2.6 5.8 8.6</td>
<td>2.6 10.1</td>
<td>2.6 10.5</td>
</tr>
<tr>
<td>t PZH</td>
<td>OE</td>
<td>CLR</td>
<td>1.2 2.8 4.8</td>
<td>1.2 5.3</td>
<td>1.2 5.2</td>
</tr>
<tr>
<td>t PHL</td>
<td>A</td>
<td>ERR</td>
<td>1.2 2.8 5.7</td>
<td>1.2 6.3</td>
<td>1.2 6.2</td>
</tr>
<tr>
<td>t PZL</td>
<td>OE</td>
<td>A, B or PARITY</td>
<td>1.3 3.6 5.8</td>
<td>1.3 6.6</td>
<td>1.3 6.5</td>
</tr>
<tr>
<td>t PHZ</td>
<td>OE</td>
<td>A, B or PARITY</td>
<td>1.9 4.4 7.3</td>
<td>1.9 8</td>
<td>1.9 7.9</td>
</tr>
<tr>
<td>t PLZ</td>
<td>OE</td>
<td>A, B or PARITY</td>
<td>2.2 4.4 7.7</td>
<td>2.2 8</td>
<td>2.2 8.1</td>
</tr>
</tbody>
</table>

† All typical values are at V CC = 5 V.
‡ These limits may vary among suppliers.
### PARAMETER MEASUREMENT INFORMATION

**LOAD CIRCUIT**

- From Output Under Test
- $C_L = 50 \text{ pF}$ (see Note A)

**Table:**

<table>
<thead>
<tr>
<th>TEST</th>
<th>S1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}/t_{PHL}$</td>
<td>Open</td>
</tr>
<tr>
<td>$t_{PLZ}/t_{PZL}$</td>
<td>7 V</td>
</tr>
<tr>
<td>$t_{PHZ}/t_{PZH}$</td>
<td>Open</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ERR</th>
<th>S1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PHL}$</td>
<td>7 V</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>7 V</td>
</tr>
</tbody>
</table>

**Figure 1. Load Circuit and Voltage Waveforms**

**NOTES:**

A. $C_L$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}, Z_O = 50 \Omega, t_r \leq 2.5 \text{ ns}, t_f \leq 2.5 \text{ ns}$

D. The outputs are measured one at a time with one transition per measurement.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74ABT833DW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>24</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>ABT833</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M—1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
D. Falls within JEDEC MS–013 variation AD.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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