

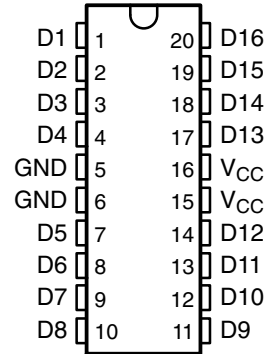
# SN74ACT1073

## 16-BIT BUS-TERMINATION ARRAY WITH BUS-HOLD FUNCTION

SCAS193A – MARCH 1992 – REVISED NOVEMBER 2002

- Designed to Ensure Defined Voltage Levels on Floating Bus Lines in CMOS Systems
- 4.5-V to 5.5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Reduces Undershoot and Overshoot Caused By Line Reflections
- Repetitive Peak Forward Current . . .  $I_{FRM} = 100$  mA
- Inputs Are TTL-Voltage Compatible
- Low Power Consumption (Like CMOS)
- Center-Pin  $V_{CC}$  and GND Configuration Minimizes High-Speed Switching Noise
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

DW OR NS PACKAGE  
(TOP VIEW)



### description/ordering information

This device is designed to terminate bus lines in CMOS systems. The integrated low-impedance diodes clamp the voltage of undershoots and overshoots caused by line reflections and ensure signal integrity. The device also contains a bus-hold function that consists of a CMOS-buffer stage with a high-resistance feedback path between its output and its input. The SN74ACT1073 prevents bus lines from floating without using pullup or pulldown resistors.

The high-impedance inputs of these internal buffers are connected to the input terminals of the device. The feedback path on each internal buffer stage keeps a bus line tied to the bus holder at the last valid logic state generated by an active driver before the bus switches to the high-impedance state.

### ORDERING INFORMATION

$T_A$	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74ACT1073DW
		Tape and reel	SN74ACT1073DWR
	SOP – NS	Tape and reel	SN74ACT1073NSR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

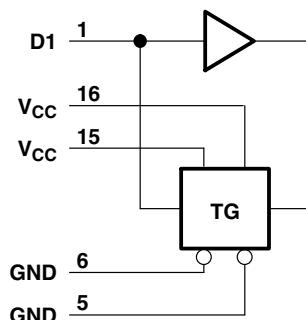
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# SN74ACT1073 16-BIT BUS-TERMINATION ARRAY WITH BUS-HOLD FUNCTION

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## logic diagram, one of sixteen channels (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	.....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	.....	-0.5 V to $V_{CC} + 0.5$ V
Continuous input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	.....	$\pm 20$ mA
Positive-peak input clamp current, $I_{IK}$ ( $V_I > V_{CC}$ ) ( $t_w < 1 \mu s$ , duty cycle $< 20\%$ )	.....	100 mA
Negative-peak input clamp current, $I_{IK}$ ( $V_I < 0$ ) ( $t_w < 1 \mu s$ , duty cycle $< 20\%$ )	.....	-100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DW package	.....	58°C/W
	NS package	60°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTE 1: The input negative-voltage rating may be exceeded if the input clamp-current rating is observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2.5		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
		MIN	TYP†	MAX			
$I_{IL}$	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V},$ $V_I = 0.8 \text{ V}$	0.15	0.3	0.9	0.1	1	mA
$I_{IH}$	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V},$ $V_I = 2.5 \text{ V}$	-0.2	-0.5	-1.4	-0.15	-1.5	mA
$V_{IKL}$	$I_{IN} = -18 \text{ mA}$			-1.5		-1.5	V
$V_{IKH}$	$I_{IN} = 18 \text{ mA}$			$V_{CC}+2$		$V_{CC}+2$	V
$I_{CC}^\ddagger$	$V_{CC} = 5.5 \text{ V},$ Inputs open			4		40	$\mu\text{A}$
$\Delta I_{CC}^\S$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND			0.9		1	mA
$C_i$	$V_I = V_{CC}$ or GND		3				pF

† All typical values are at  $V_{CC} = 5 \text{ V}$ .

‡ Inputs may be set high or low prior to the  $I_{CC}$  measurement.

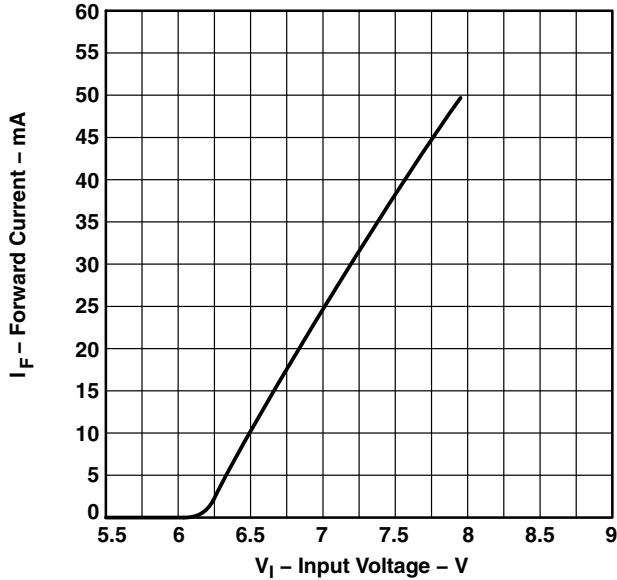
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or  $V_{CC}$ .

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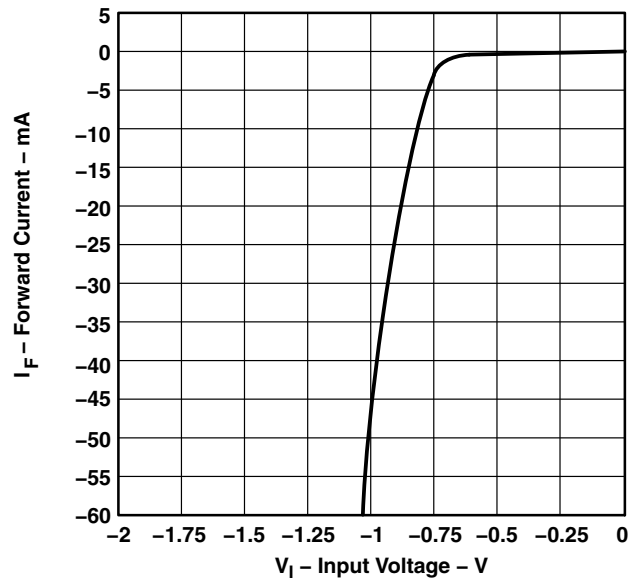
**TYPICAL CHARACTERISTICS**

**FORWARD CURRENT  
 vs  
 INPUT VOLTAGE  
 (UPPER CLAMPING DIODE)**



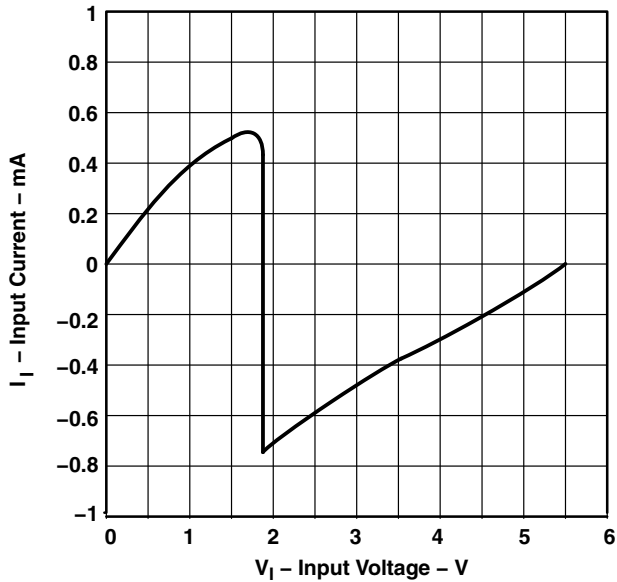
**Figure 1**

**FORWARD CURRENT  
 vs  
 INPUT VOLTAGE  
 (LOWER CLAMPING DIODE)**



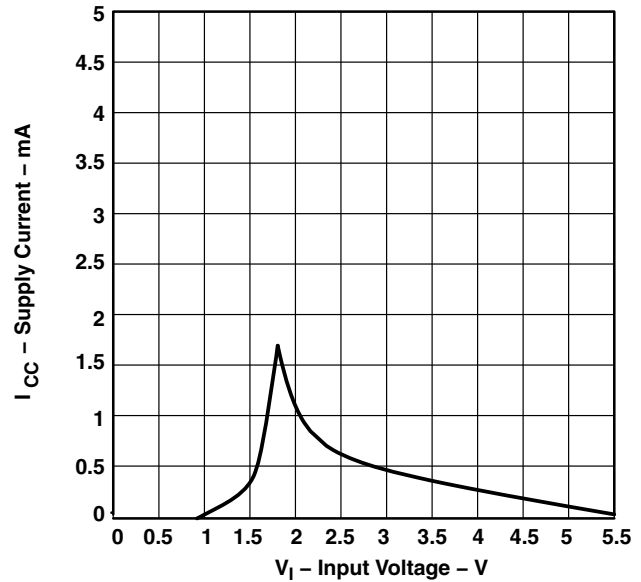
**Figure 2**

**INPUT CURRENT  
 vs  
 INPUT VOLTAGE**



**Figure 3**

**SUPPLY CURRENT  
 vs  
 INPUT VOLTAGE**

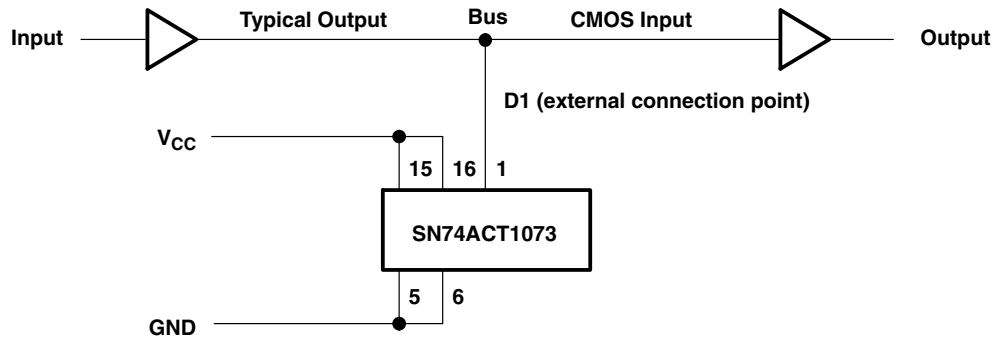


**Figure 4**



**APPLICATION INFORMATION**

The SN74ACT1073 terminates the output of a driving device and holds the input of the driven device at the logic level of the driver output prior to establishment of the high-impedance state on that output (see Figure 5).



**Figure 5. Bus-Hold Application**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT1073DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT1073	<a href="#">Samples</a>
SN74ACT1073DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT1073	<a href="#">Samples</a>
SN74ACT1073NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT1073	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT1073DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ACT1073NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT1073DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ACT1073NSR	SO	NS	20	2000	367.0	367.0	45.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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