SNx4AHC244 Octal Buffers/Drivers With 3-State Outputs

1 Features
- Operating Range 2-V to 5.5-V $V_{CC}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications
- Network Switches
- Power Infrastructures
- PCs and Notebooks
- Wearable Health and Fitness Devices
- Tests and Measurements

3 Description
These octal buffers and drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information(1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNx4AHC244</td>
<td>SSOP (20)</td>
<td>7.20 mm × 5.30 mm</td>
</tr>
<tr>
<td></td>
<td>SOIC (20)</td>
<td>12.80 mm × 7.50 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP (20)</td>
<td>12.60 mm × 5.30 mm</td>
</tr>
<tr>
<td></td>
<td>VQFN (20)</td>
<td>4.50 mm × 3.50 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic
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# Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (July 2003) to Revision K

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<tr>
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<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Updated document to new TI data sheet format.</td>
<td>1</td>
</tr>
<tr>
<td>• Removed Ordering Information table.</td>
<td>1</td>
</tr>
<tr>
<td>• Added Military Disclaimer to Features list.</td>
<td>1</td>
</tr>
<tr>
<td>• Added Applications.</td>
<td>1</td>
</tr>
<tr>
<td>• Added Pin Functions table.</td>
<td>3</td>
</tr>
<tr>
<td>• Added Handling Ratings table.</td>
<td>4</td>
</tr>
<tr>
<td>• Changed MAX ambient temperature in Recommended Operating Conditions table.</td>
<td>4</td>
</tr>
<tr>
<td>• Added Thermal Information table.</td>
<td>5</td>
</tr>
<tr>
<td>• Added Typical Characteristics.</td>
<td>7</td>
</tr>
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</table>
6 Pin Configuration and Functions

**Pin Functions**

<table>
<thead>
<tr>
<th>NO.</th>
<th>NAME</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1OE</td>
<td>I</td>
<td>Output Enable 1</td>
</tr>
<tr>
<td>2</td>
<td>1A1</td>
<td>I</td>
<td>1A1 Input</td>
</tr>
<tr>
<td>3</td>
<td>2Y4</td>
<td>O</td>
<td>2Y4 Output</td>
</tr>
<tr>
<td>4</td>
<td>1A2</td>
<td>I</td>
<td>1A2 Input</td>
</tr>
<tr>
<td>5</td>
<td>2Y3</td>
<td>O</td>
<td>2Y3 Output</td>
</tr>
<tr>
<td>6</td>
<td>1A3</td>
<td>I</td>
<td>1A3 Input</td>
</tr>
<tr>
<td>7</td>
<td>2Y2</td>
<td>O</td>
<td>2Y2 Output</td>
</tr>
<tr>
<td>8</td>
<td>1A4</td>
<td>I</td>
<td>1A4 Input</td>
</tr>
<tr>
<td>9</td>
<td>2Y1</td>
<td>O</td>
<td>2Y1 Output</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>—</td>
<td>Ground pin</td>
</tr>
<tr>
<td>11</td>
<td>2A1</td>
<td>I</td>
<td>2A1 Input</td>
</tr>
<tr>
<td>12</td>
<td>1Y4</td>
<td>O</td>
<td>1Y4 Output</td>
</tr>
<tr>
<td>13</td>
<td>2A2</td>
<td>I</td>
<td>2A2 Input</td>
</tr>
<tr>
<td>14</td>
<td>1Y3</td>
<td>O</td>
<td>1Y3 Output</td>
</tr>
<tr>
<td>15</td>
<td>2A3</td>
<td>I</td>
<td>2A3 Input</td>
</tr>
<tr>
<td>16</td>
<td>1Y2</td>
<td>O</td>
<td>1Y2 Output</td>
</tr>
<tr>
<td>17</td>
<td>2A4</td>
<td>I</td>
<td>2A4 Input</td>
</tr>
<tr>
<td>18</td>
<td>1Y1</td>
<td>O</td>
<td>1Y1 Output</td>
</tr>
<tr>
<td>19</td>
<td>2OE</td>
<td>I</td>
<td>Output Enable 2</td>
</tr>
<tr>
<td>20</td>
<td>VCC</td>
<td>—</td>
<td>Power Pin</td>
</tr>
</tbody>
</table>
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_I)</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_O)</td>
<td>–0.5</td>
<td>(V_{CC} + 0.5)</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IK})</td>
<td>(V_I &lt; 0)</td>
<td>–20</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{OK})</td>
<td>(V_O &lt; 0) or (V_O &gt; V_{CC})</td>
<td>±20</td>
<td>mA</td>
</tr>
<tr>
<td>(I_O)</td>
<td>(V_O = 0) to (V_{CC})</td>
<td>±25</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>±50</td>
<td>mA</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>(V_{(ESD)})</td>
<td>0</td>
<td>1500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>(SN54AHC244)</th>
<th>(SN74AHC244)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>2</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>(V_{CC} = 2) V</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>(V_{CC} = 2) V</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>(V_I)</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_O)</td>
<td>0</td>
<td>(V_{CC})</td>
<td>V</td>
</tr>
<tr>
<td>(I_{OH})</td>
<td>(V_{CC} = 2) V</td>
<td>–50</td>
<td>–50 μA</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td>(V_{CC} = 2) V</td>
<td>50</td>
<td>50 μA</td>
</tr>
<tr>
<td>(\Delta V/\Delta t)</td>
<td>(V_{CC} = 2) V</td>
<td>100</td>
<td>100 ns/V</td>
</tr>
<tr>
<td>(T_A)</td>
<td>–55</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) All unused inputs of the device must be held at \(V_{CC}\) or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
### 7.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>SN74AHCT244</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DB</td>
</tr>
<tr>
<td></td>
<td>20 PINS</td>
</tr>
<tr>
<td>$R_{JA}$ Junction-to-ambient thermal resistance</td>
<td>99.9</td>
</tr>
<tr>
<td>$R_{JC(top)}$ Junction-to-case (top) thermal resistance</td>
<td>61.7</td>
</tr>
<tr>
<td>$R_{JB}$ Junction-to-board thermal resistance</td>
<td>55.2</td>
</tr>
<tr>
<td>$\psi_{JT}$ Junction-to-top characterization parameter</td>
<td>22.6</td>
</tr>
<tr>
<td>$\psi_{JB}$ Junction-to-board characterization parameter</td>
<td>54.8</td>
</tr>
<tr>
<td>$R_{JC(bot)}$ Junction-to-case (bottom) thermal resistance</td>
<td>n/a</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

### 7.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>V&lt;sub&gt;CC&lt;/sub&gt;</th>
<th>$T_A = 25^\circ\text{C}$</th>
<th>SN54AHC244</th>
<th>SN74AHC244</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>$I_{OH} = -50 \mu A$</td>
<td>2 V</td>
<td>1.9</td>
<td>2</td>
<td>1.9</td>
<td>1.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 V</td>
<td>2.9</td>
<td>3</td>
<td>2.9</td>
<td>2.9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>4.4</td>
<td>4.5</td>
<td>4.4</td>
<td>4.4</td>
</tr>
<tr>
<td></td>
<td>$I_{OH} = -4 mA$</td>
<td>3 V</td>
<td>2.58</td>
<td>2.48</td>
<td>2.48</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{OH} = -8 mA$</td>
<td>4.5 V</td>
<td>3.94</td>
<td>3.8</td>
<td>3.8</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$I_{OL} = 50 \mu A$</td>
<td>2 V</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3 V</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{OL} = 4 mA$</td>
<td>3 V</td>
<td>0.36</td>
<td>0.5</td>
<td>0.44</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{OL} = 8 mA$</td>
<td>4.5 V</td>
<td>0.36</td>
<td>0.5</td>
<td>0.44</td>
<td></td>
</tr>
<tr>
<td>$I_I$</td>
<td>$V_I = 5.5 V \text{ or GND}$</td>
<td>0 V to 5.5 V</td>
<td>±0.1</td>
<td>±1(1)</td>
<td>±1</td>
<td></td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>$V_O = V_{CC} \text{ or GND}$, $V_I (OE) = V_{IL} \text{ or } V_{IH}$</td>
<td>5.5 V</td>
<td>±0.25</td>
<td>±2.5</td>
<td>±2.5</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{OC}$</td>
<td>$V_I = V_{CC} \text{ or GND}$, $I_O = 0$</td>
<td>5.5 V</td>
<td>4</td>
<td>40</td>
<td>40</td>
<td>µA</td>
</tr>
<tr>
<td>$C_I$</td>
<td>$V_I = V_{CC} \text{ or GND}$</td>
<td>5 V</td>
<td>2</td>
<td>10</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>$C_O$</td>
<td>$V_O = V_{CC} \text{ or GND}$</td>
<td>5 V</td>
<td>3.5</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC} = 0$ V.
### 7.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 3.3 \, \text{V} \pm 0.3 \, \text{V}$ (unless otherwise noted) (see Figure 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>LOAD CAPACITANCE</th>
<th>$T_A = 25^\circ\text{C}$</th>
<th>SN54AHC244</th>
<th>SN74AHC244</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A</td>
<td>Y</td>
<td>$C_L = 15 , \text{pF}$</td>
<td>$5.8^{(1)}$</td>
<td>$8.4^{(1)}$</td>
<td>$1^{(1)}$</td>
<td>$10^{(1)}$</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 15 , \text{pF}$</td>
<td>$6.6^{(1)}$</td>
<td>$10.6^{(1)}$</td>
<td>$1^{(1)}$</td>
<td>$12.5^{(1)}$</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 15 , \text{pF}$</td>
<td>$5^{(1)}$</td>
<td>$9.7^{(1)}$</td>
<td>$1^{(1)}$</td>
<td>$11^{(1)}$</td>
</tr>
<tr>
<td>$t_{PZL}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 15 , \text{pF}$</td>
<td>$5^{(1)}$</td>
<td>$9.7^{(1)}$</td>
<td>$1^{(1)}$</td>
<td>$11^{(1)}$</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>A</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>8.3</td>
<td>11.9</td>
<td>1 13.5</td>
<td>1 13.5</td>
</tr>
<tr>
<td>$t_{PZL}$</td>
<td>A</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>9.1</td>
<td>14.1</td>
<td>1 16</td>
<td>1 16</td>
</tr>
<tr>
<td>$t_{PHZ}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>10.3</td>
<td>14</td>
<td>1 16</td>
<td>1 16</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>10.3</td>
<td>14</td>
<td>1 16</td>
<td>1 16</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>1.5</td>
<td>1.5</td>
<td>1 1.5</td>
<td>1.5</td>
</tr>
</tbody>
</table>

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

### 7.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5 \, \text{V} \pm 0.5 \, \text{V}$ (unless otherwise noted) (see Figure 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>LOAD CAPACITANCE</th>
<th>$T_A = 25^\circ\text{C}$</th>
<th>SN54AHC244</th>
<th>SN74AHC244</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>A</td>
<td>Y</td>
<td>$C_L = 15 , \text{pF}$</td>
<td>$3.9^{(1)}$</td>
<td>$5.5^{(1)}$</td>
<td>$1^{(1)}$</td>
<td>$6.5^{(1)}$</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 15 , \text{pF}$</td>
<td>$4.7^{(1)}$</td>
<td>$7.3^{(1)}$</td>
<td>$1^{(1)}$</td>
<td>$8.5^{(1)}$</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 15 , \text{pF}$</td>
<td>$5^{(1)}$</td>
<td>$7.2^{(1)}$</td>
<td>$1^{(1)}$</td>
<td>$8.5^{(1)}$</td>
</tr>
<tr>
<td>$t_{PZL}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 15 , \text{pF}$</td>
<td>$5^{(1)}$</td>
<td>$7.2^{(1)}$</td>
<td>$1^{(1)}$</td>
<td>$8.5^{(1)}$</td>
</tr>
<tr>
<td>$t_{PHZ}$</td>
<td>A</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>5.4</td>
<td>7.5</td>
<td>1 8.5</td>
<td>1 8.5</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>A</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>6.2</td>
<td>9.3</td>
<td>1 10.5</td>
<td>1 10.5</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>6.7</td>
<td>9.2</td>
<td>1 10.5</td>
<td>1 10.5</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>$\overline{OE}$</td>
<td>Y</td>
<td>$C_L = 50 , \text{pF}$</td>
<td>6.7</td>
<td>9.2</td>
<td>1 10.5</td>
<td>1 10.5</td>
</tr>
</tbody>
</table>

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.
7.8 Noise Characteristics

\( V_{CC} = 5 \text{ V}, \ C_L = 50 \text{ pF}, \ T_A = 25^\circ \text{C} \) (See\(^{(1)}\))

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>( SN74AHC244 )</th>
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<tbody>
<tr>
<td></td>
<td>MIN</td>
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<tr>
<td>( V_{OL(P)} )</td>
<td></td>
</tr>
<tr>
<td>( V_{OL(V)} )</td>
<td></td>
</tr>
<tr>
<td>( V_{OH(V)} )</td>
<td></td>
</tr>
<tr>
<td>( V_{IH(D)} )</td>
<td></td>
</tr>
<tr>
<td>( V_{IL(D)} )</td>
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</tbody>
</table>

\(^{(1)}\) Characteristics are for surface-mount packages only.

7.9 Operating Characteristics

\( V_{CC} = 5 \text{ V}, \ T_A = 25^\circ \text{C} \)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP</th>
<th>UNIT</th>
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</thead>
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<tr>
<td>( C_{pd} )</td>
<td>No load, ( f = 1 \text{ MHz} )</td>
<td>8.6</td>
<td>pF</td>
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</table>

7.10 Typical Characteristics

![Figure 1. TPD vs Temperature](image1)

![Figure 2. TPD vs \( V_{CC} \)](image2)
8 Parameter Measurement Information

From Output Under Test

\[ R_L = 1 \text{k}\Omega \]

\[ \text{C_L} \]

(see Note A)

Test Point

\[ \text{S1} \]

\[ \text{Open} \]

\[ \text{GND} \]

From Output Under Test

\[ \text{C_L} \]

(see Note A)

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

Timing Input

\[ 50\% \text{ V}_{\text{CC}} \]

\[ \text{V}_{\text{CC}} \]

Data Input

\[ 50\% \text{ V}_{\text{CC}} \]

\[ 0 \text{ V} \]

VOLTAGE WAVEFORMS

PULSE DURATION

Input

\[ 50\% \text{ V}_{\text{CC}} \]

\[ 0 \text{ V} \]

\[ 50\% \text{ V}_{\text{CC}} \]

VCC

VCC

VCC

0 V

0 V

0 V

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

INVERTING AND NONINVERTING OUTPUTS

Input

\[ 50\% \text{ V}_{\text{CC}} \]

\[ 50\% \text{ V}_{\text{CC}} \]

\[ 0 \text{ V} \]

\[ t_{\text{PLH}} \]

\[ t_{\text{PHL}} \]

\[ t_{\text{PHL}} \]

\[ t_{\text{PLH}} \]

\[ t_{\text{PZL}} \]

\[ t_{\text{PZH}} \]

Output Control

\[ 50\% \text{ V}_{\text{CC}} \]

\[ 50\% \text{ V}_{\text{CC}} \]

\[ 0 \text{ V} \]

\[ \text{VOH} \]

\[ \text{VOL} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{CC}} \]

\[ \text{V}_{\text{OL}} + 0.3 \text{ V} \]

\[ \text{VOH} - 0.3 \text{ V} \]

\[ = \text{V}_{\text{CC}} \]

\[ = \text{V}_{\text{OL}} \]

\[ = 0 \text{ V} \]

Output Waveform 1

S1 at \text{V}_{\text{CC}}

(see Note B)

Output Waveform 2

S1 at GND

(see Note B)

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES

LOW-AND HIGH-LEVEL ENABLING

NOTES:

A. \( \text{C}_L \) includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: \( \text{PRR} \leq 1 \text{MHz}, \text{Z}_0 = 50 \Omega, t_r \leq 3 \text{ ns}, t_f \leq 3 \text{ ns}. \)

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms
9 Detailed Description

9.1 Overview
The SNx4AHC244 devices are organized as two 4-bit buffers/line drivers with separate output-enable (OE) inputs. When OE is low, the device passes data from the A inputs to the Y outputs. When OE is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to \( V_{CC} \) through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

9.2 Functional Block Diagram

![Logic Diagram](image)

Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description
- \( V_{CC} \) is optimized at 5 V
- Allows down voltage translation
  - Inputs accept \( V_{IH} \) levels of 5.5 V
- Slow edge rates minimize output ringing

9.4 Device Functional Modes

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>OE</td>
<td>A</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
</tr>
</tbody>
</table>

Table 1. Function Table (Each 4-Bit Buffer/Driver)
10 Application and Implementation

10.1 Application Information

The SNx4AHC244 is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can except voltages to 5.5 V at any valid $V_{CC}$ making it ideal for down translation.

10.2 Typical Application

![Typical Application Diagram](image)

**Figure 5. Typical Application Diagram**

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

- **Recommended input conditions**
  - Specified high and low levels. See $(V_{IH}$ and $V_{IL}$) in *Recommended Operating Conditions*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$

- **Recommended output conditions**
  - Load currents should not exceed 25 mA per output and 50 mA total for the part
  - Outputs should not be pulled above $V_{CC}$
11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the Recommended Operating Conditions table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple VCC pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 7 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

12.2 Layout Example

![Figure 7. Layout Diagram](image-url)
13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
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</thead>
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<tr>
<td>SN54AHC244</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
<tr>
<td>SN74AHC244</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
<td>Click here</td>
</tr>
</tbody>
</table>

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — Ti Glossary.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<tbody>
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## Orderable Device Information

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<th>Orderable Device</th>
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<th>Package Type</th>
<th>Package Drawing</th>
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<th>Op Temp (°C)</th>
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<td>5962-9678201QS A SNJ54AHC244W</td>
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</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JEDEC low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC244, SN54AHC244-SP, SN74AHC244:

- Catalog: SN74AHC244, SN54AHC244
- Automotive: SN74AHC244-Q1, SN74AHC244-Q1
- Enhanced Product: SN74AHC244-EP, SN74AHC244-EP
- Military: SN54AHC244
- Space: SN54AHC244-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

![Reel Dimensions Diagram](image)

#### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram](image)

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
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### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

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<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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W (R—GDFP—F20)  CERAMIC DUAL FLATPACK

- Base and Seating Plane
- 0.300 (7.62) 0.245 (6.22)
- 0.009 (0.23) 0.004 (0.10)
- 0.320 (8.13) MAX

- 0.540 (13.72) MAX
- 0.022 (0.56) 0.015 (0.38)
- 0.050 (1.27)
- 0.005 (0.13) MIN

- 0.370 (9.40) 0.250 (6.35)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil—Std 1835 GDFP2—F20
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS-004
**NOTES:**
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

CERAMIC DUAL IN-LINE PACKAGE

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<tr>
<th>DIM</th>
<th>PINS **</th>
<th>14</th>
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<tbody>
<tr>
<td>A</td>
<td>0.300</td>
<td>0.300</td>
<td>0.300</td>
<td>0.300</td>
<td></td>
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<tr>
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<td>(7.62 BSC)</td>
<td>(7.62 BSC)</td>
<td>(7.62 BSC)</td>
<td>(7.62 BSC)</td>
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<tr>
<td>B MAX</td>
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<td>.840</td>
<td>.960</td>
<td>1.060</td>
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<td></td>
<td>(19.94)</td>
<td>(21.34)</td>
<td>(24.38)</td>
<td>(26.92)</td>
<td></td>
</tr>
<tr>
<td>B MIN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
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<tr>
<td></td>
<td>(7.62)</td>
<td>(7.62)</td>
<td>(7.87)</td>
<td>(7.62)</td>
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<td>0.245</td>
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<td></td>
<td>(6.22)</td>
<td>(6.22)</td>
<td>(5.59)</td>
<td>(6.22)</td>
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</table>
DGV (R-PDSO-G**)  
PLASTIC SMALL-OUTLINE  
24 PINS SHOWN  

NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 per side.  
D. Falls within JEDEC: 24/48 Pins – MO-153  
14/16/20/56 Pins – MO-194
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
N (R-PDIP-T**)  PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

<table>
<thead>
<tr>
<th>PIN</th>
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<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
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<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
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</table>

MS-001 VARIATION

AA  BB  AC  AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\text{Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).}\]
\[\text{The 20 pin end lead shoulder width is a vendor option, either half or full width.}\]
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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