description

This 64-bit memory features high speed and fast fall-through times. It is organized as 16 words by 4 bits.

A first-in, first-out (FIFO) memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates up to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load-clock (LDCK) input and is read out on a low-to-high transition at the unload-clock (UNCK) input. The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect on the data residing in memory. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory is monitored by the FULL and EMPTY output flags. The FULL output is low when the memory is full and high when it is not full. The EMPTY output is low when the memory is empty and high when it is not empty.

A low level on the reset (RST) input resets the internal stack-control pointers and also sets EMPTY low and sets FULL high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK, after either a RST pulse or from an empty condition, causes EMPTY to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the FULL or EMPTY output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

The SN74ALS232B is characterized for operation from 0°C to 70°C.
logic symbol†

† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0.

Pin numbers shown are for the DW and N packages.
logic diagram (positive logic)

Pin numbers shown are for the DW and N packages.
SN74ALS232B
16 × 4 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY


timing diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, \( V_{CC} \) ................................................................. –0.5 V to 7 V
Input voltage range, \( V_I \) ................................................................. –0.5 V to 7 V
Voltage range applied to a disabled 3-state output ................................................................. –0.5 V to 5.5 V
Package thermal impedance, \( \theta_{JA} \) (see Note 2): DW package ........................................... 105°C/W
FN package ................................................................. 83°C/W
N package ................................................................. 78°C/W
Storage temperature range, \( T_{stg} \) ................................................................. –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.
### recommended operating conditions (see Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Supply voltage</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>High-level input voltage</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Low-level input voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>High-level output current</td>
<td>Q outputs</td>
<td>–2.6</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FULL, EMPTY</td>
<td>–0.4</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Low-level output current</td>
<td>Q outputs</td>
<td>24</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FULL, EMPTY</td>
<td>8</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>Operating free-air temperature</td>
<td>0</td>
<td>70</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTE 3:** To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates limits for maximum V<sub>IL</sub>, minimum V<sub>IH</sub>, or minimum pulse duration can cause a false clock or improper operation of the internal read and write pointers.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;IK&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>–1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>Q outputs</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 4.5 V, I&lt;sub&gt;i&lt;/sub&gt; = –18 mA</td>
<td>2.4</td>
<td>3.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>FULL, EMPTY</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 4.5 V to 5.5 V, I&lt;sub&gt;OH&lt;/sub&gt; = –2.6 mA</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; to V&lt;sub&gt;CC&lt;/sub&gt;–</td>
<td>- V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Q outputs</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 4.5 V</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 12 mA</td>
<td>0.25</td>
<td>0.4</td>
</tr>
<tr>
<td></td>
<td>FULL, EMPTY</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 4.5 V</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 24 mA</td>
<td>0.35</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 4.5 V</td>
<td>I&lt;sub&gt;OL&lt;/sub&gt; = 8 mA</td>
<td>0.25</td>
<td>0.4</td>
</tr>
<tr>
<td>I&lt;sub&gt;OZH&lt;/sub&gt;</td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.5 V, V&lt;sub&gt;O&lt;/sub&gt; = 2.7 V</td>
<td>20</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I&lt;sub&gt;OZL&lt;/sub&gt;</td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.5 V, V&lt;sub&gt;O&lt;/sub&gt; = 0.4 V</td>
<td>–20</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I&lt;sub&gt;IH&lt;/sub&gt;</td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.5 V, V&lt;sub&gt;I&lt;/sub&gt; = 7 V</td>
<td>0.1</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;IL&lt;/sub&gt;</td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.5 V, V&lt;sub&gt;I&lt;/sub&gt; = 2.7 V</td>
<td>20</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I&lt;sub&gt;IQ&lt;/sub&gt;</td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.5 V, V&lt;sub&gt;O&lt;/sub&gt; = 2.25 V</td>
<td>–30</td>
<td>–112</td>
<td>mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;ICC&lt;/sub&gt;</td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5.5 V</td>
<td>80</td>
<td>125</td>
<td>mA</td>
</tr>
</tbody>
</table>

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I<sub>OS</sub>. 
SN74ALS232B
16 × 4 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY


Timing requirements over recommended operating free-air temperature range (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_clock†</td>
<td>Clock frequency</td>
<td>LDCK</td>
<td>40 MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UNCK</td>
<td>40 MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>f_w</td>
<td>Pulse duration</td>
<td>RST low</td>
<td>18 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDCK low</td>
<td>15 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDCK high</td>
<td>10 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UNCK low</td>
<td>15 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>UNCK high</td>
<td>10 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_su</td>
<td>Setup time</td>
<td>Data before LDCK†</td>
<td>8 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDCK inactive before RST†</td>
<td>5 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_h</td>
<td>Hold time</td>
<td>Data after LDCK†</td>
<td>5 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDCK inactive after RST†</td>
<td>5 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

† The maximum possible clock frequency is 40 MHz. The maximum clock frequency when using a 50% duty cycle is 33.3 MHz.

Switching characteristics (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>MIN</th>
<th>TYP‡</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_max</td>
<td>LDCK, UNCK</td>
<td>Any Q</td>
<td>14 ns</td>
<td>23</td>
<td>6</td>
<td>30 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>UNCK</td>
<td>15 ns</td>
<td>23</td>
<td>6</td>
<td>30 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_plh</td>
<td>LDCK†</td>
<td>EMPTY</td>
<td>13 ns</td>
<td>20</td>
<td>5</td>
<td>25 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>UNCK</td>
<td>15 ns</td>
<td>22</td>
<td>6</td>
<td>27 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RST†</td>
<td>EMPTY</td>
<td>15 ns</td>
<td>21</td>
<td>5</td>
<td>26 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LDCK†</td>
<td>FULL</td>
<td>15 ns</td>
<td>22</td>
<td>6</td>
<td>27 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>UNCK†</td>
<td>FULL</td>
<td>13 ns</td>
<td>20</td>
<td>5</td>
<td>25 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RST†</td>
<td>FULL</td>
<td>16 ns</td>
<td>23</td>
<td>7</td>
<td>28 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_en</td>
<td>OE†</td>
<td>Q</td>
<td>5 ns</td>
<td>12</td>
<td>1</td>
<td>14 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t_dis</td>
<td>OE↓</td>
<td>Q</td>
<td>5 ns</td>
<td>12</td>
<td>1</td>
<td>16 ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

‡ Typical values at V_CC = 5 V, T_A = 25°C.
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR 3-STATE OUTPUTS

From Output Under Test

C_L = 50 pF (see Note A)

Test Point

S1

Open

R1 = 500 Ω

R2 = 500 Ω

LOAD CIRCUIT FOR 3-STATE OUTPUTS

From Output Under Test

C_L = 50 pF (see Note A)

Test Point

S1

Open

R1 = 500 Ω

R2 = 500 Ω

VOLTAGE WAVEFORMS

SETUP AND HOLD TIMES

Timing

Input

Data

Input

(see Note C)

VOLTAGE WAVEFORMS

PROPAGATION DELAY TIMES

In-Phase Output

Out-of-Phase Output

VOLTAGE WAVEFORMS

PULSE DURATION

High-Level Pulse

Low-Level Pulse

VOLTAGE WAVEFORMS

ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

Waveform 1

S1 Closed (see Note B)

Waveform 2

S1 Open (see Note B)

NOTES:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_o = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Top-Side Markings (4)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74ALS232BDW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>ALS232B</td>
<td></td>
</tr>
<tr>
<td>SN74ALS232BN</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>SN74ALS232BN</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
9. Board assembly site may have different recommendations for stencil design.
**MECHANICAL DATA**

**N (R-PDIP-T**)**

**PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

**NOTES:**

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

▽ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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