Sn74CB3T3125 Quadruple FET Bus Switch
2.5-V, 3.3-V Low-Voltage Bus Switch with 5-V-Tolerant Level Shifter

1 Features
- Output Voltage Translation Tracks VCC
- Supports Mixed-Mode Signal Operation On All Data I/O Ports
  - 5-V Input Down to 3.3-V Output-Level Shift With 3.3-V VCC
  - 5-V/3.3-V Input Down to 2.5-V Output-Level Shift With 2.5-V VCC
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_on) Characteristics (r_on = 5 Ω Typical)
- Low Input/Output Capacitance Minimizes Loading (Cio(OFF) = 4.5 pF Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption (Icc = 20 μA Max)
- Vcc Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- Ioff Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications
- Supports Digital Applications: Level Translation, USB Interface, Bus Isolation
- Ideal for Low-Power Portable Equipment

3 Description
The Sn74CB3T3125 is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_on), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks Vcc. The Sn74CB3T3125 supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Typical DC Voltage-Translation Characteristics).

The Sn74CB3T3125 is organized as four 1-bit bus switches with separate output-enable (1OE, 2OE, 3OE, 4OE) inputs. It can be used as four 1-bit bus switches or as one 4-bit bus switch. When OE is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CB3T3125</td>
<td>VQFN – RGY (14)</td>
<td>3.50 mm x 3.50 mm</td>
</tr>
<tr>
<td></td>
<td>TSSOP – PW (14)</td>
<td>5.00 mm x 4.40 mm</td>
</tr>
<tr>
<td></td>
<td>TVSOP – DGV (14)</td>
<td>3.60 mm x 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical DC Voltage-Translation Characteristics

If the input high voltage (Vin) level is greater than or equal to Vcc + 1 V, and less than or equal to 5.5 V, the output high voltage (Vout) level will be equal to approximately the Vcc voltage level.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2012) to Revision C  Page

• Added Application list, Device Information table, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ............................... 1

• Removed Ordering Information table. .............................................................. 1

• Changed $t_{on} V_{CC} = 3.3$ V MAX value From: 4.4 ns To: 8 ns in the Switching Characteristic .............................................................. 5

Changes from Revision A (April 2009) to Revision B  Page

• Updated Typical DC Voltage-Translation Characteristics .............................................................. 1
5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1OE</td>
<td>I</td>
<td>Active-low enable for switch 1</td>
</tr>
<tr>
<td>1A</td>
<td>I/O</td>
<td>Switch 1 A terminal</td>
</tr>
<tr>
<td>1B</td>
<td>I/O</td>
<td>Switch 1 B terminal</td>
</tr>
<tr>
<td>2OE</td>
<td>I</td>
<td>Active-low enable for switch 2</td>
</tr>
<tr>
<td>2A</td>
<td>I/O</td>
<td>Switch 2 A terminal</td>
</tr>
<tr>
<td>2B</td>
<td>I/O</td>
<td>Switch 2 B terminal</td>
</tr>
<tr>
<td>GND</td>
<td>-</td>
<td>Ground</td>
</tr>
<tr>
<td>3A</td>
<td>I/O</td>
<td>Switch 3 A terminal</td>
</tr>
<tr>
<td>3B</td>
<td>I/O</td>
<td>Switch 3 B terminal</td>
</tr>
<tr>
<td>3OE</td>
<td>I</td>
<td>Active-low enable for switch 3</td>
</tr>
<tr>
<td>4A</td>
<td>I/O</td>
<td>Switch 4 A terminal</td>
</tr>
<tr>
<td>4B</td>
<td>I/O</td>
<td>Switch 4 B terminal</td>
</tr>
<tr>
<td>4OE</td>
<td>I</td>
<td>Active-low enable for switch 4</td>
</tr>
<tr>
<td>VCC</td>
<td>-</td>
<td>Supply voltage pin</td>
</tr>
</tbody>
</table>

Product Folder Links: SN74CB3T3125
6 Specifications

6.1 Absolute Maximum Ratings\(^{(1)}\)

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IN})</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IO})</td>
<td>–0.5</td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>(I_{IK})</td>
<td>(V_{IN} &lt; 0)</td>
<td>–50</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{I/OK})</td>
<td>(V_{IO} &lt; 0)</td>
<td>–50</td>
<td>mA</td>
</tr>
<tr>
<td>(I_{IO})</td>
<td>128</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(T_{stg})</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) \(V_{I}\) and \(V_{O}\) are used to denote specific conditions for \(V_{IO}\).

(5) \(I_{I}\) and \(I_{O}\) are used to denote specific conditions for \(I_{IO}\).

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(ESD)})</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±1000</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC})</td>
<td>2.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>1.7</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>0</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IO})</td>
<td>0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>(T_{A})</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) All unused control inputs of the device must be held at \(V_{CC}\) or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>Thermal Metric(^{(1)})</th>
<th>(\text{SN74CB3T3125})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{UA})</td>
<td>Junction-to-ambient thermal resistance</td>
<td>55.5</td>
</tr>
<tr>
<td>(R_{UC(top)})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>56.9</td>
</tr>
<tr>
<td>(R_{UB})</td>
<td>Junction-to-board thermal resistance</td>
<td>30.9</td>
</tr>
<tr>
<td>(\psi_{JT})</td>
<td>Junction-to-top characterization parameter</td>
<td>3.6</td>
</tr>
<tr>
<td>(\psi_{JB})</td>
<td>Junction-to-board characterization parameter</td>
<td>30.9</td>
</tr>
<tr>
<td>(R_{UC(bot)})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>14.6</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
### 6.5 Electrical Characteristics\(^{(1)}\)

over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP(^{(2)})</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{IK})</td>
<td>(V_{CC} = 3) (V), (I_I = -18) mA</td>
<td>(-1.2)</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{OH})</td>
<td>See Figure 3 through Figure 5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_I)</td>
<td>Control inputs (V_{CC} = 3.6) (V), (V_{IN} = 3.6) (V) to 5.5 (V) or GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{OZ}) (^{(3)})</td>
<td>(V_{CC} = 3.6) (V), (V_O = 0) to 5.5 (V), (V_I = 0), Switch OFF, (V_{IN} = V_{CC}) or GND</td>
<td>(\pm 10)</td>
<td></td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{off})</td>
<td>(V_{CC} = 0), (V_O = 0) to 5.5 (V), (V_I = 0)</td>
<td></td>
<td></td>
<td>10</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{CC})</td>
<td>Control inputs (V_{CC} = 3.6) (V), (I_{CC} = 0), Switch ON or OFF, (V_{IN} = V_{CC}) or GND</td>
<td></td>
<td>20</td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(V_{I/O} = V_{CC} + 0.6) (V)</td>
<td></td>
<td></td>
<td>300</td>
<td></td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(C_{in})</td>
<td>Control inputs (V_{CC} = 3.3) (V), (V_{IN} = V_{CC}) or GND</td>
<td></td>
<td></td>
<td>3</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{io(OFF)})</td>
<td>(V_{CC} = 3.3) (V), (V_{I/O} = 5.5) (V), 3.3 (V), or GND, Switch OFF, (V_{IN} = V_{CC}) or GND</td>
<td></td>
<td></td>
<td>4.5</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{io(ON)})</td>
<td>(V_{CC} = 3.3) (V), Switch ON, (V_{IN} = V_{CC}) or GND</td>
<td></td>
<td></td>
<td>4</td>
<td>pF</td>
</tr>
<tr>
<td>(r_{on}) (^{(5)})</td>
<td>(V_{CC} = 2.3) (V), (I_O = 24) mA, (V_I = 0)</td>
<td></td>
<td></td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>(V_{CC} = 2.3) (V), (I_O = 16) mA, (V_I = 0)</td>
<td></td>
<td></td>
<td>5</td>
<td>8</td>
<td>(\Omega)</td>
</tr>
<tr>
<td>(V_{CC} = 2.3) (V), (I_O = 32) mA, (V_I = 0)</td>
<td></td>
<td></td>
<td>5</td>
<td>7</td>
<td>(\Omega)</td>
</tr>
</tbody>
</table>

(1) \(V_{IN}\) and \(I_I\) refer to control inputs. \(V_O\), \(I_O\), and \(I_{OZ}\) refer to data pins.
(2) All typical values are at \(V_{CC} = 3.3\) \(V\) (unless otherwise noted), \(T_A = 25^\circ\)C.
(3) For I/O ports, the parameter \(I_{OZ}\) includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than \(V_{CC}\) or GND.
(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

### 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>(V_{CC} = 2.5) (V) ± 0.2 (V)</th>
<th>(V_{CC} = 3.3) (V) ± 0.3 (V)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{pd}) (^{(1)})</td>
<td>A or B</td>
<td>B or A</td>
<td>0.15</td>
<td>0.25</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{en})</td>
<td>(OE)</td>
<td>A or B</td>
<td>1</td>
<td>8.5</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{dis})</td>
<td>(OE)</td>
<td>A or B</td>
<td>1</td>
<td>9</td>
<td>ns</td>
</tr>
</tbody>
</table>

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
6.7 Typical Characteristics

**Figure 1. Data Output Voltage vs Data Input Voltage**

V<sub>CC</sub> = 2.3 V

I<sub>O</sub> = 1 µA

T<sub>A</sub> = 25°C

**Figure 2. Data Output Voltage vs Data Input Voltage**

V<sub>CC</sub> = 3 V

I<sub>O</sub> = 1 µA

T<sub>A</sub> = 25°C

**Figure 3. Output Voltage High vs Supply Voltage**

V<sub>CC</sub> = 2.3 V to 3.6 V

V<sub>I</sub> = 5.5 V

T<sub>A</sub> = 85°C

**Figure 4. Output Voltage High vs Supply Voltage**

V<sub>CC</sub> = 2.3 V to 3.6 V

V<sub>I</sub> = 5.5 V

T<sub>A</sub> = 25°C

**Figure 5. Output Voltage High vs Supply Voltage**

V<sub>CC</sub> = 2.3 V to 3.6 V

V<sub>I</sub> = 5.5 V

T<sub>A</sub> = -40°C
7 Parameter Measurement Information

![Test Circuit Diagram](image)

<table>
<thead>
<tr>
<th>TEST</th>
<th>$V_{CC}$</th>
<th>S1</th>
<th>$R_L$</th>
<th>$V_i$</th>
<th>$C_L$</th>
<th>$V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{pd(s)}$</td>
<td>2.5 V ± 0.2 V</td>
<td>Open</td>
<td>500</td>
<td>3.6 V or GND</td>
<td>30 pF</td>
<td>0.3 V</td>
</tr>
<tr>
<td></td>
<td>3.3 V ± 0.3 V</td>
<td>Open</td>
<td>500</td>
<td>5.5 V or GND</td>
<td>50 pF</td>
<td>0.15 V</td>
</tr>
<tr>
<td>$t_{PLZ/PHZ}$</td>
<td>2.5 V ± 0.2 V</td>
<td>2.0 $V_{CC}$</td>
<td>500</td>
<td>GND</td>
<td>30 pF</td>
<td>0.3 V</td>
</tr>
<tr>
<td></td>
<td>3.3 V ± 0.3 V</td>
<td>2.0 $V_{CC}$</td>
<td>500</td>
<td>GND</td>
<td>50 pF</td>
<td>0.15 V</td>
</tr>
</tbody>
</table>

**NOTES:**
A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
C. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{on}$.
F. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{on}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{on}$. The $t_{pd}$ propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

**Figure 6. Test Circuit and Voltage Waveforms**
8 Detailed Description

8.1 Overview
The SN74CB3T3215 device is organized as four 1-bit bus switches with separate output-enable (1OE, 2OE, 3OE, and 4 OE) inputs. When OE is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When OE is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports. This device is fully specified for partial-power-down applications using Ioff. The Ioff feature ensures that damaging current will not backflow through the device when it is powered down. The SN74CB3T3125 device has isolation during power off. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

![Simplified Schematic, Each FET Switch (SW)](image)

Figure 7. Simplified Schematic, Each FET Switch (SW)
8.3 Feature Description

The SN74CB3T3125 is ideal for low-power portable equipment. Power consumption is low by design, \( I_{CC} = 20 \mu A \). On-state resistance is low (\( r_{on} = 5 \Omega \)) it has bidirectional data flow with near zero propagation delay. The devices minimize loading due to the low input/output capacitance \( C_{IO(OFF)} = 4.5 \text{ pF} \) Typical. Operating VCC range from 2.3 V to 3.6 V. The output tracks VCC. Data and control inputs provide undershoot clamp diodes. Control inputs can be driven by TTL or 5-V/3.3-V CMOS outputs. It supports mixed-mode signal operation on all data I/O ports. Data I/Os support 0- to 5-V signaling levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V). The device is protected from damaging current, \( I_{OFF} \), supports partial shutdown which prevents the current from flowing back through the device when it is powered down. In addition, it has 5-V tolerant I/Os with device powered up or powered down. The device is latch-up resistant with 250 mA exceeding the JESD 17 standard, providing protection from destruction due to latch-up. This device is protected against electrostatic discharge. It is tested per JESD 22 using 2000-V Human-Body Model (A114-B, Class II), and 1000-V Charged-Device Model (C101).

8.4 Device Functional Modes

Table 1 lists the functional modes for the SN74CB3T3125.

<table>
<thead>
<tr>
<th>INPUT OE</th>
<th>INPUT/OUTPUT A</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>B</td>
<td>A port = B port</td>
</tr>
<tr>
<td>H</td>
<td>Z</td>
<td>Disconnect</td>
</tr>
</tbody>
</table>

Figure 8. Logic Diagram (Positive Logic)
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
This application is specifically to connect a 5-V bus to a 3.3 V device. Ideally, set VCC to 3.3 V. It is assumed that communication in this particular application is one-directional, going from the bus controller to the device.

9.2 Typical Application

![Application Circuit Diagram](image)

**Figure 9. Application Circuit**

9.2.1 Design Requirements
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Because this design is for down-translating voltage, no pull-up resistors are required.

9.2.2 Detailed Design Procedure
1. Recommended Input conditions – Specified high and low levels. See \( V_{IH} \) and \( V_{IL} \) in **Recommended Operating Conditions** – Inputs are overvoltage tolerant allowing them to go as high as 7 V at any valid VCC.
2. Recommend output conditions – Load currents should not exceed 128 mA on each channel.
Typical Application (continued)

9.2.3 Application Curves

![Data Output Voltage vs Data Input Voltage](image)

\[ V_{CC} = 3 \text{ V} \quad I_0 = 1 \mu\text{A} \quad T_A = 25\degree\text{C} \]

**Figure 10. Data Output Voltage vs Data Input Voltage**

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions.

Each VCC terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-\(\mu\text{F}\) bypass capacitor is recommended. If there are multiple pins labeled VCC, then a 0.01-\(\mu\text{F}\) or 0.022-\(\mu\text{F}\) capacitor is recommended for each VCC because the VCC pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example VCC and VDD, a 0.1-\(\mu\text{F}\) bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-\(\mu\text{F}\) and 1-\(\mu\text{F}\) capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.
11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

![Figure 11. Example Layout](image)

<table>
<thead>
<tr>
<th>WORST</th>
<th>BETTER</th>
<th>BEST</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Worst Corner" /></td>
<td><img src="image" alt="Better Corner" /></td>
<td><img src="image" alt="Best Corner" /></td>
</tr>
</tbody>
</table>

W

2W

W

1W min.
12 Device and Documentation Support

12.1 Device Support

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary
**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74CB3T3125DGVR</td>
<td>ACTIVE</td>
<td>TVSOP</td>
<td>DGV</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>KS125</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3T3125PW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>KS125</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3T3125PWG4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>KS125</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3T3125PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>KS125</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3T3125PWRE4</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>KS125</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74CB3T3125RGYR</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>KS125</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Q1, Q2, Q3, Q4
- Sprocket Holes
- User Direction of Feed
- Pocket Quadrants

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
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</thead>
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<td>SN74CB3T3125DGVR</td>
<td>TVSOP</td>
<td>DGV</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.8</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
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<tr>
<td>SN74CB3T3125PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
<tr>
<td>SN74CB3T3125RGYR</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>3.75</td>
<td>1.15</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
<td></td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
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<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
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<tr>
<td>SN74CB3T3125DGVR</td>
<td>TVSOP</td>
<td>DGV</td>
<td>14</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
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<tr>
<td>SN74CB3T3125PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74CB3T3125RGYR</td>
<td>VQFN</td>
<td>RGY</td>
<td>14</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 per side.  
D. Falls within JEDEC: 24/48 Pins – MO-153  
14/16/20/56 Pins – MO-194  

<table>
<thead>
<tr>
<th>DIM</th>
<th>16</th>
<th>20</th>
<th>24</th>
<th>38</th>
<th>48</th>
<th>56</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>3.70</td>
<td>3.70</td>
<td>5.10</td>
<td>5.10</td>
<td>7.90</td>
<td>9.80</td>
</tr>
<tr>
<td>A MIN</td>
<td>3.50</td>
<td>3.50</td>
<td>4.90</td>
<td>4.90</td>
<td>7.70</td>
<td>9.60</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
MECHANICAL DATA

RGY (S-PQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD

Pin 1 Index Area
Top and Bottom

1.00
0.80

0.20 Nominal
Lead Frame

Sealing Plane

0.05
0.00
Sealing Height

0.50

2.00

1.50

Bottom View

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. PQFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.

4203539–2/1 06/2011
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal paste, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions](image-url)

**NOTE:** All linear dimensions are in millimeters.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC–7351 is recommended for alternate designs.  
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SQFN PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. 
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.  
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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