SN74GTL2014 4-Channel LVTTL to GTL Transceiver

1 Features

• Operates as a GTL–/GTL/GTL+ to LVTTL or LVTTL to GTL–/GTL/GTL+ Translator
• The LVTTL Inputs are Tolerant up to 5.5 V Allowing Direct Access to TTL or 5 V CMOS
• The GTL Input/Output Operate up to 3.6 V, Allowing the Device to be Used in High Voltage Open-Drain Applications
• VREF Goes Down to 0.5 V for Low Voltage CPU Usage
• Partial Power-Down Permitted
• Latch-up Protection Exceed 500 mA per JESD78
• Package Option: TSSOP14
• –40°C to 85°C Operating Temperature Range
• ESD Protection on All Terminals
  – 2000 V HBM, JESD22-A114
  – 1000 V CDM, IEC61000-4-2

2 Applications

• Server
• Base Station
• Wireline Communication

3 Description

The SN74GTL2014 is a 4-channel translator to interface between 3.3-V LVTTL chip set I/O and Xeon processor GTL–/GTL/GTL+ I/O.

The SN74GTL2014 integrates ESD protection cells on all terminals and is available in a TSSOP package (5.0 mm × 4.4 mm). The device is characterized over the free air temperature range of –40°C to 85°C.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74GTL2014</td>
<td>TSSOP (14)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
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4 Revision History

Changes from Original (February 2014) to Revision A

- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. .............................................................. 1
- Updated Specifications section .................................. 4
- Updated LVTTL/TTL to GTL–/GTL/GTL+ application schematic. .............................................................. 9
- Updated LVTTL/TTL to GTL–/GTL/GTL+ application schematic. .............................................................. 11
- Added Power Supply Recommendations .......................... 12
5 Pin Configuration and Functions

TSSOP Package (14 Pin) (Top View)

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>LVTTL data input/output</td>
</tr>
<tr>
<td>A01</td>
<td></td>
</tr>
<tr>
<td>A02</td>
<td></td>
</tr>
<tr>
<td>A03</td>
<td></td>
</tr>
<tr>
<td>B0</td>
<td>GTL data input/output</td>
</tr>
<tr>
<td>B01</td>
<td></td>
</tr>
<tr>
<td>B02</td>
<td></td>
</tr>
<tr>
<td>B03</td>
<td></td>
</tr>
<tr>
<td>DIR</td>
<td>Direction control input (LVTTL)</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>VREF</td>
<td>GTL reference voltage</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

Specified at $T_A = -40^\circ$C to $85^\circ$C unless otherwise noted$^{(1)}$

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ Supply voltage</td>
<td>$-0.5$</td>
<td>$4.6$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{IK}$ Input clamping current, $V_I &lt; 0$ V</td>
<td>$-50$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_{SEL}$ Input control voltages $SEL^{(2)(3)}$</td>
<td>$-0.5$</td>
<td>$6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_I$ Input voltage</td>
<td>A port</td>
<td>$-0.5$</td>
<td>$7$</td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>$-0.5$</td>
<td>$4.6$</td>
</tr>
<tr>
<td>$I_{OK}$ Control input clamp current, $V_O &lt; 0$ V</td>
<td>$-50$</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$V_O$ Output voltage</td>
<td>A port</td>
<td>$-0.5$</td>
<td>$7$</td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>$-0.5$</td>
<td>$4.6$</td>
</tr>
<tr>
<td>$I_{OL}$ Current into any output in the low state</td>
<td>A port</td>
<td>$40$</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>$80$</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OH}$ Current into any output in the high state</td>
<td>$-40$</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified

(3) $V_I$ and $V_O$ are used to denote specific conditions for $V_{IO}$

6.2 Handling Ratings

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{stg}$ Storage temperature range</td>
<td>$-55$</td>
<td>$150$</td>
<td>°C</td>
</tr>
<tr>
<td>$V_{ESD}^{(1)}$ Human Body Model (HBM), JEDEC: JESD22-A114$^{(2)}$</td>
<td>All pins</td>
<td>$0$</td>
<td>$2$</td>
</tr>
<tr>
<td></td>
<td>IEC61000-4-2 contact discharge$^{(3)}$</td>
<td>All pins</td>
<td>$0$</td>
</tr>
</tbody>
</table>

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have higher performance.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)$^{(1)}$

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ Supply voltage</td>
<td>$3$</td>
<td>$3.3$</td>
<td>$3.6$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{TT}$ Termination voltage</td>
<td>GDL</td>
<td>$0.85$</td>
<td>$0.9$</td>
<td>$0.95$</td>
</tr>
<tr>
<td></td>
<td>GDL</td>
<td>$1.14$</td>
<td>$1.2$</td>
<td>$1.26$</td>
</tr>
<tr>
<td></td>
<td>GDL</td>
<td>$1.35$</td>
<td>$1.5$</td>
<td>$1.65$</td>
</tr>
<tr>
<td>$V_{REF}$ Reference voltage</td>
<td>Overall</td>
<td>$0.5$</td>
<td>$2$</td>
<td>$3V_{TT}$</td>
</tr>
<tr>
<td></td>
<td>GDL</td>
<td>$0.5$</td>
<td>$0.6$</td>
<td>$0.63$</td>
</tr>
<tr>
<td></td>
<td>GDL+</td>
<td>$0.76$</td>
<td>$0.8$</td>
<td>$0.84$</td>
</tr>
<tr>
<td></td>
<td>GDL+</td>
<td>$0.87$</td>
<td>$1$</td>
<td>$1.1$</td>
</tr>
<tr>
<td>$V_I$ Input voltage</td>
<td>A port</td>
<td>$0$</td>
<td>$3.3$</td>
<td>$5.5^{(2)}$</td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>$0$</td>
<td>$V_{TT}$</td>
<td>$3.6$</td>
</tr>
<tr>
<td>$V_{IH}$ High-level input voltage</td>
<td>A port and DIR</td>
<td>$2$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>B port</td>
<td>$V_{REF} + 50$ mV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

(2) The $V_{IL(max)}$ of LVTTTL port is $3.6$ V if configured as output (DIR=L)
Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TEST CONDITIONS</th>
<th>(-40^\circ\text{C} \text{ TO } 85^\circ\text{C})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{IL}}) Low-level input voltage</td>
<td>(V_{\text{CC}} = 3 \text{ to } 3.6 \text{ V}, I_{\text{OH}} = \text{–}100 \mu\text{A})</td>
<td>(V_{\text{CC}} \text{ } 0.2)</td>
</tr>
<tr>
<td>B port</td>
<td>(V_{\text{CC}} = 3 \text{ V}, I_{\text{OH}} = \text{–}16 \text{ mA})</td>
<td>2</td>
</tr>
<tr>
<td>(I_{\text{OH}}) High-level input current</td>
<td>A port</td>
<td>0.28</td>
</tr>
<tr>
<td>B port</td>
<td>(V_{\text{CC}} = 3 \text{ V}, I_{\text{OL}} = 8 \text{ mA})</td>
<td></td>
</tr>
<tr>
<td>(I_{\text{OL}}) Low-level output current</td>
<td>A port</td>
<td>0.55</td>
</tr>
<tr>
<td>B port</td>
<td>(V_{\text{CC}} = 3 \text{ V}, I_{\text{OL}} = 16 \text{ mA})</td>
<td>0.23</td>
</tr>
<tr>
<td>(V_{\text{OL}}) Low-level output voltage</td>
<td>A port</td>
<td>(V_{\text{CC}} = 3.6 \text{ V}, V_{\text{IL}} = V_{\text{CC}})</td>
</tr>
<tr>
<td>B port</td>
<td>(V_{\text{CC}} = 3.6 \text{ V}, V_{\text{IL}} = 0 \text{ V})</td>
<td>(\pm 1)</td>
</tr>
<tr>
<td>(I_{\text{I}}) Input current</td>
<td>A port</td>
<td>(V_{\text{CC}} = 3.6 \text{ V}, V_{\text{I}} = V_{\text{TT}} \text{ or } \text{GND})</td>
</tr>
<tr>
<td>B port</td>
<td>(V_{\text{CC}} = 3.6 \text{ V}, V_{\text{I}} = 5.5 \text{ V})</td>
<td>5</td>
</tr>
<tr>
<td>(I_{\text{off}}) OFF-state output current on A port (I_{\text{off}}) OFF-state output current on B port</td>
<td>(V_{\text{CC}} = 0 \text{ V}, V_{\text{IO}} = 0 \text{ to } 3.6 \text{ V})</td>
<td>(\pm 10)</td>
</tr>
<tr>
<td>B port</td>
<td>(V_{\text{CC}} = 0 \text{ V}, V_{\text{IO}} = 3.6 \text{ to } 5.5 \text{ V})</td>
<td>(\pm 100)</td>
</tr>
<tr>
<td>(\Delta I_{\text{CC}}) A port or control input</td>
<td>(V_{\text{CC}} = 3.6 \text{ V}, V_{\text{I}} = V_{\text{CC}} \text{ or } \text{GND}, I_{\text{D}} = 0)</td>
<td>3</td>
</tr>
<tr>
<td>B port</td>
<td>(V_{\text{CC}} = 3.6 \text{ V}, V_{\text{I}} = V_{\text{TT}} \text{ or } \text{GND}, I_{\text{D}} = 0)</td>
<td>3</td>
</tr>
<tr>
<td>(C_{\text{t}}) Input capacitance of control pin</td>
<td>(V_{\text{I}} = 3.0 \text{ V or } 0 \text{ V})</td>
<td>2</td>
</tr>
<tr>
<td>B port</td>
<td>(V_{\text{O}} = 3 \text{ V or } 0)</td>
<td>4</td>
</tr>
<tr>
<td>(C_{\text{Do}}) A port or control input</td>
<td>(V_{\text{O}} = V_{\text{TT}} \text{ or } 0)</td>
<td>5.46</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>(\text{SN74GTL2014})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{JA}}) Junction-to-ambient thermal resistance</td>
<td>136.8</td>
</tr>
<tr>
<td>(R_{\text{JC(top)}}) Junction-to-case (top) thermal resistance</td>
<td>63.0</td>
</tr>
<tr>
<td>(R_{\text{JB}}) Junction-to-board thermal resistance</td>
<td>78.6</td>
</tr>
<tr>
<td>(\psi_{\text{JT}}) Junction-to-top characterization parameter</td>
<td>11.9</td>
</tr>
<tr>
<td>(\psi_{\text{JB}}) Junction-to-board characterization parameter</td>
<td>77.9</td>
</tr>
</tbody>
</table>

\(\text{(1)}\) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

Specified at \(T_{\text{A}} = \text{–}40^\circ\text{C} \text{ TO } 85^\circ\text{C}\) (unless otherwise noted)
6.6 Dynamic Electrical Characteristics

over operating range, T_A = –40°C to 85°C, V_CC = 1.65 to 4.6 V, GND = 0 V for GTL (see Functional Block Diagram)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>GTL-</th>
<th>GTL</th>
<th>GTL+</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>V_CC = 3.3 V ± 0.3 V</td>
<td>V_CC = 3.3 V ± 0.3 V</td>
<td>V_CC = 3.3 V ± 0.3 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_REF = 0.6 V</td>
<td>V_REF = 0.8 V</td>
<td>V_REF = 1 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V_TT = 0.9 V</td>
<td>V_TT = 1.2 V</td>
<td>V_TT = 1.5 V</td>
<td></td>
</tr>
<tr>
<td>t_PDL (low to high propagation delay)</td>
<td>An to Bn</td>
<td>2.8 5</td>
<td>2.8 5</td>
<td>ns</td>
</tr>
<tr>
<td>t_PHL (high to low propagation delay)</td>
<td>3.3 7</td>
<td>3.4 7</td>
<td>3.4 7</td>
<td></td>
</tr>
<tr>
<td>t_PDL (low to high propagation delay)</td>
<td>Bn to An</td>
<td>5.3 8</td>
<td>5.2 8</td>
<td>ns</td>
</tr>
<tr>
<td>t_PHL (high to low propagation delay)</td>
<td>5.2 8</td>
<td>4.9 7.16</td>
<td>4.7 7.16</td>
<td></td>
</tr>
</tbody>
</table>

6.7 Typical Characteristics

Figure 1. GTL Vth+ and Vth– vs VREF (25°C)

Figure 2. GTL Vth+ and Vth– vs VREF (–40°C)

Figure 3. GTL Vth+ and Vth– vs VREF (125°C)
7 Parameter Measurement Information

Voltage waveforms and propagation delay times are shown in Figure 4.

**VTT** = 1.2 V, **VREF** = 0.8 V for GTL and **VTT** = 1.5 V, **VREF** = 1 V for GTL+

**LOAD CIRCUIT FOR A OUTPUTS**

**LOAD CIRCUIT FOR B OUTPUTS**

**VOLTAGE WAVEFORM 1**

**PROPAGATION DELAY TIMES**

(A port to B port)†

**VOLTAGE WAVEFORM 2**

**PROPAGATION DELAY TIMES**

(B port to B port)†

**VOLTAGE WAVEFORM 3**

**PROPAGATION DELAY TIMES**

(B port to A port)†

**VOLTAGE WAVEFORM 4**

**PROPAGATION DELAY TIMES**

(ENn to A port)†

**VOLTAGE WAVEFORM 5**

**PROPAGATION DELAY TIMES**

(B port to A (I/O) port)†

**VOLTAGE WAVEFORM 6**

**ENABLE AND DISABLE TIMES**

(EN2 to A (I/O) port)†

† All control inputs are LVTTL levels.

NOTES:

A. **CL** includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, **ZO** = 50 Ω, **t** ≤ 2.5 ns, **t** ≤ 2.5 ns.

C. The outputs are measured one at a time, with one transition per measurement.

Figure 4. Load Circuits and Voltage Waveforms
8 Detailed Description

8.1 Overview
The GTL2014 is a 4-channel translating transceiver designed for 3.3-V LVTTL system interface with a GTL–/GTL/GTL+ bus, where GTL–/GTL/GTL+ refers to the reference voltage of the GTL bus and the input/output voltage thresholds associated with it.

The direction pin allows the part to function as either a GTL-to-LVTTL sampling receiver or as a LVTTL-to-GTL interface.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 5 V tolerance on LVTTL input
The GTL2014 LVTTL inputs (only) are tolerant up to 5.5 V and allows direct access to TTL or 5 V CMOS inputs. The LVTTL outputs are not 5.5 V tolerant.

8.3.2 3.6 V tolerance on GTL Input/Output
The GTL2014 GTL inputs and outputs operate up to 3.6 V, allowing the device to be used in higher voltage open-drain output applications.

8.3.3 Ultra-Low VREF and High Bandwidth
GTL2014’s VREF tracks down to 0.5 V for low voltage CPUs with excellent propagation delay performance. This feature allows the GTL2014 to support high data rates with the GTL– bus.

8.4 Device Functional Modes
The GTL2014 performs translation in two directions. One direction is GTL–/GTL/GTL+ to LVTTL when DIR is tied to GND. With appropriate VREF set up, the GTL input can be compliant with GTL–/GTL/GTL+. Another direction is LVTTL to GTL–/GTL/GTL+ when DIR is tied to VCC. 3.6 V tolerance on the GTL output allows the GTL outputs to pull up to any voltage level under 3.6 V.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
GTL2014 is the voltage translator for GTL–/GTL/GTL+ to LVTTL or LVTTL to GTL–/GTL/GTL+. Please find the reference schematic and recommend value for passive component in the Typical Application.

9.2 Typical Application

9.2.1 GTL–/GTL/GTL+ to LVTTL
Select appropriate VTT/VREF based upon GTL–/GTL/GTL+. The parameters in Recommended Operating Conditions are compliant to the GTL specification.

Figure 5. Application Diagram for GTL to LVTTL
Typical Application (continued)

9.2.1.1 Design Requirements

The GTL2014 requires industrial standard LVTTL and GTL inputs. The design example in Application Information show standard voltage level and typical resistor values.

NOTE
Only LVTTL terminals (A1/A2/A3/A4) are tolerant to 5 V.

9.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:
1. Select direction base upon application (GTL–/GTL/GTL+ to LVTTL or LVTTL to GTL–/GTL/GTL+).
2. Set up appropriate DIR pin and VREF/VTT.
3. Choose correct pullup resistor value base upon data rate and driving current requirement (for LVTTL to GTL–/GTL/GTL+).

9.2.1.3 Application Curve

![Application Curve Graph]

Figure 6. GTL-to-LVTTL, VREF = 1 V, VIN = 1.5 V, 100 MHz
Typical Application (continued)

9.2.2 LVTTL/TTL to GTL–/GTL/GTL+

Because GTL is an open-drain interface, the selection of pullup resistor depends on the application requirement (for example, data rate) and PCB trace capacitance.

![Application Diagram for LVTTL to GTL](image)

**Figure 7. Application Diagram for LVTTL to GTL**

9.2.2.1 Design Requirements

The GTL2014 requires industrial standard LVTTL and GTL inputs. The design example in the Application Information section show standard voltage level and typical resistor values.

**NOTE**

Only LVTTL terminals (A1/A2/A3/A4) are tolerant to 5 V.

9.2.2.2 Detailed Design Procedure

To begin the design process, determine the following:
1. Select direction based upon application (GTL–/GTL/GTL+ to LVTTL or LVTTL to GTL–/GTL/GTL+).
2. Set up appropriate DIR pin and VREF/VTT.
3. Choose correct pullup resistor value base upon data rate and driving current requirement (for LVTTL to GTL–/GTL/GTL+).
Typical Application (continued)

9.2.2.3  Application Curve

![Graph showing application curve for LVTTL-to-GTL, VREF = 1 V, VTT = 1.5 V, 10 MHz.]

Figure 8. LVTTL-to-GTL, VREF = 1 V, VTT = 1.5 V, 10 MHz

10  Power Supply Recommendations

Because GTL is a low voltage interface, TI recommends a 0.1-µF decoupling capacitor for VREF.

11  Layout

11.1  Layout Guidelines

Typically, GTL/LVTTL is running at a low data rate; however, the GTL2014 is optimized for excellent propagation delay, slew rate, bandwidth, and is able support 100-MHz frequencies.

11.2  Layout Example

![Diagram showing layout example for GTL trace.]

Figure 9. Layout Example for GTL Trace
12 Device and Documentation Support

12.1 Trademarks
All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.3 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74GTL2014PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>CU SN Level-1-260C-UNLIM</td>
<td>-40 to 85</td>
<td>GT14</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74GTL2014PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
<tr>
<td>SN74GTL2014PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74GTL2014PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
<tr>
<td>SN74GTL2014PWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>364.0</td>
<td>364.0</td>
<td>27.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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