Wide Operating Voltage Range of 2 V to 6 V
Outputs Can Drive Up To 10 LSTTL Loads
Low Power Consumption, 40–µA Max I CC
Typical t pd = 13 ns
±4-mA Output Drive at 5 V
Low Input Current of 1 µA Max

description/ordering information

The 'HC112 devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the fall time of the CLK pulse. Following the hold-time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops perform as toggle flip-flops by tying J and K high.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>TA</th>
<th>PACKAGE†</th>
<th>ORDERABLE PART NUMBER</th>
<th>TOP-SIDE MARKING</th>
</tr>
</thead>
<tbody>
<tr>
<td>−40°C to 85°C</td>
<td>PDIP − N</td>
<td>Tube of 25</td>
<td>SN74HC112N</td>
</tr>
<tr>
<td></td>
<td>SOIC − D</td>
<td>Tube of 40</td>
<td>SN74HC112D</td>
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<tr>
<td></td>
<td>SOIC − D</td>
<td>Reel of 2500</td>
<td>SN74HC112DR</td>
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<tr>
<td>−55°C to 125°C</td>
<td>CDIP − J</td>
<td>Tube of 25</td>
<td>SNJ54HC112J</td>
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<tr>
<td></td>
<td>CFP − W</td>
<td>Tube of 150</td>
<td>SNJ54HC112W</td>
</tr>
<tr>
<td></td>
<td>LCCC − FK</td>
<td>Tube of 55</td>
<td>SNJ54HC112FK</td>
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</table>

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
**FUNCTION TABLE**

<table>
<thead>
<tr>
<th>PRE</th>
<th>CLR</th>
<th>CLK</th>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>(\overline{Q})</th>
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</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>L</td>
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<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H†</td>
<td>H†</td>
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<tr>
<td>H</td>
<td>H</td>
<td>↓</td>
<td>L</td>
<td>L</td>
<td>Q₀</td>
<td>(\overline{Q₀})</td>
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<tr>
<td>H</td>
<td>H</td>
<td>↓</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>↓</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
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<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Q₀</td>
<td>(\overline{Q₀})</td>
</tr>
</tbody>
</table>

† This configuration is nonstable; that is, it does not persist when either PRE or CLR returns to its inactive (high) level.

**logic diagram, each flip-flop (positive logic)**

![Logic Diagram](image-url)
absolute maximum ratings over operating free-air temperature range†

Supply voltage range, \( V_{CC} \) ...................................................... \(-0.5 \) V to 7 V  
Input clamp current, \( I_{IK} \) (\( V_I < 0 \) or \( V_I > V_{CC} \)) (see Note 1) ........................................ -20 mA  
Output clamp current, \( I_{OK} \) (\( V_O < 0 \) or \( V_O > V_{CC} \)) (see Note 1) ........................................ -20 mA  
Continuous output current, \( I_O \) (\( V_O = 0 \) to \( V_{CC} \)) ........................................ -25 mA  
Continuous current through \( V_{CC} \) or GND ........................................ -50 mA  
Package thermal impedance, \( \theta_{JA} \) (see Note 2): D package ........................................ 73°C/W  
N package ........................................ 67°C/W  
Storage temperature range, \( T_{stg} \) ...................................................... \(-65^\circ\)C to 150°C  

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

<table>
<thead>
<tr>
<th>VCC</th>
<th>Supply voltage</th>
<th>SN54HC112</th>
<th>SN74HC112</th>
<th>UNIT</th>
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<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>NOM</td>
<td>MAX</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>2 V</td>
<td>1.5</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>4.5 V</td>
<td>3.15</td>
<td>3.15</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>6 V</td>
<td>4.2</td>
<td>4.2</td>
<td></td>
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<tr>
<td>Vih</td>
<td>High-level input voltage</td>
<td>VCC = 2 V</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td>VCC = 4.5 V</td>
<td>1.35</td>
<td>1.35</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCC = 6 V</td>
<td>1.8</td>
<td>1.8</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Low-level input voltage</td>
<td>VCC = 2 V</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>VCC = 4.5 V</td>
<td>1.35</td>
<td>1.35</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCC = 6 V</td>
<td>1.8</td>
<td>1.8</td>
<td></td>
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<tr>
<td>V1</td>
<td>Input voltage</td>
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<td>VCC</td>
<td>0</td>
</tr>
<tr>
<td>VO</td>
<td>Output voltage</td>
<td>0</td>
<td>VCC</td>
<td>0</td>
</tr>
<tr>
<td>( t_{\text{f}} ) ‡</td>
<td>Input transition (rise and fall) time</td>
<td>VCC = 2 V</td>
<td>1000 ns</td>
<td>1000 ns</td>
</tr>
<tr>
<td></td>
<td>VCC = 4.5 V</td>
<td>500 ns</td>
<td>500 ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VCC = 6 V</td>
<td>400 ns</td>
<td>400 ns</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Operating free-air temperature</td>
<td>(-55 ) °C</td>
<td>125 °C</td>
<td>(-40 ) °C</td>
</tr>
</tbody>
</table>

‡ If this device is used in the threshold region (from \( V_{IL_{\text{max}}} = 0.5 \) V to \( V_{IH_{\text{min}}} = 1.5 \) V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at \( t_{\text{f}} = 1000 \) ns and \( V_{CC} = 2 \) V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

NOTE 3: All unused inputs of the device must be held at \( V_{CC} \) or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
## Electrical Characteristics

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>VCC</th>
<th>$T_A = 25^\circ C$</th>
<th>SN54HC112</th>
<th>SN74HC112</th>
<th>UNIT</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
<td>MIN</td>
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<td>$V_{OH}$</td>
<td>$V_I = V_{IH}$</td>
<td>2 V</td>
<td>1.9</td>
<td>1.998</td>
<td>1.9</td>
<td></td>
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<tr>
<td></td>
<td>or $V_{IL}$</td>
<td>4.5 V</td>
<td>4.4</td>
<td>4.499</td>
<td>4.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 V</td>
<td>5.9</td>
<td>5.999</td>
<td>5.9</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{OH} = -20\ \mu A$</td>
<td>4.5 V</td>
<td>3.98</td>
<td>4.3</td>
<td>3.7</td>
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<td>6 V</td>
<td>5.48</td>
<td>5.8</td>
<td>5.2</td>
<td>5.34</td>
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<tr>
<td>$V_{OL}$</td>
<td>$V_I = V_{IH}$</td>
<td>2 V</td>
<td>0.002</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>or $V_{IL}$</td>
<td>4.5 V</td>
<td>0.001</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 V</td>
<td>0.001</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td>$I_{OL} = 20\ \mu A$</td>
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<td>0.26</td>
<td>0.4</td>
<td>0.33</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 V</td>
<td>0.15</td>
<td>0.26</td>
<td>0.4</td>
<td>0.33</td>
</tr>
<tr>
<td>$I_I$</td>
<td>$V_I = V_{CC}$</td>
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<td>±0.1</td>
<td>100</td>
<td>±1000</td>
<td>±1000</td>
</tr>
<tr>
<td></td>
<td>or 0</td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<td>$I_{CC}$</td>
<td>$V_I = V_{CC}$</td>
<td>6 V</td>
<td>4</td>
<td>80</td>
<td>40</td>
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<tr>
<td></td>
<td>or 0, $I_O = 0$</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_i$</td>
<td>$V_I = V_{CC}$</td>
<td>2 V</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>or 0</td>
<td>6 V</td>
<td></td>
<td></td>
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</table>

## Timing Requirements

<table>
<thead>
<tr>
<th>$f_{clock}$</th>
<th>Clock frequency</th>
<th>VCC</th>
<th>$T_A = 25^\circ C$</th>
<th>SN54HC112</th>
<th>SN74HC112</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
<td>MAX</td>
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<tr>
<td>$f_{clock}$</td>
<td>Clock frequency</td>
<td>2 V</td>
<td>5</td>
<td>150</td>
<td>150</td>
<td>125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>25</td>
<td>17</td>
<td>20</td>
<td>21</td>
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<tr>
<td></td>
<td></td>
<td>6 V</td>
<td></td>
<td>20</td>
<td>24</td>
<td>29</td>
</tr>
<tr>
<td>$t_w$</td>
<td>Pulse duration</td>
<td>PRE or CLR low</td>
<td>2 V</td>
<td>100</td>
<td>150</td>
<td>125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>20</td>
<td>30</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 V</td>
<td>17</td>
<td>25</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLK high or low</td>
<td>2 V</td>
<td>100</td>
<td>150</td>
<td>125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>20</td>
<td>30</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 V</td>
<td>17</td>
<td>25</td>
<td>21</td>
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</tr>
<tr>
<td>$t_{su}$</td>
<td>Setup time before CLK↓</td>
<td>Data (J, K)</td>
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<td>150</td>
<td>125</td>
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<td></td>
<td>4.5 V</td>
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<td>30</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 V</td>
<td>17</td>
<td>25</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>PRE or CLR inactive</td>
<td>2 V</td>
<td>100</td>
<td>150</td>
<td>125</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>20</td>
<td>30</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 V</td>
<td>17</td>
<td>25</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td>$t_h$</td>
<td>Hold time, data after CLK↓</td>
<td>PRE or CLR inactive</td>
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<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.5 V</td>
<td>0</td>
<td>0</td>
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<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 V</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</tr>
</tbody>
</table>
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>$V_{CC}$</th>
<th>$T_A = 25^\circ C$</th>
<th>SN54HC112</th>
<th>SN74HC112</th>
<th>UNIT</th>
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<tbody>
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<td>$f_{\text{max}}$</td>
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<td>10</td>
<td>3.4</td>
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<td></td>
<td></td>
<td>4.5 V</td>
<td>25</td>
<td>50</td>
<td>17</td>
<td>20</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>6 V</td>
<td>29</td>
<td>60</td>
<td>20</td>
<td>24</td>
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<tr>
<td>$t_{\text{pd}}$</td>
<td>PRE or CLR</td>
<td>Q or $\bar{Q}$</td>
<td>2 V</td>
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<td>165</td>
<td>245</td>
<td>205</td>
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<td></td>
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<td>4.5 V</td>
<td>16</td>
<td>33</td>
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<td>41</td>
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<td>6 V</td>
<td>13</td>
<td>28</td>
<td>42</td>
<td>35</td>
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<tr>
<td></td>
<td>CLK</td>
<td>Q or $\bar{Q}$</td>
<td>2 V</td>
<td>56</td>
<td>125</td>
<td>185</td>
<td>155</td>
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<td></td>
<td></td>
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<td>25</td>
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<td></td>
<td></td>
<td>6 V</td>
<td>13</td>
<td>21</td>
<td>31</td>
<td>26</td>
</tr>
<tr>
<td>$t_t$</td>
<td>Q or $\bar{Q}$</td>
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<td>75</td>
<td>110</td>
<td>95</td>
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<td></td>
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<td></td>
<td></td>
<td>6 V</td>
<td>8</td>
<td>13</td>
<td>19</td>
<td>16</td>
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</table>

operating characteristics, $T_A = 25^\circ C$

<table>
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<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYP</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{pd}$</td>
<td>Power dissipation capacitance</td>
<td>No load</td>
<td>35</td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES

HIGH-LEVEL PULSE

LOW-LEVEL PULSE

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES:
A. $C_L$ includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
C. For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

Figure 1. Load Circuit and Voltage Waveforms
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
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<tbody>
<tr>
<td>84088012A</td>
<td>ACTIVE</td>
<td>LCCC</td>
<td>FK</td>
<td>20</td>
<td>1</td>
<td>TBD</td>
<td>POST-PLATE</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>84088012A</td>
<td>Samples</td>
</tr>
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<td>8408801EA</td>
<td>ACTIVE</td>
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<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>8408801EA</td>
<td>Samples</td>
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<td>CFP</td>
<td>W</td>
<td>16</td>
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<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
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<td>8408801FA</td>
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<td>-55 to 125</td>
<td>8408801FA</td>
<td>Samples</td>
</tr>
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</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.
RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HC112, SN74HC112 :

- Catalog: SN74HC112
- Military: SN54HC112

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
TAPE AND REEL INFORMATION

**Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Reel Diameter (mm)** | **Reel Width W1 (mm)** | **A0 (mm)** | **B0 (mm)** | **K0 (mm)** | **P1 (mm)** | **W (mm)** | **Pin1 Quadrant**
---|---|---|---|---|---|---|---|---|---|---|---|---
SN74HC112DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1

*All dimensions are nominal.*

**Definitions:**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

---

Pack Materials-Page 1
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

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<th>NO. OF TERMINALS **</th>
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A SQ

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<tr>
<td>0.028 (0.71)</td>
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<tr>
<td>0.022 (0.54)</td>
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<tr>
<td>0.020 (0.51)</td>
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<td>0.010 (0.25)</td>
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B SQ

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<tr>
<td>0.064 (1.63)</td>
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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS-004
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS INSTRUMENTS  
www.ti.com
W (R—GDFP—F16)  CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1.14)  
0.026 (0.66)

0.080 (2.03)  
0.055 (1.40)

0.285 (7.24)  
0.245 (6.22)

0.305 (7.75) MAX

0.008 (0.20)  
0.004 (0.10)

0.019 (0.48)  
0.015 (0.38)

0.050 (1.27)

0.005 (0.13) MIN

4 Places

0.360 (9.14)  
0.250 (6.35)

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2—F16
NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.
**NOTES:**

A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

\[\text{Falls within JEDEC MS--001, except 18 and 20 pin minimum body length (Dim A).}\]

\[\text{The 20 pin end lead shoulder width is a vendor option, either half or full width.}\]
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