SN74LS07 Hex Buffers and Drivers With Open-Collector High-Voltage Outputs

1 Features
- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays

2 Applications
- AV Receivers
- Audio Docks: Portable
- Blu-ray Players and Home Theaters
- MP3 Players or Recorders
- Personal Digital Assistants (PDA)
- Solid-State Drives (SSD): Client and Enterprise
- TVs: LCD, Digital, and High-Definition (HDTV)
- Tablets: Enterprise
- Video Analytics: Server
- Wireless Headsets, Keyboards, and Mice

3 Description
These hex buffers and drivers feature high-voltage open-collector outputs to interface with high-level circuits or for driving high-current loads. They are also characterized for use as buffers for driving TTL inputs. The SN74LS07 devices have a rated output voltage of 30 V. The maximum sink current is 40 mA.

These circuits are compatible with most TTL families. Inputs are diode-clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 140 mW, and average propagation delay time is 12 ns.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE (PINS)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LS07D</td>
<td>SOIC (14)</td>
<td>8.65 mm × 3.90 mm</td>
</tr>
<tr>
<td>SN74LS07DB</td>
<td>SSOP (14)</td>
<td>6.20 mm × 5.30 mm</td>
</tr>
<tr>
<td>SN74LS07N</td>
<td>PDIP (14)</td>
<td>19.30 mm × 6.35 mm</td>
</tr>
<tr>
<td>SN74LS07NS</td>
<td>SO (14)</td>
<td>10.30 mm × 5.30 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

A ——— Y

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4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2004) to Revision D Page

- Added Device Information table, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section .................................................. 1
- Deleted SN54LS07 and SN74LS17 from the data sheet because they are obsolete and no longer supplied .............. 1
- Deleted Ordering Information table ........................................... 1
5 Pin Configuration and Functions

D, DB, N, or NS Packages
14-Pin SOIC, SSOP, PDIP, SO
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I</td>
<td>Input 1</td>
</tr>
<tr>
<td>2</td>
<td>O</td>
<td>Output 1</td>
</tr>
<tr>
<td>3</td>
<td>I</td>
<td>Input 2</td>
</tr>
<tr>
<td>4</td>
<td>O</td>
<td>Output 2</td>
</tr>
<tr>
<td>5</td>
<td>I</td>
<td>Input 3</td>
</tr>
<tr>
<td>6</td>
<td>O</td>
<td>Output 3</td>
</tr>
<tr>
<td>7</td>
<td>—</td>
<td>Ground pin</td>
</tr>
<tr>
<td>8</td>
<td>O</td>
<td>Output 4</td>
</tr>
<tr>
<td>9</td>
<td>I</td>
<td>Input 4</td>
</tr>
<tr>
<td>10</td>
<td>O</td>
<td>Output 5</td>
</tr>
<tr>
<td>11</td>
<td>I</td>
<td>Input 5</td>
</tr>
<tr>
<td>12</td>
<td>O</td>
<td>Output 6</td>
</tr>
<tr>
<td>13</td>
<td>I</td>
<td>Input 6</td>
</tr>
<tr>
<td>14</td>
<td>—</td>
<td>Power pin</td>
</tr>
</tbody>
</table>

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Product Folder Links: SN74LS07
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC}) Supply voltage</td>
<td>7</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL}) Input voltage(^{(2)})</td>
<td>7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{OL}) Output voltage(^{(2)})(^{(3)})</td>
<td>30</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(T_J) Operating virtual junction temperature</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>(T_{stg}) Storage temperature</td>
<td>–65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND.

(3) This is the maximum voltage that should be applied to any output when it is in the off state.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(E_{SD}) Electrostatic discharge</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±1000</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{CC}) Supply voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>(V_{IH}) High-level input voltage</td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{IL}) Low-level input voltage</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{OH}) High-level output voltage</td>
<td>30</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{OL}) Low-level output current</td>
<td>40</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>(T_A) Operating free-air temperature</td>
<td>0</td>
<td>70</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) All unused inputs of the device must be held at \(V_{CC}\) or GND to ensure proper device operation. See the TI application report, Implications of Slow or Floating CMOS Inputs, SCBA004.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>D (SOIC)</th>
<th>DB (SSOP)</th>
<th>N (PDIP)</th>
<th>NS (SO)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>85.2</td>
<td>97.4</td>
<td>50.2</td>
<td>82.8</td>
</tr>
<tr>
<td>(R_{JC(top)}) Junction-to-case (top) thermal resistance</td>
<td>43.5</td>
<td>49.8</td>
<td>37.5</td>
<td>40.9</td>
</tr>
<tr>
<td>(R_{JB}) Junction-to-board thermal resistance</td>
<td>39.7</td>
<td>44.5</td>
<td>30</td>
<td>41.4</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>10.9</td>
<td>16.5</td>
<td>22.3</td>
<td>12.4</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>39.4</td>
<td>44</td>
<td>29.9</td>
<td>41.1</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
6.5 Electrical Characteristics
over recommended operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS(1)</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IK}</td>
<td>V_{CC} = MIN, I_{I} = –12 mA</td>
<td>–1.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{OH}</td>
<td>V_{CC} = MIN, V_{IH} = 2 V</td>
<td>0.25</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{OL}</td>
<td>V_{CC} = MIN, V_{IL} = 0.8 V</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{I}</td>
<td>V_{CC} = MAX, V_{I} = 7 V</td>
<td>1</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IH}</td>
<td>V_{CC} = MAX, V_{I} = 2.4 V</td>
<td>20</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IL}</td>
<td>V_{CC} = MAX, V_{I} = 0.4 V</td>
<td>–0.2</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IIL}</td>
<td>V_{CC} = MAX</td>
<td>14</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IOL}</td>
<td>V_{CC} = MAX</td>
<td>45</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) I_{OL} = 40 mA

6.6 Switching Characteristics
V_{CC} = 5 V, T_{A} = 25°C (see Figure 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{PLH}</td>
<td>A</td>
<td>Y</td>
<td></td>
<td>6</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>t_{PHL}</td>
<td></td>
<td></td>
<td></td>
<td>19</td>
<td>30</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6.7 Typical Characteristics

![Figure 1. t_{PLH} vs. Temperature](image)

Figure 1. t_{PLH} vs. Temperature
7 Parameter Measurement Information

A. $C_L$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for $t_{PLH}$, $t_{PHL}$, $t_{PHZ}$, and $t_{PLZ}$; S1 is open and S2 is closed for $t_{PZH}$; S1 is closed and S2 is open for $t_{PZL}$.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \, \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
G. The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms
8 Detailed Description

8.1 Overview

The outputs of the SN74LS07 device are open-collector and can be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current for the SN74LS07 is 40 mA.

Inputs can be driven from 2.5-V, 3.3-V (LVTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.

![Schematic (Gate)](image)

Resistor values shown are nominal.

**Figure 3. Schematic (Gate)**

8.2 Functional Block Diagram

![Diagram]

8.3 Feature Description

- Allows for up translation
  - Inputs accept voltages to 5.25 V
  - Outputs accept voltages to 30 V
- High Sink-Current Capability
  - Up to 40 mA

8.4 Device Functional Modes

Table 1 lists the functions of this device.

<table>
<thead>
<tr>
<th>INPUT A</th>
<th>OUTPUT Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Hi-Z</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The SN74LS07 device is a high-drive, open-drain CMOS device that can be used for a multitude of buffer-type functions. It can produce 40 mA of drive current at 5 V. Therefore, this device is ideal for driving multiple inputs. The inputs are 5.25-V tolerant and outputs are 30-V tolerant.

9.2 Typical Application
Multiple channels of the SN74LS07 device can be used to create a positive AND logic function, as shown in Figure 4. Additionally, the SN74LS07 device can be used to drive an LED by sinking up to 40 mA, which may be more than the previous stage can sink.

![Figure 4. Typical Application Diagram](image)

9.2.1 Design Requirements
Ensure that the inputs are in a known state as defined by $V_{IH}$ and $V_{IL}$ noted in Recommended Operating Conditions, or else the outputs may be in an unknown state.

9.2.2 Detailed Design Procedure
1. Recommended Input Conditions
   - For specified high and low level, see $V_{IH}$ and $V_{IL}$ in Recommended Operating Conditions.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.25 V.
2. Recommend Output Conditions
   - Load currents must not exceed 40 mA per output.
   - Outputs must not be pulled above 30 V.
Typical Application (continued)

9.2.3 Application Curve

![Graph showing t_{PHL} vs Temperature](image)

**Figure 5. t_{PHL} vs Temperature**

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating indicated in **Recommended Operating Conditions**.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} pins, then TI recommends either a 0.01-µF or 0.022-µF capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and a 1-µF capacitor are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.
11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 6 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

11.2 Layout Example

Figure 6. Layout Diagram
12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:
- Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LS07D</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>50</td>
<td>Green</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS07</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS07DBR</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DB</td>
<td>14</td>
<td>2000</td>
<td>Green</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS07</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS07DBRG4</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DB</td>
<td>14</td>
<td>2000</td>
<td>Green</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS07</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS07DR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>Green</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS07</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS07DRE4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>Green</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>LS07</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS07N</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>14</td>
<td>25</td>
<td>Green</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>SN74LS07N</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS07NSR</td>
<td>ACTIVE</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>Green</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>74LS07</td>
<td>Samples</td>
</tr>
<tr>
<td>SN74LS07NSRG4</td>
<td>ACTIVE</td>
<td>SO</td>
<td>NS</td>
<td>14</td>
<td>2000</td>
<td>Green</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>74LS07</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

**Device** | **Package Type** | **Package Drawing** | **Pins** | **SPQ** | **Reel Diameter (mm)** | **Reel Width W1 (mm)** | **A0 (mm)** | **B0 (mm)** | **K0 (mm)** | **P1 (mm)** | **W (mm)** | **Pin1 Quadrant**
---|---|---|---|---|---|---|---|---|---|---|---|---|---
SN74LS07DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1

*All dimensions are nominal.*

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

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**TAPE DIMENSIONS**

**REEL DIMENSIONS**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

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www.ti.com 20-Dec-2018
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
<tr>
<td>SN74LS07DR</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
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</table>
MECHANICAL DATA

NS (R-PDSO-G**)
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

<table>
<thead>
<tr>
<th>DIM</th>
<th>14</th>
<th>16</th>
<th>20</th>
<th>24</th>
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<tbody>
<tr>
<td>A MAX</td>
<td>10,50</td>
<td>10,50</td>
<td>12,90</td>
<td>15,30</td>
</tr>
<tr>
<td>A MIN</td>
<td>9,90</td>
<td>9,90</td>
<td>12,30</td>
<td>14,70</td>
</tr>
</tbody>
</table>

4040062/C.03/03
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\text{Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.}\]
\[\text{Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.}\]
E. Reference JEDEC MS-012 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
N (R-PDIP-T**)  PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

<table>
<thead>
<tr>
<th>PINS</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
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</thead>
<tbody>
<tr>
<td>DIM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
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<table>
<thead>
<tr>
<th>VARIATION</th>
<th>AA</th>
<th>BB</th>
<th>AC</th>
<th>AD</th>
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<tbody>
<tr>
<td>MS-001</td>
<td></td>
<td></td>
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<td></td>
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</tbody>
</table>

** NOTES: **
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
⚠️ The 20 pin end lead shoulder width is a vendor option, either half or full width.
DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.
D. Falls within JEDEC MO-150
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