SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS175  02E36, JANUARY 1980 – REVISED MARCH 1988

- Will Not Trigger from Clear
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- 'LS422 Has Internal Timing Resistor

description

The 'LS422 and 'LS423 are identical to 'LS122 and 'LS123 except they cannot be triggered via clear.

These d-c triggered multivibrators feature output-pulse-width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The 'LS422 contains an internal timing resistor that allows the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the ganged low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS422 and 'LS423 have enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond. The 'LS422 RINT is nominally 10 k ohms.

The SN54LS422 and SN54LS423 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74LS422 and SN74LS423 are characterized for operation from 0°C to 70°C.

SN54LS422 . . . J OR W PACKAGE
SN74LS422 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

SN54LS423 . . . J OR W PACKAGE
SN74LS423 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)

NOTES: 1. An external timing capacitor may be connected between CEXT and REXT/CEXT (positive).
2. To use the internal timing resistor of 'LS422, connect RINT to VCC.
3. For improved pulse width accuracy and repeatability, connect an external resistor between REXT/CEXT and VCC with RINT open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between RINT or REXT/CEXT and VCC.
**LS422 FUNCTION TABLE**

<table>
<thead>
<tr>
<th>CLEAR</th>
<th>A1</th>
<th>A2</th>
<th>B1</th>
<th>B2</th>
<th>Q</th>
<th>Ø</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
<td>H</td>
<td>H</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>T</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>T</td>
<td>T</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>M</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>M</td>
<td>M</td>
<td>N</td>
<td>N</td>
</tr>
</tbody>
</table>

**LS423 FUNCTION TABLE**

<table>
<thead>
<tr>
<th>CLEAR</th>
<th>A</th>
<th>B</th>
<th>Q</th>
<th>Ø</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>T</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>T</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>H</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
</tbody>
</table>

1. These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

---

**RETRIGGER PULSE**

(See Note)

**OUTPUT Q**

**OUTPUT WITH/OUT RETRIGGER**

**OUTPUT PULSE CONTROL USING RETRIGGER PULSE**

**CLEAR**

**OUTPUT Q**

**OUTPUT WITH/OUT CLEAR**

**OUTPUT PULSE CONTROL USING CLEAR INPUT**

**NOTE:** Retrigger pulses starting before 0.22 C<sub>pu</sub> (in picofractals) nanoseconds after the initial trigger pulse will be ignored and the output pulse will remain unchanged.

**FIGURE 1—TYPICAL INPUT/OUTPUT PULSES**
logic symbols

\[ \text{logic diagrams (positive logic)} \]

\[ \text{Pin numbers shown are for D, J, N, and W packages.} \]

\[ \text{schematics of inputs and outputs} \]
### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MN</th>
<th>Nom</th>
<th>Max</th>
<th>MN</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, VCC</td>
<td>4.5</td>
<td>5</td>
<td>5.5</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>High-level output current, I_{OH}</td>
<td>-400</td>
<td>-400</td>
<td>-400</td>
<td>-400</td>
<td>-400</td>
<td>-400</td>
<td>μA</td>
</tr>
<tr>
<td>Low-level output current, I_{OL}</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>mA</td>
</tr>
<tr>
<td>Pulse width, t_w</td>
<td>40</td>
<td>40</td>
<td>ns</td>
<td>40</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>External timing resistance, R_{ext}</td>
<td>5</td>
<td>180</td>
<td>5</td>
<td>250</td>
<td>5</td>
<td>250</td>
<td>kΩ</td>
</tr>
<tr>
<td>External capacitance, C_{ext}</td>
<td>No restriction</td>
<td>No restriction</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wiring capacitance at R_{ext}/C_{ext} terminal</td>
<td>50</td>
<td>50</td>
<td>pF</td>
<td>50</td>
<td>50</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Operating free-air temperature, T_{A}</td>
<td>-55</td>
<td>125</td>
<td>0</td>
<td>70</td>
<td>70</td>
<td>0</td>
<td>°C</td>
</tr>
</tbody>
</table>

### Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions†</th>
<th>SN74LS†</th>
<th>SN74LS†</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IH} High-level input voltage</td>
<td>MIN</td>
<td>Nom</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>V_{IL} Low-level input voltage</td>
<td>7</td>
<td>2</td>
<td>2</td>
<td>7</td>
</tr>
<tr>
<td>V_{IC} Input clamp voltage</td>
<td>V_{CC} - MIN,</td>
<td>-1.5</td>
<td>-1.5</td>
<td></td>
</tr>
<tr>
<td>V_{OH} High-level output voltage</td>
<td>VCC = MIN,</td>
<td>2.5</td>
<td>2.5</td>
<td></td>
</tr>
<tr>
<td>V_{OL} Low-level output voltage</td>
<td>VCC = MIN, V_{IL} = V_{IH}, I_{OL} = 2 mA</td>
<td>0.25</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>I_1 Input current at</td>
<td>VCC = MAX, V_{IH} = 2 V, I_{OL} = 2 mA</td>
<td>0.25</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td>maximum input voltage</td>
<td>I_{IH} = 2.7 V,</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>I_{IL} Low-level input current</td>
<td>VCC = MAX, V_{IL} = 0.4 V,</td>
<td>20</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>I_{OS} Short-circuit output current</td>
<td>VCC = MAX,</td>
<td>-0.4</td>
<td>-0.4</td>
<td></td>
</tr>
<tr>
<td>I_{CC} Supply current</td>
<td>VCC = MAX, See Note 6</td>
<td>12</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>(current or trigger level)</td>
<td>LS422</td>
<td>12</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LS423</td>
<td>12</td>
<td>12</td>
<td></td>
</tr>
</tbody>
</table>

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_{A} = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 5. To measure V_{OH} at Q, V_{OL} at Q, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V.
6. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

### Switching Characteristics, V_{CC} = 5 V, T_{A} = 25°C, see note 7

<table>
<thead>
<tr>
<th>Parameter</th>
<th>From (Input)</th>
<th>To (Output)</th>
<th>Test Conditions</th>
<th>MN</th>
<th>Typ</th>
<th>MAX</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{PLH}</td>
<td>A</td>
<td>Q</td>
<td>C_{ext} = 0, C_{L} = 15 pF, R_{L} = 2 kΩ</td>
<td>23</td>
<td>33</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t_{PHL}</td>
<td>A</td>
<td>Q</td>
<td>V_{CC} = 5 kΩ, R_{L} = 2 kΩ</td>
<td>32</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t_{PLH}</td>
<td>A</td>
<td>Q</td>
<td>V_{CC} = 5 kΩ, R_{L} = 2 kΩ</td>
<td>34</td>
<td>56</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t_{WQ (min)}</td>
<td>A or B</td>
<td>Q</td>
<td>C_{ext} = 1000 pF, C_{L} = 15 pF, R_{L} = 2 kΩ</td>
<td>4</td>
<td>6.5</td>
<td>s</td>
<td></td>
</tr>
<tr>
<td>t_{WQ}</td>
<td>A or B</td>
<td>Q</td>
<td>C_{ext} = 1000 pF, C_{L} = 15 pF, R_{L} = 2 kΩ</td>
<td>4</td>
<td>6.5</td>
<td>s</td>
<td></td>
</tr>
</tbody>
</table>

† t_{WQ} = width of pulse output Q.

NOTE 7: Load circuits and voltage waveforms are shown in Section 1.
TYPICAL APPLICATION DATA FOR 'LS422, 'LS423†

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when \( C_{\text{EXT}} \leq 1000 \text{ pF} \), use Figure 3. For \( C_{\text{EXT}} \) between 0.1 nF and 1 \( \mu \text{F} \), the pulse width may be defined as:

\[
t_w = K \times R_T \times C_{\text{EXT}}
\]

with \( K \) obtained from Figure 4.

When \( C_{\text{EXT}} \geq 1 \mu \text{F} \), the output pulse width is defined as:

\[
t_w = 0.33 \times R_T \times C_{\text{EXT}}
\]

Where

- \( R_T \) is in kilohms (internal or external timing resistance)
- \( C_{\text{EXT}} \) is in \( \mu \text{F} \)
- \( t_w \) is in nanoseconds

For maximum noise immunity, system ground should be applied to the \( C_{\text{EXT}} \) node, even though the \( C_{\text{EXT}} \) node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS422 and 'LS423, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.

'LS422, 'LS423

TYPICAL OUTPUT PULSE WIDTH

VS

EXTERNAL TIMING CAPACITANCE

\[ V_{\text{CC}} = 5 \text{ V} \]

\[ T_A = 25^\circ \text{C} \]

\[ RT = 250k \text{ ohms} \]

\[ RT = 160k \text{ ohms} \]

\[ RT = 100k \text{ ohms} \]

\[ RT = 50k \text{ ohms} \]

\[ RT = 10k \text{ ohms} \]

\[ RT = 5k \text{ ohms} \]

\[ RT = 1k \text{ ohms} \]

\[ RT = 100 \text{ ohms} \]

\[ RT = 10 \text{ ohms} \]

† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 3
**SN54LS422, SN54LS423, SN74LS422, SN74LS423**

**RETRIGGERABLE MONOSTABLE MULTIVIBRATORS**

**TYPICAL APPLICATION DATA FOR 'LS422, 'LS423 †**

**MULTIPLIER FACTOR**

vs

**EXTERNAL CAPACITOR**

(K IS INDEPENDENT OF R)

![Multiplier Factor vs External Capacitor](image)

**DISTRIBUTION OF UNIT**

vs

**OUTPUT PULSE WIDTH**

![Distribution of Unit vs Output Pulse Width](image)

**VARIATION IN OUTPUT PULSE WIDTH**

vs

**SUPPLY VOLTAGE**

![Variation in Output Pulse Width vs Supply Voltage](image)

**VARIATION IN OUTPUT PULSE WIDTH**

vs

**FREE-AIR TEMPERATURE**

![Variation in Output Pulse Width vs Free-Air Temperature](image)

**NOTE 8:** For the LS422, the internal timing resistor, Rint was used. For the LS422/423, an external timing resistor was used for Rint.

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 8.25 V are applicable for SN54LS422 and SN54LS423 only.
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

![Reel Diagram](image)

### TAPE DIMENSIONS

- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

### TAPE AND REEL INFORMATION

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LS423NSR</td>
<td>SO</td>
<td>NS</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>8.2</td>
<td>10.5</td>
<td>2.5</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74LS423NSR</td>
<td>SO</td>
<td>NS</td>
<td>16</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
</tr>
</tbody>
</table>
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