SN74LV1T34 Single Power Supply Single Buffer GATE CMOS Logic Level Shifter

1 Features

- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Single-Supply Voltage Translator at 5-V, 3.3-V, 2.5-V, and 1.8-V V_{CC}
- Operating Range of 1.65 V to 5.5 V
- Up Translation
  - 1.2 V(1) to 1.8 V at 1.8-V V_{CC}
  - 1.5 V(1) to 2.5 V at 2.5-V V_{CC}
  - 1.8 V(1) to 3.3 V at 3.3-V V_{CC}
  - 3.3 V to 5.0 V at 5.0-V V_{CC}
- Down Translation
  - 3.3 V to 1.8 V at 1.8-V V_{CC}
  - 3.3 V to 2.5 V at 2.5-V V_{CC}
  - 5 V to 3.3 V at 3.3-V V_{CC}
- Logic Output is Referenced to V_{CC}
- Output Drive
  - 8 mA Output Drive at 5.0 V
  - 7 mA Output Drive at 3.3 V
  - 3 mA Output Drive at 1.8 V
- Characterized up to 50 MHz at 3.3 V V_{CC}
- 5-V Tolerance on Input Pins
- –40°C to +125°C Operating Temperature Range
- Supports Standard Logic Pinouts
- CMOS Output Backward Compatible With AUP1G and LVC1G Families

(1) Refer to the V_{IH}/V_{IL} and output drive for lower V_{CC} condition

2 Applications

- Industrial Controllers
- Telecom
- Portable Applications
- Servers
- PC and Notebooks

3 Description

The SN74LV1T34 device is a low voltage CMOS gate logic that operates at a wider voltage range for industrial, portable, and telecom applications. The output level is referenced to the supply voltage and is able to support 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

The input is designed with a lower threshold circuit to match 1.8 V input logic at V_{CC} = 3.3 V and can be used in 1.8 V to 3.3 V level up translation. In addition, the 5 V tolerant input pins enable down translation (that is, 3.3 V to 2.5 V output at V_{CC} = 2.5 V). The wide V_{CC} range of 1.8 V to 5.5 V allows generation of desired output levels to connect to controllers or processors.

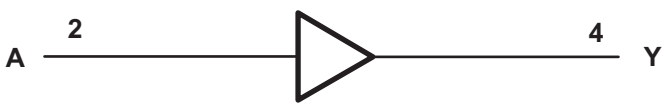
The SN74LV1T34 device is designed with current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV1T34DBV	SOT-23 (5)	2.90 mm x 1.60 mm
SN74LV1T34DCK	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2014) to Revision B — **Page**

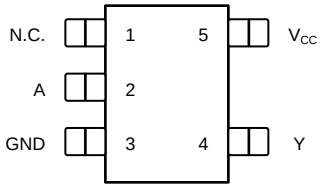
- Deleted DPW Package throughout data sheet ... 1
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Device Support*, *Documentation Support*, *Receiving Notification of Documentation Updates*, and *Community Resources* ... 1
- Added *Typical Characteristics* ... 7
- Deleted function table for the Supply V_{cc} = 3.3 V test case ... 9

Changes from Original (December 2013) to Revision A — **Page**

- Updated document formatting. ... 1

5 Pin Configuration and Functions

DBV or DCK Package
5-Pin SOT-23 or SC70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	2	I	Input A
GND	3	—	Ground
N.C.	1	—	No Connect
V_{CC}	5	—	Power Supply
Y	4	O	Output Y

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current			±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	1000	
		Machine Model (A115-A)	200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		–3	mA
		V_{CC} = 2.5 V		–5	
		V_{CC} = 3.3 V		–7	
		V_{CC} = 5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		3	mA
		V_{CC} = 2.5 V		5	
		V_{CC} = 3.3 V		7	
		V_{CC} = 5 V		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V		20	ns/V
		V_{CC} = 3.3 V or 2.5 V		20	
		V_{CC} = 5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		DBV	DCK	UNIT
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to +125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{IH}	High-level input voltage		V_{CC} = 1.65 V to 1.8 V	0.95			1		V
			V_{CC} = 2 V	0.99			1.03		
			V_{CC} = 2.25 V to 2.5 V	1.145			1.18		
			V_{CC} = 2.75 V	1.22			1.25		
			V_{CC} = 3 V to 3.3 V	1.37			1.39		
			V_{CC} = 3.6 V	1.47			1.48		
			V_{CC} = 4.5 V to 5 V	2.02			2.03		
			V_{CC} = 5.5 V	2.1			2.11		
V_{IL}	Low-level input voltage		V_{CC} = 1.65 V to 2 V			0.57		0.55	V
			V_{CC} = 2.25 V to 2.75 V			0.75		0.71	
			V_{CC} = 3 V to 3.6 V			0.8		0.65	
			V_{CC} = 4.5 V to 5.5 V			0.8		0.8	

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V_{OH}	I_{OH} = –20 µA	1.65 V to 5.5 V	V_{CC} – 0.1			V_{CC} – 0.1		V
	I_{OH} = –2.0 mA	1.65 V	1.28			1.21		
		1.8 V	1.5			1.45		
	I_{OH} = –3.0 mA	2.3 V	2			1.93		
	I_{OH} = –3.0 mA	2.5 V	2.25			2.15		
	I_{OH} = –3.0 mA	3 V	2.78			2.7		V
	I_{OH} = –5.5 mA		2.6			2.49		
	I_{OH} = –5.5 mA	3.3 V	2.9			2.8		
	I_{OH} = –4.0 mA	4.5 V	4.2			4.1		
	I_{OH} = –8.0 mA		4.1			3.95		
	I_{OH} = –8.0 mA	5 V	4.6			4.5		
V_{OL}	I_{OL} = 20 µA	1.65 V to 5.5 V			0.1		0.1	V
	I_{OL} = 2.0 mA	1.65 V			0.2		0.25	
	I_{OH} = 3.0 mA	2.3 V			0.15		0.2	
	I_{OL} = 3.0 mA	3 V			0.11		0.15	
	I_{OL} = 5.5 mA				0.21		0.252	
	I_{OL} = 4.0 mA	4.5 V			0.15		0.2	
	I_{OL} = 8.0 mA				0.3		0.35	
I_I A input	V_I = 0 V or V_{CC}	0 V, 1.8 V, 2.5 V, 3.3 V, 5.5 V			0.1		±1	µA
I_{CC}	V_I = 0 V or V_{CC}; I_O = 0; Open on loading	5 V			1		10	µA
		3.3 V			1		10	
		2.5 V			1		10	
		1.8 V			1		10	
ΔI_{CC}	One input at 0.3 V or 3.4 V Other inputs at 0 or V_{CC}, I_O = 0	5.5 V			1.35		1.5	mA
	One input at 0.3 V or 1.1 V Other inputs at 0 or V_{CC}, I_O = 0	1.8 V			10		10	µA
C_i	V_I = V_{CC} or GND	3.3 V		2	10	2	10	pF
C_o	V_O = V_{CC} or GND	3.3 V		2.5		2.5		pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	FREQUENCY (TYP)	V_{CC}	C_L	T_A = 25°C			T_A = –65°C to 125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Any In	Y	DC to 50 MHz	5.0 V	15 pF		2.7	5.5		3.4	6.5	ns
					30 pF		3	6.5		4.1	7.5	
				3.3 V	15 pF		4	7		5	8	ns
					30 pF		4.9	8		6	9	
			DC to 25 MHz	2.5 V	15 pF		5.8	8.5		6.8	9.5	ns
					30 pF		6.5	9.5		7.5	10.5	
			DC to 15 MHz	1.8 V	15 pF		10.5	13		11.8	14	ns
					30 pF		12	14.5		12	15.5	

6.7 Operating Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 1 MHz and 10 MHz	1.8 V ± 0.15 V	14	pF
			2.5 V ± 0.2 V	14	
			3.3 V ± 0.3 V	14	
			5 V ± 0.5 V	14	

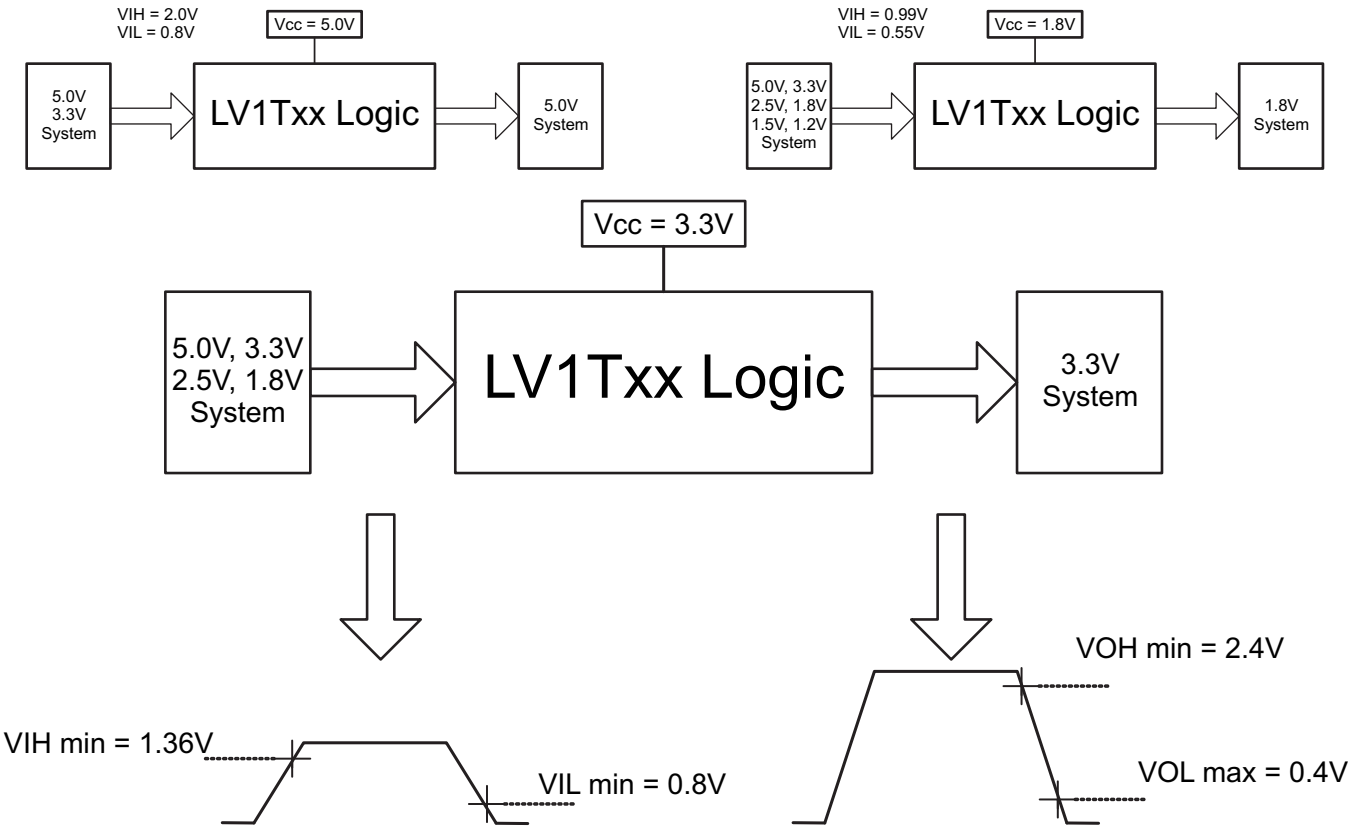
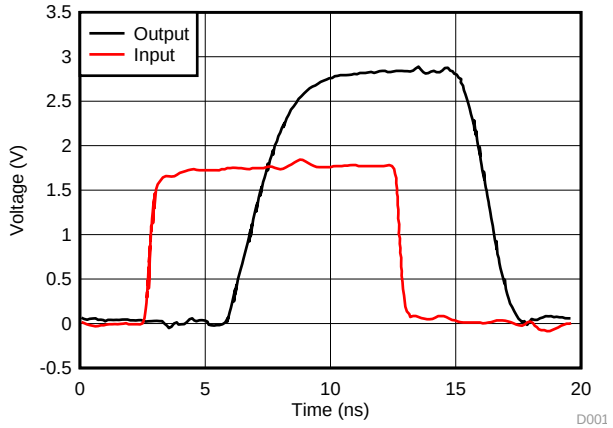


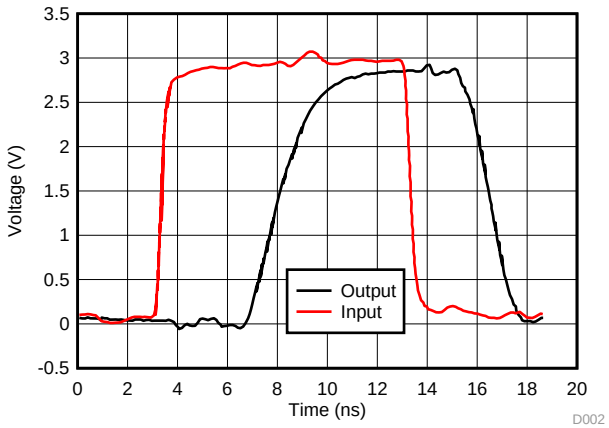
Figure 1. Switching Thresholds For 1.8-V to 3.3-V Translation

6.8 Typical Characteristics



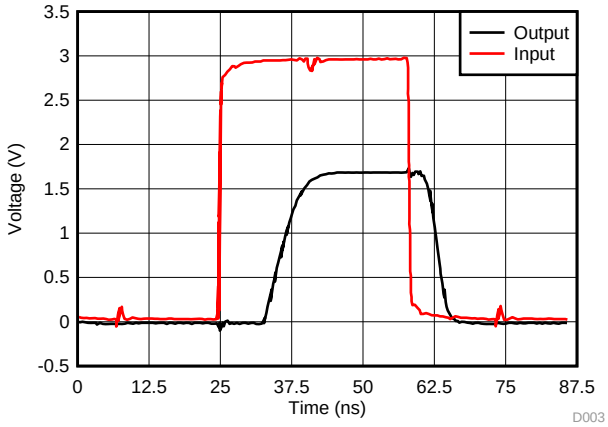
1.8 V to 3.3 V at 3.3-V V_{CC}

Figure 2. Switching Characteristics at 50 MHz Excellent Signal Integrity



3.3 V to 3.3 V at 3.3-V V_{CC}

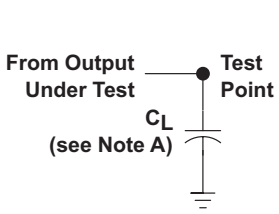
Figure 3. Switching Characteristics at 50 MHz Excellent Signal Integrity



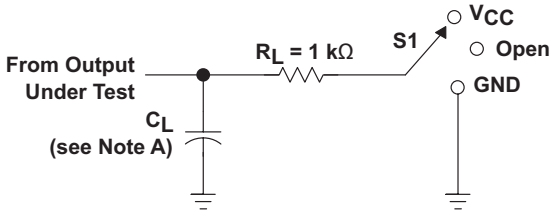
3.3 V to 1.8 V at 1.8-V V_{CC}

Figure 4. Switching Characteristics at 15 MHz Excellent Signal Integrity

7 Parameter Measurement Information

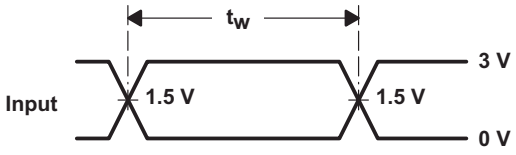


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

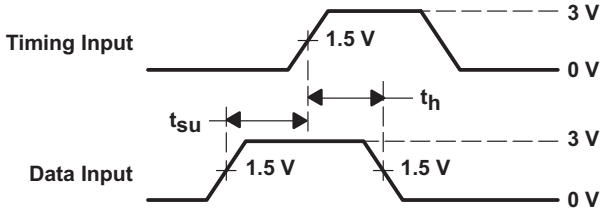


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

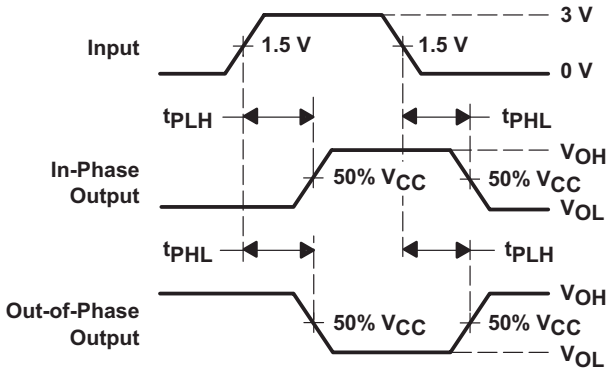
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



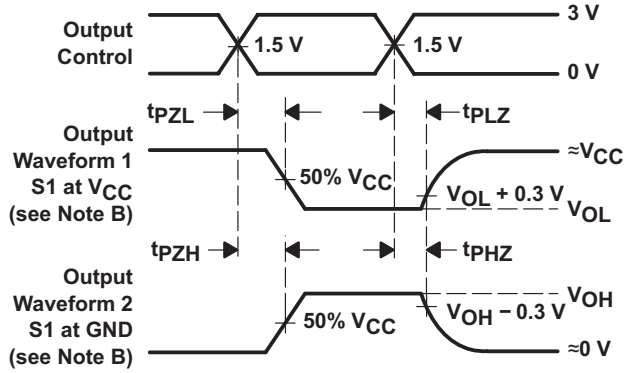
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram

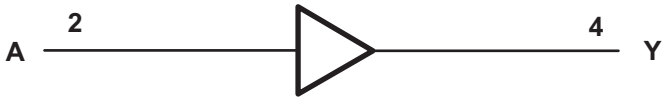


Figure 6. Logic Diagram

8.2 Device Functional Modes

Table 1 is the function table for the SN74LV1T34.

Table 1. Function Table

INPUT (LOWER LEVEL INPUT)	OUTPUT (V_{CC} CMOS)
A	Y
H	H
L	L

9 Device and Documentation Support

9.1 Device Support

Table 2. Additional Product Selection

DEVICE	PACKAGE	DESCRIPTION
SN74LV1T00	DCK, DBV	2-Input Positive-NAND Gate
SN74LV1T02	DCK, DBV	2-Input Positive-NOR Gate
SN74LV1T04	DCK, DBV	Inverter Gate
SN74LV1T08	DCK, DBV	2-Input Positive-AND Gate
SN74LV1T34	DCK, DBV	Single Buffer Gate
SN74LV1T14	DCK, DBV	Single Schmitt-Trigger Inverter Gate
SN74LV1T32	DCK, DBV	2-Input Positive-OR Gate
SN74LV1T86	DCK, DBV	Single 2-Input Exclusive-Or Gate
SN74LV1T125	DCK, DBV	Single Buffer Gate with 3-State Output
SN74LV1T126	DCK, DBV	Single Buffer Gate with 3-State Output
SN74LV4T125	RGY, PW	Quadruple Bus Buffer Gate With 3-State Outputs

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004.

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV1T34DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(NEJ3, NEJJ, NEJS)	Samples
SN74LV1T34DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	NEJ3	Samples
SN74LV1T34DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	(WJ3, WJJ, WJS)	Samples
SN74LV1T34DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		WJ3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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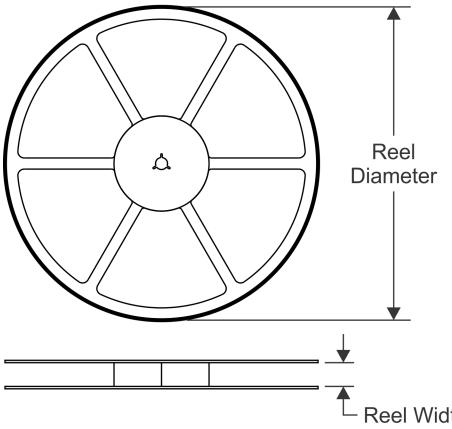
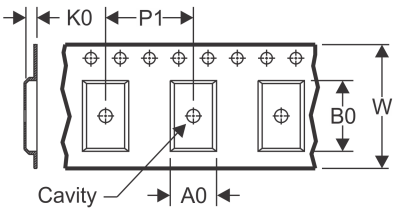
TAPE AND REEL INFORMATION

REEL DIMENSIONS

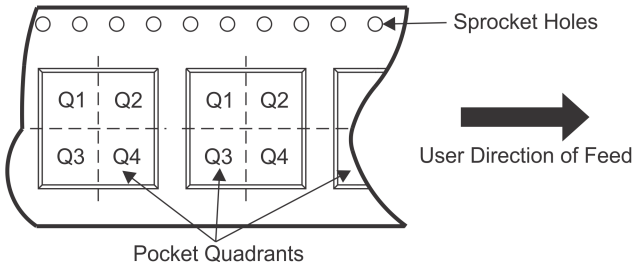


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

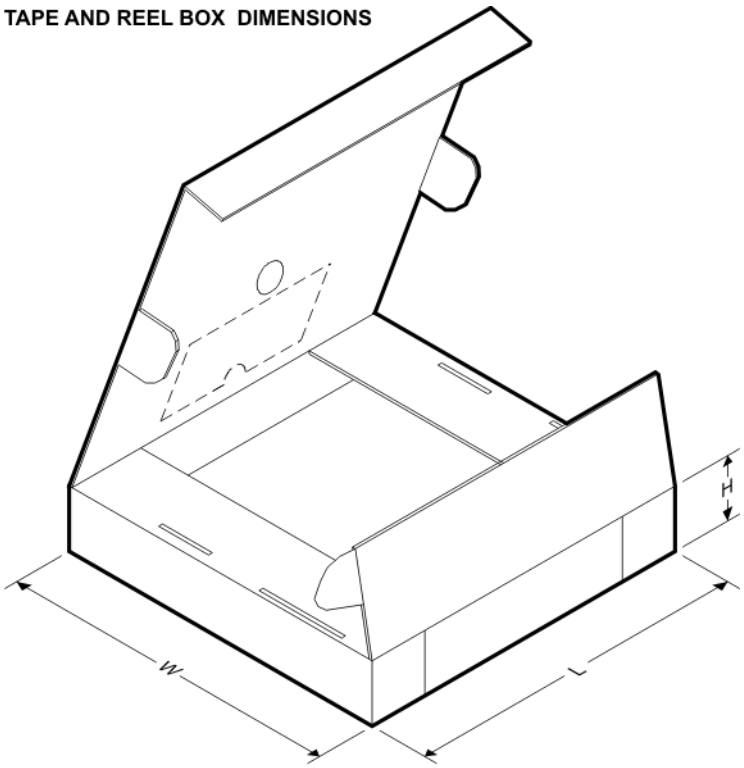
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV1T34DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LV1T34DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LV1T34DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LV1T34DBVRG4	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LV1T34DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LV1T34DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LV1T34DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

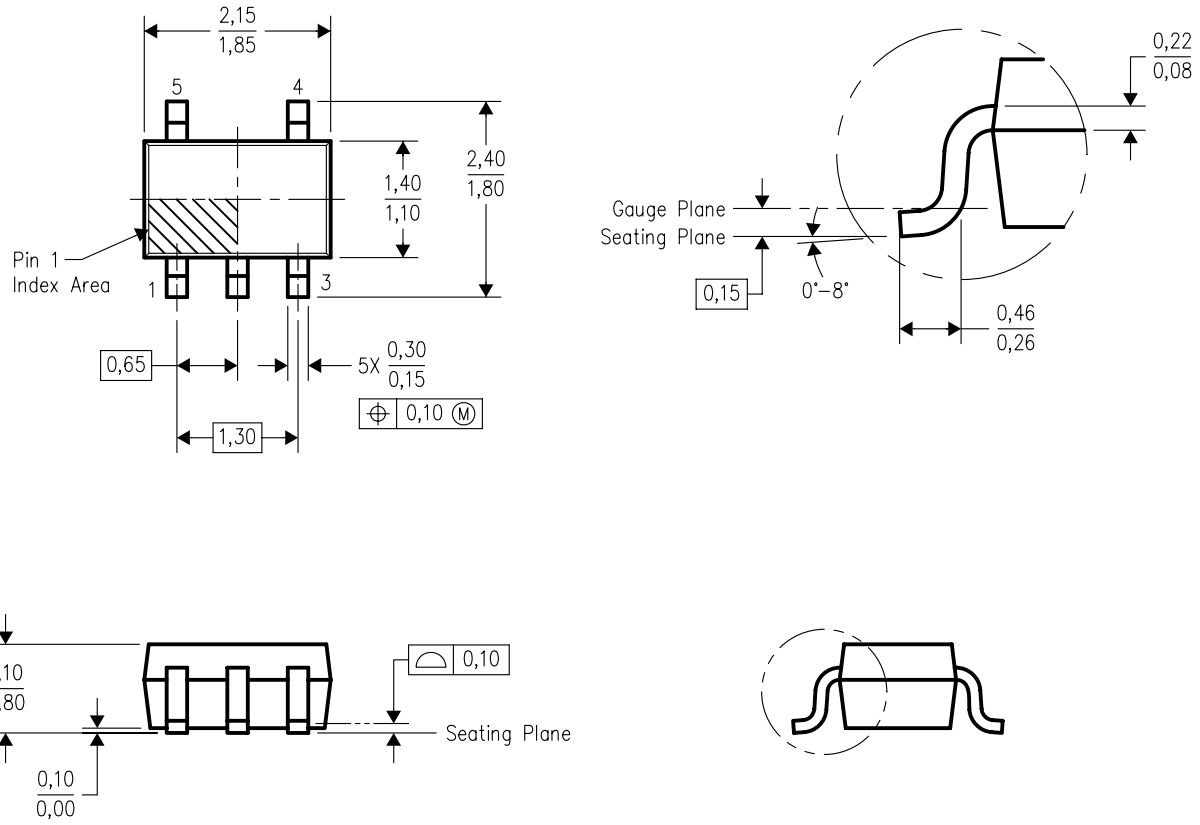
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV1T34DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T34DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LV1T34DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T34DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LV1T34DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LV1T34DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LV1T34DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0

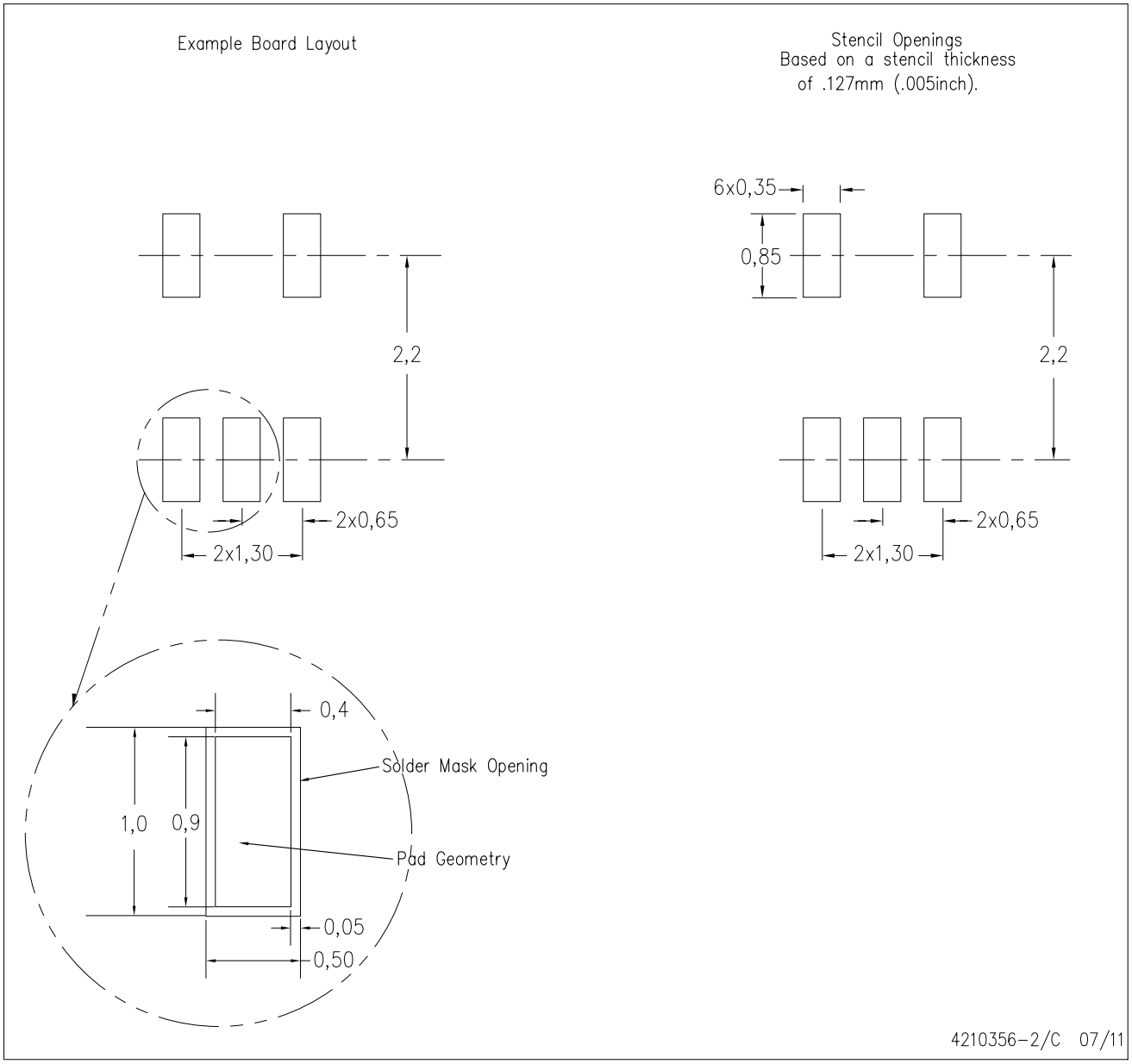
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



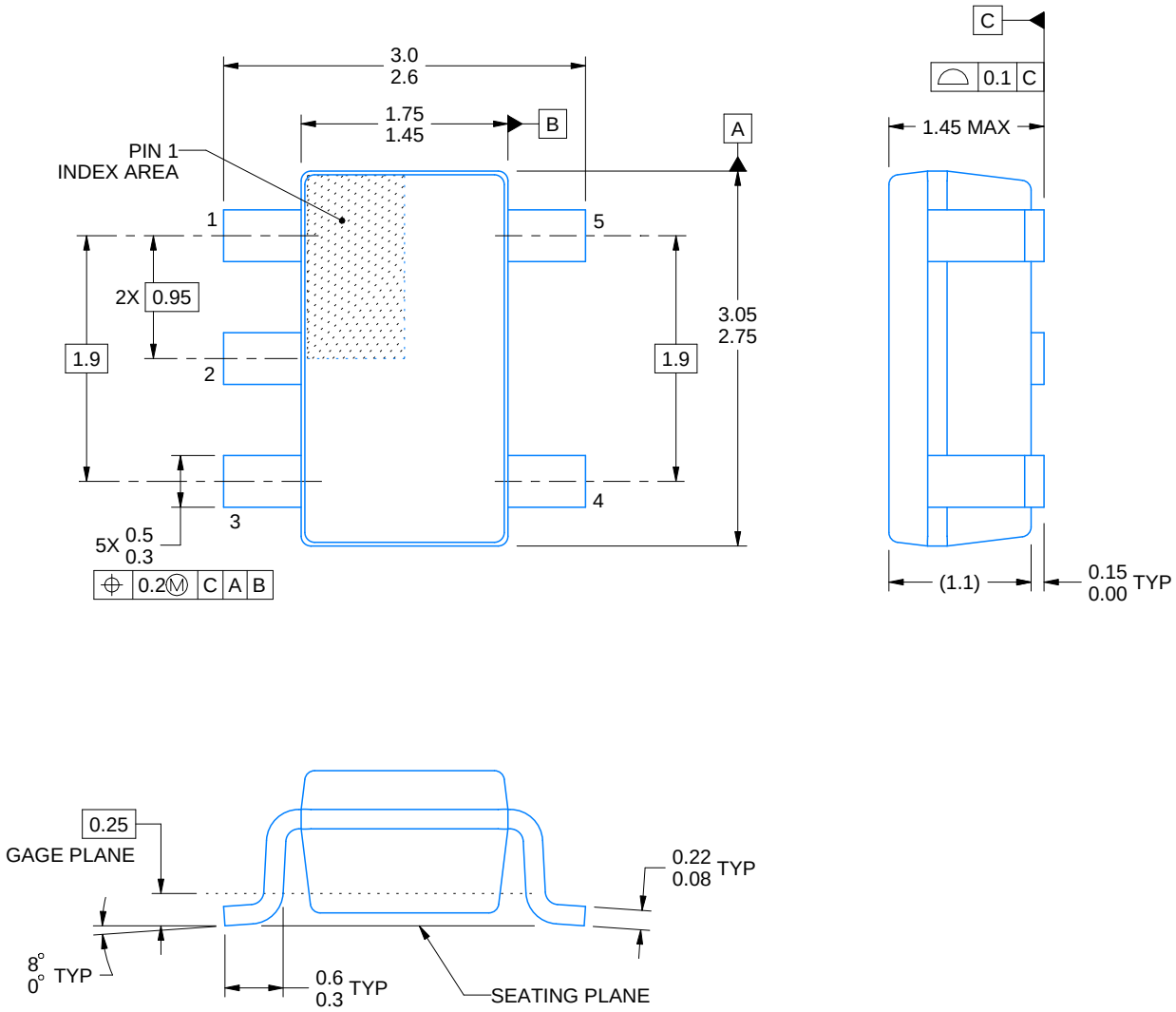
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

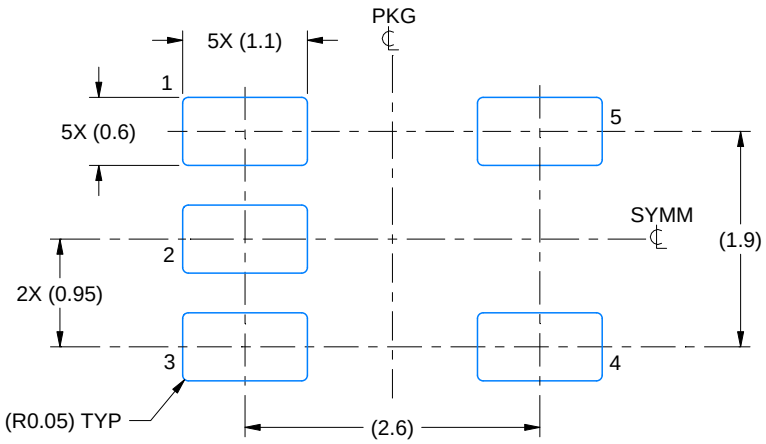
SMALL OUTLINE TRANSISTOR



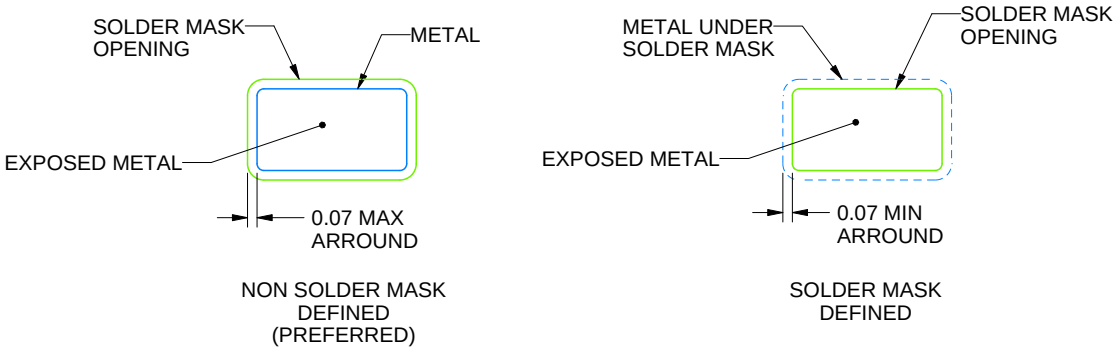
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

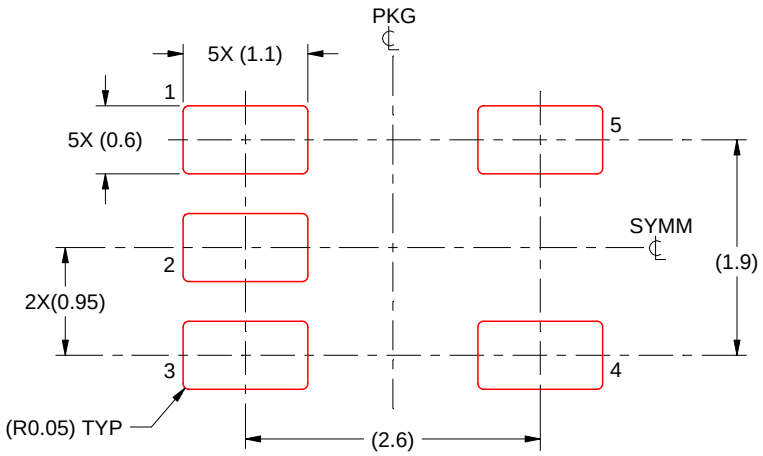


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265