**SN74S1050**

12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current... 200 mA
- 12-Bit Array Structure Suited for Bus-Oriented Systems
- ESD Protection Exceeds 10 kV Per MIL-STD-883C, Method 3015
- Package Options Include Plastic “Small Outline” Packages and Standard Plastic 300 mil DIPs

**description**

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 12-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1050 is characterized for operation from 0°C to 70°C.

**schematic diagram**

```
  1  2  3  4  5  6  7  8  9 10 11 12 13 14 15 16
D01  D02  D03  D04  D05  D06  D07  D08  D09  D10  D11  D12

   GND       GND       GND       GND
```

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SN74S1050
12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Steady-state reverse voltage, VR .................................................. 7 V
- Continuous forward current, IF; any D terminal from GND .............. 60 mA
total through all GND terminals .................................................. 170 mA
- Repetitive peak forward current, ‡ IPFM; any D terminal from GND .... 200 mA
total through all GND terminals .................................................. 1 A
- Continuous total power dissipation at or below 25°C free-air temperature .. 625 mW
- Operating free-air temperature range ....................................... 0°C to 70°C
- Storage temperature range ......................................................... -65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡These values apply for tW ≤ 100 μs, duty cycle ≤ 20%.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>IR Static reverse current</td>
<td>VR = 7 V</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>VR Static forward voltage</td>
<td>IF = 18 mA</td>
<td>0.75</td>
<td>0.95</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VR Peak forward voltage</td>
<td>IF = 50 mA</td>
<td>0.95</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>CT Total capacitance</td>
<td>VR = 0 V</td>
<td>1.46</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CT Total capacitance</td>
<td>VR = 2 V</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ix Internal crosstalk current</td>
<td>Total IF = 1 A, See Note 2</td>
<td>0.6</td>
<td>2</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Ix Internal crosstalk current</td>
<td>Total IF = 198 mA, See Note 2</td>
<td>0.02</td>
<td>0.2</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

†All typical values are at T A = 25°C.

NOTE 2: Ix is measured under the following conditions with one diode static and all others switching:

Switching diodes: tW = 100 μs, duty cycle - 20%; static diode: VR = 5 V.

The static diode's input current is the internal crosstalk current Ix.

switching characteristics at 25°C free-air temperature (see Figures 1 and 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>tTR Reverse recovery time</td>
<td>IF = 10 mA, IR(REC) = 10 mA, IR(REC) = 1 mA, RL = 100 Ω</td>
<td>8</td>
<td>16</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

INPUT PULSE (See Note A)

OUTPUT WAVEFORM (See Note B)

FIGURE 1. FORWARD RECOVERY VOLTAGE

INPUT PULSE (See Note C) 10%

OUTPUT WAVEFORM (See Note B)

FIGURE 2. REVERSE RECOVERY TIME

NOTES:
A. The input pulse is supplied by a pulse generator having the following characteristics: \( t_f = 20 \) ns, \( Z_{out} = 50 \) \( \Omega \), \( f = 600 \) Hz, duty cycle = 0.01.
B. The output waveform is monitored by an oscilloscope having the following characteristics: \( t_r < 350 \) ps, \( R_m = 50 \) \( \Omega \), \( C_m = \leq 5 \) pF.
C. The input pulse is supplied by a pulse generator having the following characteristics: \( t_f = 0.8 \) ns, \( Z_{out} = 50 \) \( \Omega \), \( t_w = \approx 50 \) ns, duty cycle \( \leq 0.01 \).

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SN74S1050
12-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.), or on the CLOCK lines of many clocked devices can result in improper operation of the device. The SN74S1050 and SN74S1062 diode termination arrays help suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to Ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients by the diode tracks the current-voltage characteristic curve for the diode. A typical current-voltage curve for the SN74S1050/S1062 is shown in Figure 3.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 4 was evaluated. The resulting waveforms with and without the diode are shown in Figure 5.

The maximum effectiveness of the diode in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

![Figure 3. Typical Current-Voltage Curve](image)

**VARIABLE 1:**

- **V1** - CH1
- LINEAR SWEEP
- START 0.000 V
- STOP 2.000 V
- STOP 0.010 V

**CONSTANTS:**

- **VH**  V31  3.5000 V
- **VL**  V32  0.0000 V

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FIGURE 4. DIODE TEST SETUP

FIGURE 5. SCOPE DISPLAY

Y-COORDINATE = 1.800 VOLTS/DIV
TIMEBASE = 5.00 ns/VOLTS
VMARKER 1 = -1.353 VOLTS
VMARKER 2 = -3.647 VOLTS
OFFSET = 0.000 VOLTS
DELAY = 56.500 ns
DELTA V = -2.293 VOLTS
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74S1050D</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>S1050</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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MECHANICAL DATA

D (R-PDSO-C16)

PLASTIC SMALL OUTLINE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
   ▲ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.
   ▲ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E. Reference JEDEC MS-012 variation AC.
NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.