Designed to Reduce Reflection Noise
Repetitive Peak Forward Current to 200 mA
16-Bit Array Structure Suited for Bus-Oriented Systems
Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

Description

This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of a 16-bit high-speed Schottky diode array suitable for clamping to $V_{CC}$ and/or GND.

The SN74S1053 is characterized for operation from $0^\circ C$ to $70^\circ C$.

Schematic diagrams

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

- Steady-state reverse voltage, $V_R$: Any D terminal from GND or to VCC .......................... 7 V
- Continuous forward current, $I_F$: Any D terminal from GND or VCC ...................................... 50 mA
  - Total through all GND or VCC terminals .......................................................... 170 mA
- Repetitive peak forward current‡, $I_{FRM}$: Any D terminal from GND or VCC .................. 200 mA
  - Total through all GND or VCC terminals .......................................................... 1.2 A
- Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 1) .......... 625 mW
- Storage temperature range, $T_{stg}$: .............................................................. –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_w \leq 100 \mu s$, duty cycle $\leq 20\%$.

NOTE 1: For operation above 25°C free-air temperature, derate linearly at the rate of 5 mW/°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### single-diode operation (see Note 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP $\S$</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_F$ Static forward voltage</td>
<td>To VCC</td>
<td>$I_F = 18 \text{ mA}$</td>
<td>0.85</td>
<td>1.05</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_F = 50 \text{ mA}$</td>
<td>1.05</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>From GND</td>
<td>$I_F = 18 \text{ mA}$</td>
<td>0.75</td>
<td>0.95</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_F = 50 \text{ mA}$</td>
<td>0.95</td>
<td>1.2</td>
<td></td>
</tr>
<tr>
<td>$V_{FM}$ Peak forward voltage</td>
<td>To VCC</td>
<td>$I_F = 200 \text{ mA}$</td>
<td>1.45</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_R$ Static reverse current</td>
<td>To VCC</td>
<td>$V_R = 7 \text{ V}$</td>
<td>5</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td>From GND</td>
<td>$V_R = 7 \text{ V}$</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_t$ Total capacitance</td>
<td>$V_R = 0 \text{ V}$, $f = 1 \text{ MHz}$</td>
<td>8</td>
<td>16</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_R = 2 \text{ V}$, $f = 1 \text{ MHz}$</td>
<td>4</td>
<td>8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$\S$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25\°C$.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

### multiple-diode operation

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP $\S$</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_x$ Internal crosstalk current</td>
<td>Total $I_F$ current = 1 A, See Note 3</td>
<td>0.8</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Total $I_F$ current = 198 mA, See Note 3</td>
<td>0.02</td>
<td>0.2</td>
<td></td>
<td></td>
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</tbody>
</table>

$\S$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25\°C$.

NOTE 3: $I_x$ is measured under the following conditions with one diode static, and all others switching:
- Switching diodes: $I_{w} = 100 \mu s$, duty cycle $= 20\%$
- Static diode: $V_R = 5 \text{ V}$
- The static diode input current is the internal crosstalk current $I_x$.

### switching characteristics, $T_A = 25\°C$ (see Figures 1 and 2)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{rr}$ Reverse recovery time</td>
<td>$I_F = 10 \text{ mA}$, $I_{RM(REC)} = 10 \text{ mA}$, $I_{R(REC)} = 1 \text{ mA}$, $R_L = 100 \Omega$</td>
<td>8</td>
<td>16</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

![Diagram of measurement setup]

NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_r = 20$ ns, $Z_O = 50 \, \Omega$, freq = 500 Hz, duty cycle = 1%.

B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50 \, \Omega$, $C_i \leq 5$ pF.

**Figure 1. Forward Recovery Voltage**

![Diagram of measurement setup]

NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_f = 0.5$ ns, $Z_O = 50 \, \Omega$, $t_w \geq 50$ ns, duty cycle = 1%.

B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50 \, \Omega$, $C_i \leq 5$ pF.

**Figure 2. Reverse Recovery Time**
APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1053 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. Typical current versus voltage curves for the SN74S1053 are shown in Figures 3 and 4.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 5 was evaluated. The resulting waveforms with and without the diode are shown in Figure 6.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes also can be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

![Diode Forward Current vs Diode Forward Voltage](image)

**Figure 3. Typical Input Current vs Input Voltage (Lower Diode)**
Figure 4. Typical Input Current vs Input Voltage (Upper Diode)
APPLICATION INFORMATION

\[ Z_0 = 50 \ \Omega \]
Length = 36 in.

Figure 5. Diode Test Setup

31.500 ns  
56.500 ns  
81.500 ns

End-of-Line Without Diode

End-of-Line With Diode

Figure 6. Oscilloscope Display

Ch 2 = 1.880 V/div  
Timebase = 5.00 ns/V  
Memory 1 = 1.880 V/div  
Vmarker 1 = –1.353 V  
Vmarker 2 = –3.647 V

Offset = 0.000 V  
Delay = 56.500 ns  
Delta V = –2.293 V
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN74S1053DBR</td>
<td>ACTIVE</td>
<td>SSOP</td>
<td>DB</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>S1053</td>
<td><img src="https://www.ti.com" alt="Samples" /></td>
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<tr>
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<td>SOIC</td>
<td>DW</td>
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<td>S1053</td>
<td><img src="https://www.ti.com" alt="Samples" /></td>
</tr>
<tr>
<td>SN74S1053DWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>S1053</td>
<td><img src="https://www.ti.com" alt="Samples" /></td>
</tr>
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<td>N / A for Pkg Type</td>
<td>0 to 70</td>
<td>SN74S1053N</td>
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<td>SN74S1053NSR</td>
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<td>NS</td>
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<td>Green (RoHS &amp; no Sb/Br)</td>
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<td>Level-1-260C-UNLIM</td>
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<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>70</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>S1053</td>
<td><img src="https://www.ti.com" alt="Samples" /></td>
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<tr>
<td>SN74S1053PWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 70</td>
<td>S1053</td>
<td><img src="https://www.ti.com" alt="Samples" /></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

![Reel Dimensions Diagram]

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>Dimension designed to accommodate the component width</td>
</tr>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram]

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<tbody>
<tr>
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<td>SSOP</td>
<td>DB</td>
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<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>8.2</td>
<td>7.5</td>
<td>2.5</td>
<td>12.0</td>
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<td>Q1</td>
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<td>16.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>SSOP</td>
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<td>2000</td>
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<tr>
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<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
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</tbody>
</table>

*All dimensions are nominal*
NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.

E. Falls within JEDEC MO-153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
MECHANICAL DATA

NS (R-PDSO-G**)
14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

<table>
<thead>
<tr>
<th>DIM</th>
<th>14</th>
<th>16</th>
<th>20</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>10.50</td>
<td>10.50</td>
<td>12.90</td>
<td>15.30</td>
</tr>
<tr>
<td>A MIN</td>
<td>9.90</td>
<td>9.90</td>
<td>12.30</td>
<td>14.70</td>
</tr>
</tbody>
</table>

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