

# TCA9546A Low Voltage 4-Channel I<sup>2</sup>C and SMBus Switch with Reset Function

## 1 Features

- 1-of-4 Bidirectional Translating Switches
- I<sup>2</sup>C Bus and SMBus Compatible
- Active-Low Reset Input
- Three Address Pins, Allowing up to Eight TCA9546A Devices on the I<sup>2</sup>C Bus
- Channel Selection Via I<sup>2</sup>C Bus, in Any Combination
- Power-up With All Switch Channels Deselected
- Low R<sub>ON</sub> Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA Per JESD 78
- ESD Protection Exceeds JESD 22
  - 4000-V Human-Body Model (A114-A)
  - 1500-V Charged-Device Model (C101)

## 2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I<sup>2</sup>C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

## 3 Description

The TCA9546A is a quad bidirectional translating switch controlled via the I<sup>2</sup>C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SC<sub>n</sub>/SD<sub>n</sub> channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active-low reset ( $\overline{\text{RESET}}$ ) input allows the TCA9546A to recover from a situation in which one of the downstream I<sup>2</sup>C buses is stuck in a low state. Pulling  $\overline{\text{RESET}}$  low resets the I<sup>2</sup>C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

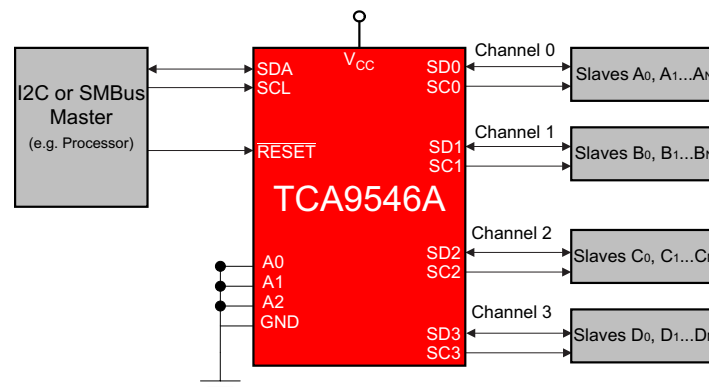
The pass gates of the switches are constructed such that the VCC pin can be used to limit the maximum high voltage, which will be passed by the TCA9546A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5-V tolerant.

### Device Information<sup>(1)</sup>

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
TCA9546A	TSSOP (16)	5.00 mm x 4.40 mm
	SOIC (16)	9.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Simplified Application Diagram



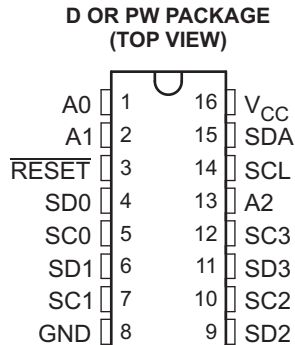
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## 5 Revision History

Changes from Original (April 2014) to Revision A	Page
• Added D package to the datasheet. ....	<b>1</b>
• Changed Handling Ratings table to ESD Ratings. ....	<b>4</b>
• Added D package to the Thermal Information table. ....	<b>4</b>

## 6 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NO. D, PW	
A0	1	Address input 0. Connect directly to V <sub>CC</sub> or ground.
A1	2	Address input 1. Connect directly to V <sub>CC</sub> or ground.
RESET	3	Active low reset input. Connect to V <sub>CC</sub> or V <sub>DPUM</sub> <sup>(1)</sup> through a pull-up resistor, if not used.
SD0	4	Serial data 0. Connect to V <sub>DPU0</sub> <sup>(1)</sup> through a pull-up resistor.
SC0	5	Serial clock 0. Connect to V <sub>DPU0</sub> <sup>(1)</sup> through a pull-up resistor.
SD1	6	Serial data 1. Connect to V <sub>DPU1</sub> <sup>(1)</sup> through a pull-up resistor.
SC1	7	Serial clock 1. Connect to V <sub>DPU1</sub> <sup>(1)</sup> through a pull-up resistor.
GND	8	Ground
SD2	9	Serial data 2. Connect to V <sub>DPU2</sub> <sup>(1)</sup> through a pull-up resistor.
SC2	10	Serial clock 2. Connect to V <sub>DPU2</sub> <sup>(1)</sup> through a pull-up resistor.
SD3	11	Serial data 3. Connect to V <sub>DPU3</sub> <sup>(1)</sup> through a pull-up resistor.
SC3	12	Serial clock 3. Connect to V <sub>DPU3</sub> <sup>(1)</sup> through a pull-up resistor.
A2	13	Address input 2. Connect directly to V <sub>CC</sub> or ground.
SCL	14	Serial clock line. Connect to V <sub>DPUM</sub> <sup>(1)</sup> through a pull-up resistor.
SDA	15	Serial data line. Connect to V <sub>DPUM</sub> <sup>(1)</sup> through a pull-up resistor.
VCC	16	Supply power

(1) V<sub>DPUX</sub> is the pull-up reference voltage for the associated data line. V<sub>DPUM</sub> is the master I<sup>2</sup>C master reference voltage and V<sub>DPU0</sub>-V<sub>DPU3</sub> are the slave channel reference voltages.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
I <sub>I</sub>	Input current		±20	mA
I <sub>O</sub>	Output current		±25	mA
	Continuous current through V <sub>CC</sub>		±100	mA
	Continuous current through GND		±100	mA
P <sub>tot</sub>	Total power dissipation		400	mW
T <sub>A</sub>	Operating free-air temperature range	-40	85	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 7.3 Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	6
		A2–A0, $\overline{\text{RESET}}$	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	-0.5	0.3 × V <sub>CC</sub>
		A2–A0, $\overline{\text{RESET}}$	-0.5	0.3 × V <sub>CC</sub>
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TCA9546A		UNIT	
	D	PW		
	16 PINS	16 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	92.3	122.3	°C/W
R <sub>θJctop</sub>	Junction-to-case (top) thermal resistance	52.3	56.6	
R <sub>θJB</sub>	Junction-to-board thermal resistance	50.1	57.4	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	17.7	10.9	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	49.8	66.8	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics<sup>(1)</sup>

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>PORR</sub>	Power-on reset voltage, V <sub>CC</sub> rising	No load,	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>			1.2	1.5	V
V <sub>PORF</sub>	Power-on reset voltage, V <sub>CC</sub> falling <sup>(4)</sup>	No load,	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>		0.8	1		
V <sub>pass</sub>	Switch output voltage	V <sub>SWin</sub> = V <sub>CC</sub> ,	I <sub>SWout</sub> = -100 μA	5 V		3.6		V
				4.5 V to 5.5 V		2.6	4.5	
				3.3 V		1.9		
				3 V to 3.6 V	1.6		2.8	
				2.5 V		1.4		
				2.3 V to 2.7 V	1.0		1.8	
				1.8 V		0.8		
				1.65 V to 1.95 V	0.5		1.1	
I <sub>OL</sub>	SDA	V <sub>OL</sub> = 0.4 V		1.65 V to 5.5 V	3	7		mA
		V <sub>OL</sub> = 0.6 V			6	10		
I <sub>i</sub>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>		1.65 V to 5.5 V			±1	μA
	SC3–SC0, SD3–SD0						±1	
	A2–A0						±1	
	RESET						±1	
I <sub>CC</sub>	Operating mode	f <sub>SCL</sub> = 400 kHz	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup> I <sub>O</sub> = 0 t <sub>r,max</sub> = 300 ns	5.5 V		50		μA
				3.6 V		20		
				2.7 V		11		
				1.65 V		6		
		f <sub>SCL</sub> = 100 kHz	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup> I <sub>O</sub> = 0 t <sub>r,max</sub> = 1 μs	5.5 V		35		
				3.6 V		14		
				2.7 V		5		
				1.65 V		2		
	Standby mode	Low inputs	V <sub>I</sub> = GND <sup>(3)</sup> I <sub>O</sub> = 0	5.5 V		1.6	2	
				3.6 V		1.0	1.3	
				2.7 V		0.7	1.1	
				1.65 V		0.4	0.55	
High inputs	V <sub>I</sub> = V <sub>CC</sub> I <sub>O</sub> = 0	5.5 V		1.6	2			
		3.6 V		1.0	1.3			
		2.7 V		0.7	1.1			
		1.65 V		0.4	0.55			
ΔI <sub>CC</sub>	Supply-current change	SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V <sub>CC</sub> or GND <sup>(3)</sup>	1.65 V to 5.5 V		2	15	μA
			SCL or SDA input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND <sup>(3)</sup>	1.65 V to 5.5 V		2	15	
C <sub>i</sub>	A2–A0	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>		1.65 V to 5.5 V		4.5	6	pF
	RESET					4.5	5.5	
C <sub>i(OFF)</sub> <sup>(5)</sup>	SCL, SDA	V <sub>I</sub> = V <sub>CC</sub> or GND <sup>(3)</sup>	Switch OFF	1.65 V to 5.5 V		15	19	pF
	SC3–SC0, SD3–SD0					6	8	

(1) For operation between specified voltage ranges, refer to the worst-case parameter in both applicable ranges.

(2) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V<sub>CC</sub>), T<sub>A</sub> = 25°C.

(3) RESET = V<sub>CC</sub> (held high) when all other input voltages, V<sub>I</sub> = GND.

(4) The power-on reset circuit resets the I<sup>2</sup>C bus logic with V<sub>CC</sub> < V<sub>PORF</sub>.

(5) C<sub>i(OFF)</sub> depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON.

## Electrical Characteristics<sup>(1)</sup> (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
R <sub>ON</sub>	Switch on-state resistance	V <sub>O</sub> = 0.4 V	I <sub>O</sub> = 15 mA	4.5 V to 5.5 V	4	10	16	Ω
				3 V to 3.6 V	5	13	20	
		V <sub>O</sub> = 0.4 V	I <sub>O</sub> = 10 mA	2.3 V to 2.7 V	7	16	45	
				1.65 V to 1.95 V	10	25	70	

## 7.6 I<sup>2</sup>C Interface Timing Requirements

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 5](#))

		STANDARD MODE I <sup>2</sup> C BUS		FAST MODE I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	
f <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	100	0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	250		100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0 <sup>(1)</sup>		0 <sup>(1)</sup>		μs
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1000	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time		300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output fall time	10-pF to 400-pF bus	300	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start	4.7		1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	4.7		0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	4		0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup	4		0.6		μs
t <sub>vdL(Data)</sub>	Valid-data time (high to low) <sup>(3)</sup>	SCL low to SDA output low valid	1		1	μs
t <sub>vdH(Data)</sub>	Valid-data time (low to high) <sup>(3)</sup>	SCL low to SDA output high valid	0.6		0.6	μs
t <sub>vd(ack)</sub>	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low	1		1	μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH</sub> min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.

(2) C<sub>b</sub> = total bus capacitance of one bus line in pF

(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see [Figure 5](#))

## 7.7 Switching Characteristics

 over recommended operating free-air temperature range, C<sub>L</sub> ≤ 100 pF (unless otherwise noted) (see [Figure 5](#))

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pd</sub> <sup>(1)</sup>	Propagation delay time	R <sub>ON</sub> = 20 Ω, C <sub>L</sub> = 15 pF	SDA or SCL	SDn or SCn	0.3	ns
		R <sub>ON</sub> = 20 Ω, C <sub>L</sub> = 50 pF			1	

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### 7.8 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{WL}$	Pulse duration, $\overline{\text{RESET}}$ low	6		ns
$t_{rst}^{(1)}$	$\overline{\text{RESET}}$ time (SDA clear)		500	ns
$t_{REC(STA)}$	Recovery time from $\overline{\text{RESET}}$ to start	0		ns

(1)  $t_{rst}$  is the propagation delay measured from the time the  $\overline{\text{RESET}}$  pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of  $t_{WL}$ .

### 7.9 Typical Characteristics

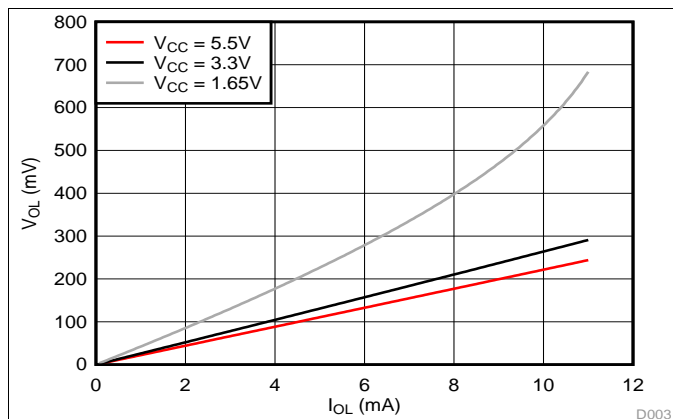


Figure 1. SDA Output Low Voltage ( $V_{OL}$ ) vs Load Current ( $I_{OL}$ ) at Three  $V_{CC}$  Levels

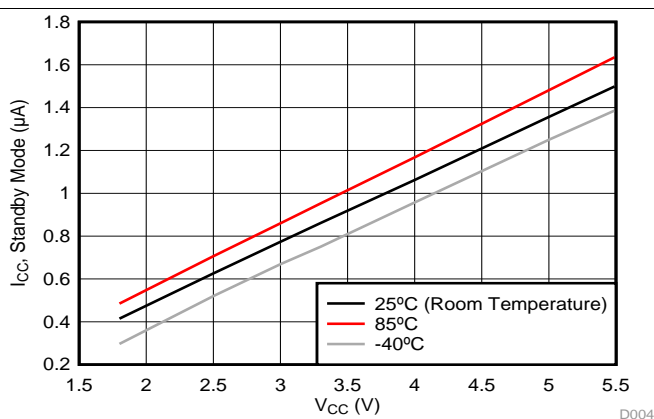


Figure 2. Standby Current ( $I_{CC}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperature Points

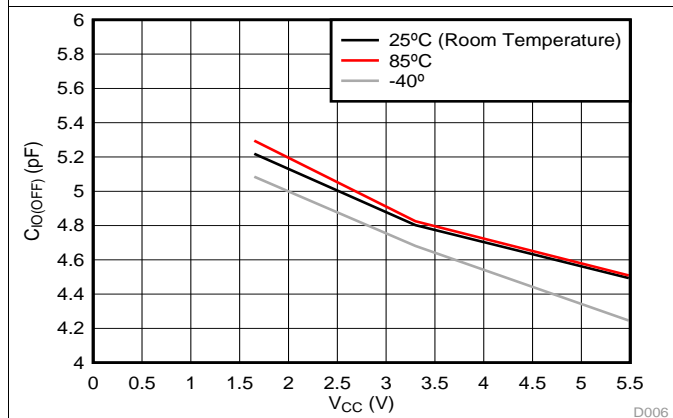


Figure 3. Slave channel (SCn/SDn) capacitance ( $C_{iO(OFF)}$ ) vs. Supply Voltage ( $V_{CC}$ ) at Three Temperature Points

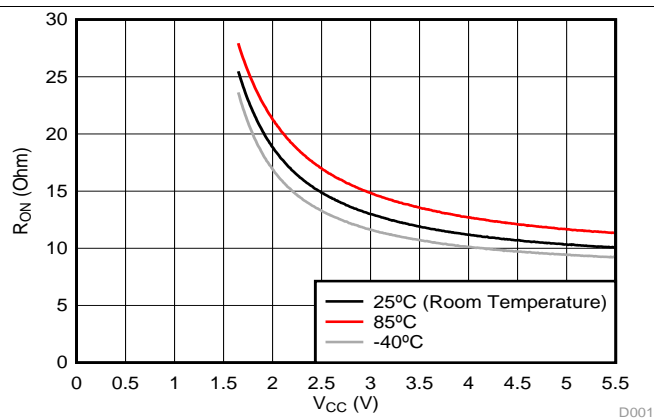


Figure 4. ON-Resistance ( $R_{ON}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperatures





Parameter Measurement Information (continued)

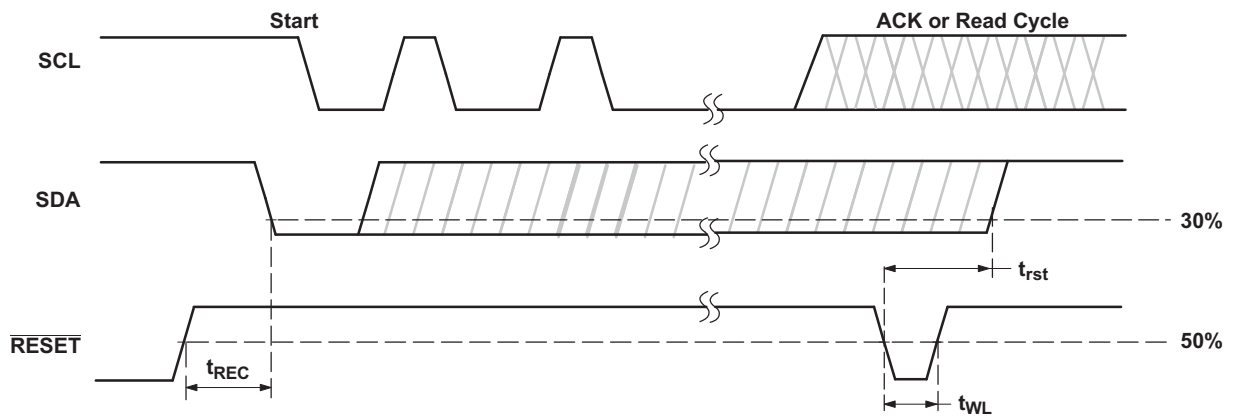


Figure 6. Reset Timing

## 9 Detailed Description

### 9.1 Overview

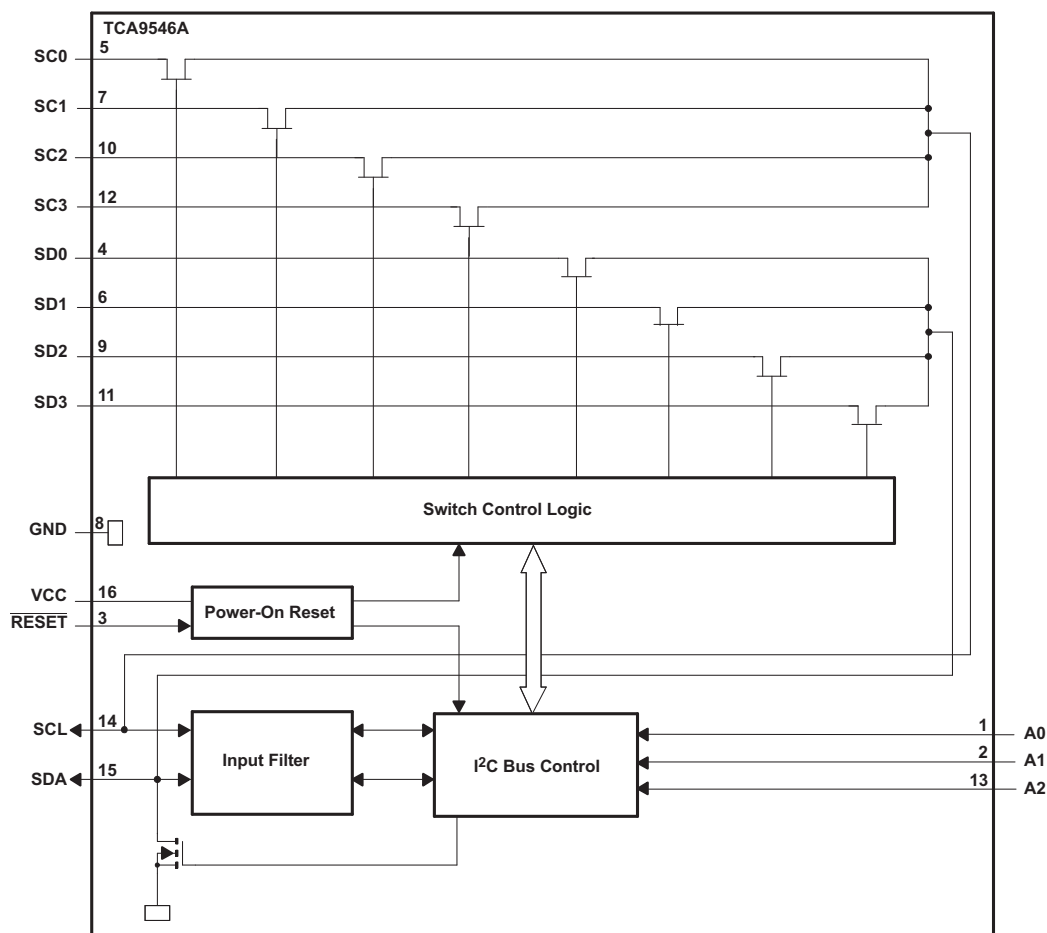
The TCA9546A is a 4-channel, bidirectional translating I<sup>2</sup>C switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the four channels.

The device offers an active-low  $\overline{\text{RESET}}$  input which resets the state machine and allows the TCA9546A to recover should one of the downstream I<sup>2</sup>C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V<sub>CC</sub>, also known as a power-on reset (POR). Both the RESET function and a POR will cause all channels to be deselected.

The connections of the I<sup>2</sup>C data path are controlled by the same I<sup>2</sup>C master device that is switched to communicate with multiple I<sup>2</sup>C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The TCA9546A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

The TCA9546A is a 4-channel, bidirectional translating switch for I<sup>2</sup>C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The TCA9546A features I<sup>2</sup>C control using a single 8-bit control register in which the four least significant bits control the enabling and disabling of the 4 switch channels of I<sup>2</sup>C data flow. Depending on the application, voltage translation of the I<sup>2</sup>C bus can also be achieved using the TCA9546A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I<sup>2</sup>C bus enters a fault state, the TCA9546A can be reset to resume normal operation using the  $\overline{\text{RESET}}$  pin feature or by a power-on reset which results from cycling power to the device.

### 9.4 Device Functional Modes

#### 9.4.1 $\overline{\text{RESET}}$ Input

The  $\overline{\text{RESET}}$  input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of  $t_{\text{WL}}$ , the TCA9546A resets its registers and I<sup>2</sup>C state machine and deselects all channels. The  $\overline{\text{RESET}}$  input must be connected to  $V_{\text{CC}}$  through a pull-up resistor.

#### 9.4.2 Power-On Reset

When power is applied to  $V_{\text{CC}}$ , an internal power-on reset holds the TCA9546A in a reset condition until  $V_{\text{CC}}$  has reached  $V_{\text{POR}}$ . At this point, the reset condition is released, and the TCA9546A registers and I<sup>2</sup>C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter,  $V_{\text{CC}}$  must be lowered below  $V_{\text{POR}}$  to reset the device.

### 9.5 Programming

#### 9.5.1 I<sup>2</sup>C Interface

The I<sup>2</sup>C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 7).

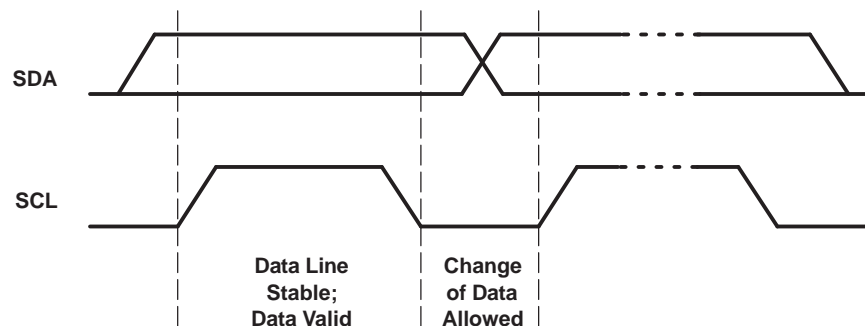
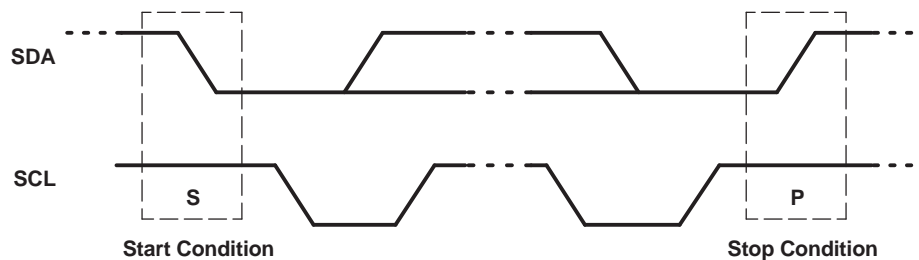


Figure 7. Bit Transfer

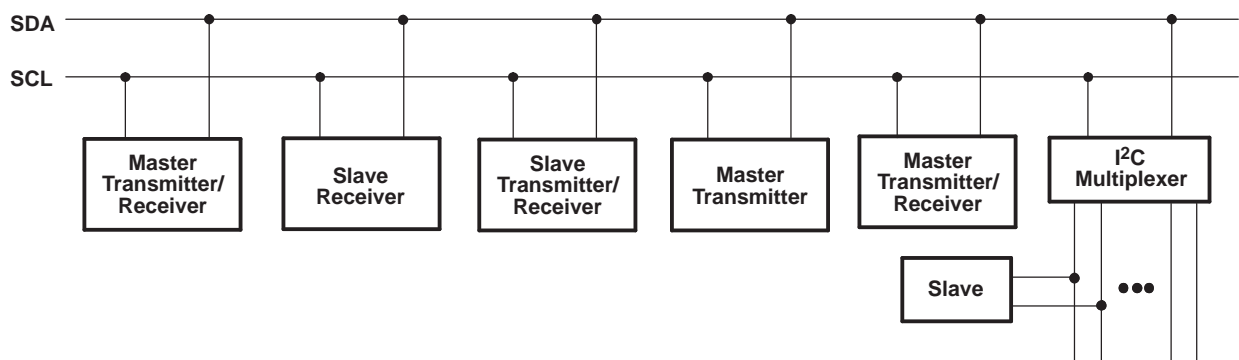
Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 8).

## Programming (continued)



**Figure 8. Definition of Start and Stop Conditions**

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see [Figure 9](#)).



**Figure 9. System Configuration**

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 10](#)). Setup and hold times must be taken into account.

Programming (continued)

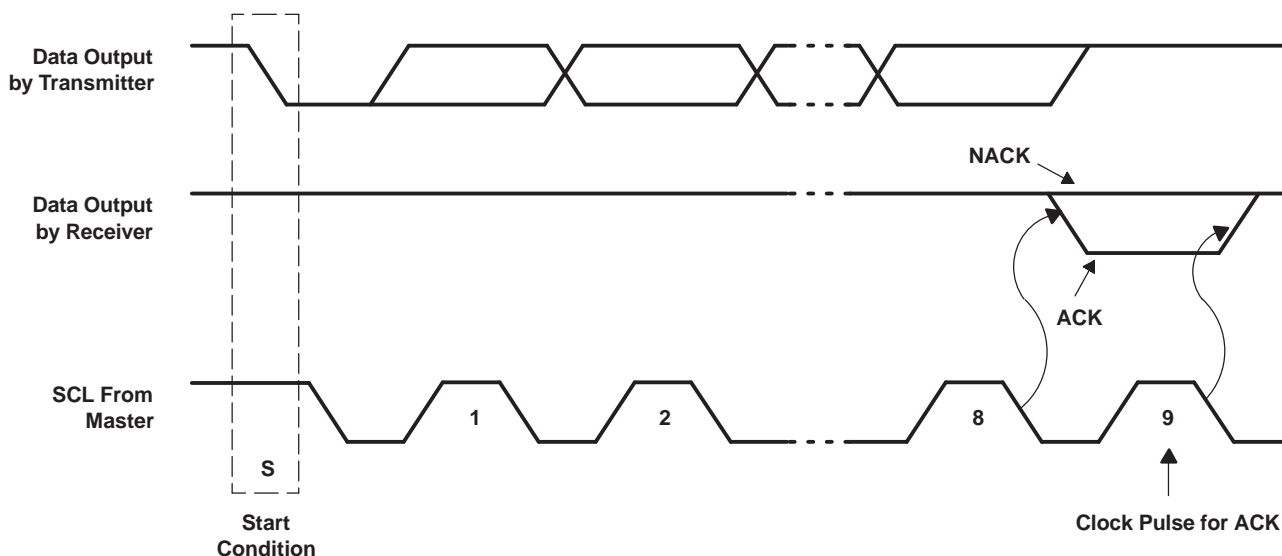


Figure 10. Acknowledgment on the I<sup>2</sup>C Bus

Data is transmitted to the TCA9546A control register using the write mode shown in Figure 11.

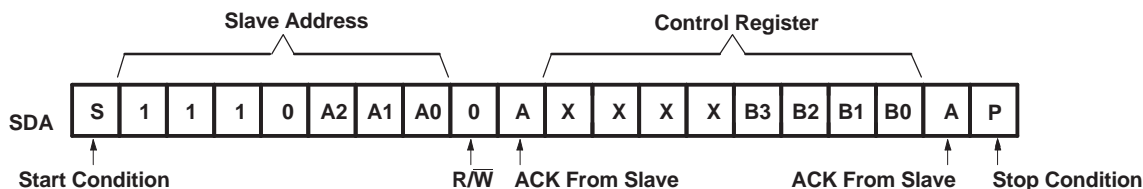


Figure 11. Write Control Register

Data is read from the TCA9546A control register using the read mode shown in Figure 12.

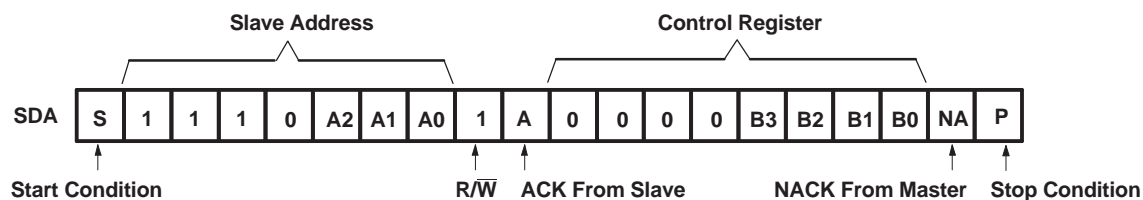


Figure 12. Read Control Register



**Control Register (continued)**
**Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)<sup>(1)</sup>**

B7	B6	B5	B4	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	X	0	Channel 1 disabled
							1	Channel 1 enabled
X	X	X	X	X	X	X	0	Channel 2 disabled
							1	Channel 2 enabled
X	X	X	X	X	X	X	0	Channel 3 disabled
							1	Channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

(1) Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 and 2 are enabled. Care should be taken not to exceed the maximum bus capacity.

## 10 Application and Implementation

### 10.1 Application Information

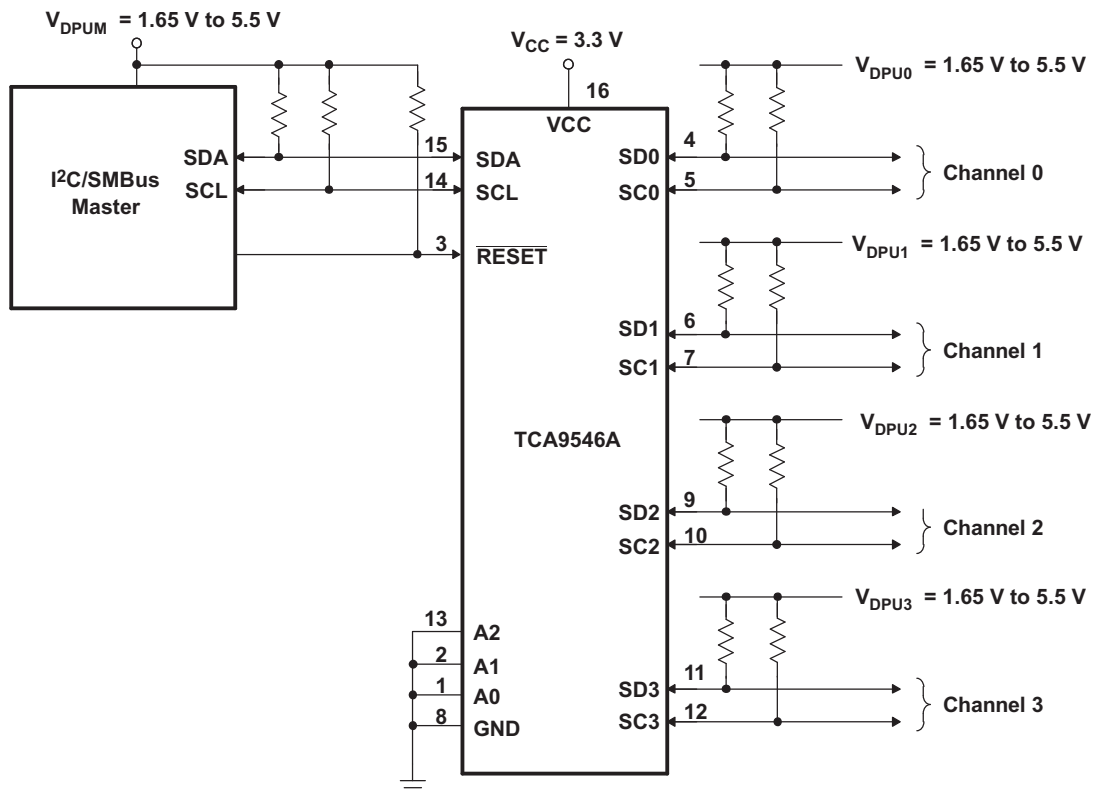
Applications of the TCA9546A will contain an I<sup>2</sup>C (or SMBus) master device and up to four I<sup>2</sup>C slave devices. The downstream channels are ideally used to resolve I<sup>2</sup>C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I<sup>2</sup>C master can move on and read the next channel.

In an application where the I<sup>2</sup>C bus will contain many additional slave devices that do not result in I<sup>2</sup>C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See [Design Requirements](#) and [Detailed Design Procedure](#)).

### 10.2 Typical Application

A typical application of the TCA9546A will contain anywhere from 1 to 5 separate data pull-up voltages,  $V_{DPUX}$ , one for the master device ( $V_{DPUM}$ ) and one for each of the selectable slave channels ( $V_{DPU0} - V_{DPU3}$ ). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage,  $V_{PASS} = V_{DPUX}$ . Once the maximum  $V_{PASS}$  is known,  $V_{CC}$  can be selected easily using [Figure 16](#). In an application where voltage translation is necessary, additional design requirements must be considered (See [Design Requirements](#)).

[Figure 15](#) shows an application in which the TCA9546A can be used.



**Figure 15. TCA9546A Typical Application Schematic**



## Typical Application (continued)

### 10.2.1 Design Requirements

The A0, A1, and A2 pins are hardware selectable to control the slave address of the TCA9546A. These pins may be tied directly to GND or  $V_{CC}$  in the application.

If multiple slave channels will be activated simultaneously in the application, then the total  $I_{OL}$  from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors,  $R_p$ .

The pass-gate transistors of the TCA9546A are constructed such that the  $V_{CC}$  voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C bus to another.

Figure 16 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the [Electrical Characteristics](#) section of this data sheet). In order for the TCA9546A to act as a voltage translator, the  $V_{pass}$  voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V,  $V_{pass}$  must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 16,  $V_{pass(max)}$  is 2.7 V when the TCA9546A supply voltage is 4 V or lower, so the TCA9546A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 15).

### 10.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors,  $R_p$ , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of  $V_{DPUX}$ ,  $V_{OL(max)}$ , and  $I_{OL}$ :

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

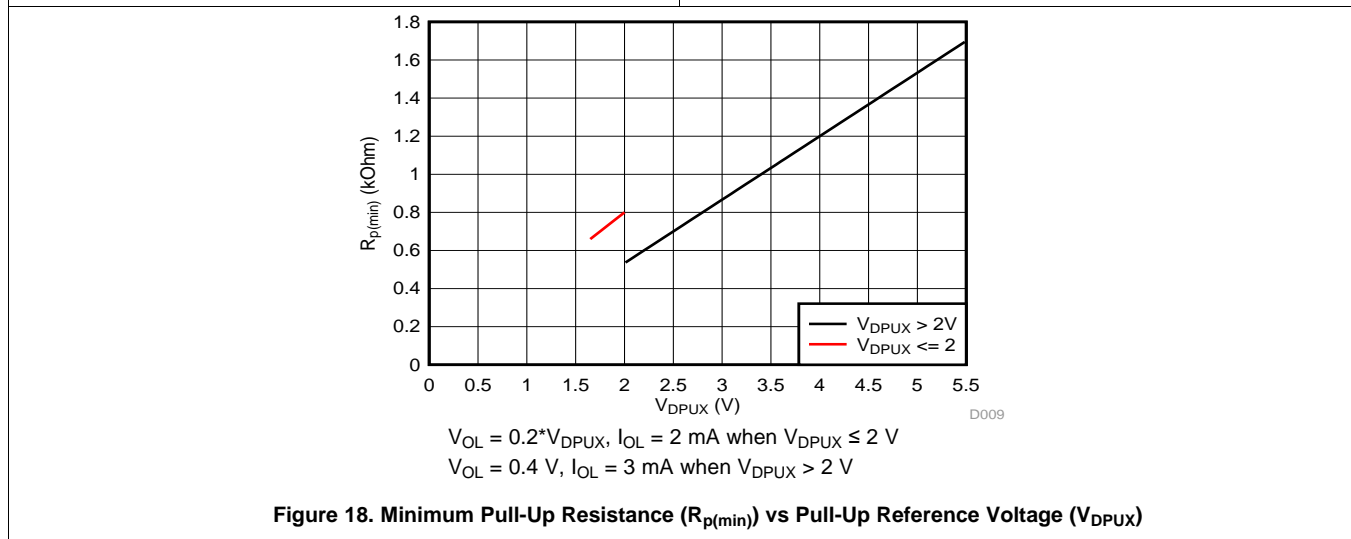
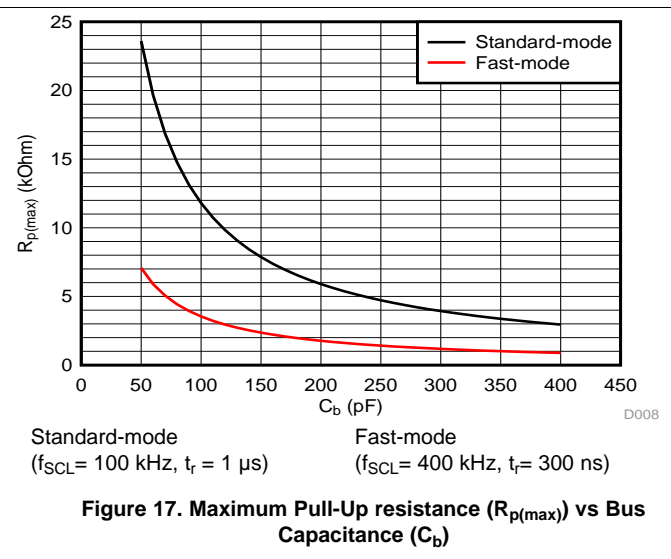
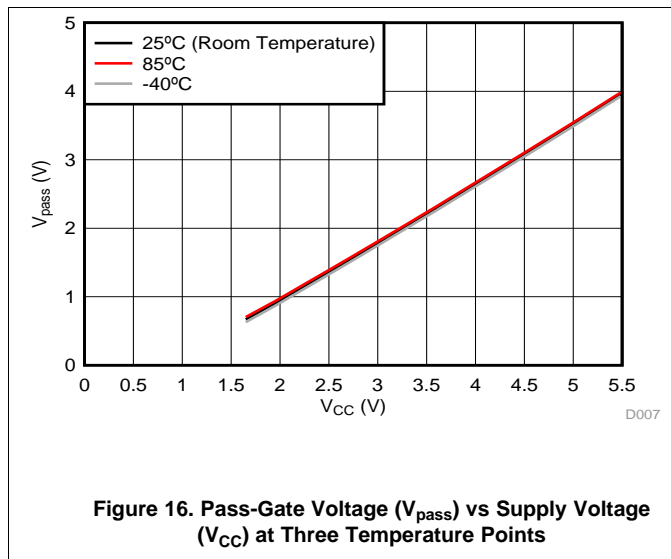
The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$ :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9546A,  $C_{iO(OFF)}$ , the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

Typical Application (continued)

10.2.3 TCA9546A Application Curves



## 11 Power Supply Recommendations

The operating power-supply voltage range of the TCA9546A is 1.65 V to 5.5 V applied at the VCC pin. When the TCA9546A is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I<sup>2</sup>C bus logic is initialized properly.

### 11.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9546A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in Figure 19.

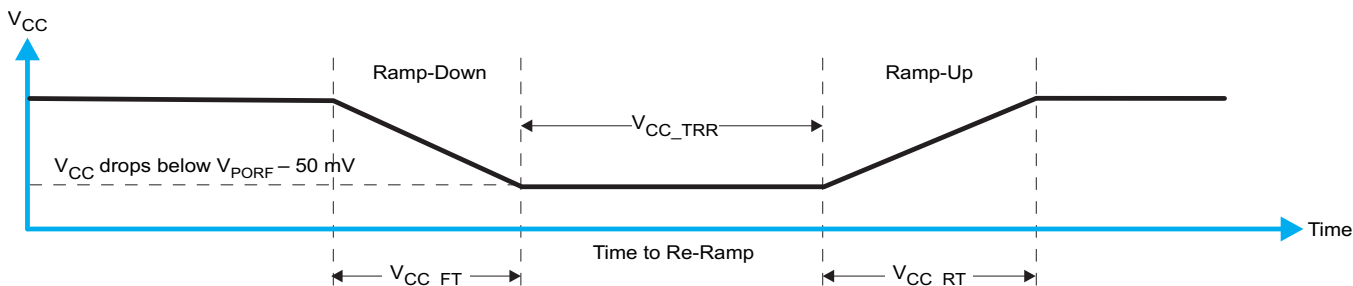


Figure 19. V<sub>CC</sub> is Lowered Below the POR Threshold, Then Ramped Back Up to V<sub>CC</sub>

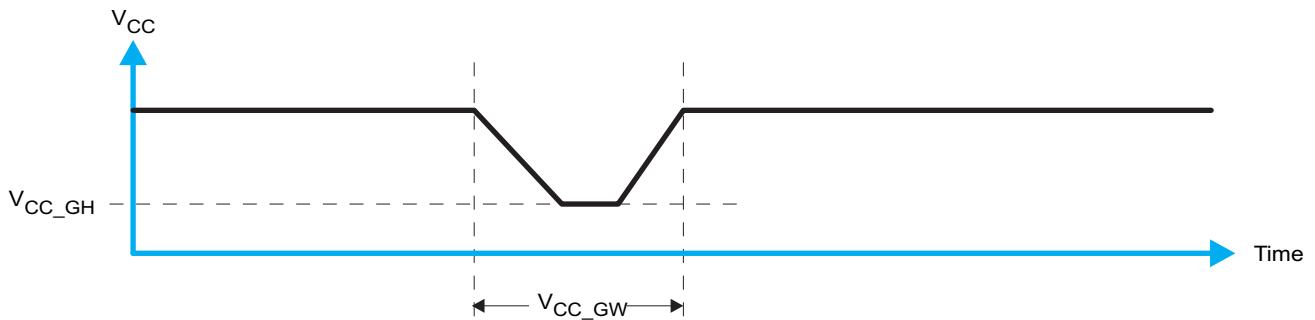
Table 2 specifies the performance of the power-on reset feature for TCA9546A for both types of power-on reset.

Table 2. Recommended Supply Sequencing And Ramp Rates<sup>(1)</sup>

PARAMETER		MIN	TYP	MAX	UNIT
V <sub>CC_FT</sub>	Fall time	See Figure 19	1	100	ms
V <sub>CC_RT</sub>	Rise time	See Figure 19	0.1	100	ms
V <sub>CC_TRR</sub>	Time to re-ramp (when V <sub>CC</sub> drops below V <sub>PORF(min)</sub> – 50 mV or when V <sub>CC</sub> drops to GND)	See Figure 19	40		μs
V <sub>CC_GH</sub>	Level that V <sub>CC</sub> can glitch down to, but not cause a functional disruption when V <sub>CC_GW</sub> = 1 μs	See Figure 20		1.2	V
V <sub>CC_GW</sub>	Glitch width that will not cause a functional disruption when V <sub>CC_GH</sub> = 0.5 × V <sub>CC</sub>	See Figure 20		10	μs
V <sub>PORF</sub>	Voltage trip point of POR on falling V <sub>CC</sub>	See Figure 21	0.8	1.25	V
V <sub>PORR</sub>	Voltage trip point of POR on rising V <sub>CC</sub>	See Figure 21	1.05	1.5	V

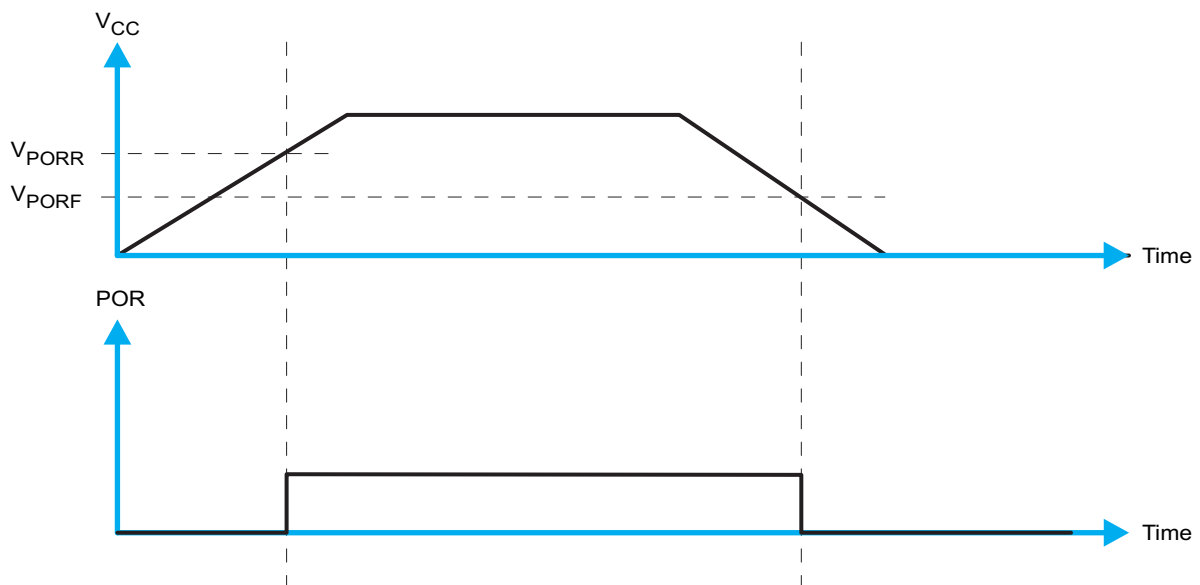
(1) All supply sequencing and ramp rate values are measured at T<sub>A</sub> = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 20 and Table 2 provide more information on how to measure these specifications.



**Figure 20. Glitch Width and Glitch Height**

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. Figure 21 and Table 2 provide more details on this specification.



**Figure 21.  $V_{POR}$**

## 12 Layout

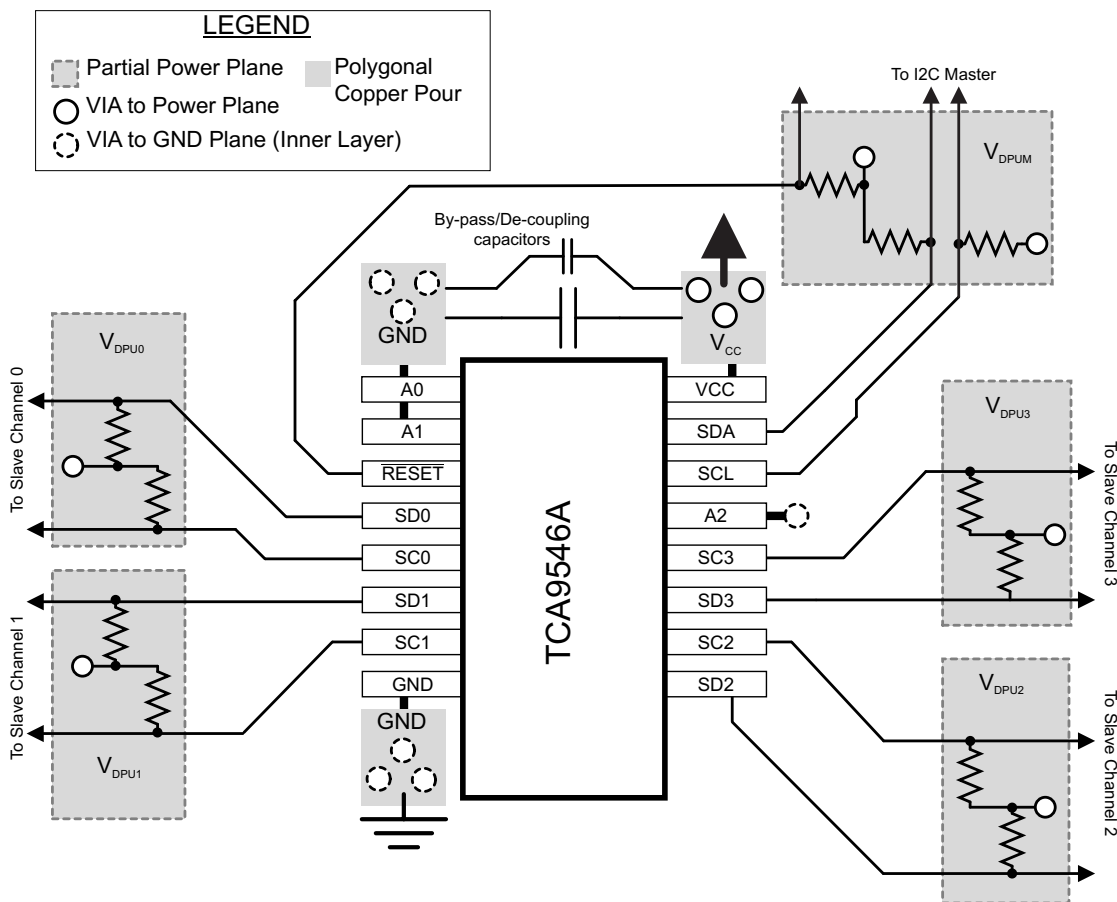
### 12.1 Layout Guidelines

For PCB layout of the TCA9546A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V<sub>DPUX</sub> voltages and V<sub>CC</sub> could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V<sub>DPU0</sub>, V<sub>DPU1</sub>, V<sub>DPU2</sub>, and V<sub>DPU3</sub> may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I<sup>2</sup>C bus capacitance added by PCB parasitics, data lines (SC<sub>n</sub> and SD<sub>n</sub>) should be as short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

### 12.2 Layout Example



## 13 Device and Documentation Support

### 13.1 Trademarks

All trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9546ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TCA9546A	<a href="#">Samples</a>
TCA9546APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW546A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9546ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TCA9546APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9546ADR	SOIC	D	16	2500	367.0	367.0	38.0
TCA9546APWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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