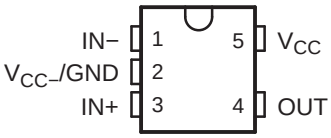
# SINGLE DIFFERENTIAL COMPARATOR

**Check for Samples: TL331-Q1**

## FEATURES

- **Qualified for Automotive Applications**
- **Single Supply or Dual Supplies**
- **Wide Range of Supply Voltage: 2 V to 36 V**
- **Low Supply-Current Drain Independent of Supply Voltage: 0.4 mA Typ.**
- **Low Input Bias Current: 25 nA Typ.**
- **Low Input Offset Voltage: 2 mV Typ.**
- **Common-Mode Input Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ±36 V**
- **Low Output Saturation Voltage**
- **Output Compatible With TTL, MOS, and CMOS**

**DBV PACKAGE**
**(TOP VIEW)**




## DESCRIPTION AND ORDERING INFORMATION

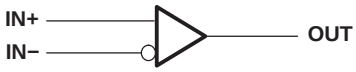
This device consists of a single voltage comparator designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible if the difference between the two supplies is 2 V to 36 V and $V_{CC}$ is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. To achieve wired-AND relationships, one can connect the output to other open-collector outputs.

**ORDERING INFORMATION(1)**

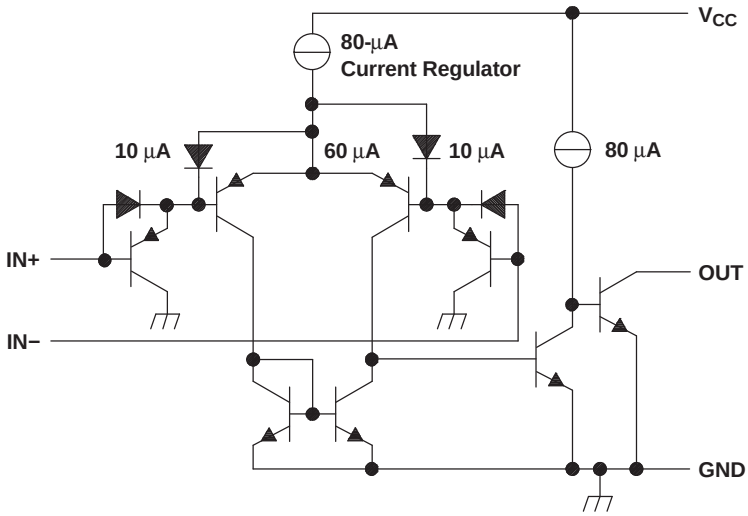
| $T_A$ | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | SOT-23 – DBV | Reel of 3000 | TL331IDBVRQ1 | TQ1U |
| –40°C to 125°C | SOT-23 – DBV | Reel of 3000 | TL331QDBVRQ1 | T1RU |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

### LOGIC DIAGRAM




### SCHEMATIC




| COMPONENT COUNT | |
|---|---|
| Epi-FET | 1 |
| Diodes | 2 |
| Resistors | 1 |
| Transistors | 20 |

Note: Current values shown are nominal.

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | |
|---|---|---|
| $V_{CC}$ | Supply voltage(2) | 36 V |
| $V_{ID}$ | Differential input voltage(3) | ±36 V |
| $V_I$ | Input voltage range (either input) | –0.3 V to 36 V |
| $V_O$ | Output voltage | 36 V |
| $I_O$ | Output current | 20 mA |
| | Duration of output short-circuit to ground(4) | Unlimited |
| $T_J$ | Operating virtual junction temperature | 150°C |
| $T_{stg}$ | Storage temperature range | –65°C to 150°C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to $V_{CC}$ can cause excessive heating and eventual destruction.

## THERMAL INFORMATION

| THERMAL METRIC[1] | | TL331-Q1 DBV 5 PINS | UNIT |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance[2] | 218.3 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance[3] | 87.3 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance[4] | 44.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter[5] | 4.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter[6] | 44.1 | °C/W |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance[7] | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{CC}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS[1] | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IO}$ | Input offset voltage | $V_{CC}$ = 5 V to 30 V, $V_O$ = 1.4 V, $V_{IC} = V_{IC(min)}$ | 25°C | | 2 | 5 | mV |
| | | | –40°C to 125°C | | | 9 | |
| $I_{IO}$ | Input offset current | $V_O$ = 1.4 V | 25°C | | 5 | 50 | nA |
| | | | –40°C to 125°C | | | 250 | |
| $I_{IB}$ | Input bias current | $V_O$ = 1.4 V | 25°C | | –25 | –250 | nA |
| | | | –40°C to 125°C | | | –400 | |
| $V_{ICR}$ | Common-mode input voltage range[2] | | 25°C | 0 to $V_{CC}$ – 1.5 | | | V |
| | | | –40°C to 125°C | 0 to $V_{CC}$ – 2 | | | |
| $A_{VD}$ | Large-signal differential-voltage amplification | $V_{CC}$ = 15 V, $V_O$ = 1.4 V to 11.4 V, $R_L \geq$ 15 kΩ to $V_{CC}$ | 25°C | 50 | 200 | | V/mV |
| $I_{OH}$ | High-level output current | $V_{OH}$ = 5 V, $V_{ID}$ = 1 V | 25°C | | 0.1 | 50 | nA |
| | | $V_{OH}$ = 30 V, $V_{ID}$ = 1 V | –40°C to 125°C | | | 1 | µA |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA, $V_{ID}$ = –1 V | 25°C | | 150 | 400 | mV |
| | | | –40°C to 125°C | | | 700 | |
| $I_{OL}$ | Low-level output current | $V_{OL}$ = 1.5 V, $V_{ID}$ = –1 V | 25°C | 6 | | | mA |
| $I_{CC}$ | Supply current | $R_L$ = ∞, $V_{CC}$ = 5 V | 25°C | | 0.4 | 0.7 | mA |

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+}$ – 1.5 V at 25ºC, but either or both inputs can go to 30 V without damage.

## SWITCHING CHARACTERISTICS

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|
| Response time | $R_L$ connected to 5 V through 5.1 kΩ, $C_L$ = 15 pF[1] [2] | 100-mV input step with 5-mV overdrive | 1.3 | µs |
| | | TTL-level input step | 0.3 | |

(1) $C_L$ includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

## REVISION HISTORY

**Changes from Revision B (September 2012) to Revision C** **Page**

- Added a Thermal Information table ..... 3
- Changed $V_{ICR}$ in the Electrical Characteristics ..... 3
- Changed test conditions of $I_{OL}$ in the Electrical Characteristics ..... 3

**Changes from Revision A (July 2010) to Revision B** **Page**

- Changed $V_{ICR}$ in the Electrical Characteristics ..... 3

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL331IDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TQ1U | Samples |
| TL331QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T1RU | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF TL331-Q1 :**

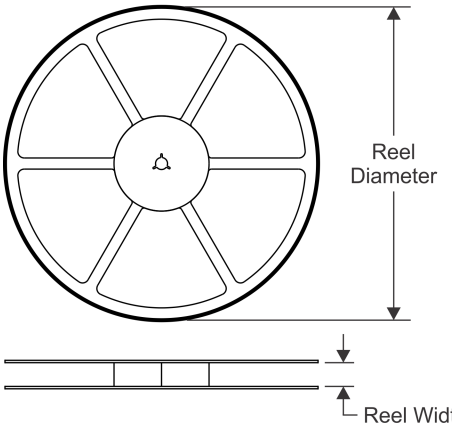
- Catalog: TL331
- Enhanced Product: TL331-EP

NOTE: Qualified Version Definitions:

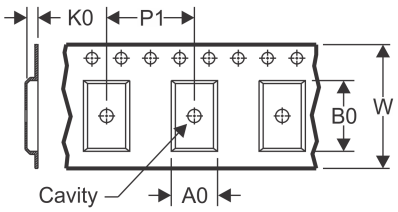
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

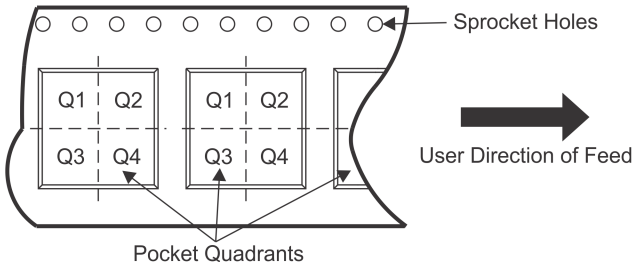



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

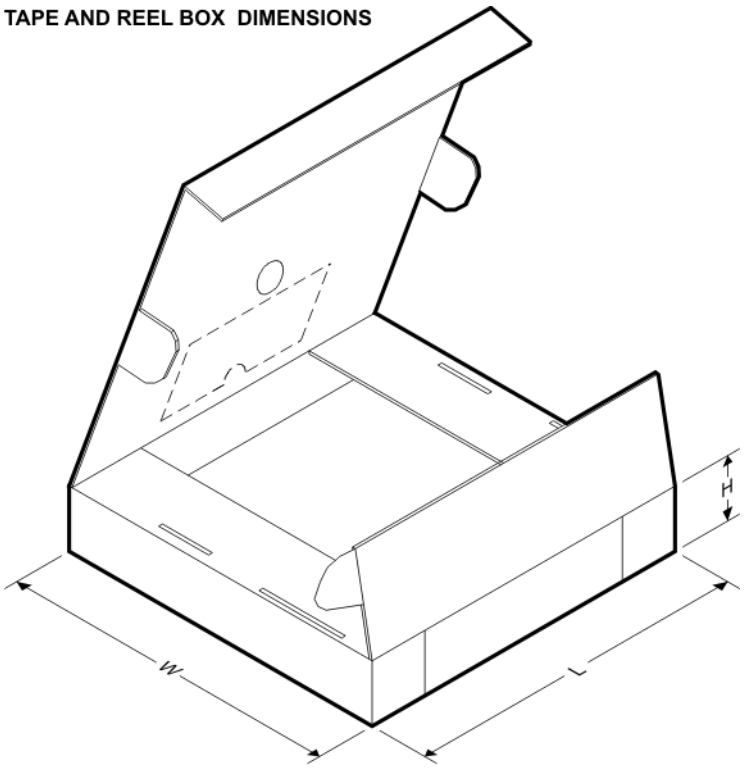
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL331IDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TL331QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

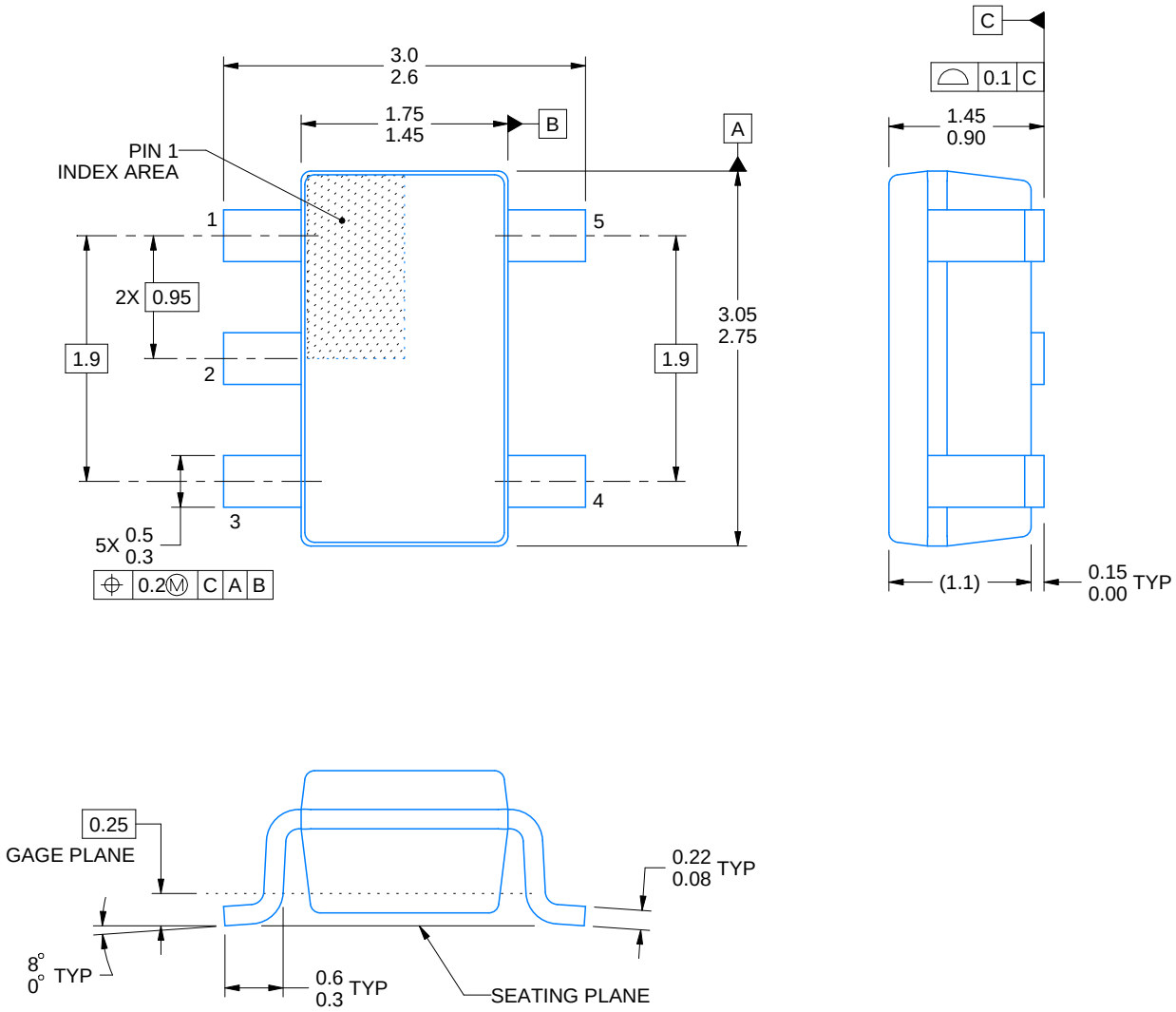
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL331IDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |
| TL331QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 203.0 | 203.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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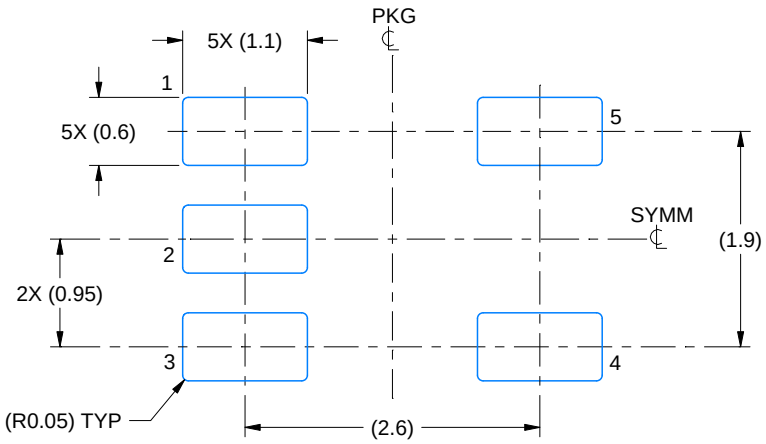
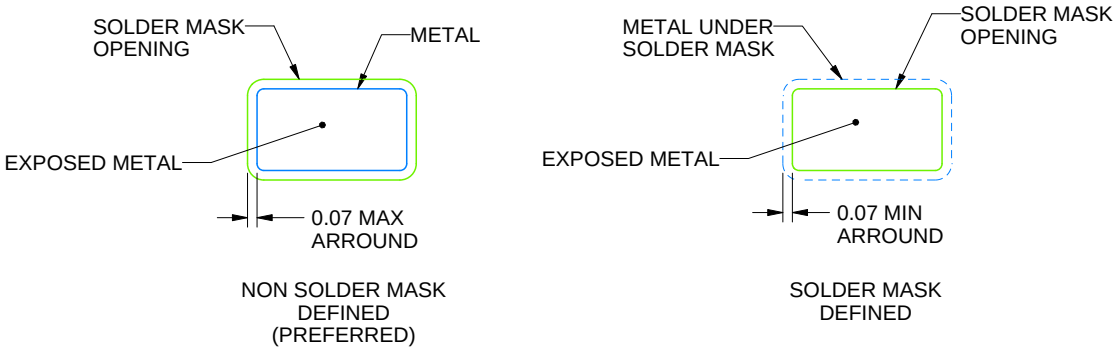
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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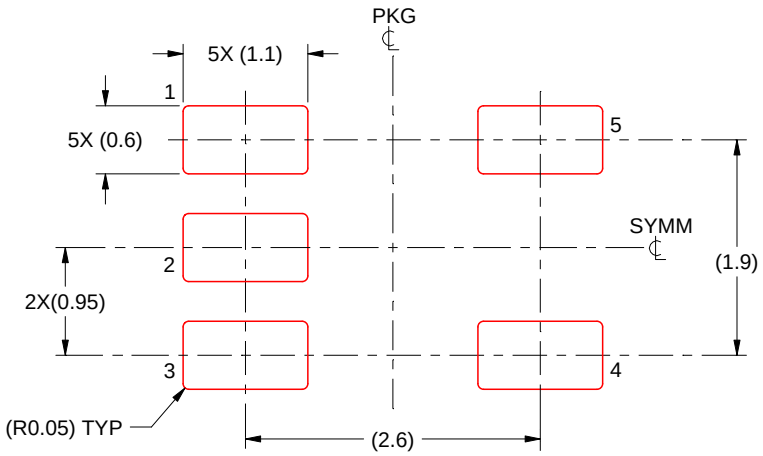
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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