1 Features

- Qualified for Automotive Applications
- Qualified in Accordance With AEC-Q100
- Output Swing Includes Both Supply Rails
- Low Noise: 9 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current: 1 pA Typical
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth: 2.2 MHz Typical
- High Slew Rate: 3.6 V/μs Typical
- Low Input Offset Voltage 2500-μV Max at T_A = 25°C
- Macromodel Included

2 Applications

- Supports Extreme Temperature Applications:
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Extreme (−40°C to 150°C) Temperature Range
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability
- Texas Instruments’ high temperature products use highly-optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures. All devices are characterized and qualified for 1000 hours continuous operating life at maximum rated temperature.

3 Description

The TLC2274 is a quadruple operational amplifier from Texas Instruments. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC2274 offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher speed applications. These device offers comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC2274 has a noise voltage of 9nV/√Hz, two times lower than competitive solutions.

The TLC2274, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, this device works well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this device a great choice when interfacing with analog-to-digital converters (ADCs). This family is fully characterized at 5 V and ±5 V.

It offers increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows the device to be used in a wider range of applications.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC2274-HT</td>
<td>TSSOP (14)</td>
<td>6.60 mm × 5.10 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Maximum Peak-to-Peak Output Voltage vs Supply Voltage

![Graph showing Maximum Peak-to-Peak Output Voltage vs Supply Voltage](image)

(1) Custom temperature ranges available

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An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

<table>
<thead>
<tr>
<th>DATE</th>
<th>REVISION</th>
<th>NOTES</th>
</tr>
</thead>
<tbody>
<tr>
<td>January 2015</td>
<td>*</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
5 Pin Configuration and Functions

Figure 1. Equivalent Schematic (Each Amplifier)

Table 1. Actual Device Component Count

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>TLC2274</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistors</td>
<td>76</td>
</tr>
<tr>
<td>Resistors</td>
<td>52</td>
</tr>
<tr>
<td>Diodes</td>
<td>18</td>
</tr>
<tr>
<td>Capacitors</td>
<td>6</td>
</tr>
</tbody>
</table>

(1) Includes both amplifiers and all ESD, bias, and trim circuitry
6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD+} Supply voltage (2)</td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>V_{DD-} Supply voltage (2)</td>
<td>–8</td>
<td>V</td>
</tr>
<tr>
<td>V_D Differential input voltage (3)</td>
<td>–16</td>
<td>16</td>
</tr>
<tr>
<td>V_{I+} Input voltage (2) Any input</td>
<td>V_{DD-} – 0.3</td>
<td>V_{DD+}</td>
</tr>
<tr>
<td>I_{I+} Input current Any input</td>
<td>–5</td>
<td>5</td>
</tr>
<tr>
<td>I_{O} Output current</td>
<td>–50</td>
<td>50</td>
</tr>
<tr>
<td>Total current into V_{DD+}</td>
<td>–50</td>
<td>50</td>
</tr>
<tr>
<td>Total current out of V_{DD-}</td>
<td>–50</td>
<td>50</td>
</tr>
<tr>
<td>Duration of short-circuit current at (or below) 25°C (4) Unlimited</td>
<td>Unlimited</td>
<td></td>
</tr>
<tr>
<td>T_A Operating free-air temperature</td>
<td>–40</td>
<td>150</td>
</tr>
<tr>
<td>T_{stg} Storage temperature</td>
<td>–65</td>
<td>150</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.

(3) Differential voltages are at I_{IN+} with respect to I_{IN-}. Excessive current will flow if input is brought below V_{DD-} – 0.3 V.

(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{ESD} Electrostastic discharge</td>
<td>±2500 V</td>
</tr>
<tr>
<td>Human-body model (HBM), per AEC Q100-002 (1)</td>
<td></td>
</tr>
<tr>
<td>Charged-device model (CDM), per AEC Q100-011 All pins</td>
<td>±1500 V</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DD+} Supply voltage</td>
<td>±2.2</td>
<td>±8</td>
</tr>
<tr>
<td>V_{I+} Input voltage</td>
<td>V_{DD-} – V_{DD+} – 1.5</td>
<td>V</td>
</tr>
<tr>
<td>V_{IC} Common-mode input voltage</td>
<td>V_{DD-} – V_{DD+} – 1.5</td>
<td>V</td>
</tr>
<tr>
<td>T_A Operating free-air temperature</td>
<td>–40</td>
<td>150</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC (1)</th>
<th>TLC2274</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{OJA} Junction-to-ambient thermal resistance</td>
<td>106.0</td>
<td>°C/W</td>
</tr>
<tr>
<td>R_{JJA,JC,top} Junction-to-case (top) thermal resistance</td>
<td>35.5</td>
<td></td>
</tr>
<tr>
<td>R_{JJB} Junction-to-board thermal resistance</td>
<td>47.6</td>
<td></td>
</tr>
<tr>
<td>\psi_{JT} Junction-to-top characterization parameter</td>
<td>2.4</td>
<td></td>
</tr>
<tr>
<td>\psi_{JB} Junction-to-board characterization parameter</td>
<td>47.1</td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics, $V_{DD} = 5$ V

at specified free-air temperature, $V_{DD} = 5$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$T_A$&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IO}$ Input offset voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>μV</td>
</tr>
<tr>
<td>$aV_{IO}$ Temperature coefficient of</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>μV/°C</td>
</tr>
<tr>
<td>input offset voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>μV/°C</td>
</tr>
<tr>
<td>Input offset voltage long-term drift&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>$V_{IC} = 0$ V, $V_{O} = 0$ V, $V_{DD} = 12.5$ V, $R_S = 50$ Ω</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>μV/°C</td>
</tr>
<tr>
<td>$I_{IO}$ Input offset current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>$I_{IB}$ Input bias current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>$V_{ICR}$ Common-mode input voltage</td>
<td>$R_S = 50$ Ω, $</td>
<td>V_{IC}</td>
<td>\leq 5$ mV</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{DH}$ High-level output voltage</td>
<td>$I_{DH} = -20$ μA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DH} = -200$ μA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DH} = -1$ mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$V_{IC} = 2.5$ V, $I_{OL} = 50$ μA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$V_{IC} = 2.5$ V, $I_{OL} = 500$ μA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$ Low-level output voltage</td>
<td>$V_{IC} = 2.5$ V, $I_{OL} = 5$ mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$A_{VD}$ Large-signal differential</td>
<td>$V_{IC} = 2.5$ V, $V_{O} = 1$ V to 4 V, $R_L = 10$ kΩ&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td>$A_{VD}$ Large-signal differential</td>
<td>$V_{IC} = 2.5$ V, $V_{O} = 1$ V to 4 V, $R_L = 1$ MΩ&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td>$r_{id}$ Differential input resistance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$r_i$ Common-mode input resistance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$c_i$ Common-mode input capacitance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$z_o$ Closed-loop output impedance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>CMRR Common-mode rejection ratio</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$k_{SVR}$ Supply voltage rejection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$k_{SVR}$ Supply voltage rejection</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$I_{DD}$ Supply current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Full range is −40°C to 150°C for this part.

<sup>(2)</sup> Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

<sup>(3)</sup> Referenced to 2.5 V
6.6 Operating Characteristics, \( V_{\text{DD}} = 5 \text{ V} \)

at specified free-air temperature, \( V_{\text{DD}} = 5 \text{ V} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A^{(1)} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR Slew rate at unity gain</td>
<td>( V_O = 0.5 \text{ V to } 2.5 \text{ V}, ) ( R_L = 10 \text{ k}\Omega^{(2)} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>\text{V/\mu s}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25°C</td>
<td>2.3</td>
<td>3.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Full range</td>
<td>1.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{in}} )</td>
<td>Equivalent input noise voltage</td>
<td>f = 10 Hz</td>
<td>25°C</td>
<td>50</td>
<td></td>
<td>\text{nV/\sqrt{Hz}}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>f = 1 kHz</td>
<td>25°C</td>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{Nppl}} )</td>
<td>Peak-to-peak equivalent input noise voltage</td>
<td>f = 0.1 to 1 Hz</td>
<td>25°C</td>
<td>1</td>
<td></td>
<td>\text{\mu V}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>f = 0.1 to 10 Hz</td>
<td>25°C</td>
<td>1.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{\text{in}} )</td>
<td>Equivalent input noise current</td>
<td></td>
<td>25°C</td>
<td>0.6</td>
<td></td>
<td>\text{fA/\sqrt{Hz}}</td>
</tr>
<tr>
<td>THD + N</td>
<td>Total harmonic distortion plus noise</td>
<td>( V_O = 0.5 \text{ V to } 2.5 \text{ V}, ) ( R_L = 10 \text{ k}\Omega^{(2)} ) f = 20 kHz</td>
<td>25°C</td>
<td>0.004%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Gain-bandwidth product</td>
<td>f = 10 kHz, ( R_L = 10 \text{ k}\Omega^{(2)} )</td>
<td>25°C</td>
<td>0.03%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( B_{\text{DM}} )</td>
<td>Maximum output-swing bandwidth</td>
<td>( V_{\text{Oppp}} = 2 \text{V}, ) ( R_L = 10 \text{ k}\Omega^{(2)} )</td>
<td>25°C</td>
<td>2.18 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_s )</td>
<td>Settling time</td>
<td>( A_v = 1, ) ( C_L = 100 \text{ pF}^{(2)} )</td>
<td>To 0.1%</td>
<td>1.5</td>
<td></td>
<td>\text{\mu s}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( A_v = 10, ) ( C_L = 100 \text{ pF}^{(2)} )</td>
<td>To 0.01%</td>
<td>2.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \phi_m )</td>
<td>Phase margin at unity gain</td>
<td>( R_L = 10 \text{ k}\Omega, ) ( C_L = 100 \text{ pF}^{(2)} )</td>
<td>25°C</td>
<td>50°</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \text{Gain margin} )</td>
<td></td>
<td>( R_L = 10 \text{ k}\Omega, ) ( C_L = 100 \text{ pF}^{(2)} )</td>
<td>25°C</td>
<td>10</td>
<td></td>
<td>\text{dB}</td>
</tr>
</tbody>
</table>

(1) Full range is -40°C to 150°C for this part.
(2) Referenced to 2.5 V
## 6.7 Electrical Characteristics, $V_{DD\pm} = \pm 5$ V

at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>$T_A$ (1)</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IO}$</td>
<td>Input offset voltage</td>
<td>$V_{IC} = 0$ V, $R_S = 50$ Ω</td>
<td>$V_O = 0$ V</td>
<td>25°C</td>
<td>300</td>
<td>2500</td>
</tr>
<tr>
<td>$\alpha_{VIO}$</td>
<td>Temperature coefficient of input offset voltage</td>
<td>$V_{IC} = 0$ V, $R_S = 50$ Ω</td>
<td>$V_O = 0$ V</td>
<td>25°C to 125°C</td>
<td>2</td>
<td>μV/°C</td>
</tr>
<tr>
<td></td>
<td>Input offset voltage long-term drift (2)</td>
<td>$V_{IC} = 0$ V, $R_S = 50$ Ω</td>
<td>$V_O = 0$ V</td>
<td>25°C</td>
<td>0.002</td>
<td>μV/μmo</td>
</tr>
<tr>
<td>$I_{IO}$</td>
<td>Input offset current</td>
<td>$V_{IC} = 0$ V, $R_S = 50$ Ω</td>
<td>$V_O = 0$ V</td>
<td>25°C</td>
<td>0.5</td>
<td>60</td>
</tr>
<tr>
<td>$I_{IB}$</td>
<td>Input bias current</td>
<td>$V_{IC} = 0$ V, $R_S = 50$ Ω</td>
<td>$V_O = 0$ V</td>
<td>25°C</td>
<td>1</td>
<td>60</td>
</tr>
<tr>
<td>$V_{ICR}$</td>
<td>Common-mode input voltage range</td>
<td>$R_S = 50$ Ω</td>
<td>$</td>
<td>V_{IO}</td>
<td>\leq 5$ mV</td>
<td>25°C</td>
</tr>
<tr>
<td></td>
<td>Maximum positive peak output voltage</td>
<td>$V_{IC} = 0$ V, $</td>
<td>V_O</td>
<td>\leq 5$ mV</td>
<td>$R_S = 50$ Ω</td>
<td>25°C</td>
</tr>
<tr>
<td>$V_{OM+}$</td>
<td>Maximum negative peak output voltage</td>
<td>$V_{IC} = 0$ V, $</td>
<td>V_O</td>
<td>\leq 5$ mV</td>
<td>$R_S = 50$ Ω</td>
<td>25°C</td>
</tr>
<tr>
<td>$A_{VD}$</td>
<td>Large-signal differential voltage amplification</td>
<td>$V_{IC} = \pm 4$ V, $R_L = 10$ kΩ</td>
<td>$R_L = 1$ MΩ</td>
<td>25°C</td>
<td>20</td>
<td>50</td>
</tr>
<tr>
<td>$r_{ds}$</td>
<td>Differential input resistance</td>
<td>25°C</td>
<td>$10^{12}$</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$r_i$</td>
<td>Common-mode input resistance</td>
<td>25°C</td>
<td>$10^{12}$</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$c_i$</td>
<td>Common-mode input capacitance</td>
<td>$f = 10$ kHz, N package</td>
<td>25°C</td>
<td>8</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>$z_o$</td>
<td>Closed-loop output impedance</td>
<td>$f = 1$ MHz, $AV = 10$</td>
<td>25°C</td>
<td>130</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection ratio</td>
<td>$V_{IC} = -5$ V to 2.7 V, $R_S = 50$ Ω</td>
<td>$V_O = 0$ V</td>
<td>25°C</td>
<td>75</td>
<td>80</td>
</tr>
<tr>
<td>$k_{SVR}$</td>
<td>Supply voltage rejection ratio ($\Delta V_{OC}/\Delta V_{IO}$)</td>
<td>$V_{IC} = \pm 2.2$ V to ±8 V, $V_O = 0$ V, No load</td>
<td>25°C</td>
<td>80</td>
<td>95</td>
<td>dB</td>
</tr>
<tr>
<td>$I_{IO}$</td>
<td>Supply current</td>
<td>$V_{IC} = 0$ V, No load</td>
<td>Full range</td>
<td>4.4</td>
<td>6</td>
<td>mA</td>
</tr>
</tbody>
</table>

(1) Full range is -40°C to 150°C for this part.

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
6.8 Operating Characteristics, \( V_{\text{DD}} = \pm 5 \text{ V} \)

at specified free-air temperature, \( V_{\text{DD}} = \pm 5 \text{ V} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>( T_A )(^{(1)} )</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SR</td>
<td>( V_O = \pm 2.3 \text{ V}, ) ( R_L = 10 \text{ k}\Omega ) ( C_L = 100 \text{ pF} )</td>
<td>25°C</td>
<td>2.3</td>
<td>3.6</td>
<td>V/\mu s</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Full range</td>
<td></td>
<td>1.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_I )</td>
<td>( f = 10 \text{ Hz} )</td>
<td>25°C</td>
<td>50</td>
<td></td>
<td></td>
<td>nV/\sqrt{Hz}</td>
</tr>
<tr>
<td></td>
<td>( f = 1 \text{ kHz} )</td>
<td>25°C</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{NPP}} )</td>
<td>( f = 0.1 \text{ to } 1 \text{ Hz} )</td>
<td>25°C</td>
<td>1</td>
<td></td>
<td></td>
<td>\mu V</td>
</tr>
<tr>
<td></td>
<td>( f = 0.1 \text{ to } 10 \text{ Hz} )</td>
<td>25°C</td>
<td>1.4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_n )</td>
<td>Equivalent input noise current</td>
<td>25°C</td>
<td>0.6</td>
<td></td>
<td></td>
<td>fA/\sqrt{Hz}</td>
</tr>
<tr>
<td>THD + N</td>
<td>( V_O = \pm 2.3 \text{ V}, ) ( f = 20 \text{ kHz}, ) ( R_L = 10 \text{ k}\Omega )</td>
<td>25°C</td>
<td>0.0011%</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( A_v = 1 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( A_v = 10 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( A_v = 100 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain-bandwidth product</td>
<td>( f = 10 \text{ kHz}, ) ( C_L = 100 \text{ pF} ) ( R_L = 10 \text{ k}\Omega )</td>
<td>25°C</td>
<td>2.25</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( B_{OM} )</td>
<td>Maximum output-swing bandwidth</td>
<td>25°C</td>
<td>0.54</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>( V_{O\text{PP}} = 4.6 \text{ V}, ) ( R_L = 10 \text{ k}\Omega ) ( A_v = 1, ) ( C_L = 100 \text{ pF} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \tau_s )</td>
<td>Settling time</td>
<td>( A_v = -1, ) ( \text{Step} = -2.3 \text{ V} \text{ to } 2.3 \text{ V}, ) ( R_L = 10 \text{ k}\Omega ) ( C_L = 100 \text{ pF} ) To 0.1%</td>
<td>25°C</td>
<td>1.5</td>
<td></td>
<td>\mu s</td>
</tr>
<tr>
<td></td>
<td>To 0.01%</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \phi_{\text{m}} )</td>
<td>Phase margin at unity gain</td>
<td>25°C</td>
<td>52°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain margin</td>
<td>( R_L = 10 \text{ k}\Omega , ) ( C_L = 100 \text{ pF} )</td>
<td>25°C</td>
<td>10</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

(1) Full range is −40°C to 150°C for this part.

A. See data sheet for Absolute Maximum Ratings and minimum Recommended Operating Conditions.
B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 2. TLC2274EPWRQ1 Operating Life Derating Chart
Figure 3. Estimated Wire Bond Life
6.9 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

---

![Figure 4. Distribution of TLC2274 Input Offset Voltage](image1)

![Figure 5. Input Offset Voltage vs Common-Mode Voltage](image2)

![Figure 6. Input Offset Voltage vs Common-Mode Voltage](image3)

![Figure 7. Input Voltage vs Supply Voltage](image4)

![Figure 8. Input Voltage vs Free-Air Temperature](image5)

![Figure 9. High-Level Output Voltage vs High-Level Output Current](image6)

---

Submit Documentation Feedback

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Product Folder Links: TLC2274-HT
Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

- **Figure 10. Low-Level Output Voltage vs Low-Level Output Current**
- **Figure 11. Low-Level Output Voltage vs Low-Level Output Current**
- **Figure 12. Maximum Positive Peak Output Voltage vs Output Current**
- **Figure 13. Maximum Negative Peak Output Voltage vs Output Current**
- **Figure 14. Maximum Peak-to-Peak Output Voltage vs Frequency**
- **Figure 15. Short-Circuit Output Current vs Supply Voltage**
Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

Figure 16. Output Voltage vs Differential Input Voltage

Figure 17. Output Voltage vs Differential Input Voltage

Figure 18. Large-Signal Differential Voltage Amplification vs Load Resistance

Figure 19. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

Figure 20. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

Figure 21. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

![Diagram](image-url)

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Typical Characteristics (continued)

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![Diagram](image-url)

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Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

![Diagram](image-url)

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Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

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**Figure 21. Large-Signal Differential Voltage Amplification vs Free-Air Temperature**

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

![Diagram](image-url)

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**Figure 20. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency**

**Figure 21. Large-Signal Differential Voltage Amplification vs Free-Air Temperature**

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.
Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

![Figure 22. Large-Signal Differential Voltage Amplification vs Free-Air Temperature](image1)

![Figure 23. Output Impedance vs Frequency](image2)

![Figure 24. Output Impedance vs Frequency](image3)

![Figure 25. Common-Mode Rejection Ratio vs Frequency](image4)

![Figure 26. Common-Mode Rejection Ratio vs Free-Air Temperature](image5)

![Figure 27. Supply-Voltage Rejection Ratio vs Frequency](image6)
Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

Figure 28. Supply-Voltage Rejection Ratio vs Frequency

Figure 29. Supply-Voltage Rejection Ratio vs Free-Air Temperature

Figure 30. Slew Rate vs Load Capacitance

Figure 31. Slew Rate vs Free-Air Temperature

Figure 32. Inverting Large-Signal Pulse Response

Figure 33. Inverting Large-Signal Pulse Response
Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

---

**Figure 34. Voltage-Follower Large-Signal Pulse Response**

**Figure 35. Voltage-Follower Large-Signal Pulse Response**

**Figure 36. Inverting Small-Signal Pulse Response**

**Figure 37. Inverting Small-Signal Pulse Response**

**Figure 38. Voltage-Follower Small-Signal Pulse Response**

**Figure 39. Voltage-Follower Small-Signal Pulse Response**
Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

Figure 40. Equivalent Input Noise Voltage vs Frequency

Figure 41. Equivalent Input Noise Voltage vs Frequency

Figure 42. Noise Voltage Over a 10-s Period

Figure 43. Integrated Noise Voltage vs Frequency

Figure 44. Total Harmonic Distortion Plus Noise vs Frequency

Figure 45. Gain-Bandwidth Product vs Supply Voltage
7 Detailed Description

7.1 Overview
The TLC2274 device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. These devices offer comparable ac performance while having better noise, input offset voltage and power dissipation than existing CMOS operational amplifiers. The TLC2274 device, exhibiting high input impedance and low noise, is excellent for small signal conditioning for high-impedance sources, such as piezoelectric transducers. It offers increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows the device to be used in a wider range of applications.

7.2 Functional Block Diagram

7.3 Feature Description
These devices use the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages, very high input impedances, and extremely low input offset and bias currents. In addition, the rail-to-rail output feature with single- or split-supplies, makes this device a great choice when interfacing with analog-to-digital converters (ADCs).
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Macromodel Information

Macromodel information provided was derived using Microsim Parts, the model generation software used with Microsim PSpice. The Boyle macromodel (1) and subcircuit in Figure 46 are generated using the TLC227x typical electrical and operating characteristics at $T_A = 25^\circ C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

---

8.2 Typical Application

The TLC2274 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 48 and Figure 49 show its ability to drive loads up to 1000 pF while maintaining good gain and phase margins (Rnull = 0).

**Figure 46. Boyle Macromodels and Subcircuit**

**Figure 47. Typical Application Schematic**
Typical Application (continued)

8.2.1 Design Requirements

As per Equation 1:

Table 2. Design Parameters

<table>
<thead>
<tr>
<th>Improvement in Phase Margin</th>
<th>UGBW (kHz)</th>
<th>R null (Ω)</th>
<th>CL (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1000</td>
<td>0</td>
<td>1000</td>
</tr>
<tr>
<td>7.15</td>
<td>1000</td>
<td>20</td>
<td>1000</td>
</tr>
<tr>
<td>17.43</td>
<td>1000</td>
<td>50</td>
<td>1000</td>
</tr>
<tr>
<td>32.12</td>
<td>1000</td>
<td>100</td>
<td>1000</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

A smaller series resistor ($R_{null}$) at the output of the device (see Figure 47) improves the gain and phase margins when driving large capacitive loads. Figure 48 and Figure 49 show the effects of adding series resistances of 10 Ω, 50 Ω, 100 Ω, 200 Ω, and 500 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, Equation 1 can be used.

$$\Delta \phi_{m1} = \tan^{-1} \left(2 \times \pi \times UGBW \times R_{null} \times C_L \right)$$

where
- $\Delta \phi_{m1}$ = Improvement in phase margin
- $UGBW$ = Unity-gain bandwidth frequency
- $R_{null}$ = Output series resistance
- $C_L$ = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 47). To use equation 1, UGBW must be approximated from Figure 47. Using Equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 51. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin. Using Figure 47, with Equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

8.2.3 Application Curves

$T_A = 25^\circ C$
$T_A = 25^\circ C$

Figure 50. Unity-Gain Bandwidth vs Load Capacitance

Figure 51. Overestimation of Phase Margin vs Load Capacitance
9 Power Supply Recommendations

TLC2274 operates from ±2.2- to ±8-V. In addition, key parameters are assured over the specified temperature range, –55°C to 125°C. Parameters which vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

10 Layout

10.1 Layout Guidelines

The TLC2274 has very-low offset voltage and drift. To achieve highest performance, optimize circuit layout and mechanical conditions. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the TLC2274. Cancel these thermal potentials by assure that they are equal in both input terminals.

- Keep the thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as cooling fans.

10.2 Layout Example

Figure 52. Board Layout Example
11 Device and Documentation Support

11.1 Trademarks
LinCMOS is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC2274EPWRQ1</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 150</td>
<td>2274EQ1</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC2274-HT:

- Catalog: TLC2274
- Automotive: TLC2274-Q1
- Enhanced Product: TLC2274-EP
- Military: TLC2274M

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.
E. Falls within JEDEC MO-153
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