Voltage-Controlled Oscillator (VCO) Section:
- Ring Oscillator Using Only One External Bias Resistor (R_{BIAS})
- Lock Frequency:
  - 43 MHz to 100 MHz (V_{DD} = 5 V \pm 5\%, T_A = -20^\circ C to 75^\circ C, \times 1 Output)
  - 37 MHz to 55 MHz (V_{DD} = 3 V \pm 5\%, T_A = -20^\circ C to 75^\circ C)

Phase-Frequency Detector (PFD) Section
- Includes a High-Speed Edge-Triggered Detector With Internal Charge Pump
- Independent VCO, PFD Power-Down Mode
- Thin Small-Outline Package (14 terminal)
- CMOS Technology
- Typical Applications:
  - Frequency Synthesis
  - Modulation/Demodulation
  - Fractional Frequency Division
- CMOS Input Logic Level

description
The TLC2933 is designed for phase-locked-loop (PLL) systems and is composed of a voltage-controlled oscillator (VCO) and an edge-triggered-type phase frequency detector (PFD). The oscillation frequency range of the VCO is set by an external bias resistor (R_{BIAS}). The high-speed PFD with internal charge pump detects the phase difference between the reference frequency input and signal frequency input from the external counter. Both the VCO and the PFD have inhibit functions that can be used as a power-down mode. With the high-speed and stable VCO characteristics, the TLC2933 is well suited for use in high-performance PLL systems.

functional block diagram

available options

<table>
<thead>
<tr>
<th>T_A</th>
<th>PACKAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>-20^\circ C to 75^\circ C</td>
<td>SMALL OUTLINE (PW)</td>
</tr>
</tbody>
</table>

† The PW package is available taped and reeled. Add an R suffix to device type (e.g., TLC2993IPWR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIAS</td>
<td>13</td>
<td>I</td>
<td>Bias supply. An external resistor (R_{BIAS}) between VCO V_{DD} and BIAS supplies bias for adjusting the oscillation frequency range.</td>
</tr>
<tr>
<td>FIN−A</td>
<td>4</td>
<td>I</td>
<td>Input reference frequency f_{(REF IN)} is applied to FIN−A.</td>
</tr>
<tr>
<td>FIN−B</td>
<td>5</td>
<td>I</td>
<td>Input for VCO external counter output frequency f_{(FIN−B)}. FIN−B is nominally provided from the external counter.</td>
</tr>
<tr>
<td>LOGIC GND</td>
<td>7</td>
<td></td>
<td>Ground for the internal logic.</td>
</tr>
<tr>
<td>LOGIC V_{DD}</td>
<td>1</td>
<td></td>
<td>Power supply for the internal logic. This power supply should be separate from VCO V_{DD} to reduce cross-coupling between supplies.</td>
</tr>
<tr>
<td>NC</td>
<td>8</td>
<td></td>
<td>No internal connection.</td>
</tr>
<tr>
<td>PFD INHIBIT</td>
<td>9</td>
<td>I</td>
<td>PFD inhibit control. When PFD INHIBIT is high, PFD OUT is in the high-impedance state, see Table 2.</td>
</tr>
<tr>
<td>PFD OUT</td>
<td>6</td>
<td>O</td>
<td>PFD output. When the PFD INHIBIT is high, PFD OUT is in the high-impedance state.</td>
</tr>
<tr>
<td>TEST</td>
<td>2</td>
<td>I</td>
<td>Test terminal. TEST connects to ground for normal operation.</td>
</tr>
<tr>
<td>VCO GND</td>
<td>11</td>
<td></td>
<td>Ground for VCO.</td>
</tr>
<tr>
<td>VCO IN</td>
<td>12</td>
<td>I</td>
<td>VCO control voltage input. Nominally the external loop filter output connects to VCO IN to control VCO oscillation frequency.</td>
</tr>
<tr>
<td>VCO INHIBIT</td>
<td>10</td>
<td>I</td>
<td>VCO inhibit control. When VCO INHIBIT is high, VCO OUT is low (see Table 1).</td>
</tr>
<tr>
<td>VCO OUT</td>
<td>3</td>
<td>O</td>
<td>VCO output. When VCO INHIBIT is high, VCO OUT is low.</td>
</tr>
<tr>
<td>VCO V_{DD}</td>
<td>14</td>
<td></td>
<td>Power supply for VCO. This power supply should be separated from LOGIC V_{DD} to reduce cross-coupling between supplies.</td>
</tr>
</tbody>
</table>

detailed description

VCO Oscillation Frequency

The VCO oscillation frequency is determined by an external resistor (R_{BIAS}) connected between the VCO V_{DD} and the BIAS terminals. The oscillation frequency and range depends on this resistor value. While all resistor values within the specified range result in excellent low temperature coefficients, the bias resistor value for the minimum temperature coefficient is nominally 2.2 k\Omega with 3-V V_{DD} and nominally 2.4 k\Omega with 5-V V_{DD}. For the lock frequency range refer to the recommended operating conditions. Figure 1 shows the typical frequency variation and VCO control voltage.

![Figure 1. VCO Oscillation Frequency](image-url)
VCO inhibit function

The VCO has an externally controlled inhibit function which inhibits the VCO output. A high level on the VCO INHIBIT terminal stops the VCO oscillation and powers down the VCO. The output maintains a low level during the power-down mode as shown in Table 1.

<table>
<thead>
<tr>
<th>VCO INHIBIT</th>
<th>VCO OSCILLATOR</th>
<th>VCO OUT</th>
<th>IDD(VCO)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>Active</td>
<td>Active</td>
<td>Normal</td>
</tr>
<tr>
<td>High</td>
<td>Stopped</td>
<td>Low level</td>
<td>Power Down</td>
</tr>
</tbody>
</table>

Table 1. VCO Inhibit Function

PFD operation

The PFD is a high-speed, edge-triggered detector with an internal charge pump. The PFD detects the phase difference between two frequency inputs supplied to FIN–A and FIN–B as shown in Figure 2. Nominally the reference is supplied to FIN–A, and the frequency from the external counter output is fed to FIN–B. For clock recovery PLL systems, other types of phase detectors should be used.

<table>
<thead>
<tr>
<th>PFD INHIBIT</th>
<th>DETECTION</th>
<th>PFD OUT</th>
<th>IDD(PFD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>Active</td>
<td>Active</td>
<td>Normal</td>
</tr>
<tr>
<td>High</td>
<td>Stopped</td>
<td>Hi-Z</td>
<td>Power Down</td>
</tr>
</tbody>
</table>

Table 2. VCO Output Control Function

Figure 2. PFD Function Timing Chart

PFD inhibit control

A high level on the PFD INHIBIT terminal places PFD OUT in the high-impedance state and the PFD stops phase detection as shown in Table 2. A high level on the PFD INHIBIT terminal can also be used as the power-down mode for the PFD.
schematics

VCO block schematic

PFD block schematic

absolute maximum ratings†

Supply voltage (each supply), \( V_{DD} \) (see Note 1) ................................. 7 V
Input voltage range (each input), \( V_I \) (see Note 1) ............................. \(-0.3 \) V to \( V_{DD} + 0.3 \) V
Input current (each input), \( I_I \) .................................................. \( \pm 20 \) mA
Output current (each output), \( I_O \) .................................................. \( \pm 20 \) mA
Continuous total power dissipation at (or below) \( T_A = 25^\circ C \) (see Note 2) ...................... 700 mW
Operating free-air temperature range, \( T_A \) ........................................... \(-20^\circ C \) to \( 75^\circ C \)
Storage temperature range, \( T_{stg} \) .................................................... \(-65^\circ C \) to \( 150^\circ C \)
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds ......................... \( 260^\circ C \)

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values are with respect to network ground terminal.
2. For operation above \( 25^\circ C \) free-air temperature, derate linearly at the rate of 5.6 mW/°C.
**recommended operating conditions**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, (V_{DD}) (each supply, see Note 3)</td>
<td>(V_{DD} = 3\ V)</td>
<td>2.85</td>
<td>3</td>
<td>3.15</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>(V_{DD} = 5\ V)</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage, (V_I) (inputs except VCO IN)</td>
<td>(V_{DD})</td>
<td>0</td>
<td>(V_{DD})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output current, (I_O) (each output)</td>
<td>(0\ \pm\ 2\ mA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCO control voltage at VCO IN</td>
<td>(V_{DD})</td>
<td>1</td>
<td>(V_{DD})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Lock frequency</td>
<td>(V_{DD} = 3\ V)</td>
<td>37</td>
<td>55</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{DD} = 5\ V)</td>
<td>43</td>
<td>100</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Bias resistor, (R_{BIAS})</td>
<td>(V_{DD} = 3\ V)</td>
<td>1.8</td>
<td>2.7</td>
<td>k\Omega</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{DD} = 5\ V)</td>
<td>2.2</td>
<td>3</td>
<td>k\Omega</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE 3:** It is recommended that the logic supply terminal (LOGIC \(V_{DD}\)) and the VCO supply terminal (VCO \(V_{DD}\)) be at the same voltage and separated from each other.

**electrical characteristics over recommended operating free-air temperature range, \(V_{DD} = 3\ V\)**

(unless otherwise noted)

**VCO section**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OH})</td>
<td>High-level output voltage</td>
<td>(I_{OH} = -2\ mA)</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Low-level output voltage</td>
<td>(I_{OL} = 2\ mA)</td>
<td>0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{IT+})</td>
<td>Positive input threshold voltage at TEST, VCO INHIBIT</td>
<td>0.9</td>
<td>1.5</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td>(I_I)</td>
<td>Input current at TEST, VCO INHIBIT</td>
<td>(V_I = V_{DD}) or ground</td>
<td>(\pm\ 1\ \mu A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Z_{I(VCO\ IN)})</td>
<td>Input impedance at VCO IN</td>
<td>(VCO\ IN = 1/2\ V_{DD})</td>
<td>10</td>
<td></td>
<td>M\Omega</td>
</tr>
<tr>
<td>(I_{DD,(INH)})</td>
<td>VCO supply current (inhibit)</td>
<td>See Note 4</td>
<td>0.01</td>
<td>1</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{DD,(VCO)})</td>
<td>VCO supply current</td>
<td>See Note 5</td>
<td>5.1</td>
<td>15</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES:**
4. The current into VCO \(V_{DD}\) and LOGIC \(V_{DD}\) when VCO INHIBIT = \(V_{DD}\) and PFD INHIBIT is high.
5. The current into VCO \(V_{DD}\) and LOGIC \(V_{DD}\) when VCO \(I_N = 1/2 \ V_{DD}\), \(R_{BIAS} = 2.4\ k\Omega\), VCO INHIBIT = ground, and PFD INHIBIT is high.

**PFD section**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{OH})</td>
<td>High-level output voltage</td>
<td>(I_{OH} = -2\ mA)</td>
<td>2.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_{OL})</td>
<td>Low-level output voltage</td>
<td>(I_{OL} = 2\ mA)</td>
<td>0.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{OZ})</td>
<td>High-impedance-state output current</td>
<td>PFD INHIBIT = high, (V_I = V_{DD}) or ground</td>
<td>(\pm\ 1\ \mu A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{IH})</td>
<td>High-level input voltage at FIN–A, FIN–B</td>
<td>2.1</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{IL})</td>
<td>Low-level input voltage at FIN–A, FIN–B</td>
<td>0.9</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(V_{IT+})</td>
<td>Positive input threshold voltage at PFD INHIBIT</td>
<td>0.9</td>
<td>1.5</td>
<td>2.1</td>
<td>V</td>
</tr>
<tr>
<td>(C_I)</td>
<td>Input capacitance at FIN–A, FIN–B</td>
<td></td>
<td>5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(Z_I)</td>
<td>Input impedance at FIN–A, FIN–B</td>
<td></td>
<td>10</td>
<td></td>
<td>M\Omega</td>
</tr>
<tr>
<td>(I_{DD,(Z)})</td>
<td>High-impedance-state PFD supply current</td>
<td>See Note 6</td>
<td>0.01</td>
<td>1</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(I_{DD,(PFD)})</td>
<td>PFD supply current</td>
<td>See Note 7</td>
<td>0.7</td>
<td>4</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES:**
6. The current into LOGIC \(V_{DD}\) when FIN–A and FIN–B = ground, PFD INHIBIT = \(V_{DD}\), PFD OUT open, and VCO OUT is inhibited.
7. The current into LOGIC \(V_{DD}\) when FIN–A and FIN–B = 30 MHz (\(V_{PP}(I) = 3\ V\), rectangular wave), PFD INHIBIT = GND, PFD OUT open, and VCO OUT is inhibited.
operating characteristics over recommended operating free-air temperature range, $V_{DD} = 3\, V$ (unless otherwise noted)

### VCO section

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{osc}$</td>
<td>$R_{BIAS} = 2.4, k\Omega$, $V_{CO, IN} = 1/2, V_{DD}$</td>
<td>38</td>
<td>48</td>
<td>55</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{s(fosc)}$</td>
<td>Time to stable oscillation (see Note 8)</td>
<td>Measured from $V_{CO, INHIBIT}$↓</td>
<td>10</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{r}$</td>
<td>Rise time, $V_{CO, OUT}$↑</td>
<td>$C_L = 15, pF$, See Figure 3</td>
<td>3.3</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f}$</td>
<td>Fall time, $V_{CO, OUT}$↓</td>
<td>$C_L = 15, pF$, See Figure 3</td>
<td>2</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>Duty cycle at $V_{CO, OUT}$</td>
<td>$R_{BIAS} = 2.4, k\Omega$, $V_{CO, IN} = 1/2, V_{DD}$</td>
<td>45%</td>
<td>50%</td>
<td>55%</td>
<td></td>
</tr>
<tr>
<td>$\alpha(fosc)$</td>
<td>Temperature coefficient of oscillation frequency</td>
<td>$R_{BIAS} = 2.4, k\Omega$, $V_{CO, IN} = 1/2, V_{DD}$; $T_A = -20^\circ C$ to $75^\circ C$</td>
<td>0.03</td>
<td>%/°C</td>
<td></td>
</tr>
<tr>
<td>$k_{SVS(fosc)}$</td>
<td>Supply voltage coefficient of oscillation frequency</td>
<td>$R_{BIAS} = 2.4, k\Omega$, $V_{CO, IN} = 1.5, V$, $V_{DD} = 2.85, V$ to $3.15, V$</td>
<td>0.04</td>
<td>%/mV</td>
<td></td>
</tr>
<tr>
<td>Jitter absolute (see Note 9)</td>
<td>$R_{BIAS} = 2.4, k\Omega$</td>
<td>100</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
</tbody>
</table>

**NOTES:**
8. The time period to stabilize the VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed printed circuit board (PCB) with no device socket.

### PFD section

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{max}$</td>
<td>Maximum operating frequency</td>
<td>30</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>Disable time, PFD INHIBIT↑ to PFD OUT Hi-Z</td>
<td>20</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHZ}$</td>
<td>Disable time, PFD INHIBIT↑ to PFD OUT Hi-Z</td>
<td>18</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZL}$</td>
<td>Enable time, PFD INHIBIT↓ to PFD OUT low</td>
<td>4.1</td>
<td>18</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PH}$</td>
<td>Enable time, PFD INHIBIT↓ to PFD OUT high</td>
<td>4.8</td>
<td>18</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise time, PFD OUT↑</td>
<td>$C_L = 15, pF$, See Figure 4</td>
<td>3.1</td>
<td>9</td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall time, PFD OUT↓</td>
<td></td>
<td>1.5</td>
<td>9</td>
<td>ns</td>
</tr>
</tbody>
</table>
electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 5\, \text{V}$ (unless otherwise noted)

### VCO section

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>High-level output voltage</td>
<td>$I_{OH} = -2, \text{mA}$</td>
<td>4.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage</td>
<td>$I_{OL} = 2, \text{mA}$</td>
<td></td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>$V_{IT+}$</td>
<td>Positive input threshold voltage at TEST, VCO INHIBIT</td>
<td></td>
<td>1.5</td>
<td>2.5</td>
<td>3.5</td>
</tr>
<tr>
<td>$I_{I}$</td>
<td>Input current at TEST, VCO INHIBIT</td>
<td>$V_I = V_{DD}$ or ground</td>
<td></td>
<td></td>
<td>$\pm 1$</td>
</tr>
<tr>
<td>$Z_{I(VCO, IN)}$</td>
<td>Input impedance at VCO IN</td>
<td>VCO IN = $1/2, V_{DD}$</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DD(INH)}$</td>
<td>VCO supply current (inhibit)</td>
<td>See Note 4</td>
<td>0.01</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$I_{DD(VCO)}$</td>
<td>VCO supply current</td>
<td>See Note 5</td>
<td>14</td>
<td>35</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
4. The current into VCO $V_{DD}$ and LOGIC $V_{DD}$ when VCO INHIBIT = $V_{DD}$, and PFD INHIBIT high.
5. The current into VCO $V_{DD}$ and LOGIC $V_{DD}$ when VCO IN = $1/2\, V_{DD}$, $R_{BIAS} = 2.4\, \text{kΩ}$, VCO INHIBIT = ground, and PFD INHIBIT high.

### PFD section

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>High-level output voltage</td>
<td>$I_{OH} = 2, \text{mA}$</td>
<td>4.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage</td>
<td>$I_{OL} = 2, \text{mA}$</td>
<td></td>
<td>0.2</td>
<td></td>
</tr>
<tr>
<td>$I_{OZ}$</td>
<td>High-impedance-state output current</td>
<td>PFD INHIBIT = high, $V_I = V_{DD}$ or ground</td>
<td></td>
<td></td>
<td>$\pm 1$</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>High-level input voltage at FIN−A, FIN−B</td>
<td></td>
<td>3.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Low-level input voltage at FIN−A, FIN−B</td>
<td></td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IT+}$</td>
<td>Positive input threshold voltage at PFD INHIBIT</td>
<td></td>
<td>1.5</td>
<td>2.5</td>
<td>3.5</td>
</tr>
<tr>
<td>$C_{I}$</td>
<td>Input capacitance at FIN−A, FIN−B</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Z_{I}$</td>
<td>Input impedance at FIN−A, FIN−B</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{DD(Z)}$</td>
<td>High-impedance-state PFD supply current</td>
<td>See Note 6</td>
<td>0.01</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$I_{DD(PFD)}$</td>
<td>PFD supply current</td>
<td>See Note 10</td>
<td>2.6</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
6. The current into LOGIC $V_{DD}$ when FIN−A and FIN−B = ground, PFD INHIBIT = $V_{DD}$, PFD OUT open, and VCO OUT is inhibited.
10. The current into LOGIC $V_{DD}$ when FIN−A and FIN−B = 50 MHz ($V_{(PP)} = 3\, \text{V}$, rectangular wave), PFD INHIBIT = ground, PFD OUT open, and VCO OUT is inhibited.
operating characteristics over recommended operating free-air temperature range, $V_{DD} = 5\,V$ (unless otherwise noted)

### VCO section

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{osc}$ Operating oscillation frequency</td>
<td>$R_{\text{BIAS}} = 2.4,k\Omega$, $V_{\text{CO IN}} = 1/2,V_{DD}$</td>
<td>64</td>
<td>80</td>
<td>96</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_s(f_{osc})$ Time to stable oscillation (see Note 8)</td>
<td>Measured from $V_{\text{CO INHIBIT}}\downarrow$</td>
<td>10</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>$t_r$ Rise time, $V_{\text{CO OUT}}\uparrow$</td>
<td>$C_L = 15,pF$, See Figure 3</td>
<td>2.1</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$ Fall time, $V_{\text{CO OUT}}\downarrow$</td>
<td>$C_L = 15,pF$, See Figure 3</td>
<td>1.5</td>
<td>4</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Duty cycle at $V_{\text{CO OUT}}$</td>
<td>$R_{\text{BIAS}} = 2.4,k\Omega$, $V_{\text{CO IN}} = 1/2,V_{DD}$</td>
<td>45%</td>
<td>50%</td>
<td>55%</td>
<td>%</td>
</tr>
<tr>
<td>$\alpha(f_{osc})$ Temperature coefficient of oscillation frequency</td>
<td>$R_{\text{BIAS}} = 2.4,k\Omega$, $V_{\text{CO IN}} = 1/2,V_{DD}$, $-20^\circ\text{C}$ to $75^\circ\text{C}$</td>
<td>0.03</td>
<td></td>
<td></td>
<td>%$/^\circ\text{C}$</td>
</tr>
<tr>
<td>$k_{SVS}(f_{osc})$ Supply voltage coefficient of oscillation frequency</td>
<td>$R_{\text{BIAS}} = 2.4,k\Omega$, $V_{\text{CO IN}} = 2.5,V$, $V_{DD} = 4.75,V$ to $5.25,V$</td>
<td>0.02</td>
<td></td>
<td></td>
<td>%$/mV$</td>
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<tr>
<td>Jitter absolute (see Note 9)</td>
<td>$R_{\text{BIAS}} = 2.4,k\Omega$</td>
<td>100</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
</tbody>
</table>

**NOTES:**
8. The time period to stabilize the VCO oscillation frequency after the VCO INHIBIT terminal is changed to a low level.
9. Jitter performance is highly dependent on circuit layout and external device characteristics. The jitter specification was made with a carefully designed printed circuit board (PCB) with no device socket.

### PFD section

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{max}$ Maximum operating frequency</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{PLZ}$ Disable time, PFD INHIBIT$\uparrow$ to PFD OUT Hi-Z</td>
<td>See Figures 4 and 5 and Table 3</td>
<td>20</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHZ}$ Disable time, PFD INHIBIT$\uparrow$ to PFD OUT Hi-Z</td>
<td>See Figures 4 and 5 and Table 3</td>
<td>17</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLI}$ Enable time, PFD INHIBIT$\downarrow$ to PFD OUT low</td>
<td>See Figures 4 and 5 and Table 3</td>
<td>3.7</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}$ Enable time, PFD INHIBIT$\downarrow$ to PFD OUT high</td>
<td>See Figures 4 and 5 and Table 3</td>
<td>3.4</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_r$ Rise time, PFD OUT$\uparrow$</td>
<td>$C_L = 15,pF$, See Figure 4</td>
<td>1.7</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$ Fall time, PFD OUT$\downarrow$</td>
<td>$C_L = 15,pF$, See Figure 4</td>
<td>1.3</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
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</table>
PARAMETER MEASUREMENT INFORMATION

VCO OUT

Figure 3. VCO Output Voltage Waveform

(a) PFD OUT Hi-Z Timing To and From a High Level (see Figure 5 and Table 3)
(b) PFD OUT Hi-Z Timing To and From a Low Level (see Figure 5 and Table 3)

† FIN–A and FIN–B are for reference phase only, not for timing.

Figure 4. PFD Output Voltage Waveform

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>$R_L$</th>
<th>$C_L$</th>
<th>$S_1$</th>
<th>$S_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PZH}$</td>
<td>1 kΩ</td>
<td>15 pF</td>
<td>Open</td>
<td>Closed</td>
</tr>
<tr>
<td>$t_{PHZ}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_r$</td>
<td></td>
<td></td>
<td>Open</td>
<td>Closed</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3. PFD Output Test Conditions

Test Point

DUT

VDD

PFD OUT

$R_L$

$S_1$

$S_2$

$C_L$

Figure 5. PFD Output Test Conditions
TYPICAL CHARACTERISTICS

Figure 6

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

Figure 7

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

Figure 8

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE

Figure 9

VCO OSCILLATION FREQUENCY
vs
VCO CONTROL VOLTAGE
TYPICAL CHARACTERISTICS

**Figure 10**

VCO OSCILLATION FREQUENCY

vs

VCO CONTROL VOLTAGE

- $f_{osc} - VCO$ Oscillation Frequency - MHz
- $VDD = 5$ V
- $R_{BIAS} = 2.2$ kΩ
- $75°C$
- $25°C$
- $-20°C$

![Graph showing VCO Oscillation Frequency vs VCO Control Voltage](image)

**Figure 11**

VCO OSCILLATION FREQUENCY

vs

VCO CONTROL VOLTAGE

- $f_{osc} - VCO$ Oscillation Frequency - MHz
- $VDD = 5$ V
- $R_{BIAS} = 2.4$ kΩ
- $75°C$
- $25°C$
- $-20°C$

![Graph showing VCO Oscillation Frequency vs VCO Control Voltage](image)

**Figure 12**

VCO OSCILLATION FREQUENCY

vs

VCO CONTROL VOLTAGE

- $f_{osc} - VCO$ Oscillation Frequency - MHz
- $VDD = 5$ V
- $R_{BIAS} = 2.7$ kΩ
- $75°C$
- $25°C$
- $-20°C$

![Graph showing VCO Oscillation Frequency vs VCO Control Voltage](image)

**Figure 13**

VCO OSCILLATION FREQUENCY

vs

VCO CONTROL VOLTAGE

- $f_{osc} - VCO$ Oscillation Frequency - MHz
- $VDD = 5$ V
- $R_{BIAS} = 3$ kΩ
- $75°C$
- $25°C$
- $-20°C$

![Graph showing VCO Oscillation Frequency vs VCO Control Voltage](image)
TYPICAL CHARACTERISTICS

**RECOMMENDED LOCK FREQUENCY vs BIAS RESISTOR**

For $V_{DD} = 3 \, \text{V} \pm 5\%$

$T_A = -20^\circ \text{C}$ to $75^\circ \text{C}$

*MAX* and *MIN* values shown.

**Figure 14**

---

**RECOMMENDED LOCK FREQUENCY vs BIAS RESISTOR**

For $V_{DD} = 5 \, \text{V} \pm 5\%$

$T_A = -20^\circ \text{C}$ to $75^\circ \text{C}$

*MAX* and *MIN* values shown.

**Figure 15**

---

---

---
APPLICATION INFORMATION

gain of VCO and PFD

Figure 16 is a block diagram of the PLL. The divider N value depends on the input frequency and the desired VCO output frequency according to the system application requirements. The Kp and Kv values are obtained from the operating characteristics of the device as shown in Figure 16. Kp is defined from the phase detector VOL and VOH specifications and the equation shown in Figure 16(b). Kv is defined from Figures 8, 9, 10, and 11 as shown in Figure 16(c).

The parameters for the block diagram with the units are as follows:

- \( K_v \): VCO gain (rad/s/V)
- \( K_p \): PFD gain (V/rad)
- \( K_f \): LPF gain (V/V)
- \( K_N \): countdown divider gain (1/N)

external counter

When a large N counter is required by the application, there is a possibility that the PLL response becomes slow due to the counter response delay time. In the case of a high frequency application, the counter delay time should be accounted for in the overall PLL design.

RBIAS

The external bias resistor sets the VCO center frequency with 1/2 VDD applied to the VCO IN terminal. For the most accurate results, a metal-film resistor is the better choice but a carbon-composition resistor can also be used with excellent results. A 0.22 \( \mu \)F capacitor should be connected from the BIAS terminal to ground as close to the device terminals as possible.

hold-in range

From the technical literature, the maximum hold-in range for an input frequency step for the three types of filter configurations shown in Figure 17 is as follows:

\[
\Delta \omega_H = 0.8 \left( K_p \right) \left( K_v \right) \left( K_f (\infty) \right)
\]

(1)

Where

- \( K_f (\infty) \) = the filter transfer function value at \( \omega = \infty \)
APPLICATION INFORMATION

low-pass-filter (LPF) configurations

Many excellent references are available that include detailed design information about LPFs and should be consulted for additional information. Lag-lead filters or active filters are often used. Examples of LPFs are shown in Figure 17. When the active filter of Figure 17(c) is used, the reference should be applied to FIN-B because of the amplifier inversion. Also, in practical filter implementations, C2 is used as additional filtering at the VCO input. The value of C2 should be equal to or less than one tenth the value of C1.

\[
T_1 = \frac{C_1 R_1}{R_1} \\
T_2 = \frac{C_1 R_2}{R_2}
\]

Figure 17. LPF Examples for PLL

the passive filter

The transfer function for the low-pass filter shown in Figure 17(b) is:

\[
\frac{V_O}{V_{IN}} = \frac{1 + s \cdot T_2}{1 + s \cdot (T_1 + T_2)}
\]  

(2)

where

\[T_1 = R_1 \cdot C_1 \] and \[T_2 = R_2 \cdot C_1\]

Using this filter makes the closed-loop PLL system a type 1 second-order system. The response curves of this system to a unit step are shown in Figure 18.

the active filter

When using the active filter shown in Figure 17(c), the phase detector inputs must be reversed since the filter adds an additional inversion. Therefore, the input reference frequency should be applied to the FIN-B terminal and the output of the VCO divider should be applied to the input reference terminal, FIN-A.

The transfer function for the active filter shown in Figure 17(c) is:

\[
F(s) = \frac{1 + s \cdot R_2 \cdot C_1}{s \cdot R_1 \cdot C_1}
\]  

(3)

Using this filter makes the closed-loop PLL system a type 2 second-order system. The response curves of this system to a unit step are shown in Figure 19.
APPLICATION INFORMATION

Using the lag-lead filter in Figure 17(b) and divider N value, the transfer function for phase and frequency are shown in equations 4 and 5. Note that the transfer function for phase differs from the transfer function for frequency by only the divider N value. The difference arises from the fact that the feedback for phase is unity while the feedback for frequency is 1/N.

Hence, the transfer function of Figure 17(a) for phase is

\[
\frac{\Phi_2(s)}{\Phi_1(s)} = \frac{K_p \cdot K_v}{N \cdot (T1 + T2)} \left[ \frac{1 + s \cdot T2}{s^2 + s \left( 1 + \frac{K_p \cdot K_v \cdot T2}{N \cdot (T1 + T2)} \right) + \frac{K_p \cdot K_v}{N \cdot (T1 + T2)}} \right]
\]  

(4)

and the transfer function for frequency is

\[
\frac{F_{\text{OUT}}(s)}{F_{\text{REF}}(s)} = \frac{K_p \cdot K_v}{(T1 + T2)} \left[ \frac{1 + s \cdot T2}{s^2 + s \left( 1 + \frac{K_p \cdot K_v \cdot T2}{N \cdot (T1 + T2)} \right) + \frac{K_p \cdot K_v}{N \cdot (T1 + T2)}} \right]
\]  

(5)

The standard 2-pole denominator is \( D = s^2 + 2 \zeta \omega_n s + \omega_n^2 \) and comparing the coefficients of the denominator of equation (4) and (5) with the standard 2-pole denominator gives the following results.

\[
\omega_n = \sqrt{\frac{K_p \cdot K_v}{N \cdot (T1 + T2)}}
\]  

(6)

Solving for \( T1 + T2 \)

\[
T1 + T2 = \frac{K_p \cdot K_v}{N \cdot \omega_n^2}
\]

and by using this value for \( T1 + T2 \) in equation (6) the damping factor is

\[
\zeta = \frac{\omega_n}{2} \left( T2 + \frac{N}{K_p \cdot K_v} \right)
\]  

(7)

solving for \( T2 \)

\[
T2 = \frac{2 \zeta}{\omega_n} \frac{N}{K_p \cdot K_v}
\]  

(8)

then by substituting for \( T2 \) in equation (6)

\[
T1 = \frac{K_v \cdot K_p}{N \cdot \omega_n^2} - \frac{2 \zeta}{\omega_n} + \frac{N}{K_p \cdot K_v}
\]  

(9)
APPLICATION INFORMATION

From the circuit constants and the initial design parameters then

\[
R_2 = \left[ \frac{2\zeta}{\omega_n} - \frac{N}{K_p \cdot K_V} \right] \frac{1}{C_1} \tag{10}
\]

\[
R_1 = \left[ \frac{K_p \cdot K_V}{\omega_n^2} - \frac{2\zeta}{\omega_n} + \frac{N}{K_p \cdot K_V} \right] \frac{1}{C_1} \tag{11}
\]

The capacitor, \(C_1\), is usually chosen between 1 \(\mu\)F and 0.1 \(\mu\)F to allow for reasonable resistor values and physical capacitor size.
Figure 18. Type 1 Second-Order Step Response
Figure 19. Type 2 Second-Order Step Response
APPLICATION INFORMATION

Figure 20. Evaluation and Operation Schematic

PCB layout considerations

The TLC2933 contains a high frequency oscillator; therefore, very careful breadboarding and PCB layout is required for evaluation.

The following design recommendations benefit the TLC2933 user:

- External analog and digital circuitry should be physically separated and shielded as much as possible to reduce system noise.
- Radio frequency (RF) breadboarding or RF PCB techniques should be used throughout the evaluation and production process.
- Wide ground leads or a ground plane should be used on the PCB layouts to minimize parasitic inductance and resistance. The ground plane is the better choice for noise reduction.
- LOGIC V_DD and VCO V_DD should be separate PCB traces and connected to the best filtered supply point available in the system to minimize supply cross-coupling.
- VCO V_DD to ground and LOGIC V_DD to ground should be decoupled with a 0.1-µF capacitor placed as close as possible to the appropriate device terminals.
- The no-connection (NC) terminal on the package should be connected to ground to prevent stray pickup.
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC2933IPW</td>
<td>NRND</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-20 to 75</td>
<td>Y2933</td>
<td></td>
</tr>
<tr>
<td>TLC2933IPWG4</td>
<td>NRND</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-20 to 75</td>
<td>Y2933</td>
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</tr>
<tr>
<td>TLC2933IPWR</td>
<td>NRND</td>
<td>TSSOP</td>
<td>PW</td>
<td>14</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-20 to 75</td>
<td>Y2933</td>
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<td>TLC2933IPWRG4</td>
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<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-20 to 75</td>
<td>Y2933</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

- **TBD**: The Pb-Free/Green conversion plan has not been defined.

- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
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### TAPE AND REEL INFORMATION

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<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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</thead>
<tbody>
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<td>TSSOP</td>
<td>PW</td>
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<td>2000</td>
<td>330.0</td>
<td>12.4</td>
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<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

**Dimensions:**
- **A0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **K0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

**Diagram Notes:**
- **Reel Diameter (W1)**
- **Pocket Quadrants**
- **User Direction of Feed**
- **Sprocket Holes**

**Notes:**
- [www.ti.com](http://www.ti.com) 29-Sep-2019

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Pack Materials-Page 1
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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<td>367.0</td>
<td>367.0</td>
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