1 Features
- 16 Channels
- 12 bit (4096 Steps) Grayscale PWM Control
- Dot Correction
  - 6 bit (64 Steps)
  - Storable in Integrated EEPROM
- Drive Capability (Constant-Current Sink)
  - 0 mA to 60 mA (V<sub>CC</sub> < 3.6 V)
  - 0 mA to 120 mA (V<sub>CC</sub> > 3.6 V)
- LED Power Supply Voltage up to 17 V
- V<sub>CC</sub> = 3 V to 5.5 V
- Serial Data Interface
- Controlled In-Rush Current
- 30 MHz Data Transfer Rate
- CMOS Level I/O
- Error Information
  - LOD: LED Open Detection
  - TEF: Thermal Error Flag

2 Applications
- Monocolor, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Backlighting
- General, High-Current LED Drive

3 Description
The TLC5940 is a 16-channel, constant-current sink LED driver. Each channel has an individually adjustable 4096-step grayscale PWM brightness control and a 64-step, constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED channels and other LED drivers. The dot correction data is stored in an integrated EEPROM. Both grayscale control and dot correction are accessible through a serial interface. A single external resistor sets the maximum current value of all 16 channels.

The TLC5940 features two error information circuits. The LED open detection (LOD) indicates a broken or disconnected LED at an output terminal. The thermal error flag (TEF) indicates an overtemperature condition.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC5940</td>
<td>PDIP (28)</td>
<td>35.69 mm × 6.73 mm</td>
</tr>
<tr>
<td></td>
<td>HTSSOP (28)</td>
<td>9.70 mm × 4.40 mm</td>
</tr>
<tr>
<td></td>
<td>VQFN (32)</td>
<td>5.00 mm × 5.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.
Table of Contents

1 Features ................................................................. 1
2 Applications ............................................................ 1
3 Description ............................................................. 1
4 Revision History ....................................................... 2
5 Pin Configuration and Functions ......................... 3
6 Specifications .......................................................... 5
   6.1 Absolute Maximum Ratings ............................... 5
   6.2 ESD Ratings ........................................................ 5
   6.3 Recommended Operating Conditions .................... 5
   6.4 Thermal Information ............................................. 6
   6.5 Electrical Characteristics ...................................... 7
   6.6 Switching Characteristics ....................................... 8
   6.7 Typical Characteristics .......................................... 9
7 Parameter Measurement Information ....................... 11
   7.1 Test Parameter Equations .................................... 12
8 Detailed Description ................................................ 13
   8.1 Overview ............................................................ 13
8.2 Functional Block Diagram ..................................... 13
8.3 Feature Description .............................................. 13
8.4 Device Functional Modes ....................................... 18
9 Application and Implementation ......................... 23
   9.1 Application Information ...................................... 23
   9.2 Typical Application .............................................. 23
10 Power Supply Recommendations ............................ 25
11 Layout ................................................................. 25
   11.1 Layout Guidelines .............................................. 25
   11.2 Layout Example ................................................ 25
   11.3 Power Dissipation Calculation ............................. 26
12 Device and Documentation Support ....................... 27
   12.1 Community Resources ....................................... 27
   12.2 Trademarks ....................................................... 27
   12.3 Electrostatic Discharge Caution ......................... 27
   12.4 Glossary .......................................................... 27
13 Mechanical, Packaging, and Orderable Information .... 27

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2007) to Revision D Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ........................................ 1

Changes from Revision B (September 2007) to Revision C Page

• Changed t\textsubscript{sus} setup time from: 30 ms to: 30 ns ......................................................... 6
5 Pin Configuration and Functions

**PWP Package**
28-Pin HTSSOP
Top View

- GND 1
- BLANK 2
- XLAT 3
- SCLK 4
- SIN 5
- VPRG 6
- OUT0 7
- OUT1 8
- OUT2 9
- OUT3 10
- OUT4 11
- OUT5 12
- OUT6 13
- OUT7 14
- 28 VCC
- 27 IREF
- 26 DCPRG
- 25 GSCLK
- 24 SOUT
- 23 XERR
- 22 OUT15
- 21 OUT14
- 20 OUT13
- 19 OUT12
- 18 OUT11
- 17 OUT10
- 16 OUT9
- 15 OUT8

**NT Package**
28-Pin PDIP
Top View

- OUT1 1
- OUT2 2
- OUT3 3
- OUT4 4
- OUT5 5
- OUT6 6
- OUT7 7
- OUT8 8
- OUT9 9
- OUT10 10
- OUT11 11
- OUT12 12
- OUT13 13
- OUT14 14
- 28 OUT0
- 27 VPRG
- 26 SIN
- 25 SCLK
- 24 XLAT
- 23 BLANK
- 22 GND
- 21 VCC
- 20 IREF
- 19 DCPRG
- 18 GSCLK
- 17 SOUT
- 16 XERR
- 15 OUT15

**RHB Package**
32-Pin VQFN
Top View

- GSCLK 24
- OUT 25
- OUT15 26
- OUT14 27
- OUT13 28
- OUT12 29
- OUT11 30
- OUT10 31
- OUT9 32
- OUT8 33
- OUT7 34
- OUT6 35
- OUT5 36
- 16 DCPRG
- 15 VCC
- 14 NC
- 13 NC
- 12 NC
- 11 OUT7
- 10 OUT6
- 9 OUT5
- 8 SCLK
- 7 SIN
- 6 VPRG
- 5 BLANK
- 4 OUT0
- 3 OUT1
- 2 XLAT
- 1 XERR

NC – No internal connection
## Pin Functions

<table>
<thead>
<tr>
<th>NAME</th>
<th>DIP NO.</th>
<th>PWP NO.</th>
<th>RHB NO.</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>BLANK</td>
<td>23</td>
<td>2</td>
<td>31</td>
<td>I</td>
<td>Blank all outputs. When BLANK = H, all OUTn outputs are forced OFF. GS counter is also reset. When BLANK = L, OUTn are controlled by grayscale PWM control.</td>
</tr>
<tr>
<td>DCPRG</td>
<td>19</td>
<td>26</td>
<td>25</td>
<td>I</td>
<td>Switch DC data input. When DCPRG = L, DC is connected to EEPROM. When DCPRG = H, DC is connected to the DC register. DCPRG also controls EEPROM writing, when VPRG = $V_{(PRG)}$. EEPROM data = 3 Fh (default)</td>
</tr>
<tr>
<td>GND</td>
<td>22</td>
<td>1</td>
<td>30</td>
<td>G</td>
<td>Ground</td>
</tr>
<tr>
<td>GSCLK</td>
<td>18</td>
<td>25</td>
<td>24</td>
<td>I</td>
<td>Reference clock for grayscale PWM control</td>
</tr>
<tr>
<td>IREF</td>
<td>20</td>
<td>27</td>
<td>26</td>
<td>I</td>
<td>Reference current terminal</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>—</td>
<td>12</td>
<td>—</td>
<td>No connection</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>—</td>
<td>13</td>
<td>—</td>
<td>No connection</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>—</td>
<td>28</td>
<td>—</td>
<td>No connection</td>
</tr>
<tr>
<td>NC</td>
<td>—</td>
<td>—</td>
<td>29</td>
<td>—</td>
<td>No connection</td>
</tr>
<tr>
<td>OUT0</td>
<td>28</td>
<td>7</td>
<td>4</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT1</td>
<td>1</td>
<td>8</td>
<td>5</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT2</td>
<td>2</td>
<td>9</td>
<td>6</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT3</td>
<td>3</td>
<td>10</td>
<td>7</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT4</td>
<td>4</td>
<td>11</td>
<td>8</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT5</td>
<td>5</td>
<td>12</td>
<td>9</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT6</td>
<td>6</td>
<td>13</td>
<td>10</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT7</td>
<td>7</td>
<td>14</td>
<td>11</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT8</td>
<td>8</td>
<td>15</td>
<td>14</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT9</td>
<td>9</td>
<td>16</td>
<td>15</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT10</td>
<td>10</td>
<td>17</td>
<td>16</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT11</td>
<td>11</td>
<td>18</td>
<td>17</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT12</td>
<td>12</td>
<td>19</td>
<td>18</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT13</td>
<td>13</td>
<td>20</td>
<td>19</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT14</td>
<td>14</td>
<td>21</td>
<td>20</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>OUT15</td>
<td>15</td>
<td>22</td>
<td>21</td>
<td>O</td>
<td>Constant current output</td>
</tr>
<tr>
<td>SCLK</td>
<td>25</td>
<td>4</td>
<td>1</td>
<td>I</td>
<td>Serial data shift clock</td>
</tr>
<tr>
<td>SIN</td>
<td>26</td>
<td>5</td>
<td>2</td>
<td>I</td>
<td>Serial data input</td>
</tr>
<tr>
<td>SOUT</td>
<td>17</td>
<td>24</td>
<td>23</td>
<td>O</td>
<td>Serial data output</td>
</tr>
<tr>
<td>VCC</td>
<td>21</td>
<td>28</td>
<td>27</td>
<td>I</td>
<td>Power supply voltage</td>
</tr>
<tr>
<td>VPRG</td>
<td>27</td>
<td>6</td>
<td>3</td>
<td>I</td>
<td>Multifunction input pin. When VPRG = GND, the device is in GS mode. When VPRG = $V_{CC}$, the device is in DC mode. When VPRG = $V_{(PRG)}$, DC register data can programmed into DC EEPROM with DCPRG=HIGH. EEPROM data = 3 Fh (default)</td>
</tr>
<tr>
<td>XERR</td>
<td>16</td>
<td>23</td>
<td>22</td>
<td>O</td>
<td>Error output. XERR is an open-drain terminal. XERR goes L when LOD or TEF is detected.</td>
</tr>
<tr>
<td>XLAT</td>
<td>24</td>
<td>3</td>
<td>32</td>
<td>I</td>
<td>Level triggered latch signal. When XLAT = high, the TLC5940 writes data from the input shift register to either GS register (VPRG = low) or DC register (VPRG = high). When XLAT = low, the data in GS or DC register is held constant.</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage(^{(2)})</td>
<td>VCC</td>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>V(<em>{(BLANK)}), V(</em>{(DCPRG)}), V(<em>{(SCLK)}), V(</em>{(XLAT)}), V(<em>{(SIN)}), V(</em>{(IREF)})</td>
<td>–0.3</td>
<td>V(_{CC}) +0.3</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>V(<em>{(SOUT)}), V(</em>{(XERR)})</td>
<td>–0.3</td>
<td>V(_{CC}) +0.3</td>
</tr>
<tr>
<td>V(<em>{(OUT0)}) to V(</em>{(OUT15)})</td>
<td>–0.3</td>
<td>18</td>
<td>V</td>
</tr>
<tr>
<td>Output current (dc)</td>
<td></td>
<td>130</td>
<td>mA</td>
</tr>
<tr>
<td>EEPROM program range</td>
<td></td>
<td>–0.3</td>
<td>24</td>
</tr>
<tr>
<td>EEPROM write cycles</td>
<td></td>
<td>50</td>
<td>—</td>
</tr>
<tr>
<td>Storage temperature, T(_{stg})</td>
<td>–55</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{(ESD)}) Electrostatic discharge</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
</tr>
<tr>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±500</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{CC}) Supply Voltage</td>
<td>3</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V(_{O}) Voltage applied to output (OUT0–OUT15)</td>
<td>17</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{IH}) High-level input voltage</td>
<td>0.8 V(_{CC})</td>
<td>V(_{CC})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V(_{IL}) Low-level input voltage</td>
<td>GND</td>
<td>0.2 V(_{CC})</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I(_{OH}) High-level output current</td>
<td>V(_{CC}) = 5 V at SOUT</td>
<td>–1 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I(_{OL}) Low-level output current</td>
<td>V(_{CC}) = 5 V at SOUT, XERR</td>
<td>1 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I(_{OLC}) Constant output current</td>
<td>OUT0 to OUT15, V(_{CC}) &lt; 3.6 V</td>
<td>60 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>OUT0 to OUT15, V(_{CC}) &gt; 3.6 V</td>
<td>120 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(_{(VPRG)}) EEPROM program voltage</td>
<td>20</td>
<td>22</td>
<td>23</td>
<td>V</td>
</tr>
<tr>
<td>T(_{A}) Operating free-air temperature range</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>AC CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V(<em>{CC}) = 3 V to 5.5 V, T(</em>{A}) = –40°C to 85°C (unless otherwise noted)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>f(_{(SCLK)}) Data shift clock frequency</td>
<td>SCLK</td>
<td>16</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>f(_{(GSCLK)}) Grayscale clock frequency</td>
<td>GSCLK</td>
<td>16</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>t(<em>{w0})/t(</em>{w0}) SCLK pulse duration</td>
<td>SCLK = H/L (see Figure 11)</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(<em>{w1})/t(</em>{w1}) GSCLK pulse duration</td>
<td>GSCLK = H/L (see Figure 11)</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(_{w2}) XLAT pulse duration</td>
<td>XLAT = H (see Figure 11)</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(_{w3}) BLANK pulse duration</td>
<td>BLANK = H (see Figure 11)</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
Recommended Operating Conditions (continued)

<table>
<thead>
<tr>
<th>Setup time</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{su0} )</td>
<td>SIN to SCLK ↑(1) (see Figure 11)</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{su1} )</td>
<td>SCLK ↓ to XLAT ↑ (see Figure 11)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{su2} )</td>
<td>VPRG ↑ ↓ to SCLK ↑ (see Figure 11)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{su3} )</td>
<td>VPRG ↑ XLAT ↑ (see Figure 11)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{su4} )</td>
<td>BLANK ↓ to GCLK ↑ (see Figure 11)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{su5} )</td>
<td>XLAT ↑ to GCLK ↑ (see Figure 11)</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{su6} )</td>
<td>VPRG ↑ to DCPRG ↑ (see Figure 16)</td>
<td>1</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hold Time</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{h0} )</td>
<td>SCLK ↑ to SIN (see Figure 11)</td>
<td>3</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{h1} )</td>
<td>XLAT ↓ to SCLK ↑ (see Figure 11)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{h2} )</td>
<td>SCLK ↑ to VPRG ↑ ↓ (see Figure 11)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{h3} )</td>
<td>XLAT ↓ to VPRG ↑ ↓ (see Figure 11)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{h4} )</td>
<td>GCLK ↑ to BLANK ↑ (see Figure 11)</td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{h5} )</td>
<td>DCPRG ↑ to VPRG ↓ (see Figure 11)</td>
<td>1</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( t_{\text{prog}} )</td>
<td>Programming time for EEPROM (see Figure 16)</td>
<td>20</td>
<td></td>
<td>ms</td>
</tr>
</tbody>
</table>

(1) ↑ and ↓ indicates a rising edge, and a falling edge respectively.

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TLC940</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\text{JA}} )</td>
<td>Junction-to-ambient thermal resistance</td>
<td>36.7</td>
</tr>
<tr>
<td>( R_{\text{JC}(\text{top})} )</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>18.9</td>
</tr>
<tr>
<td>( R_{\text{JB}} )</td>
<td>Junction-to-board thermal resistance</td>
<td>15.9</td>
</tr>
<tr>
<td>( \psi_{\text{JT}} )</td>
<td>Junction-to-top characterization parameter</td>
<td>0.6</td>
</tr>
<tr>
<td>( \psi_{\text{JB}} )</td>
<td>Junction-to-board characterization parameter</td>
<td>15.8</td>
</tr>
<tr>
<td>( R_{\text{JC}(\text{bot})} )</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>2.3</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics

\( V_{CC} = 3 \text{ V to 5.5 V}, \ T_A = -40^\circ \text{C to 85^\circ C} \) (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OH} )</td>
<td>High-level output voltage</td>
<td>( I_{OH} = -1 \text{ mA}, \ SOUT )</td>
<td>( V_{CC} -0.5 )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Low-level output voltage</td>
<td>( I_{OL} = 1 \text{ mA}, \ SOUT )</td>
<td></td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>( I_I )</td>
<td>Input current</td>
<td>( V_I = V_{CC} ) or GND; BLANK, DCPRG, GSCLK, SCLK, SIN, XLAT</td>
<td>( -1 )</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>( V_I = \text{GND; VPRG} )</td>
<td></td>
<td>( -1 )</td>
<td>1</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>( V_I = V_{CC}; \ VPRG )</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_I = 22 \text{ V; VPRG; DCPRG} = V_{CC} )</td>
<td></td>
<td>4</td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( I_{II} )</td>
<td>Input current</td>
<td>( V_I = V_{CC} ); \ VPRG</td>
<td>0.9</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>( V_I = 22 \text{ V; VPRG; DCPRG} = V_{CC} )</td>
<td></td>
<td>5.2</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Supply current</td>
<td>No data transfer, all output OFF, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 10 \text{ kΩ} )</td>
<td>0.9</td>
<td>6</td>
<td>mA</td>
</tr>
<tr>
<td>( V_O = 1 \text{ V}, \ R_{\text{REF}} = 1.3 \text{ kΩ} )</td>
<td></td>
<td>5.2</td>
<td>12</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>( V_O = 1 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω} )</td>
<td></td>
<td>Data transfer 30MHz, all output ON, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 1.3 \text{ kΩ} )</td>
<td>16</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>( V_O = 1 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω} )</td>
<td></td>
<td>Data transfer 30MHz, all output ON, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω} )</td>
<td>30</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>( I_{O(LC)} )</td>
<td>Constant sink current (see Figure 10)</td>
<td>All output OFF, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω} )</td>
<td>54</td>
<td>61</td>
<td>69</td>
</tr>
<tr>
<td>( I_{Lq} )</td>
<td>Leakage output current</td>
<td>All output OFF, ( V_O = 15 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω}, \ OUT0 ) to ( OUT15 )</td>
<td></td>
<td>0.1</td>
<td>μA</td>
</tr>
<tr>
<td>( \Delta I_{O(LC0)} )</td>
<td>Constant sink current error (see Figure 10)</td>
<td>All output ON, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω}, \ OUT0 ) to ( OUT15, -20^\circ \text{C to 85^\circ C} )</td>
<td>( \pm 1% )</td>
<td>( \pm 4% )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All output ON, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω}, \ OUT0 ) to ( OUT15(1) )</td>
<td>( \pm 1% )</td>
<td>( \pm 8% )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All output ON, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 320 \text{ Ω}, \ OUT0 ) to ( OUT15, -20^\circ \text{C to 85^\circ C} )</td>
<td>( \pm 1% )</td>
<td>( \pm 6% )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>All output ON, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 320 \text{ Ω}, \ V_{CC} = 4.5 \text{ V to 5.5 V}, \ OUT0 ) to ( OUT15(1) )</td>
<td>( \pm 1% )</td>
<td>( \pm 8% )</td>
<td></td>
</tr>
<tr>
<td>( \Delta I_{O(LC1)} )</td>
<td>Constant sink current error (see Figure 10)</td>
<td>Device to device, Averaged current from ( OUT0 ) to ( OUT15, \ R_{\text{REF}} = 1920 \text{ Ω} ) ((20 \text{ mA})(2))</td>
<td>( -2% )</td>
<td>( +0.4% )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Device to device, Averaged current from ( OUT0 ) to ( OUT15(2) )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta I_{O(LC2)} )</td>
<td>Constant sink current error (see Figure 10)</td>
<td>Device to device, Averaged current from ( OUT0 ) to ( OUT15, \ R_{\text{REF}} = 480 \text{ Ω} ) ((80 \text{ mA})(2))</td>
<td>( -2.7% )</td>
<td>( +2% )</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Device to device, Averaged current from ( OUT0 ) to ( OUT15(2) )</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \Delta I_{O(LC3)} )</td>
<td>Line regulation (see Figure 10)</td>
<td>All output ON, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω}, \ OUT0 ) to ( OUT15, V_{CC} = 3 \text{ V to 5.5 V}(3) )</td>
<td>( \pm 1% )</td>
<td>( \pm 4% )</td>
<td>%/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All output ON, ( V_O = 1 \text{ V}, \ R_{\text{REF}} = 320 \text{ Ω}, \ OUT0 ) to ( OUT15(4) )</td>
<td>( \pm 1% )</td>
<td>( \pm 5.5% )</td>
<td>%/V</td>
</tr>
<tr>
<td>( \Delta I_{O(LC4)} )</td>
<td>Load regulation (see Figure 10)</td>
<td>All output ON, ( V_O = 1 \text{ V} ) to ( 3 \text{ V}, \ R_{\text{REF}} = 640 \text{ Ω}, \ OUT0 ) to ( OUT15(4) )</td>
<td>( \pm 2% )</td>
<td>( \pm 6% )</td>
<td>%/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All output ON, ( V_O = 1 \text{ V} ) to ( 3 \text{ V}, \ R_{\text{REF}} = 320 \text{ Ω}, \ OUT0 ) to ( OUT15(4) )</td>
<td>( \pm 2% )</td>
<td>( \pm 8% )</td>
<td>%/V</td>
</tr>
<tr>
<td>( T_{(TEF)} )</td>
<td>Thermal error flag threshold</td>
<td>Junction temperature((5))</td>
<td>150</td>
<td>170</td>
<td>°C</td>
</tr>
<tr>
<td>( V_{(LED)} )</td>
<td>LED open detection threshold</td>
<td></td>
<td>0.3</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>( V_{(IREF)} )</td>
<td>Reference voltage output</td>
<td>( R_{\text{REF}} = 640 \text{ Ω} )</td>
<td>1.20</td>
<td>1.24</td>
<td>1.28</td>
</tr>
</tbody>
</table>

(1) The deviation of each output from the average of OUT0-15 constant current. It is calculated by Equation 1 in Test Parameter Equations.
(2) The deviation of average of OUT1-15 constant current from the ideal constant-current value. It is calculated by Equation 2 in Test Parameter Equations. The ideal current is calculated by Equation 3 in Test Parameter Equations.
(3) The line regulation is calculated by Equation 4 in Test Parameter Equations.
(4) The load regulation is calculated by Equation 5 in Test Parameter Equations.
(5) Not tested. Specified by design.
### 6.6 Switching Characteristics

$V_{CC} = 3V$ to 5.5V, $T_A = -40°C$ to 85°C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{r0}$</td>
<td>Rise time SOUT</td>
<td>16</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{r1}$</td>
<td>Rise time OUTn, $V_{CC} = 5V, T_A = 60°C, DCn = 3 Fh</td>
<td>10</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f0}$</td>
<td>Fall time SOUT</td>
<td>16</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{f1}$</td>
<td>Fall time OUTn, $V_{CC} = 5V, T_A = 60°C, DCn = 3 Fh</td>
<td>10</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd0}$</td>
<td>Propagation delay time SCLK to SOUT (see Figure 11)</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd1}$</td>
<td>Propagation delay time BLANK to OUT0</td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd2}$</td>
<td>Propagation delay time OUTn to XERR (see Figure 11)</td>
<td>1000</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd3}$</td>
<td>Propagation delay time GSCLK to OUT0 (see Figure 11)</td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd4}$</td>
<td>Propagation delay time XLAT to OUT (dot correction) (see Figure 11)</td>
<td>60</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd5}$</td>
<td>Propagation delay time DCPRG to OUT0 (see Figure 11)</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_d$</td>
<td>Output delay time OUTn to OUT(n+1) (see Figure 11)</td>
<td>20</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{on-err}$</td>
<td>Output on-time error $t_{on} = T_{gsclk}$ (see Figure 11), GSn = 01h, GSCLK = 11 MHz</td>
<td>10</td>
<td>–50</td>
<td>–90</td>
<td>ns</td>
</tr>
</tbody>
</table>
6.7 Typical Characteristics

Figure 1. Reference Resistor vs Output Current

Figure 2. Power Dissipation Rate vs Free-Air Temperature

Figure 3. Output Current vs Output Voltage

Figure 4. Output Current vs Output Voltage

Figure 5. Constant Output Current, $\Delta I_{OLC}$ vs Ambient Temperature

Figure 6. Constant Output Current, $\Delta I_{OLC}$ vs Output Current
Typical Characteristics (continued)

Figure 7. Output Current vs DOT Correction Linearity (ABS Value)

Figure 8. Output Current vs DOT Correction Linearity (ABS Value)
7 Parameter Measurement Information

Resistor values are equivalent resistances, and they are not tested.

![Equivalent Circuits Diagram](image-url)

Figure 9. Input and Output Equivalent Circuits
### Parameter Measurement Information (continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Circuit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{01} \cdot t_{f0} \cdot t_{pd0} )</td>
<td><a href="#">Circuit Diagram</a></td>
</tr>
<tr>
<td>( t_{r1} \cdot t_{f1} \cdot t_{pd1} \cdot t_{pd2} \cdot t_{pd3} \cdot t_{pd4} \cdot t_{pd5} \cdot t_{d} )</td>
<td><a href="#">Circuit Diagram</a></td>
</tr>
</tbody>
</table>

**Circuit Diagrams**

- **SOUT Testpoint** with \( C_L = 15\text{pF} \)
- **OUTn Testpoint** with \( C_L = 15\text{pF} \)
- **V\(_{(\text{IREF})}\)** Testpoint with \( R_{(\text{IREF})} = 640\Omega \)
- **V\(_{\text{CC}}\)** with \( 470k\Omega \)

**Figure 10. Parameter Measurement Circuits**

### 7.1 Test Parameter Equations

1. \[
   \Delta(\%) = \frac{I_{\text{OUTn}} - I_{\text{OUTavg} \_0-15}}{I_{\text{OUTavg} \_0-15}} \times 100
\]

2. \[
   \Delta(\%) = \frac{I_{\text{OUTavg}} - I_{\text{OUT(IDEAL)}}}{I_{\text{OUT(IDEAL)}}} \times 100
\]

3. \[
   I_{\text{OUT(IDEAL)}} = 31.5 \times \left( \frac{1.24V}{R_{\text{IREF}}} \right)
\]

4. \[
   \Delta(\% / V) = \frac{I_{\text{OUTn}} \text{ at } V_{\text{CC}} = 5.5V - I_{\text{OUTn}} \text{ at } V_{\text{CC}} = 3.0V}{I_{\text{OUTn}} \text{ at } V_{\text{CC}} = 3.0V} \times 100 \times 2.5
\]

5. \[
   \Delta(\% / V) = \frac{I_{\text{OUTn}} \text{ at } V_{\text{OUTn}} = 3.0V - I_{\text{OUTn}} \text{ at } V_{\text{OUTn}} = 1.0V}{I_{\text{OUTn}} \text{ at } V_{\text{OUTn}} = 1.0V} \times 100 \times 2.0
\]
8 Detailed Description

8.1 Overview
The TLC5940 is a 16-channel constant current sink driver. Each channel has an individually-adjustable, 4096-step, pulse width modulation (PWM), grayscale (GS) brightness control, and a 64-step dot correction brightness control. GS data and DC data are input via a serial interface port. The dot correction data is stored in an integrated EEPROM. The TLC5940 has a 120-mA current capability. The maximum current value of all channels is determined by an external resistor. The TLC5940 has a LED open detection (LOD) function that indicates a broken or disconnected LED at an output terminal and a thermal error flag (TEF) indicates an overtemperature condition.

8.2 Functional Block Diagram

8.3 Feature Description

8.3.1 Serial Interface
The TLC5940 has a flexible serial interface, which can be connected to microcontrollers or digital signal processors in various ways. Only 3 pins are needed to input data into the device. The rising edge of SCLK signal shifts the data from the SIN pin to the internal register. After all data is clocked in, a high-level pulse of XLAT signal latches the serial data to the internal registers. The internal registers are level-triggered latches of XLAT signal. All data are clocked in with the MSB first. The length of serial data is 96 bit or 192 bit, depending on the programming mode. Grayscale data and dot correction data can be entered during a grayscale cycle. Although new grayscale data can be clocked in during a grayscale cycle, the XLAT signal should only latch the grayscale data at the end of the grayscale cycle. Latching in new grayscale data immediately overwrites the existing grayscale data. Figure 11 shows the timing chart. More than two TLC5940s can be connected in series by connecting an SOUT pin from one device to the SIN pin of the next device. An example of cascading two TLC5940s is shown in Figure 12 and the timing chart is shown in Figure 13. The SOUT pin can also be connected to the controller to receive status information from TLC5940 as shown in Figure 22.
Feature Description (continued)

Figure 11. Serial Data Input Timing Chart

Figure 12. Cascading Two TLC5940 Devices
8.3.2 Error Information Output

The open-drain output XERR is used to report both of the TLC5940 error flags, TEF and LOD. During normal operating conditions, the internal transistor connected to the XERR pin is turned off. The voltage on XERR is pulled up to \( V_{CC} \) through an external pullup resistor. If TEF or LOD is detected, the internal transistor is turned on, and XERR is pulled to GND. Since XERR is an open-drain output, multiple ICs can be OR'ed together and pulled up to \( V_{CC} \) with a single pullup resistor. This reduces the number of signals needed to report a system error (see Figure 22).

To differentiate LOD and TEF signal from XERR pin, LOD can be masked out with BLANK = HIGH.

### Table 1. XERR Truth Table

<table>
<thead>
<tr>
<th>ERROR CONDITION</th>
<th>ERROR INFORMATION</th>
<th>SIGNALS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEMPERATURE</td>
<td>OUTn VOLTAGE</td>
<td>TEF</td>
</tr>
<tr>
<td>( T_J &lt; T_{(TEF)} )</td>
<td>Don't Care</td>
<td>L</td>
</tr>
<tr>
<td>( T_J = T_{(TEF)} )</td>
<td>Don't Care</td>
<td>H</td>
</tr>
<tr>
<td>( T_J &lt; T_{(TEF)} )</td>
<td>OUTn &gt; ( V_{(LED)} )</td>
<td>L</td>
</tr>
<tr>
<td>( T_J &gt; T_{(TEF)} )</td>
<td>OUTn &lt; ( V_{(LED)} )</td>
<td>L</td>
</tr>
<tr>
<td>( T_J &gt; T_{(TEF)} )</td>
<td>OUTn &gt; ( V_{(LED)} )</td>
<td>H</td>
</tr>
</tbody>
</table>
8.3.3 TEF: Thermal Error Flag
The TLC5940 provides a temperature error flag (TEF) circuit to indicate an overtemperature condition of the IC. If the junction temperature exceeds the threshold temperature (160°C typical), TEF becomes H and XERR pin goes to low level. When the junction temperature becomes lower than the threshold temperature, TEF becomes L and XERR pin becomes high impedance. TEF status can also be read out from the TLC5940 status register.

8.3.4 LOD: LED Open Detection
The TLC5940 has an LED-open detector that detects broken or disconnected LEDs. The LED open detector pulls the XERR pin to GND when an open LED is detected. XERR and the corresponding error bit in the Status Information Data is only active under the following open-LED conditions.
1. OUTn is on and the time tpd2 (1 μs typical) has passed.
2. The voltage of OUTn is < 0.3 V (typical)

The LOD status of each output can be also read out from the SOUT pin. See STATUS INFORMATION OUTPUT section for details. The LOD error bits are latched into the Status Information Data when XLAT returns to a low after a high. Therefore, the XLAT pin must be pulsed high then low while XERR is active in order to latch the LOD error into the Status Information Data for subsequent reading via the serial shift register.

8.3.5 Delay Between Outputs
The TLC5940 has graduated delay circuits between outputs. These circuits can be found in the constant current driver block of the device (see the functional block diagram). The fixed-delay time is 20 ns (typical), OUT0 has no delay, OUT1 has a 20-ns delay, and OUT2 has a 40-ns delay, etc. The maximum delay is 300 ns from OUT0 to OUT15. The delay works during switch on and switch off of each output channel. These delays prevent large inrush currents which reduces the bypass capacitors when the outputs turn on.

8.3.6 Output Enable
All OUTn channels of the TLC5940 can be switched off with one signal. When BLANK is set high, all OUTn channels are disabled, regardless of logic operations of the device. The grayscale counter is also reset. When BLANK is set low, all OUTn channels work under normal conditions. If BLANK goes low and then back high again in less than 300 ns, all outputs programmed to turn on still turn on for either the programmed number of grayscale clocks, or the length of time that the BLANK signal was low, which ever is lower. For example, if all outputs are programmed to turn on for 1 ms, but the BLANK signal is only low for 200 ns, all outputs still turn on for 200 ns, even though some outputs are turning on after the BLANK signal has already gone high.

<table>
<thead>
<tr>
<th>Table 2. BLANK Signal Truth Table</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BLANK</strong></td>
</tr>
<tr>
<td>LOW</td>
</tr>
<tr>
<td>HIGH</td>
</tr>
</tbody>
</table>
8.3.7 Setting Maximum Channel Current

The maximum output current per channel is programmed by a single resistor, $R_{\text{(IREF)}}$, which is placed between IREF pin and GND pin. The voltage on IREF is set by an internal band gap $V_{\text{(IREF)}}$ with a typical value of 1.24 V. The maximum channel current is equivalent to the current flowing through $R_{\text{(IREF)}}$ multiplied by a factor of 31.5. The maximum output current per channel can be calculated by Equation 6.

$$I_{\text{max}} = \frac{V_{\text{(IREF)}}}{R_{\text{(IREF)}}} \times 31.5$$

where

- $V_{\text{(IREF)}} = 1.24$ V
- $R_{\text{(IREF)}} = \text{User-selected external resistor.}$

$I_{\text{max}}$ must be set between 5 mA and 120 mA. The output current may be unstable if $I_{\text{max}}$ is set lower than 5 mA. Output currents lower than 5 mA can be achieved by setting $I_{\text{max}}$ to 5 mA or higher and then using dot correction.

Figure 1 shows the maximum output current $I_{\text{O}}$ versus $R_{\text{(IREF)}}$. $R_{\text{(IREF)}}$ is the value of the resistor between IREF terminal to GND, and $I_{\text{O}}$ is the constant output current of OUT0 to OUT15. A variable power supply may be connected to the IREF pin through a resistor to change the maximum output current per channel. The maximum output current per channel is 31.5 times the current flowing out of the IREF pin.
8.4 Device Functional Modes

8.4.1 Operating Modes

The TLC5940 has operating modes depending on the signals DCPRG and VPRG. Table 3 shows the available operating modes. The TPS5940 GS operating mode (see Figure 11) and shift register values are not defined after power up. One solution to solve this is to set dot correction data after TLS5940 power-up and switch back to GS PWM mode. The other solution is to overflow the input shift register with 193 bits of dummy data and latch it while TLS540 is in GS PWM mode. The values in the input shift register, DC register and GS register are unknown just after power on. The DC and GS register values should be properly stored through the serial interface before starting the operation.

### Table 3. TLC5940 Operating Modes Truth Table

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>INPUT SHIFT REGISTER</th>
<th>MODE</th>
<th>DC VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCPRG</td>
<td>VPRG</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>GND</td>
<td>192 bit</td>
<td>Grayscale PWM Mode</td>
</tr>
<tr>
<td>H</td>
<td>VCC</td>
<td>96 bit</td>
<td>Dot Correction Data Input Mode</td>
</tr>
<tr>
<td>L</td>
<td>V(VPRG)</td>
<td>X</td>
<td>EEPROM Programming Mode</td>
</tr>
<tr>
<td>H</td>
<td></td>
<td></td>
<td>Write dc register value to EEPROM. (Default data: 3Fh)</td>
</tr>
</tbody>
</table>

8.4.2 Setting DOT Correction

The TLC5940 has the capability to fine adjust the output current of each channel OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LEDs connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0% to 100% of the maximum output current $I_{\text{max}}$. Dot correction for all channels must be entered at the same time. Equation 7 determines the output current for each output $n$.

$$I_{\text{OUT}n} = I_{\text{max}} \times \frac{\text{DCn}}{63}$$

where
- $I_{\text{max}}$ = the maximum programmable output current for each output.
- DCn = the programmed dot correction value for output n (DCn = 0 to 63).
- $n = 0$ to $15$

Equation 7 determines the output current for each output $n$.

Figure 14 shows the dot correction data packet format which consists of 6 bits x 16 channel, total 96 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc. The DC 15.5 in Figure 14 stands for the 5$^{\text{th}}$ most significant bit for output 15.

![Figure 14. Dot Correction Data Packet Format](image)

When VPRG is set to VCC, the TLC5940 enters the dot correction data input mode. The length of input shift register becomes 96 bits. After all serial data are shifted in, the TLC5940 writes the data in the input shift register to DC register when XLAT is high, and holds the data in the DC register when XLAT is low. The DC register is a level triggered latch of XLAT signal. Since XLAT is a level-triggered signal, SCLK and SIN must not be changed while XLAT is high. After XLAT goes low, data in the DC register is latched and does not change. BLANK signal does not need to be high to latch in new data. XLAT has setup time (tsu1) and hold time (th1) to SCLK as shown in Figure 15.
The TLC5940 also has an EEPROM to store dot correction data. To store data from the dot correction register to EEPROM, DCPRG is set to high after applying VPRG to the VPRG pin. Figure 16 shows the EEPROM programming timings. The EEPROM has a default value of all 1s.
8.4.3 Setting Grayscale

The TLC5940 can adjust the brightness of each channel OUTn using a PWM control scheme. The use of 12 bits per channel results in 4096 different brightness steps, respective 0% to 100% brightness. Equation 8 determines the brightness level for each output n.

\[
\text{Brightness in } \% = \frac{G_{Sn}}{4095} \times 100
\]

where

- \(G_{Sn}\) = the programmed grayscale value for output n (\(G_{Sn} = 0 \text{ to } 4095\))
- \(n = 0 \text{ to } 15\)
- Grayscale data for all OUTn

Equation 8 determines the brightness level for each output n.

Figure 18 shows the grayscale data packet format which consists of 12 bits x 16 channels, totaling 192 bits. The format is Big-Endian format. This means that the MSB is transmitted first, followed by the MSB-1, etc.

When VPRG is set to GND, the TLC5940 enters the grayscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, a rising edge of the XLAT signal latches the data into the grayscale register (see Figure 11). New grayscale data immediately becomes valid at the rising edge of the XLAT signal; therefore, new grayscale data should be latched at the end of a grayscale cycle when BLANK is high. The first GS data input cycle after dot correction requires an additional SCLK pulse after the XLAT signal to complete the grayscale update cycle. All GS data in the input shift register is replaced with status information data (SID) after updated the grayscale register.

8.4.4 Status Information Output

The TLC5940 does have a status information register, which can be accessed in grayscale mode (VPRG=GND). After the XLAT signal latches the data into the GS register the input shift register data will be replaced with status information data (SID) of the device (see Figure 18). LOD, TEF, and dot correction EEPROM data (DCPRG=LOW) or dot correction register data (DCPRG=HIGH) can be read out at SOUT pin. The status information data packet is 192 bits wide. Bits 0-15 contain the LOD status of each channel. Bit 16 contains the TEF status. If DCPRG is low, bits 24-119 contain the data of the dot-correction EEPROM. If DCPRG is high, bits 24-119 contain the data of the dot-correction register. The remaining bits are reserved. The complete status information data packet is shown in Figure 19.

SOUT outputs the MSB of the SID at the same time the SID are stored in the SID register, as shown Figure 20. The next SCLK pulse, which will be the clock for receiving the SMB of the next grayscale data, transmits MSB-1 of SID. If output voltage is < 0.3 V (typical) when the output sink current turns on, LOD status flag becomes active. The LOD status flag is an internal signal that pulls XERR pin down to low when the LOD status flag becomes active. The delay time, \(t_{pd2}\) (1 \(\mu s\) maximum), is from the time of turning on the output sink current to the time LOD status flag becomes valid. The timing for each channel's LOD status to become valid is shifted by the 30-ns (maximum) channel-to-channel turn-on time. After the first GSCLK goes high, OUT0 LOD status is valid; \(t_{pd3} + t_{pd2} = 60 \text{ ns} + 1 \mu s\). OUT1 LOD status is valid; \(t_{pd3} + t_d + t_{pd2} = 60 \text{ ns} + 30 \text{ ns} + 1 \mu s = 1.09 \mu s\). OUT2 LOD status is valid; \(t_{pd3} + 2t_d + t_{pd2} = 1.12 \mu s\), and so on. It takes 1.51 \(\mu s\) maximum (\(t_{pd3} + 15t_d + t_{pd2}\)) from the first GSCLK rising edge until all LOD become valid; \(tsuLOD\) must be > 1.51 \(\mu s\) (see Figure 20) to ensure that all LOD data are valid.
8.4.5 Grayscale PWM Operation

The grayscale PWM cycle starts with the falling edge of BLANK. The first GSCLK pulse after BLANK goes low increases the grayscale counter by one and switches on all OUTn with grayscale value not zero. Each following rising edge of GSCLK increases the grayscale counter by one. The TLC5940 compares the grayscale value of each output OUTn with the grayscale counter value. All OUTn with grayscale values equal to the counter values are switched off. A BLANK=H signal after 4096 GSCLK pulses resets the grayscale counter to zero and completes the grayscale PWM cycle (see Figure 21). When the counter reaches a count of FFFh, the counter stops counting and all outputs turn off. Pulling BLANK high before the counter reaches FFFh immediately resets the counter to zero.
Figure 21. Grayscale PWM Cycle Timing Chart
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is a 16-channel, constant sink current, LED driver. This device can be connected in series to drive many LED lamps with only a few controller ports. Output current control data, dot correction data and PWM control data can be written from the SIN input terminal.

9.2 Typical Application

![Diagram of cascading devices]

Figure 22. Cascading Devices

9.2.1 Design Requirements

For this design example, use the input parameters shown in Table 4.

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC input voltage range</td>
<td>3.0 V to 5.5 V</td>
</tr>
<tr>
<td>LED lamp (V_{LED}) input voltage range</td>
<td>&gt;Maximum LED forward voltage (V_{F}) + IC knee voltage</td>
</tr>
<tr>
<td>SIN, SCLK, XLAT, GSCLK, and BLANK voltage range</td>
<td>Low level = GND, High level = VCC</td>
</tr>
</tbody>
</table>

Table 4. Design Parameters
9.2.2 Detailed Design Procedure

9.2.2.1 Serial Data Transfer Rate

Figure 22 shows a cascading connection of \( n \) TLC5940 devices connected to a controller, building a basic module of an LED display system. The maximum number of cascading TLC5940 devices depends on the application system and is in the range of 40 devices. Equation 9 calculates the minimum frequency needed:

\[
\begin{align*}
\text{f}_{\text{GSCLK}} &= 4096 \times \text{f}_{\text{update}} \\
\text{f}_{\text{SCLK}} &= 193 \times \text{f}_{\text{update}} \times n
\end{align*}
\]

where

- \( \text{f}_{\text{GSCLK}} \): minimum frequency needed for GSCLK
- \( \text{f}_{\text{SCLK}} \): minimum frequency needed for SCLK and SIN
- \( \text{f}_{\text{update}} \): update rate of whole cascading system
- \( n \): number cascaded of TLC5940 device

9.2.2.2 Grayscale (GS) Data

There are a total of 16 sets of 12-bit GS data for the PWM control of each output. Select the GS data of each LED lamp and write the GS data to the register following the signal timing.

9.2.3 Application Curve

![Figure 23. Output Waveform with Different Grayscale PWM Data](image)

Figure 23. Output Waveform with Different Grayscale PWM Data
10 Power Supply Recommendations

The $V_{CC}$ power supply voltage should be decoupled by placing a 0.1uF ceramic capacitor close to VCC pin and GND plane. Depending on panel size, several electrolytic capacitors must be placed on board equally distributed to get a well regulated LED supply voltage ($V_{LED}$). $V_{LED}$ voltage ripple should be less than 5% of its nominal value. Furthermore, the $V_{LED}$ should be set to the voltage calculated by equation:

$$V_{LED} > V_f + 0.4V \text{ (10mA constant current example) where } V_f = \text{maximum forward voltage of all LEDs.}$$

11 Layout

11.1 Layout Guidelines

1. Place the decoupling capacitor near the VCC pin and GND plane.
2. Place the current programming resistor $R_{iref}$ close to IREF pin and IREFGND pin.
3. Route the GND pattern as widely as possible for large GND currents.
4. Routing wire between the LED cathode side and the device OUTn pin should be as short and straight as possible to reduce wire inductance.
5. When several ICs are chained, symmetric placements are recommended.

11.2 Layout Example

![Layout Recommendation Diagram](image-url)
11.3 Power Dissipation Calculation

The device power dissipation must be below the power dissipation rating of the device package to ensure correct operation. **Equation 10** calculates the power dissipation of device.

\[
P_D = \left( V_{CC} \times I_{CC} \right) + \left( V_{OUT} \times I_{MAX} \times \frac{DC_n}{63} \times d_{PWM} \times N \right)
\]

where
- \( V_{CC} \): device supply voltage
- \( I_{CC} \): device supply current
- \( V_{OUT} \): TLC5940 OUTn voltage when driving LED current
- \( I_{MAX} \): LED current adjusted by R(REF) Resistor
- \( DC_n \): maximum dot correction value for OUTn
- \( N \): number of OUTn driving LED at the same time
- \( d_{PWM} \): duty cycle defined by BLANK pin or GS PWM value

(10)
12 Device and Documentation Support

12.1 Community Resources
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks
E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary
**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PINS</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC5940PWP</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>TLC5940</td>
<td>Samples</td>
</tr>
<tr>
<td>TLC5940PWPG4</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>TLC5940</td>
<td>Samples</td>
</tr>
<tr>
<td>TLC5940PWPR</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>TLC5940</td>
<td>Samples</td>
</tr>
<tr>
<td>TLC5940PWPRG4</td>
<td>ACTIVE</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>TLC5940</td>
<td>Samples</td>
</tr>
<tr>
<td>TLC5940RHB</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RHB</td>
<td>32</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>TLC5940</td>
<td>Samples</td>
</tr>
<tr>
<td>TLC5940RHB RG4</td>
<td>ACTIVE</td>
<td>VQFN</td>
<td>RHB</td>
<td>32</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 85</td>
<td>TLC5940</td>
<td>Samples</td>
</tr>
</tbody>
</table>

---

(1) The marketing status values are defined as follows:

- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp. -** The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLC5940:**

- **Enhanced Product: TLC5940-EP**

**NOTE:** Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications
## TAPE AND REEL INFORMATION

![Reel Dimensions Diagram](image1)

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Q1: Pocket Quandrants
- Q2: Sprocket Holes
- Q3: User Direction of Feed

*All dimensions are nominal.

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC5940PWPR</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>6.9</td>
<td>10.2</td>
<td>1.8</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>TLC5940RHBR</td>
<td>VQFN</td>
<td>RHB</td>
<td>32</td>
<td>3000</td>
<td>330.0</td>
<td>12.4</td>
<td>5.3</td>
<td>5.3</td>
<td>1.5</td>
<td>8.0</td>
<td>12.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC5940PWPR</td>
<td>HTSSOP</td>
<td>PWP</td>
<td>28</td>
<td>2000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
<tr>
<td>TLC5940RHB</td>
<td>VQFN</td>
<td>RHB</td>
<td>32</td>
<td>3000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Exposed Thermal Pad Dimensions

NOTE: A. All linear dimensions are in millimeters

Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments
Example Board Layout
Via pattern and copper pad size may vary depending on layout constraints

Increasing copper area will enhance thermal performance (See Note D)

Stencil Openings
Based on a stencil thickness of .127mm (.005inch)
Reference table below for other solder stencil thicknesses

Solder Mask Over Copper

Example Solder Mask Defined Pad (See Note C, D)

Example Non Soldermask Defined Pad

Center Power Pad Solder Stencil Opening

<table>
<thead>
<tr>
<th>Stencil Thickness</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1mm</td>
<td>6.6</td>
<td>2.6</td>
</tr>
<tr>
<td>0.127mm</td>
<td>6.17</td>
<td>2.4</td>
</tr>
<tr>
<td>0.152mm</td>
<td>5.8</td>
<td>2.3</td>
</tr>
<tr>
<td>0.178mm</td>
<td>5.6</td>
<td>2.2</td>
</tr>
</tbody>
</table>

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.  
B. This drawing is subject to change without notice.  
C. QFN (Quad Flatpack No-Lead) Package configuration.  
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.  
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.  
F. Falls within JEDEC MO-220.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions](image)

Bottom View

**Exposed Thermal Pad Dimensions**

**NOTE:** A. All linear dimensions are in millimeters
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.
IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated