TLV3502-Q1, 4.5-ns Rail-to-Rail High-Speed Comparator

1 Features
- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: −40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- High Speed: 4.5 ns
- Rail-To-Rail I/O
- Supply Voltage: 2.7 V To 5.5 V
- Push-Pull CMOS Output Stage
- Shutdown
- Micro Package: SOT23-8
- Low Supply Current: 3.2 mA

2 Applications
- HEV/EV, Powertrain, and Passive Safety:
  - Threshold Detector
  - Zero-Crossing Detector
  - Window Comparator
  - Oscillator

3 Description
The TLV3502-Q1 push-pull output comparators feature a fast 4.5-ns propagation delay and operation from 2.7 V to 5.5 V. Beyond-the-rails input common-mode range makes the device an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic.

A microsize package provides options for portable and space-restricted applications. The TLV3502-Q1 device is available in the SOT23-8 (DCN) package.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV3502-Q1</td>
<td>SOT-23 (8)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the datasheet.

![Propagation Delay vs Overdrive Voltage](image)
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# 4 Revision History

Changes from Original (February 2010) to Revision A

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</thead>
<tbody>
<tr>
<td>1</td>
</tr>
<tr>
<td>4</td>
</tr>
</tbody>
</table>

- Deleted references to the TLV3501 device and changed the TLV3502 device name to TLV3502-Q1 ................................ 1
- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 4
5 Pin Configuration and Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>NAME</th>
<th>TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+IN A</td>
<td>I</td>
<td>Non inverting input, channel A</td>
</tr>
<tr>
<td>2</td>
<td>−IN A</td>
<td>I</td>
<td>Inverting input, channel A</td>
</tr>
<tr>
<td>3</td>
<td>+IN B</td>
<td>I</td>
<td>Non inverting input, channel B</td>
</tr>
<tr>
<td>4</td>
<td>−IN B</td>
<td>I</td>
<td>Inverting input, channel B</td>
</tr>
<tr>
<td>5</td>
<td>V−</td>
<td>Supply</td>
<td>Negative (lowest) power supply</td>
</tr>
<tr>
<td>6</td>
<td>OUT B</td>
<td>O</td>
<td>Output, channel B</td>
</tr>
<tr>
<td>7</td>
<td>OUT A</td>
<td>O</td>
<td>Output, channel A</td>
</tr>
<tr>
<td>8</td>
<td>V+</td>
<td>Supply</td>
<td>Positive (highest) power supply</td>
</tr>
</tbody>
</table>
# 6 Specifications

## 6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Signal input terminal voltage</td>
<td>(V−) − 0.3</td>
<td>(V+) + 0.3</td>
</tr>
<tr>
<td>Signal input terminal current</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Output short-circuit current</td>
<td>74</td>
<td>mA</td>
</tr>
<tr>
<td>Thermal impedance, junction to free air</td>
<td>200</td>
<td>°C/W</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>−40</td>
<td>125</td>
</tr>
<tr>
<td>Junction temperature</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature, T_{stg}</td>
<td>−65</td>
<td>150</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10mA or less.

(3) Short circuit to ground, one comparator per package

## 6.2 ESD Ratings

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>±750</td>
<td>V</td>
</tr>
<tr>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{S}</td>
<td>Supply voltage</td>
<td>2.2</td>
<td>2.7</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Low-level input voltage, shutdown (comparator is enabled)</td>
<td>(V+) - 1.7</td>
<td>V</td>
</tr>
<tr>
<td>V_{IH}</td>
<td>High-level input voltage, shutdown (comparator is disabled)</td>
<td>(V+) - 0.9</td>
<td>V</td>
</tr>
<tr>
<td>T_{A}</td>
<td>Operating temperature</td>
<td>−40</td>
<td>125</td>
</tr>
</tbody>
</table>

(1) When the shutdown pin is within 0.9 V of the most positive supply, the part is disabled. When it is more than 1.7 V below the most positive supply, the part is enabled.

## 6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TLV3502-Q1</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{JA}</td>
<td>Junction-to-ambient thermal resistance</td>
</tr>
<tr>
<td>R_{JC(top)}</td>
<td>Junction-to-case (top) thermal resistance</td>
</tr>
<tr>
<td>R_{JB}</td>
<td>Junction-to-board thermal resistance</td>
</tr>
<tr>
<td>ψ_{JT}</td>
<td>Junction-to-top characterization parameter</td>
</tr>
<tr>
<td>ψ_{JB}</td>
<td>Junction-to-board characterization parameter</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
6.5 Electrical Characteristics

\( T_A = 25°C \) and \( V_S = 2.7 \) V to 5.5 V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input offset voltage (^{(1)})</td>
<td>±1</td>
<td>±6.5</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( \Delta V_{OS}/\Delta T )</td>
<td>Offset voltage vs temperature</td>
<td>±5</td>
<td></td>
<td>µV/°C</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Offset voltage vs power supply</td>
<td>100</td>
<td>400</td>
<td>µV/V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input hysteresis</td>
<td>6</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input bias current</td>
<td>±2</td>
<td>±10</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input offset current (^{(2)})</td>
<td>±2</td>
<td>±10</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>( V_{CM} )</td>
<td>Common-mode voltage range</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-mode rejection</td>
<td>57</td>
<td>70</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Common-mode input impedance</td>
<td>( 10^{13} )</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>High-level voltage output from rail</td>
<td>±1 mA</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Low-level voltage output from rail</td>
<td>±1 mA</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>Input bias current of shutdown pin</td>
<td>2</td>
<td></td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>( I_Q )</td>
<td>Quiescent current per comparator</td>
<td>3.2</td>
<td>5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>( I_{QSD} )</td>
<td>Quiescent current in shutdown</td>
<td>2</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) \( V_{OS} \) is defined as the average of the positive and the negative switching thresholds.
\(^{(2)}\) The difference between \( I_{B+} \) and \( I_{B-} \).

6.6 Switching Characteristics

\( T_A = 25°C \) and \( V_S = 2.7 \) V to 5.5 V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{pd} )</td>
<td>Propagation delay time (^{(1)})(^{(2)})</td>
<td>4.5</td>
<td>6.4</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( \Delta t_{(SKEW)} )</td>
<td>Propagation delay skew (^{(3)})</td>
<td>0.5</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( f_{MAX} )</td>
<td>Maximum toggle frequency</td>
<td>80</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( t_R )</td>
<td>Rise time (^{(4)})</td>
<td>1.5</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_F )</td>
<td>Fall time (^{(4)})</td>
<td>1.5</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{OFF} )</td>
<td>Shutdown turn-off time</td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{ON} )</td>
<td>Shutdown turn-on time</td>
<td>100</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) Propagation delay cannot be accurately measured with low overdrive on automatic test equipment. This parameter is ensured by characterization at 100-mV overdrive.
\(^{(2)}\) Not production tested
\(^{(3)}\) The difference between the propagation delay going high and the propagation delay going low.
\(^{(4)}\) Measured between 10% of \( V_S \) and 90% of \( V_S \).
6.7 Typical Characteristics

\( T_A = 25^\circ\text{C}, V_S = 5 \text{ V}, \) Input Overdrive = 100 mV (unless otherwise noted)

![Figure 1. Output Response for Various Overdrive Voltages (rising)](image1)

![Figure 2. Output Response for Various Overdrive Voltages (falling)](image2)

![Figure 3. Propagation Delay vs Temperature](image3)

![Figure 4. Propagation Delay vs Temperature](image4)

![Figure 5. Propagation Delay vs Capacitive Load](image5)

![Figure 6. Propagation Delay vs Capacitive Load](image6)
Typical Characteristics (continued)

\( T_A = 25^\circ C, V_S = 5 \text{ V}, \text{ Input Overdrive} = 100 \text{ mV} \) (unless otherwise noted)

![Figure 7. Propagation Delay vs Supply Voltage](image1)

![Figure 8. Wake-Up Delay vs Temperature](image2)

![Figure 9. Response to 50-MHz Sine Wave](image3)

![Figure 10. Response to 100 MHz Sine Wave](image4)

![Figure 11. Quiescent Current vs Supply Voltage](image5)

![Figure 12. Quiescent Current vs Temperature](image6)
Typical Characteristics (continued)

$T_A = 25^\circ\text{C}, V_S = 5\ \text{V}, \text{Input Overdrive} = 100\ \text{mV} \ (\text{unless otherwise noted})$

![Figure 13. Quiescent Current vs Shutdown Voltage](image1)

![Figure 14. Quiescent Current vs Frequency](image2)
7 Detailed Description

7.1 Overview

The TLV3502-Q1 push-pull output comparator features a fast 4.5-ns propagation delay and operation from 2.7 V to 5.5 V. Beyond-the-rails input common-mode range makes it an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic.

7.2 Functional Block Diagram

![Functional Block Diagram](image)

7.3 Feature Description

The TLV3502-Q1 device feature fast 4.5-ns propagation delay with a push-pull output. The device operates from 2.7 V to 5.5 V. It has beyond-the-rails input common-mode range and rail-to-rail output directly drives either CMOS or TTL logic.

7.3.1 Input Over-Voltage Protection

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300 mV. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the comparator, as shown in Figure 15.

![Figure 15. Input Current Protection for Voltages Exceeding the Supply Voltage](image)
Feature Description (continued)

7.3.2 Relaxation Oscillator

The TLV350x can easily be configured as a simple and inexpensive relaxation oscillator. In Figure 16, the R2 network sets the trip threshold at 1/3 and 2/3 of the supply. Since this is a high-speed circuit, the resistor values are rather low to minimize the effect of parasitic capacitance. The positive input alternates between 1/3 of V+ and 2/3 of V+ depending on whether the output is low or high. The time to charge (or discharge) is 0.69R1C. Therefore, the period is 1.38R1C. For 62 pF and 1 kΩ as shown in Figure 16, the output is calculated to be 10.9 MHz. An implementation of this circuit oscillated at 9.6 MHz. Parasitic capacitance and component tolerances explain the difference between theory and actual performance.

Figure 16. Relaxation Oscillator

7.3.3 High-Speed Window Comparator

A window comparator circuit is used to determine when a signal is between two voltages. The TLV3502-Q1 device can readily be used to create a high-speed window comparator. \( V_{HI} \) is the upper voltage threshold, and \( V_{LO} \) is the lower voltage threshold. When \( V_{IN} \) is between these two thresholds, the output in Figure 17 is high. Figure 18 shows a simple means of obtaining an active low output. Note that the reference levels are connected differently between Figure 17 and Figure 18. The operating voltage range of either circuit is 2.7 V to 5.5 V.
Feature Description (continued)

Figure 17. Window Comparator—Active High

Figure 18. Window Comparator—Active Low

7.4 Device Functional Modes

This device has no special operating modes outside of the normally powered dual comparator function.
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TLV3502-Q1 device features high-speed response and includes 6 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2 V beyond the power-supply rails.

8.2 Typical Application
In this example, we will show how can we add external hysteresis to TLV3502-Q1 device to achieve greater noise immunity. First, let’s understand when and why external hysteresis may be required.

The TLV3502-Q1 device has a robust performance when used with a good layout. However, comparator inputs have little noise immunity within the range of specified offset voltage (±5 mV). For slow moving or noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. In such applications, the 6mV of internal hysteresis of the TLV3502-Q1 device might not be sufficient. In cases where greater noise immunity is desired, external hysteresis may be added by connecting a small amount of feedback to the positive input.

8.2.1 Design Requirements
Figure 19 shows a typical topology used to introduce 25 mV of additional hysteresis, for a total of 31-mV hysteresis when operating from a single 5-V supply.

8.2.2 Detailed Design Procedure
Use Equation 1 to calculate the total hysteresis.

\[ V_{HYST} = \frac{(V+) \times R1}{R1 + R2} + 6 \text{ mV} \]  

(1)

\( V_{HYST} \) sets the value of the transition voltage required to switch the comparator output by enlarging the threshold region, thereby reducing sensitivity to noise.
Typical Application (continued)

8.2.3 Application Curve

9 Power Supply Recommendations

The TLV3505-Q1 comparator is specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to 125°C. The device continues to function below this range, but performance is not specified.

Place bypass capacitors close to the power supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the Layout Guidelines section.

10 Layout

10.1 Layout Guidelines

- For any high-speed comparator or amplifier, proper design and printed circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.
- Minimizing resistance from the signal source to the comparator input is necessary in order to minimize the propagation delay of the complete circuit. The source resistance along with input and stray capacitance creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency signals. The input capacitance of the TLV3502-Q1 device along with stray capacitance from an input pin to ground results in several picofarads of capacitance.
- The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2-μF tantalum capacitor do not need to be as close to the device as the 0.1-μF capacitor, and may be shared with other devices. The 2.2-μF capacitor buffers the power-supply line against ripple, and the 0.1-μF capacitor provides a charge for the comparator during high frequency switching.
- In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane is often used to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias should be spaced randomly.
- Figure 21 shows an evaluation layout for the TLV3502-Q1 SOT23-8 package. The device is shown with SMA connectors bringing signals on and off the board. RT1, RT2, RT3 and RT4 are termination resistors for + IN A, + IN B, –IN A, and –IN B respectively. C1 and C2 are power-supply bypass capacitors. Place the 0.1-μF capacitor closest to the comparator. The ground plane is not shown, but the pads that the resistors and capacitors connect to are shown. Figure 22 shows a schematic of this circuit.
10.2 Layout Example

Figure 21. TLV3502-Q1 Sample Layout
Figure 22. Schematic for Figure 21
11 Device and Documentation Support

11.1 Trademarks
All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV3502AQDCNQR1</td>
<td>ACTIVE</td>
<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>3000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>3502</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV3502-Q1:

- Catalog: TLV3502

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0  (mm)</th>
<th>B0  (mm)</th>
<th>K0  (mm)</th>
<th>P1  (mm)</th>
<th>W   (mm)</th>
<th>Pin1 Quadrant</th>
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<tbody>
<tr>
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<td>SOT-23</td>
<td>DCN</td>
<td>8</td>
<td>3000</td>
<td>179.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
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*All dimensions are nominal.*
### TAPE AND REEL BOX DIMENSIONS

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<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
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<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLV3502AQCNRQ1</td>
<td>SOT-23</td>
<td>DCN</td>
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<td>3000</td>
<td>195.0</td>
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</tbody>
</table>

*All dimensions are nominal*
MECHANICAL DATA

DCN (R—PDSO—G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO-178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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