TLV6741 10-MHz, Low broadband noise, RRO, operational amplifier

1 Features
- Low Broadband Noise: 3.7 nV/√Hz
- Gain Bandwidth: 10 MHz
- Low Input Bias Current: 10 pA
- Low Offset Voltage: 0.15 mV
- Rail-to-Rail Output
- Unity-Gain Stable
- Low IO: 890 µA/ch
- Microsize Package: SC70 (DCK)
- Wide Supply Range: 2.25 V to 5.5 V
- ESD Protection: ±3000 V (HBM)

2 Applications
- Portable Hard Disk Drives
- Wearable Consumer Applications
- Photodiode Amplifiers
- ADC Input-Driver Amplifiers
- Precision Sensor Front-Ends
- Wireless Metering
- Handheld Test Equipment
- Test and Measurement Equipment
- Active Filters

3 Description
The TLV6741 operational amplifier (op amp) is a general-purpose CMOS op amp that provides low noise of 3.7 nV/√Hz and a wide bandwidth of 10 MHz. The low noise and wide bandwidth make the TLV6741 device attractive for a variety of precision applications that require a good balance between cost and performance. Additionally, the input bias current of the TLV6741 supports applications with high source impedance.

The robust design of the TLV6741 provides ease-of-use to the circuit designer due to its unity-gain stability, integrated RFI/EMI rejection filter, no phase reversal in overdrive conditions and high electrostatic discharge (ESD) protection (1-kV HBM). Additionally, the resistive open-loop output impedance makes it easy to stabilize with much higher capacitive loads.

This op amp is optimized for low-voltage operation as low as 2.25 V (±1.125 V) and up to 5.5 V (±2.75 V), and is specified over the temperature range of –40°C to +125°C.

The single-channel TLV6741 is available in a small-size SC70-5 package.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
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<tbody>
<tr>
<td>TLV6741</td>
<td>SC70 (5)</td>
<td>2.00 mm × 1.25 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2017) to Revision D

• Changed Operating temperature from 125 to 150 in Absolute Maximum Ratings ......................................................... 4
• Added Junction temperature spec to Absolute Maximum Ratings ......................................................................................... 4

Changes from Revision B (October 2017) to Revision C

• Changed total supply voltage total from 5 V to 5.5 V in Electrical Characteristics condition statement ................................. 5
• Added test conditions to input offset voltage parameter in Electrical Characteristics table .................................................... 5
• Deleted "V_S = 2.25 V to 5.5 V " test conditions for common-mode rejection ratio parameter in Electrical Characteristics .... 5
• Changed typical input current noise density value from 2 fA/√Hz to 26 fA/√Hz ................................................................. 5
• Added Table 1 ....................................................................................................................................................................... 6
• Deleted "C_L = 0" test condition from Figure 25 and Figure 26, Figure 27 and Figure 28 .................................................... 11
• Changed voltage step from 5 V to 2 V in Figure 32 ............................................................................................................ 12

Changes from Revision A (September 2017) to Revision B

• Changed Human-body model (HBM) value from: ±1000 to: ±3000 and Charged-device model (CDM) value from: ±250 to: 1000 ........................................................................ 4

Changes from Original (June 2017) to Revision A

• Changed device document status from: Advance Information to: Production Data ....................................................... 1
5 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>+IN</td>
<td>I</td>
<td>Noninverting input</td>
</tr>
<tr>
<td>–IN</td>
<td>I</td>
<td>Inverting input</td>
</tr>
<tr>
<td>OUT</td>
<td>O</td>
<td>Output</td>
</tr>
<tr>
<td>V+</td>
<td>—</td>
<td>Positive (highest) supply</td>
</tr>
<tr>
<td>V–</td>
<td>—</td>
<td>Negative (lowest) supply</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range, unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, V_S</td>
<td>6</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>Signal input terminals Voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-mode (V–) – 0.5 (V+) + 0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential (V+) – (V–) + 0.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>-10</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Output short-circuit</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Continuous</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Operating temperature, T_A</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction temperature, T_J</td>
<td></td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, T_stg</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001</td>
<td>±3000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101</td>
<td>±1000</td>
<td></td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_S</td>
<td>2.25 (±1.125)</td>
<td>5.5 (±2.75)</td>
<td>V</td>
</tr>
<tr>
<td>T_A</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>TLV6741</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{UA}</td>
<td>240.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-ambient thermal resistance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{UC(top)}</td>
<td>151.7</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-case (top) thermal resistance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{UB}</td>
<td>64</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board thermal resistance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>\psi_{JT}</td>
<td>34.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-top characterization parameter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>\psi_{JB}</td>
<td>63.3</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction-to-board characterization parameter</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Submit Documentation Feedback
## 6.5 Electrical Characteristics

at $T_A = 25 \, ^\circ C$, $V_S$ (total supply voltage) = $(V+) - (V-) = 5.5 \, V$, $R_L = 10 \, k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Voltage VOS</td>
<td>$V_S = 5 , V$</td>
<td>±0.15</td>
<td>±1</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>dVOS/dT</td>
<td>$T_A = -40^\circ C$ to $+125^\circ C$</td>
<td>±0.35</td>
<td>μV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>$V_S = 2.25 , V$ to $5.5 , V$, $V_{CM} = (V-)</td>
<td>104</td>
<td>130</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range VCM</td>
<td>$(V-) &lt; V_{CM} &lt; (V+) - 1.2 , V$</td>
<td>95</td>
<td>120</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_B$</td>
<td>±10</td>
<td>pA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>±10</td>
<td>pA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise</td>
<td>$I = 0.1 , Hz$ to $10 , Hz$</td>
<td>1.5</td>
<td>µV_{PP}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$e_n$</td>
<td>$I = 10 , kHz$</td>
<td>3.7</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_n$</td>
<td>$I = 1 , kHz$</td>
<td>5</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>$C_{in}$</td>
<td>Differential</td>
<td>6</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Common-mode</td>
<td>6</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Open-Loop Gain</td>
<td>$A_{OL}$</td>
<td>$(V-) + 0.04 , V &lt; V_O &lt; (V+) - 0.04 , V$, $R_L = 10 , k\Omega$</td>
<td>125</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$(V-) + 0.15 , V &lt; V_O &lt; (V+) - 0.15 , V$, $R_L = 2 , k\Omega$</td>
<td>110</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Frequency Response</td>
<td>$GBW$</td>
<td>$G = 1$</td>
<td>10</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Phase margin</td>
<td>$G = 1$, $R_L = 10 , k\Omega$</td>
<td>55</td>
<td>Degrees</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SR Slew rate</td>
<td>$G = 1$</td>
<td>4.75</td>
<td>V/µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_s$ Settling time</td>
<td>To 0.1%, 2-V step , $G = 1$</td>
<td>0.65</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>To 0.01%, 2-V step , $G = 1$</td>
<td>1.2</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Overload recovery time</td>
<td>$V_{IN} \times Gain &gt; V_S$</td>
<td>0.2</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td>THD+N Total harmonic distortion + noise</td>
<td>$V_O = 1 , V_{RMS}$, $V_{CM} = 2.5 , V$, $G = 1$, $f = 1 , kHz$, $R_L = 10 , k\Omega$, $V_S = 5.5 , V$</td>
<td>0.00035%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td>$V_O$ Voltage output swing from supply rails</td>
<td>$R_L = 10 , k\Omega$</td>
<td>8</td>
<td>10</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>ZO Open-loop output impedance</td>
<td>$I = 10 , MHz$</td>
<td>160</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Power Supply</td>
<td>$I_Q$ Quiescent current per amplifier</td>
<td>$I_Q = 0 , mA$</td>
<td>890</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_Q = 0 , mA$, $T_A = -40^\circ C$ to $+125^\circ C$</td>
<td>1.1</td>
<td>mA</td>
<td></td>
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</tbody>
</table>
Table 1. Table of Graphs

<table>
<thead>
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<th>FIGURE</th>
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<td>Figure 1</td>
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<td>Offset Voltage Drift Distribution</td>
<td>Figure 2</td>
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<tr>
<td>Offset Voltage vs Temperature</td>
<td>Figure 3</td>
</tr>
<tr>
<td>Offset Voltage vs Common-Mode Voltage</td>
<td>Figure 4</td>
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<tr>
<td>Offset Voltage vs Common-Mode Voltage</td>
<td>Figure 5</td>
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<tr>
<td>Offset Voltage vs Power Supply</td>
<td>Figure 6</td>
</tr>
<tr>
<td>I&lt;sub&gt;B&lt;/sub&gt; and I&lt;sub&gt;OS&lt;/sub&gt; vs Common-Mode Voltage</td>
<td>Figure 7</td>
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<tr>
<td>I&lt;sub&gt;B&lt;/sub&gt; and I&lt;sub&gt;OS&lt;/sub&gt; vs Temperature</td>
<td>Figure 8</td>
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<td>Figure 9</td>
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<td>Closed-Loop Gain vs Frequency</td>
<td>Figure 10</td>
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<td>V&lt;sub&gt;0&lt;/sub&gt; vs I Sourcing and Sinking</td>
<td>Figure 11</td>
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<tr>
<td>CMRR vs Temperature</td>
<td>Figure 14</td>
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<td>Figure 15</td>
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<td>Input Voltage Noise Spectral Density vs Frequency</td>
<td>Figure 16</td>
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<tr>
<td>THD + Noise vs Frequency</td>
<td>Figure 17</td>
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<tr>
<td>THD + Noise vs Frequency</td>
<td>Figure 18</td>
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<tr>
<td>THD + Noise vs Amplitude</td>
<td>Figure 19</td>
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<tr>
<td>Quiescent Current vs Supply Voltage</td>
<td>Figure 20</td>
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<td>Quiescent Current vs Temperature</td>
<td>Figure 21</td>
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<tr>
<td>Open-Loop Gain vs Temperature</td>
<td>Figure 22</td>
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<td>Open-Loop Gain vs Output Voltage</td>
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<td>Small-Signal Overshoot vs Load Capacitance</td>
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<td>Figure 26</td>
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<tr>
<td>Small-Signal Overshoot vs Load Capacitance</td>
<td>Figure 27</td>
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<tr>
<td>Small-Signal Overshoot vs Load Capacitance</td>
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<tr>
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<td>Figure 29</td>
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<td>Small-Signal Step Response</td>
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<td>Figure 33</td>
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<td>Figure 34</td>
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<td>Short-Circuit Current vs Temperature</td>
<td>Figure 35</td>
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<td>Maximum Output Voltage vs Frequency</td>
<td>Figure 36</td>
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<tr>
<td>Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR&lt;sup&gt;+&lt;/sup&gt;) vs Frequency</td>
<td>Figure 37</td>
</tr>
<tr>
<td>Phase Margin vs Capacitive Load</td>
<td>Figure 38</td>
</tr>
</tbody>
</table>
6.6 Typical Characteristics

at $T_A = 25^\circ C$, $V_S = 5.5 \, V$, $R_L = 10 \, k\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

Figure 1. Offset Voltage Production Distribution

Figure 2. Offset Voltage Drift Distribution

Figure 3. Offset Voltage vs Temperature

Figure 4. Offset Voltage vs Common-Mode Voltage

Figure 5. Offset Voltage vs Common-Mode Voltage

Figure 6. Offset Voltage vs Power Supply
Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = 5.5 \text{ V}$, $R_L = 10 \text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

---

**Figure 7. $I_B$ and $I_{OS}$ vs Common-Mode Voltage**

**Figure 8. $I_B$ and $I_{OS}$ vs Temperature**

**Figure 9. Open-Loop Gain and Phase vs Frequency**

**Figure 10. Closed-Loop Gain vs Frequency**

**Figure 11. $V_O$ vs $I$ Sourcing and Sinking**

**Figure 12. PSRR vs Frequency (Referred to Input)**
Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = 5.5$ V, $R_L = 10$ k$\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

Figure 13. CMRR vs Frequency (Referred to Input)

Figure 14. CMRR vs Temperature

Figure 15. 0.1-Hz to 10-Hz Flicker Noise

Figure 16. Input Voltage Noise Spectral Density vs Frequency

Figure 17. THD + N vs Frequency

Figure 18. THD + N vs Frequency
Typical Characteristics (continued)

at $T_A = 25^\circ$C, $V_S = 5.5$ V, $R_L = 10$ kΩ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

![Graph of THD + N vs Amplitude](image1)

$V_S = 5.5$ V, $V_{CM} = 2.5$ V, $BW = 80$ kHz, $V_{OUT} = 0.5$ Vrms

![Graph of Quiescent Current vs Supply Voltage](image2)

$A_{VDD} = 5.5$ V, $V_{ICM} = V_{OCM} = 2.75$ V

![Graph of Open-Loop Gain vs Temperature](image3)

$A_{VDD} = 5.5$ V, $V_{CM} = V_{OCM} = 2.75$ V

![Graph of Open-Loop Output Impedance vs Frequency](image4)
Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\ V$, $R_L = 10\ \Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$, unless otherwise noted.

![Graph 1](image1)

![Graph 2](image2)

![Graph 3](image3)

![Graph 4](image4)

![Graph 5](image5)

![Graph 6](image6)

![Graph 7](image7)

![Graph 8](image8)

Figure 25. Small-Signal Overshoot vs Load Capacitance

Figure 26. Small-Signal Overshoot vs Load Capacitance

Figure 27. Small-Signal Overshoot vs Load Capacitance

Figure 28. Small-Signal Overshoot vs Load Capacitance

Figure 29. No Phase Reversal

Figure 30. Overload Recovery
Typical Characteristics (continued)

at $T_A = 25^\circ C$, $V_S = 5.5\ V$, $R_L = 10\ k\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

$V_S = 1.8\ V$, $V_{ICM} = 0.9\ V$, $V_{OCM} = 0.9\ V$
$C_L = 30\ pF$, Gain = 1, $V_{IN} = 100\-mVpp$

Figure 31. Small-Signal Step Response

$V_S = 5.5\ V$, $V_{OCM} = 5.5\ V$, $C_L = 10\ pF$
$V_{ICM} = 2.75\ V$, Gain = 1, 2-V step

Figure 32. Large Signal Step Response

$V_S = 5.5\ V$, $V_{ICM} = 2.75\ V$, $V_{OCM} = 2.75\ V$
$C_L = 0$, Gain = 1, 5-V step

Figure 33. Large Signal Settling Time (Positive)

$V_S = 5.5\ V$, $V_{ICM} = 2.75\ V$, $V_{OCM} = 2.75\ V$
$C_L = 0$, Gain = 1, 5-V step

Figure 34. Large Signal Settling Time (Negative)

$V_S = 1.8\ V$, $V_S = 5.5\ V$

Figure 35. Short-Circuit Current vs Temperature

Figure 36. Maximum Output Voltage vs Frequency
Typical Characteristics (continued)

at \( T_A = 25^\circ C, V_S = 5.5 \text{ V}, R_L = 10 \text{ k}\Omega \) connected to \( V_S/2, V_{CM} = V_S/2, \) and \( V_{OUT} = V_S/2, \) unless otherwise noted.

![Figure 37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency](image1)

![Figure 38. Phase Margin vs Capacitive Load](image2)
7 Detailed Description

7.1 Overview
The TLV6741 is a ultra low-noise, rail-to-rail output operational amplifier. The device operates from a supply voltage of 2.25 V to 5.5 V, is unity-gain stable, and is suitable for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail and allows the TLV6741 op amp to be used in most single-supply applications. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications, and makes it suitable for many audio applications and also driving sampling analog-to-digital converters (ADCs).

7.2 Functional Block Diagram

![Functional Block Diagram](image)

7.3 Feature Description

7.3.1 THD+ Noise performance
TLV6741 operational amplifier has excellent distortion characteristics. THD + Noise is below 0.00035% (G = +1, \( V_O = 1 \) \( V_{RMS} \), \( V_{CM} = 2.5 \) V, \( V_S = 5.5 \) V) throughout the audio frequency range, 20 Hz to 20 kHz, with a 10-kΩ load. The broadband noise of the TLV6741 of 3.7 nV/√Hz is extremely low for a 10 MHz general purpose amplifier.

7.3.2 Operating Voltage
The TLV6741 operational amplifier is fully specified and assured for operation from 2.25 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Power-supply pins should be bypassed with 0.1-µF ceramic capacitors.

7.3.3 Rail-to-Rail Output
Designed as a low-power, low-voltage operational amplifier, the TLV6741 delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-kΩ, the output swings to within few mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails, see Figure 11.
Feature Description (continued)

7.3.4 Input and ESD Protection
The TLV6741 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings. Figure 39 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

![Figure 39. Input Current Protection](image)

7.3.5 EMI Susceptibility and Input Filtering
Op amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from its nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The TLV6741 operational amplifier family incorporate an internal input low-pass filter that reduces the op amps response to EMI. Both common-mode and differential mode filtering are provided by this filter.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. Detailed information can also be found in the application report, EMI Rejection Ratio of Operational Amplifiers, available for download from www.ti.com.

7.4 Device Functional Modes
The TLV6741 has a single functional mode. These devices are powered on as long as the power-supply voltage is between 2.25 V (±1.125 V) and 5.5 V (±2.75 V).
8 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV6741 features 10-MHz bandwidth and 4.75-V/µs slew rate with only 890-µA of supply current per channel, providing good ac performance at very-low-power consumption. DC applications are well served with a very-low input noise voltage of 3.7 nV / √Hz at 10 kHz, low input bias current, and a typical input offset voltage of 0.15 mV.

8.2 Single-Supply Electret Microphone Pre-Amplifier With Speech Filter

Electret microphones are commonly used in portable electronics because of their small size, low cost, and relatively good signal-to-noise ratio (SNR). The small package size, low operating voltage and excellent AC performance of the TLV6741 make it an excellent choice for preamplifier circuits for electret microphones. The circuit shown in Figure 40 is a single-supply preamplifier circuit for electret microphones.

![Microphone pre-amplifier diagram](attachment:image.png)

Figure 40. Microphone pre-amplifier

8.2.1 Design Requirements

The design requirements are as follows:
- Supply voltage: +3 V
- Input: 7.93 mV<sub>RMS</sub> (0.63 Pa with a –38 dB SPL microphone)
- Output: 1 V<sub>RMS</sub>
- Bandwidth: 300 Hz to 3 kHz

8.2.2 Detailed Design Procedure

The transfer function defining the relationship between \( V_{OUT} \) and the AC input signal is shown in Equation 1:
Single-Supply Electret Microphone Pre-Amplifier With Speech Filter (continued)

\[
V_{OUT} = V_{IN, AC} \times \left(1 + \frac{R_F}{R_G}\right)
\]  

(1)

The required gain can be calculated based on the expected input signal level and desired output level as shown in Equation 2

\[
G_{OPA} = \frac{V_{OUT}}{V_{IN, AC}} = \frac{1V_{RMS}}{7.93mV_{RMS}} = 126 \frac{V}{V}
\]  

(2)

Select a standard 10-kΩ feedback resistor and calculate \(R_G\).

\[
R_G = \frac{R_F}{G_{OPA} - 1} = \frac{10k\Omega}{126 \frac{V}{V} - 1} = 80\Omega \rightarrow 78.7\Omega \text{ (closest standard value)}
\]  

(3)

To minimize the attenuation in the desired passband from 300 Hz to 3 kHz, set the upper (\(f_H\)) and lower (\(f_L\)) cutoff frequencies outside of the desired bandwidth as:

\(f_L = 200\, \text{Hz}\)  

(4)

and

\(f_H = 5\, \text{kHz}\)  

(5)

Select \(C_G\) to set the \(f_L\) cutoff frequency using Equation 6

\[
C_G = \frac{1}{2 \times \pi \times R_G \times f_L} = \frac{1}{2 \times \pi \times 78.7\Omega \times 200\, \text{Hz}} = 10.11\, \mu F \rightarrow 10\, \mu F
\]  

(6)

Select \(C_F\) to set the \(f_H\) cutoff frequency using Equation 7

\[
C_F = \frac{1}{2 \times \pi \times R_F \times f_H} = \frac{1}{2 \times \pi \times 10k\Omega \times 5\, \text{kHz}} = 3.18nF \rightarrow 3.3nF \text{ (Standard Value)}
\]  

(7)

The input signal cutoff frequency should be set low enough such that low-frequency sound waves still pass through. Therefore select \(C_{IN}\) to achieve a 30-Hz cutoff frequency (\(f_{IN}\)) using Equation 8.

\[
C_{IN} = \frac{1}{2 \times \pi \times (R_1 \parallel R_2) \times f_{IN}} = \frac{1}{2 \times \pi \times 100k\Omega \times 30\, \text{Hz}} = 53nF \rightarrow 68nF \text{ (Standard Value)}
\]  

(8)

The measured transfer function for the microphone preamplifier circuit is shown in Figure 41 and the measured THD+N performance of the microphone preamplifier circuit is shown in Figure 42.
Single-Supply Electret Microphone Pre-Amplifier With Speech Filter (continued)

8.2.3 Application Curves

![Figure 41. Gain vs Frequency](image1)

![Figure 42. THD + N vs RMS Output Voltage](image2)
9 Power Supply Recommendations

The TLV6741 device is specified for operation from 2.25 V to 5.5 V (±1.125 V to ±2.75 V); many specifications apply from –40°C to +125°C. Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

**CAUTION**

Supply voltages larger than 7 V can permanently damage the device (see the Absolute Maximum Ratings).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the Layout Guidelines section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see Circuit Board Layout Techniques.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Figure 43.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
10.2 Layout Example

Figure 43. Operational Amplifier Board Layout for Noninverting Configuration

Figure 44. Schematic Used for Layout Example
11 Device and Documentation Support

11.1 Device Support

11.1.1 DFN Package

NOTE
The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V–).

11.1.2 Documentation Support

11.1.2.1 Related Documentation

For related documentation see the following:
• QFN/SON PCB Attachment.
• Quad Flatpack No-Lead Logic Packages.
• Circuit Board Layout Techniques.
• EMI Rejection Ratio of Operational Amplifiers.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support TI's Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>-40 to 125</td>
<td>18E</td>
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<td>-40 to 125</td>
<td>18E</td>
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</tr>
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</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

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<th>Device</th>
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<th>B0  (mm)</th>
<th>K0  (mm)</th>
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<td>8.0</td>
<td>Q3</td>
</tr>
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</table>

*All dimensions are nominal.*

---

**Notes:**
- **Device:** The device name.
- **Package Type:** The type of packaging.
- **Package Drawing:** The drawing number for the package.
- **Pins:** The number of pins on the device.
- **SPQ:** The quantity of parts per reel.
- **Reel Diameter:** The diameter of the reel (mm).
- **Reel Width W1:** The width of the reel (mm).
- **A0:** Dimension designed to accommodate the component width (mm).
- **B0:** Dimension designed to accommodate the component length (mm).
- **K0:** Dimension designed to accommodate the component thickness (mm).
- **P1:** Pitch between successive cavity centers (mm).
- **W:** Overall width of the carrier tape (mm).

---

**Diagram Notes:**
- **Reel Diameter:** The diameter of the reel.
- **Reel Width W1:** The width of the reel.
- **Cavity:** The area within the reel that holds the components.
- **A0:** The dimension designed to accommodate the component width.
- **B0:** The dimension designed to accommodate the component length.
- **K0:** The dimension designed to accommodate the component thickness.
- **W:** The overall width of the carrier tape.
- **P1:** The pitch between successive cavity centers.
- **Pocket Quadrants:** The areas within the reel where the components are located.
- **Sprocket Holes:** The holes used to attach the carrier tape to the reel.
- **User Direction of Feed:** The direction in which the tape is fed from the reel.

---

**Images:**
- **Reel Dimensions Diagram:** A diagram showing the dimensions of a reel.
- **Tape Dimensions:** A diagram showing the dimensions of the tape.
- **Quadrant Assignments:** A diagram showing the quadrant assignments for tape orientation.

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**Source:**
- **www.ti.com 16-Jan-2019**

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**Pack Materials-Page 1**
<table>
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</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7528 for other stencil recommendations.
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