Tiva™ TM4C123GH6PZ Microcontroller

DATA SHEET
Copyright

Copyright © 2007-2014 Texas Instruments Incorporated. Tiva and TivaWare are trademarks of Texas Instruments Incorporated. ARM and Thumb are registered trademarks and Cortex is a trademark of ARM Limited. All other trademarks are the property of others.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Texas Instruments Incorporated
108 Wild Basin, Suite 350
Austin, TX 78746
http://www.ti.com/tm4c
# Table of Contents

Revision History ......................................................................................................................................... 38

About This Document ............................................................................................................................... 42

Audience .................................................................................................................................................. 42

About This Manual ................................................................................................................................. 42

Related Documents ............................................................................................................................... 42

Documentation Conventions .................................................................................................................. 43

1 Architectural Overview ....................................................................................................................... 45

1.1 Tiva™ C Series Overview ............................................................................................................... 45

1.2 TM4C123GH6PZ Microcontroller Overview ............................................................................... 46

1.3 TM4C123GH6PZ Microcontroller Features .................................................................................. 49

1.3.1 ARM Cortex-M4F Processor Core ............................................................................................. 49

1.3.2 On-Chip Memory ....................................................................................................................... 51

1.3.3 Serial Communications Peripherals .......................................................................................... 53

1.3.4 System Integration ..................................................................................................................... 57

1.3.5 Advanced Motion Control .......................................................................................................... 63

1.3.6 Analog ......................................................................................................................................... 65

1.3.7 JTAG and ARM Serial Wire Debug ............................................................................................ 67

1.3.8 Packaging and Temperature ........................................................................................................ 67

1.4 TM4C123GH6PZ Microcontroller Hardware Details ..................................................................... 68

1.5 Kits ................................................................................................................................................ 68

1.6 Support Information ......................................................................................................................... 68

2 The Cortex-M4F Processor .................................................................................................................. 69

2.1 Block Diagram ................................................................................................................................. 70

2.2 Overview ......................................................................................................................................... 71

2.2.1 System-Level Interface .............................................................................................................. 71

2.2.2 Integrated Configurable Debug ................................................................................................. 71

2.2.3 Trace Port Interface Unit (TPIU) ............................................................................................... 72

2.2.4 Cortex-M4F System Component Details .................................................................................. 72

2.3 Programming Model ....................................................................................................................... 73

2.3.1 Processor Mode and Privilege Levels for Software Execution .................................................. 73

2.3.2 Stacks ......................................................................................................................................... 74

2.3.3 Register Map ............................................................................................................................... 74

2.3.4 Register Descriptions ................................................................................................................ 76

2.3.5 Exceptions and Interrupts .......................................................................................................... 92

2.3.6 Data Types ................................................................................................................................ 92

2.4 Memory Model ............................................................................................................................... 92

2.4.1 Memory Regions, Types and Attributes ................................................................................... 95

2.4.2 Memory System Ordering of Memory Accesses ....................................................................... 95

2.4.3 Behavior of Memory Accesses .................................................................................................. 95

2.4.4 Software Ordering of Memory Accesses .................................................................................... 96

2.4.5 Bit-Banding ............................................................................................................................... 97

2.4.6 Data Storage ............................................................................................................................. 99

2.4.7 Synchronization Primitives ...................................................................................................... 100

2.5 Exception Model ............................................................................................................................. 101

2.5.1 Exception States ....................................................................................................................... 102
Table of Contents

16  Inter-Integrated Circuit (I²C) Interface ................................................................. 1018
16.1 Block Diagram ........................................................................................................ 1019
16.2 Signal Description ................................................................................................... 1019
16.3 Functional Description ............................................................................................ 1020
16.3.1 I²C Bus Functional Overview ............................................................................. 1020
16.3.2 Available Speed Modes ....................................................................................... 1025
16.3.3 Interrupts .............................................................................................................. 1027
16.3.4 Loopback Operation ............................................................................................ 1028
16.3.5 Command Sequence Flow Charts ........................................................................ 1028
16.4 Initialization and Configuration ............................................................................ 1036
16.4.1 Configure the I²C Module to Transmit a Single Byte as a Master ....................... 1036
16.4.2 Configure the I²C Master to High Speed Mode .................................................... 1037
16.5 Register Map ............................................................................................................ 1038
16.6 Register Descriptions (I²C Master) ....................................................................... 1039
16.7 Register Descriptions (I²C Slave) ......................................................................... 1056
16.8 Register Descriptions (I²C Status and Control) .................................................... 1066

17  Controller Area Network (CAN) Module .............................................................. 1069
17.1 Block Diagram ........................................................................................................ 1070
17.2 Signal Description ................................................................................................... 1070
17.3 Functional Description ............................................................................................ 1071
17.3.1 Initialization ......................................................................................................... 1072
17.3.2 Operation .............................................................................................................. 1073
17.3.3 Transmitting Message Objects .......................................................................... 1074
17.3.4 Configuring a Transmit Message Object ............................................................. 1074
17.3.5 Updating a Transmit Message Object .................................................................. 1075
17.3.6 Accepting Received Message Objects ................................................................. 1076
17.3.7 Receiving a Data Frame ....................................................................................... 1076
17.3.8 Receiving a Remote Frame .................................................................................. 1076
17.3.9 Receive/Transmit Priority ..................................................................................... 1077
17.3.10 Configuring a Receive Message Object ............................................................... 1077
17.3.11 Handling of Received Message Objects .............................................................. 1078
17.3.12 Handling of Interrupts ....................................................................................... 1080
17.3.13 Test Mode ............................................................................................................ 1081
17.3.14 Bit Timing Configuration Error Considerations .................................................. 1083
17.3.15 Bit Time and Bit Rate ......................................................................................... 1083
17.3.16 Calculating the Bit Timing Parameters ............................................................... 1085
17.4 Register Map ............................................................................................................ 1088
17.5 CAN Register Descriptions ..................................................................................... 1089
## Table of Contents

24 Electrical Characteristics

- 24.1 Maximum Ratings
- 24.2 Operating Characteristics
- 24.3 Recommended Operating Conditions
- 24.4 Load Conditions
- 24.5 JTAG and Boundary Scan
- 24.6 Power and Brown-Out
- 24.6.1 VDDA Levels
- 24.6.2 VDD Levels
- 24.6.3 VDDC Levels
- 24.6.4 VDD Glitches
- 24.6.5 VDD Droop Response
- 24.7 Reset
- 24.8 On-Chip Low Drop-Out (LDO) Regulator
- 24.9 Clocks
- 24.9.1 PLL Specifications
- 24.9.2 PIOSC Specifications
- 24.9.3 Low-Frequency Internal Oscillator (LFIOSC) Specifications
- 24.9.4 Hibernation Clock Source Specifications
- 24.9.5 Main Oscillator Specifications
- 24.9.6 System Clock Specification with ADC Operation
- 24.9.7 System Clock Specification with USB Operation
- 24.10 Sleep Modes
- 24.11 Hibernation Module
- 24.12 Flash Memory and EEPROM
- 24.13 Input/Output Pin Characteristics
- 24.13.1 GPIO Module Characteristics
- 24.13.2 Types of I/O Pins and ESD Protection
- 24.14 Analog-to-Digital Converter (ADC)
- 24.15 Synchronous Serial Interface (SSI)
- 24.16 Inter-Integrated Circuit (I\(^2\)C) Interface
- 24.17 Universal Serial Bus (USB) Controller
- 24.18 Analog Comparator
- 24.19 Pulse-Width Modulator (PWM)
- 24.20 Current Consumption

A Package Information

- A.1 Orderable Devices
- A.2 Device Nomenclature
- A.3 Device Markings
- A.4 Packaging Diagram

Texas Instruments-Production Data

June 12, 2014
List of Figures

Figure 1-1. Tiva™ TM4C123GH6PZ Microcontroller High-Level Block Diagram ........................................... 48
Figure 2-1. CPU Block Diagram .................................................................................................................. 71
Figure 2-2. TPIU Block Diagram .................................................................................................................. 72
Figure 2-3. Cortex-M4F Register Set ......................................................................................................... 75
Figure 2-4. Bit-Band Mapping ...................................................................................................................... 99
Figure 2-5. Data Storage ............................................................................................................................. 100
Figure 2-6. Vector Table ............................................................................................................................. 107
Figure 2-7. Exception Stack Frame ........................................................................................................... 110
Figure 3-1. SRD Use Example .................................................................................................................... 128
Figure 3-2. FPU Register Bank .................................................................................................................. 131
Figure 4-1. JTAG Module Block Diagram .................................................................................................. 201
Figure 4-2. TPIU Block Diagram ................................................................................................................. 72
Figure 4-3. IDCODE Register Format ....................................................................................................... 210
Figure 4-4. BYPASS Register Format ....................................................................................................... 210
Figure 4-5. Boundary Scan Register Format ............................................................................................. 211
Figure 5-1. Basic RST Configuration ........................................................................................................ 215
Figure 5-2. External Circuitry to Extend Power-On Reset ......................................................................... 215
Figure 5-3. Reset Circuit Controlled by Switch .......................................................................................... 216
Figure 5-4. Power Architecture ................................................................................................................ 219
Figure 5-5. Main Clock Tree ....................................................................................................................... 222
Figure 5-6. Module Clock Selection .......................................................................................................... 229
Figure 7-1. Hibernation Module Block Diagram ........................................................................................ 504
Figure 7-2. Using a Crystal as the Hibernation Clock Source with VDD3ON ......................................... 506
Figure 7-3. Using a Dedicated Oscillator as the Hibernation Clock Source with VDD3ON ................. 507
Figure 7-4. Using a Regulator for Both VDD and VBAT ........................................................................... 508
Figure 7-5. Counter Behavior with a TRIM Value of 0x8002 ................................................................... 510
Figure 7-6. Counter Behavior with a TRIM Value of 0x7FFC ................................................................. 510
Figure 8-1. Internal Memory Block Diagram ............................................................................................ 534
Figure 8-2. EEPROM Block Diagram ..................................................................................................... 535
Figure 9-1. μDMA Block Diagram ............................................................................................................ 536
Figure 9-2. Example of Ping-Pong μDMA Transaction ............................................................................ 596
Figure 9-3. Memory Scatter-Gather, Setup and Configuration ................................................................. 604
Figure 9-4. Memory Scatter-Gather, μDMA Copy Sequence ................................................................. 605
Figure 9-5. Peripheral Scatter-Gather, Setup and Configuration ............................................................... 607
Figure 9-6. Peripheral Scatter-Gather, μDMA Copy Sequence ................................................................. 608
Figure 10-1. Digital I/O Pads ..................................................................................................................... 633
Figure 10-2. Analog/Digital I/O Pads ........................................................................................................ 664
Figure 10-3. GPIODATA Write Example ................................................................................................. 665
Figure 10-4. GPIODATA Read Example .................................................................................................. 665
Figure 11-1. GPTM Module Block Diagram ................................................................................................. 719
Figure 11-2. Reading the RTC Value .......................................................................................................... 726
Figure 11-3. Input Edge-Count Mode Example, Counting Down ............................................................ 728
Figure 11-4. 16-Bit Input Edge-Time Mode Example ................................................................................ 729
Figure 11-5. 16-Bit PWM Mode Example ................................................................................................. 731
Figure 11-6. CCP Output, GPTMnMATCHR > GPTMnILR .................................................................... 731
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>11-7.</td>
<td>CCP Output, GPTMTnMATCHR = GPTMTnLR</td>
<td>732</td>
</tr>
<tr>
<td>11-8.</td>
<td>CCP Output, GPTMTnLR &gt; GPTMTnMATCHR</td>
<td>732</td>
</tr>
<tr>
<td>11-9.</td>
<td>Timer Daisy Chain</td>
<td>733</td>
</tr>
<tr>
<td>12-1.</td>
<td>WDT Module Block Diagram</td>
<td>789</td>
</tr>
<tr>
<td>13-1.</td>
<td>Implementation of Two ADC Blocks</td>
<td>814</td>
</tr>
<tr>
<td>13-2.</td>
<td>ADC Module Block Diagram</td>
<td>815</td>
</tr>
<tr>
<td>13-3.</td>
<td>ADC Sample Phases</td>
<td>819</td>
</tr>
<tr>
<td>13-4.</td>
<td>Doubling the ADC Sample Rate</td>
<td>819</td>
</tr>
<tr>
<td>13-5.</td>
<td>Skewed Sampling</td>
<td>820</td>
</tr>
<tr>
<td>13-6.</td>
<td>Sample Averaging Example</td>
<td>821</td>
</tr>
<tr>
<td>13-7.</td>
<td>ADC Input Equivalency</td>
<td>822</td>
</tr>
<tr>
<td>13-8.</td>
<td>ADC Voltage Reference</td>
<td>823</td>
</tr>
<tr>
<td>13-9.</td>
<td>ADC Conversion Result</td>
<td>824</td>
</tr>
<tr>
<td>13-10.</td>
<td>Differential Voltage Representation</td>
<td>826</td>
</tr>
<tr>
<td>13-11.</td>
<td>Internal Temperature Sensor Character</td>
<td>827</td>
</tr>
<tr>
<td>13-12.</td>
<td>Low-Band Operation (CIC=0x0 and/or CTC=0x0)</td>
<td>829</td>
</tr>
<tr>
<td>13-13.</td>
<td>Mid-Band Operation (CIC=0x1 and/or CTC=0x1)</td>
<td>830</td>
</tr>
<tr>
<td>13-14.</td>
<td>High-Band Operation (CIC=0x3 and/or CTC=0x3)</td>
<td>831</td>
</tr>
<tr>
<td>14-1.</td>
<td>UART Module Block Diagram</td>
<td>913</td>
</tr>
<tr>
<td>14-2.</td>
<td>UART Character Frame</td>
<td>915</td>
</tr>
<tr>
<td>14-3.</td>
<td>IrDA Data Modulation</td>
<td>917</td>
</tr>
<tr>
<td>15-1.</td>
<td>SSI Module Block Diagram</td>
<td>974</td>
</tr>
<tr>
<td>15-2.</td>
<td>TI Synchronous Serial Frame Format (Single Transfer)</td>
<td>978</td>
</tr>
<tr>
<td>15-3.</td>
<td>TI Synchronous Serial Frame Format (Continuous Transfer)</td>
<td>979</td>
</tr>
<tr>
<td>15-4.</td>
<td>Freescale SPI Format (Single Transfer) with SPO=0 and SPH=0</td>
<td>980</td>
</tr>
<tr>
<td>15-5.</td>
<td>Freescale SPI Format (Continuous Transfer) with SPO=0 and SPH=0</td>
<td>980</td>
</tr>
<tr>
<td>15-6.</td>
<td>Freescale SPI Frame Format with SPO=0 and SPH=1</td>
<td>981</td>
</tr>
<tr>
<td>15-7.</td>
<td>Freescale SPI Frame Format (Single Transfer) with SPO=1 and SPH=0</td>
<td>982</td>
</tr>
<tr>
<td>15-8.</td>
<td>Freescale SPI Frame Format (Continuous Transfer) with SPO=1 and SPH=0</td>
<td>982</td>
</tr>
<tr>
<td>15-9.</td>
<td>Freescale SPI Frame Format with SPO=1 and SPH=1</td>
<td>983</td>
</tr>
<tr>
<td>15-10.</td>
<td>MICROWIRE Frame Format (Single Frame)</td>
<td>984</td>
</tr>
<tr>
<td>15-11.</td>
<td>MICROWIRE Frame Format (Continuous Transfer)</td>
<td>985</td>
</tr>
<tr>
<td>15-12.</td>
<td>MICROWIRE Frame Format, SSInFss Input Setup and Hold Requirements</td>
<td>985</td>
</tr>
<tr>
<td>16-1.</td>
<td>I2C Block Diagram</td>
<td>1019</td>
</tr>
<tr>
<td>16-2.</td>
<td>I2C Bus Configuration</td>
<td>1020</td>
</tr>
<tr>
<td>16-3.</td>
<td>START and STOP Conditions</td>
<td>1021</td>
</tr>
<tr>
<td>16-4.</td>
<td>Complete Data Transfer with a 7-Bit Address</td>
<td>1021</td>
</tr>
<tr>
<td>16-5.</td>
<td>R/S Bit in First Byte</td>
<td>1022</td>
</tr>
<tr>
<td>16-6.</td>
<td>Data Validity During Bit Transfer on the I2C Bus</td>
<td>1022</td>
</tr>
<tr>
<td>16-7.</td>
<td>High-Speed Data Format</td>
<td>1027</td>
</tr>
<tr>
<td>16-8.</td>
<td>Master Single TRANSMIT</td>
<td>1029</td>
</tr>
<tr>
<td>16-9.</td>
<td>Master Single RECEIVE</td>
<td>1030</td>
</tr>
<tr>
<td>16-10.</td>
<td>Master TRANSMIT of Multiple Data Bytes</td>
<td>1031</td>
</tr>
<tr>
<td>16-11.</td>
<td>Master RECEIVE of Multiple Data Bytes</td>
<td>1032</td>
</tr>
<tr>
<td>16-12.</td>
<td>Master RECEIVE with Repeated START after Master TRANSMIT</td>
<td>1033</td>
</tr>
<tr>
<td>16-13.</td>
<td>Master TRANSMIT with Repeated START after Master RECEIVE</td>
<td>1034</td>
</tr>
<tr>
<td>16-14.</td>
<td>Standard High Speed Mode Master Transmit</td>
<td>1035</td>
</tr>
<tr>
<td>16-15.</td>
<td>Slave Command Sequence</td>
<td>1036</td>
</tr>
</tbody>
</table>
Figure 17-1. CAN Controller Block Diagram ................................................................. 1070
Figure 17-2. CAN Data/Remote Frame ........................................................................ 1072
Figure 17-3. Message Objects in a FIFO Buffer ............................................................. 1080
Figure 17-4. CAN Bit Time ............................................................................................ 1084
Figure 18-1. USB Module Block Diagram ................................................................. 1121
Figure 19-1. Analog Comparator Module Block Diagram ........................................ 1237
Figure 19-2. Structure of Comparator Unit ................................................................. 1238
Figure 19-3. Comparator Internal Reference Structure .............................................. 1239
Figure 20-1. PWM Module Diagram ........................................................................ 1254
Figure 20-2. PWM Generator Block Diagram ........................................................... 1254
Figure 20-3. PWM Count-Down Mode ....................................................................... 1257
Figure 20-4. PWM Count-Up/Down Mode ................................................................. 1258
Figure 20-5. PWM Generation Example In Count-Up/Down Mode ............................. 1258
Figure 20-6. PWM Dead-Band Generator .................................................................. 1259
Figure 21-1. QEI Block Diagram ................................................................................ 1331
Figure 21-2. QEI Input Signal Logic .......................................................................... 1332
Figure 21-3. Quadrature Encoder and Velocity Predivider Operation ...................... 1334
Figure 22-1. 100-Pin LQFP Package Pin Diagram ...................................................... 1353
Figure 24-1. Load Conditions ..................................................................................... 1399
Figure 24-2. JTAG Test Clock Input Timing ............................................................... 1400
Figure 24-3. JTAG Test Access Port (TAP) Timing ..................................................... 1401
Figure 24-4. Power Assertions versus VDDA Levels .................................................. 1403
Figure 24-5. Power and Brown-Out Assertions versus VDD Levels ......................... 1404
Figure 24-6. POK assertion vs VDDC ......................................................................... 1405
Figure 24-7. POR-BOR0-BOR1 VDD Glitch Response .............................................. 1405
Figure 24-8. POR-BOR0-BOR1 VDD Droop Response ............................................. 1406
Figure 24-9. Digital Power-On Reset Timing ............................................................... 1407
Figure 24-10. Brown-Out Reset Timing ..................................................................... 1408
Figure 24-11. External Reset Timing (RST) ............................................................... 1408
Figure 24-12. Software Reset Timing ....................................................................... 1408
Figure 24-13. Watchdog Reset Timing ..................................................................... 1408
Figure 24-14. MOSC Failure Reset Timing ................................................................. 1409
Figure 24-15. Hibernation Module Timing ................................................................. 1420
Figure 24-16. ESD Protection on Fail-Safe Pins ......................................................... 1423
Figure 24-17. ESD Protection on Non-Fail-Safe Pins .................................................. 1424
Figure 24-18. ADC External Reference Filtering ....................................................... 1428
Figure 24-19. ADC Input Equivalency Diagram ....................................................... 1429
Figure 24-20. SSI Timing for TI Frame Format (FRF=01), Single Transfer Timing Measurement ................................................................. 1431
Figure 24-21. SSI Timing for MICROWIRE Frame Format (FRF=10), Single Transfer ................................................................. 1431
Figure 24-22. Master Mode SSI Timing for SPI Frame Format (FRF=00), with SPH=1 ................................................................. 1432
Figure 24-23. Slave Mode SSI Timing for SPI Frame Format (FRF=00), with SPH=1 ................................................................. 1432
Figure 24-24. I²C Timing ............................................................................................ 1433
Figure A-1. Key to Part Numbers .............................................................................. 1440
Figure A-2. TM4C123GH6PZ 100-Pin LQFP Package Diagram ................................ 1442
List of Tables

| Table 1. | Revision History ................................................................................................................................. 38 |
| Table 2. | Documentation Conventions ........................................................................................................... 43 |
| Table 1-1. TM4C123GH6PZ Microcontroller Features ........................................................................... 46 |
| Table 2-1. Summary of Processor Mode, Privilege Level, and Stack Use .................................................. 74 |
| Table 2-2. Processor Register Map ....................................................................................................... 75 |
| Table 2-3. PSR Register Combinations ................................................................................................. 81 |
| Table 2-4. Memory Map ....................................................................................................................... 92 |
| Table 2-5. Memory Access Behavior ................................................................................................... 96 |
| Table 2-6. SRAM Memory Bit-Banding Regions ..................................................................................... 98 |
| Table 2-7. Peripheral Memory Bit-Banding Regions ............................................................................. 98 |
| Table 2-8. Exception Types ................................................................................................................. 103 |
| Table 2-9. Interrupts .......................................................................................................................... 104 |
| Table 2-10. Exception Return Behavior ................................................................................................ 111 |
| Table 2-11. Faults .................................................................................................................................. 112 |
| Table 2-12. Fault Status and Fault Address Registers ........................................................................ 113 |
| Table 2-13. Cortex-M4F Instruction Summary ..................................................................................... 115 |
| Table 3-1. Core Peripheral Register Regions ...................................................................................... 122 |
| Table 3-2. Memory Attributes Summary .............................................................................................. 126 |
| Table 3-3. TEX, S, C, and B Bit Field Encoding .................................................................................. 128 |
| Table 3-4. Cache Policy for Memory Attribute Encoding ..................................................................... 129 |
| Table 3-5. AP Bit Field Encoding ....................................................................................................... 129 |
| Table 3-6. Memory Region Attributes for Tiva™ C Series Microcontrollers ............................................ 130 |
| Table 3-7. QNaN and SNaN Handling ................................................................................................. 133 |
| Table 3-8. Peripherals Register Map .................................................................................................. 134 |
| Table 3-9. Interrupt Priority Levels ................................................................................................... 164 |
| Table 3-10. Example SIZE Field Values ............................................................................................. 192 |
| Table 4-1. JTAG_SWD_SWO Signals (100LQFP) .................................................................................. 201 |
| Table 4-2. JTAG Port Pins State after Power-On Reset or RST assertion ............................................ 202 |
| Table 4-3. JTAG Instruction Register Commands .............................................................................. 208 |
| Table 5-1. System Control & Clocks Signals (100LQFP) ...................................................................... 212 |
| Table 5-2. Reset Sources .................................................................................................................. 213 |
| Table 5-3. Clock Source Options ....................................................................................................... 220 |
| Table 5-4. Possible System Clock Frequencies Using the SYSDIV Field ............................................. 223 |
| Table 5-5. Examples of Possible System Clock Frequencies Using the SYSDIV2 Field ......................... 223 |
| Table 5-6. Examples of Possible System Clock Frequencies with DIV400=1 .......................................... 224 |
| Table 5-7. System Control Register Map ............................................................................................. 232 |
| Table 5-8. RCC2 Fields that Override RCC Fields .............................................................................. 261 |
| Table 6-1. System Exception Register Map .......................................................................................... 495 |
| Table 7-1. Hibernate Signals (100LQFP) ............................................................................................. 504 |
| Table 7-2. Hibernation Module Clock Operation .................................................................................. 513 |
| Table 7-3. Hibernation Module Register Map ...................................................................................... 515 |
| Table 8-1. Flash Memory Protection Policy Combinations ................................................................... 539 |
| Table 8-2. User-Programmable Flash Memory Resident Registers ..................................................... 543 |
| Table 8-3. Flash Register Map ........................................................................................................... 550 |
| Table 9-1. μDMA Channel Assignments ............................................................................................... 597 |
| Table 9-2. Request Type Support ....................................................................................................... 599 |
Table 24-19. Crystal Parameters .......................................................................................... 1415
Table 24-20. Supported MOSC Crystal Frequencies .............................................................. 1416
Table 24-21. System Clock Characteristics with ADC Operation ............................................. 1417
Table 24-22. System Clock Characteristics with USB Operation ............................................. 1417
Table 24-23. Sleep Modes AC Characteristics ....................................................................... 1418
Table 24-24. Time to Wake with Respect to Low-Power Modes .............................................. 1418
Table 24-25. Hibernation Module Battery Characteristics ....................................................... 1420
Table 24-26. Hibernation Module AC Characteristics ............................................................. 1420
Table 24-27. Flash Memory Characteristics .......................................................................... 1421
Table 24-28. EEPROM Characteristics ................................................................................. 1421
Table 24-29. GPIO Module Characteristics ............................................................................ 1422
Table 24-30. Pad Voltage/Current Characteristics for Fail-Safe Pins ....................................... 1423
Table 24-31. Fail-Safe GPIOs that Require an External Pull-up .............................................. 1424
Table 24-32. Non-Fail-Safe I/O Pad Voltage/Current Characteristics ........................................ 1424
Table 24-33. ADC Electrical Characteristics ......................................................................... 1426
Table 24-34. SSI Characteristics .......................................................................................... 1430
Table 24-35. I²C Characteristics .......................................................................................... 1433
Table 24-36. Analog Comparator Characteristics ..................................................................... 1435
Table 24-37. Analog Comparator Voltage Reference Characteristics ..................................... 1435
Table 24-38. Analog Comparator Voltage Reference Characteristics, V_{DDA} = 3.3V, EN= 1, and
RNG = 0 ......................................................................................................................... 1435
Table 24-39. Analog Comparator Voltage Reference Characteristics, V_{DDA} = 3.3V, EN= 1, and
RNG = 1 ......................................................................................................................... 1436
Table 24-40. PWM Timing Characteristics ............................................................................. 1436
Table 24-41. Current Consumption ....................................................................................... 1437
List of Registers

The Cortex-M4F Processor ................................................................. 69
Register 1: Cortex General-Purpose Register 0 (R0) ........................................ 77
Register 2: Cortex General-Purpose Register 1 (R1) ....................................... 77
Register 3: Cortex General-Purpose Register 2 (R2) ....................................... 77
Register 4: Cortex General-Purpose Register 3 (R3) ....................................... 77
Register 5: Cortex General-Purpose Register 4 (R4) ....................................... 77
Register 6: Cortex General-Purpose Register 5 (R5) ....................................... 77
Register 7: Cortex General-Purpose Register 6 (R6) ....................................... 77
Register 8: Cortex General-Purpose Register 7 (R7) ....................................... 77
Register 9: Cortex General-Purpose Register 8 (R8) ....................................... 77
Register 10: Cortex General-Purpose Register 9 (R9) ...................................... 77
Register 11: Cortex General-Purpose Register 10 (R10) .................................. 77
Register 12: Cortex General-Purpose Register 11 (R11) .................................. 77
Register 13: Cortex General-Purpose Register 12 (R12) .................................. 77
Register 14: Stack Pointer (SP) .............................................................. 78
Register 15: Link Register (LR) ............................................................... 79
Register 16: Program Counter (PC) .......................................................... 80
Register 17: Program Status Register (PSR) ................................................ 81
Register 18: Priority Mask Register (PRIMASK) .......................................... 85
Register 19: Fault Mask Register (FAULTMASK) ....................................... 86
Register 20: Base Priority Mask Register (BASEPRI) .................................... 87
Register 21: Control Register (CONTROL) ............................................... 88
Register 22: Floating-Point Status Control (FPSC) ....................................... 90

Cortex-M4 Peripherals ........................................................................ 122
Register 1: SysTick Control and Status Register (STCTRL), offset 0x010 .......... 138
Register 2: SysTick Reload Value Register (STRELOAD), offset 0x014 ......... 140
Register 3: SysTick Current Value Register (STCURRENT), offset 0x018 ..... 141
Register 4: Interrupt 0-31 Set Enable (EN0), offset 0x100 ......................... 142
Register 5: Interrupt 32-63 Set Enable (EN1), offset 0x104 ......................... 142
Register 6: Interrupt 64-95 Set Enable (EN2), offset 0x108 ......................... 142
Register 7: Interrupt 96-127 Set Enable (EN3), offset 0x110 ......................... 142
Register 8: Interrupt 128-138 Set Enable (EN4), offset 0x110 ....................... 143
Register 9: Interrupt 0-31 Clear Enable (DIS0), offset 0x180 ....................... 144
Register 10: Interrupt 32-63 Clear Enable (DIS1), offset 0x184 ..................... 144
Register 11: Interrupt 64-95 Clear Enable (DIS2), offset 0x188 ..................... 144
Register 12: Interrupt 96-127 Clear Enable (DIS3), offset 0x18C .................... 144
Register 13: Interrupt 128-138 Clear Enable (DIS4), offset 0x190 ................. 145
Register 14: Interrupt 0-31 Set Pending (PEND0), offset 0x200 .................... 146
Register 15: Interrupt 32-63 Set Pending (PEND1), offset 0x204 .................... 146
Register 16: Interrupt 64-95 Set Pending (PEND2), offset 0x208 .................... 146
Register 17: Interrupt 96-127 Set Pending (PEND3), offset 0x20C ................. 146
Register 18: Interrupt 128-138 Set Pending (PEND4), offset 0x210 ............... 147
Register 19: Interrupt 0-31 Clear Pending (UNPEND0), offset 0x280 ............. 148
Register 20: Interrupt 32-63 Clear Pending (UNPEND1), offset 0x284 ............. 148
Register 21: Interrupt 64-95 Clear Pending (UNPEND2), offset 0x288 ............. 148
Register 22: Interrupt 96-127 Clear Pending (UNPEND3), offset 0x28C .......................................................... 148
Register 23: Interrupt 128-138 Clear Pending (UNPEND4), offset 0x290 ......................................................... 149
Register 24: Interrupt 0-31 Active Bit (ACTIVE0), offset 0x300 ..................................................................... 150
Register 25: Interrupt 32-63 Active Bit (ACTIVE1), offset 0x304 ..................................................................... 150
Register 26: Interrupt 64-95 Active Bit (ACTIVE2), offset 0x308 ..................................................................... 150
Register 27: Interrupt 96-127 Active Bit (ACTIVE3), offset 0x30C ................................................................. 150
Register 28: Interrupt 128-138 Active Bit (ACTIVE4), offset 0x310 ............................................................... 151
Register 29: Interrupt 0-3 Priority (PRI0), offset 0x400 .................................................................................... 152
Register 30: Interrupt 4-7 Priority (PRI1), offset 0x404 .................................................................................... 152
Register 31: Interrupt 8-11 Priority (PRI2), offset 0x408 .................................................................................. 152
Register 32: Interrupt 12-15 Priority (PRI3), offset 0x40C ............................................................................. 152
Register 33: Interrupt 16-19 Priority (PRI4), offset 0x410 .............................................................................. 152
Register 34: Interrupt 20-23 Priority (PRI5), offset 0x414 .............................................................................. 152
Register 35: Interrupt 24-27 Priority (PRI6), offset 0x418 .............................................................................. 152
Register 36: Interrupt 28-31 Priority (PRI7), offset 0x41C ............................................................................. 152
Register 37: Interrupt 32-35 Priority (PRI8), offset 0x420 .............................................................................. 152
Register 38: Interrupt 36-39 Priority (PRI9), offset 0x424 .............................................................................. 152
Register 39: Interrupt 40-43 Priority (PRI10), offset 0x428 ......................................................................... 152
Register 40: Interrupt 44-47 Priority (PRI11), offset 0x42C ......................................................................... 152
Register 41: Interrupt 48-51 Priority (PRI12), offset 0x430 ......................................................................... 152
Register 42: Interrupt 52-55 Priority (PRI13), offset 0x434 ......................................................................... 152
Register 43: Interrupt 56-59 Priority (PRI14), offset 0x438 ......................................................................... 152
Register 44: Interrupt 60-63 Priority (PRI15), offset 0x43C ......................................................................... 152
Register 45: Interrupt 64-67 Priority (PRI16), offset 0x440 ......................................................................... 152
Register 46: Interrupt 68-71 Priority (PRI17), offset 0x444 ......................................................................... 154
Register 47: Interrupt 72-75 Priority (PRI18), offset 0x448 ......................................................................... 154
Register 48: Interrupt 76-79 Priority (PRI19), offset 0x44C ......................................................................... 154
Register 49: Interrupt 80-83 Priority (PRI20), offset 0x450 ......................................................................... 154
Register 50: Interrupt 84-87 Priority (PRI21), offset 0x454 ......................................................................... 154
Register 51: Interrupt 88-91 Priority (PRI22), offset 0x458 ......................................................................... 154
Register 52: Interrupt 92-95 Priority (PRI23), offset 0x45C ......................................................................... 154
Register 53: Interrupt 96-99 Priority (PRI24), offset 0x460 ......................................................................... 154
Register 54: Interrupt 100-103 Priority (PRI25), offset 0x464 ..................................................................... 154
Register 55: Interrupt 104-107 Priority (PRI26), offset 0x468 ..................................................................... 154
Register 56: Interrupt 108-111 Priority (PRI27), offset 0x46C ..................................................................... 154
Register 57: Interrupt 112-115 Priority (PRI28), offset 0x470 ..................................................................... 154
Register 58: Interrupt 116-119 Priority (PRI29), offset 0x474 ..................................................................... 154
Register 59: Interrupt 120-123 Priority (PRI30), offset 0x478 ..................................................................... 154
Register 60: Interrupt 124-127 Priority (PRI31), offset 0x47C ..................................................................... 154
Register 61: Interrupt 128-131 Priority (PRI32), offset 0x480 ..................................................................... 154
Register 62: Interrupt 132-135 Priority (PRI33), offset 0x484 ..................................................................... 154
Register 63: Interrupt 136-138 Priority (PRI34), offset 0x488 ..................................................................... 154
Register 64: Software Trigger Interrupt (SWTRIG), offset 0xF00 ................................................................. 156
Register 65: Auxiliary Control (ACTLR), offset 0x008 .................................................................................. 157
Register 66: CPU ID Base (CPUID), offset 0xD00 ......................................................................................... 159
Register 67: Interrupt Control and State (INTCTRL), offset 0xD04 ............................................................ 160
Register 68: Vector Table Offset (VTABLE), offset 0x0D8 ......................................................................... 163
Register 69: Application Interrupt and Reset Control (APINT), offset 0xD0C ............................................... 164
Register 70: System Control (SYSCTRL), offset 0xD10 ................................................................. 166
Register 71: Configuration and Control (CFGCTRL), offset 0xD14 .................................................. 168
Register 72: System Handler Priority 1 (SYSPRI1), offset 0xD18 .................................................. 170
Register 73: System Handler Priority 2 (SYSPRI2), offset 0xD1C .................................................. 171
Register 74: System Handler Priority 3 (SYSPRI3), offset 0xD20 .................................................. 172
Register 75: System Handler Control and State (SYSHNDCTRL), offset 0xD24 ......................... 173
Register 76: Configurable Fault Status (FAULTSTAT), offset 0xD28 ........................................... 177
Register 77: Hard Fault Status (HFAULTSTAT), offset 0xD2C ...................................................... 183
Register 78: Memory Management Fault Address (MMADDR), offset 0xD34 ................................. 184
Register 79: Bus Fault Address (FAULTADDR), offset 0xD38 .......................................................... 185
Register 80: MPU Type (MPUTYPE), offset 0xD90 ........................................................ 186
Register 81: MPU Control (MPUCTRL), offset 0xD94 ........................................................ 187
Register 82: MPU Region Number (MPUNUMBER), offset 0xD98 ................................................... 189
Register 83: MPU Region Base Address (MPUBASE), offset 0xD9C .................................................. 190
Register 84: MPU Region Base Address Alias 1 (MPUBASE1), offset 0xDA0 ............................... 190
Register 85: MPU Region Base Address Alias 2 (MPUBASE2), offset 0xDA4 ................................. 190
Register 86: MPU Region Base Address Alias 3 (MPUBASE3), offset 0xDB4 .............................. 190
Register 87: MPU Region Attribute and Size (MPUATTR), offset 0xDA8 ......................................... 192
Register 88: MPU Region Attribute and Size Alias 1 (MPUATTR1), offset 0xDA8 ......................... 192
Register 89: MPU Region Attribute and Size Alias 2 (MPUATTR2), offset 0xDB0 ......................... 192
Register 90: MPU Region Attribute and Size Alias 3 (MPUATTR3), offset 0xDB8 ......................... 192
Register 91: Coprocessor Access Control (CPAC), offset 0xDB8 .................................................. 195
Register 92: Floating-Point Context Control (FPCC), offset 0xF34 ................................................... 196
Register 93: Floating-Point Context Address (FPCA), offset 0xF38 ................................................... 198
Register 94: Floating-Point Default Status Control (FPDSC), offset 0xF3C ........................................... 199

System Control .................................................................................................................. 212

Register 1: Device Identification 0 (DID0), offset 0x000 ................................................................. 238
Register 2: Device Identification 1 (DID1), offset 0x004 ................................................................. 240
Register 3: Brown-Out Reset Control (PBORCTL), offset 0x030 .................................................. 243
Register 4: Raw Interrupt Status (RIS), offset 0x050 ........................................................ 244
Register 5: Interrupt Mask Control (IMC), offset 0x054 ........................................................ 247
Register 6: Masked Interrupt Status and Clear (MISC), offset 0x058 ........................................... 249
Register 7: Reset Cause (RESC), offset 0x05C ........................................................ 252
Register 8: Run-Mode Clock Configuration (RCC), offset 0x060 .................................................. 254
Register 9: GPIO High-Performance Bus Control (GPIOHBCTL), offset 0x06C ............................... 258
Register 10: Run-Mode Clock Configuration 2 (RCC2), offset 0x070 ............................................. 261
Register 11: Main Oscillator Control (MOSCCTL), offset 0x07C .................................................. 264
Register 12: Deep Sleep Clock Configuration (DSLPCCLKCFG), offset 0x144 .............................. 265
Register 13: System Properties (SYSPROP), offset 0x14C .............................................................. 267
Register 14: Precision Internal Oscillator Calibration (PIOSCCAL), offset 0x150 ............................... 269
Register 15: Precision Internal Oscillator Statistics (PIOSCSTAT), offset 0x154 .............................. 271
Register 16: PLL Frequency 0 (PLLFRQ0), offset 0x160 ................................................................. 272
Register 17: PLL Frequency 1 (PLLFRQ1), offset 0x164 ................................................................. 273
Register 18: PLL Status (PLLSTAT), offset 0x168 ........................................................................ 274
Register 19: Sleep Power Configuration (SLPPWRCFG), offset 0x188 ........................................... 275
Register 20: Deep-Sleep Power Configuration (DSLPPWRCFG), offset 0x18C ................................. 277
Register 21: LDO Sleep Power Control (LDOSPCTL), offset 0x1B4 ............................................. 279
Register 22: LDO Sleep Power Calibration (LDOSPCAL), offset 0x1B8 ........................................... 281
<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>LDO Deep-Sleep Power Control (LDODPCTL)</td>
<td>0x1BC</td>
</tr>
<tr>
<td>24</td>
<td>LDO Deep-Sleep Power Calibration (LDODPCAL)</td>
<td>0x1C0</td>
</tr>
<tr>
<td>25</td>
<td>Sleep / Deep-Sleep Power Mode Status (SDPMST)</td>
<td>0x1CC</td>
</tr>
<tr>
<td>26</td>
<td>Watchdog Timer Peripheral Present (PPWD)</td>
<td>0x300</td>
</tr>
<tr>
<td>27</td>
<td>16/32-Bit General-Purpose Timer Peripheral Present (PPTIMER)</td>
<td>0x304</td>
</tr>
<tr>
<td>28</td>
<td>General-Purpose Input/Output Peripheral Present (PPGPIO)</td>
<td>0x308</td>
</tr>
<tr>
<td>29</td>
<td>Micro Direct Memory Access Peripheral Present (PPDMA)</td>
<td>0x30C</td>
</tr>
<tr>
<td>30</td>
<td>Hibernation Peripheral Present (PPHIB)</td>
<td>0x314</td>
</tr>
<tr>
<td>31</td>
<td>Universal Asynchronous Receiver/Transmitter Peripheral Present (PPUART)</td>
<td>0x318</td>
</tr>
<tr>
<td>32</td>
<td>Synchronous Serial Interface Peripheral Present (PPSSI)</td>
<td>0x31C</td>
</tr>
<tr>
<td>33</td>
<td>Inter-Integrated Circuit Peripheral Present (PPI2C)</td>
<td>0x320</td>
</tr>
<tr>
<td>34</td>
<td>Universal Serial Bus Peripheral Present (PPUSB)</td>
<td>0x328</td>
</tr>
<tr>
<td>35</td>
<td>Controller Area Network Peripheral Present (PPCAN)</td>
<td>0x334</td>
</tr>
<tr>
<td>36</td>
<td>Analog-to-Digital Converter Peripheral Present (PPADC)</td>
<td>0x338</td>
</tr>
<tr>
<td>37</td>
<td>Analog Comparator Peripheral Present (PPACMP)</td>
<td>0x33C</td>
</tr>
<tr>
<td>38</td>
<td>Pulse Width Modulator Peripheral Present (PPPWM)</td>
<td>0x340</td>
</tr>
<tr>
<td>39</td>
<td>Quadrature Encoder Interface Peripheral Present (PPQEI)</td>
<td>0x344</td>
</tr>
<tr>
<td>40</td>
<td>EEPROM Peripheral Present (PPEEPROM)</td>
<td>0x358</td>
</tr>
<tr>
<td>41</td>
<td>32/64-Bit Wide General-Purpose Timer Peripheral Present (PPWTIMER)</td>
<td>0x35C</td>
</tr>
<tr>
<td>42</td>
<td>Watchdog Timer Software Reset (SRWD)</td>
<td>0x500</td>
</tr>
<tr>
<td>43</td>
<td>16/32-Bit General-Purpose Timer Software Reset (SRTIMER)</td>
<td>0x504</td>
</tr>
<tr>
<td>44</td>
<td>General-Purpose Input/Output Software Reset (SRGPIO)</td>
<td>0x508</td>
</tr>
<tr>
<td>45</td>
<td>Micro Direct Memory Access Software Reset (SRDMA)</td>
<td>0x50C</td>
</tr>
<tr>
<td>46</td>
<td>Hibernation Software Reset (SRHIB)</td>
<td>0x514</td>
</tr>
<tr>
<td>47</td>
<td>Universal Asynchronous Receiver/Transmitter Software Reset (SRUART)</td>
<td>0x518</td>
</tr>
<tr>
<td>48</td>
<td>Synchronous Serial Interface Software Reset (PPSSI)</td>
<td>0x51C</td>
</tr>
<tr>
<td>49</td>
<td>Inter-Integrated Circuit Software Reset (SRI2C)</td>
<td>0x520</td>
</tr>
<tr>
<td>50</td>
<td>Universal Serial Bus Software Reset (SRUSB)</td>
<td>0x528</td>
</tr>
<tr>
<td>51</td>
<td>Controller Area Network Software Reset (PPCAN)</td>
<td>0x534</td>
</tr>
<tr>
<td>52</td>
<td>Analog-to-Digital Converter Software Reset (SRADC)</td>
<td>0x538</td>
</tr>
<tr>
<td>53</td>
<td>Analog Comparator Software Reset (SRACMP)</td>
<td>0x53C</td>
</tr>
<tr>
<td>54</td>
<td>Pulse Width Modulator Software Reset (SRPWM)</td>
<td>0x540</td>
</tr>
<tr>
<td>55</td>
<td>Quadrature Encoder Interface Software Reset (SRQEI)</td>
<td>0x544</td>
</tr>
<tr>
<td>56</td>
<td>EEPROM Software Reset (SREEEPROM)</td>
<td>0x558</td>
</tr>
<tr>
<td>57</td>
<td>32/64-Bit Wide General-Purpose Timer Software Reset (SRWTIMER)</td>
<td>0x55C</td>
</tr>
<tr>
<td>58</td>
<td>Watchdog Timer Run Mode Clock Gating Control (RCGCWD)</td>
<td>0x600</td>
</tr>
<tr>
<td>59</td>
<td>16/32-Bit General-Purpose Timer Run Mode Clock Gating Control (RCGCTIMER)</td>
<td>0x604</td>
</tr>
<tr>
<td>60</td>
<td>General-Purpose Input/Output Run Mode Clock Gating Control (RCGCGPIO)</td>
<td>0x608</td>
</tr>
<tr>
<td>61</td>
<td>Micro Direct Memory Access Run Mode Clock Gating Control (RCGCDMA)</td>
<td>0x60C</td>
</tr>
<tr>
<td>62</td>
<td>Hibernation Run Mode Clock Gating Control (RCGCHIB)</td>
<td>0x614</td>
</tr>
<tr>
<td>63</td>
<td>Universal Asynchronous Receiver/Transmitter Run Mode Clock Gating Control (RCGCUART)</td>
<td>0x618</td>
</tr>
<tr>
<td>64</td>
<td>Synchronous Serial Interface Run Mode Clock Gating Control (RCGCSSI)</td>
<td>0x61C</td>
</tr>
<tr>
<td>65</td>
<td>Inter-Integrated Circuit Run Mode Clock Gating Control (RCGCI2C)</td>
<td>0x620</td>
</tr>
</tbody>
</table>

*Texas Instruments-Production Data*
Register 86: Pulse Width Modulator Sleep Mode Clock Gating Control (SCGCPWM), offset 0x740 .......... 380
Register 85: Analog Comparator Sleep Mode Clock Gating Control (SCGCACMP), offset 0x73C .......... 379
Register 84: Analog-to-Digital Converter Sleep Mode Clock Gating Control (SCGCADC), offset 0x738 .... 377
Register 83: Controller Area Network Sleep Mode Clock Gating Control (SCGCCAN), offset 0x734 ....... 375
Register 82: Universal Serial Bus Sleep Mode Clock Gating Control (SCGCUSB), offset 0x728 ............... 373
Register 81: Inter-Integrated Circuit Sleep Mode Clock Gating Control (SCGC12C), offset 0x720 ........... 371
Register 80: Synchronous Serial Interface Sleep Mode Clock Gating Control (SCGCSSI), offset 0x718 .......... 370
Register 79: Universal Asynchronous Receiver/Transmitter Sleep Mode Clock Gating Control (SCGCUART), offset 0x714 .......... 369
Register 78: Hibernation Sleep Mode Clock Gating Control (SCGCHIB), offset 0x710 ......................... 368
Register 77: Micro Direct Memory Access Sleep Mode Clock Gating Control (SCGCDMA), offset 0x70C ....... 366
Register 76: General-Purpose Input/Output Sleep Mode Clock Gating Control (SCGCGPIO), offset 0x708 .................................................. 365
Register 75: 16/32-Bit General-Purpose Timer Sleep Mode Clock Gating Control (SCGCTIMER), offset 0x704 .......... 364
Register 74: Watchdog Timer Sleep Mode Clock Gating Control (SCGCWD), offset 0x700 .................... 362
Register 73: 32/64-Bit Wide General-Purpose Timer Run Mode Clock Gating Control (RCGWTIMER), offset 0x700 .................................................. 360
Register 72: EEPROM Run Mode Clock Gating Control (RCGCEEPROM), offset 0x700 .................... 359
Register 71: Quadrature Encoder Interface Run Mode Clock Gating Control (RCGCGIE), offset 0x700 ....... 357
Register 70: Pulse Width Modulator Run Mode Clock Gating Control (RCGCPWM), offset 0x6F4 .......... 355
Register 69: Analog-to-Digital Converter Run Mode Clock Gating Control (RCGCADC), offset 0x6E8 ....... 354
Register 68: Controller Area Network Run Mode Clock Gating Control (RGCCAN), offset 0x6E4 .......... 353
Register 67: Universal Asynchronous Receiver/Transmitter Run Mode Clock Gating Control (RGCCUART), offset 0x6F0 .......... 351
Register 66: Universal Serial Bus Run Mode Clock Gating Control (RGCCUSB), offset 0x6E0 .......... 349

Table of Contents

Register 66: Universal Serial Bus Run Mode Clock Gating Control (RCGCUSB), offset 0x628 ............... 353
Register 67: Controller Area Network Run Mode Clock Gating Control (RGCCAN), offset 0x634 ........... 354
Register 68: Analog-to-Digital Converter Run Mode Clock Gating Control (RCGCADC), offset 0x638 ....... 355
Register 69: Analog Comparator Run Mode Clock Gating Control (RCGCACMP), offset 0x63C .......... 356
Register 70: Pulse Width Modulator Run Mode Clock Gating Control (RCGCPWM), offset 0x640 .......... 357
Register 71: Quadrature Encoder Interface Run Mode Clock Gating Control (RCGCGIE), offset 0x644 .......... 358
Register 72: EEPROM Run Mode Clock Gating Control (RCGCEEPROM), offset 0x658 ................. 359
Register 73: 32/64-Bit Wide General-Purpose Timer Run Mode Clock Gating Control (RCGWTIMER), offset 0x65C .................................................. 360
Register 74: Watchdog Timer Sleep Mode Clock Gating Control (SCGCWD), offset 0x700 ............... 361
Register 75: 16/32-Bit General-Purpose Timer Sleep Mode Clock Gating Control (SCGCTIMER), offset 0x704 .......... 362
Register 76: General-Purpose Input/Output Sleep Mode Clock Gating Control (SCGCGPIO), offset 0x708 .................................................. 363
Register 77: Micro Direct Memory Access Sleep Mode Clock Gating Control (SCGCDMA), offset 0x70C ....... 364
Register 78: Hibernation Sleep Mode Clock Gating Control (SCGCHIB), offset 0x714 ......................... 365
Register 79: Universal Asynchronous Receiver/Transmitter Sleep Mode Clock Gating Control (SCGCUART), offset 0x718 .................................................. 366
Register 80: Synchronous Serial Interface Sleep Mode Clock Gating Control (SCGCSSI), offset 0x71C ....... 367
Register 81: Inter-Integrated Circuit Sleep Mode Clock Gating Control (SCGC12C), offset 0x720 ........... 368
Register 82: Universal Serial Bus Sleep Mode Clock Gating Control (SCGCUSB), offset 0x728 ........... 369
Register 83: Controller Area Network Sleep Mode Clock Gating Control (SCGCCAN), offset 0x734 ....... 370
Register 84: Analog-to-Digital Converter Sleep Mode Clock Gating Control (SCGCADC), offset 0x738 .... 371
Register 85: Analog Comparator Sleep Mode Clock Gating Control (SCGCACMP), offset 0x73C .......... 372
Register 86: Pulse Width Modulator Sleep Mode Clock Gating Control (SCGCPWM), offset 0x740 .......... 373
Register 87: Quadrature Encoder Interface Sleep Mode Clock Gating Control (SCGCGIE), offset 0x744 .......... 374
Register 88: EEPROM Sleep Mode Clock Gating Control (SCGCEEPROM), offset 0x758 .................... 375
Register 89: 32/64-Bit Wide General-Purpose Timer Sleep Mode Clock Gating Control (SCGWTIMER), offset 0x75C .................................................. 376
Register 90: Watchdog Timer Sleep Mode Clock Gating Control (SCGCWD), offset 0x800 ............... 377
Register 91: 16/32-Bit General-Purpose Timer Sleep Mode Clock Gating Control (DCGCWRTIMER), offset 0x804 .......... 378
Register 92: General-Purpose Input/Output Deep-Sleep Mode Clock Gating Control (DCGCGPIO), offset 0x808 .................................................. 379
Register 93: Micro Direct Memory Access Deep-Sleep Mode Clock Gating Control (DCGCDMA), offset 0x80C .................................................. 380
Register 94: Hibernation Deep-Sleep Mode Clock Gating Control (DCGCHIB), offset 0x814 .......... 381
Register 95: Universal Asynchronous Receiver/Transmitter Deep-Sleep Mode Clock Gating Control (DCGCUART), offset 0x818 .................................................. 382
Register 96: Synchronous Serial Interface Deep-Sleep Mode Clock Gating Control (DCGCSSI), offset 0x81C .................................................. 383
Register 97: Inter-Integrated Circuit Deep-Sleep Mode Clock Gating Control (DCGC12C), offset 0x820 .......... 384
Register 98: Universal Serial Bus Deep-Sleep Mode Clock Gating Control (DCGCUSB), offset 0x828 .......... 385

Texas Instruments-Production Data

June 12, 2014
<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>140</td>
<td>Deep Sleep Mode Clock Gating Control Register 0 (DCGC0)</td>
<td>0x120</td>
</tr>
<tr>
<td>139</td>
<td>Sleep Mode Clock Gating Control Register 2 (SCGC2)</td>
<td>0x118</td>
</tr>
<tr>
<td>138</td>
<td>Sleep Mode Clock Gating Control Register 1 (SCGC1)</td>
<td>0x114</td>
</tr>
<tr>
<td>137</td>
<td>Sleep Mode Clock Gating Control Register 0 (SCGC0)</td>
<td>0x110</td>
</tr>
<tr>
<td>136</td>
<td>Run Mode Clock Gating Control Register 2 (RCGC2)</td>
<td>0x108</td>
</tr>
<tr>
<td>135</td>
<td>Run Mode Clock Gating Control Register 1 (RCGC1)</td>
<td>0x104</td>
</tr>
<tr>
<td>134</td>
<td>Run Mode Clock Gating Control Register 0 (RCGC0)</td>
<td>0x100</td>
</tr>
<tr>
<td>133</td>
<td>Software Reset Control 2 (SRCR2)</td>
<td>0x048</td>
</tr>
<tr>
<td>132</td>
<td>Software Reset Control 1 (SRCR1)</td>
<td>0x044</td>
</tr>
<tr>
<td>131</td>
<td>Software Reset Control 0 (SRCR0)</td>
<td>0x040</td>
</tr>
<tr>
<td>130</td>
<td>Device Capabilities 8 (DC8)</td>
<td>0x02C</td>
</tr>
<tr>
<td>129</td>
<td>Device Capabilities 7 (DC7)</td>
<td>0x028</td>
</tr>
<tr>
<td>128</td>
<td>Device Capabilities 6 (DC6)</td>
<td>0x024</td>
</tr>
<tr>
<td>127</td>
<td>Device Capabilities 5 (DC5)</td>
<td>0x020</td>
</tr>
<tr>
<td>126</td>
<td>Device Capabilities 4 (DC4)</td>
<td>0x01C</td>
</tr>
<tr>
<td>125</td>
<td>Device Capabilities 3 (DC3)</td>
<td>0x018</td>
</tr>
<tr>
<td>124</td>
<td>Device Capabilities 2 (DC2)</td>
<td>0x014</td>
</tr>
<tr>
<td>123</td>
<td>Device Capabilities 1 (DC1)</td>
<td>0x010</td>
</tr>
<tr>
<td>122</td>
<td>Device Capabilities 0 (DC0)</td>
<td>0x008</td>
</tr>
<tr>
<td>121</td>
<td>Synchronous Serial Interface Peripheral Ready (PRSSI)</td>
<td>0x01A</td>
</tr>
<tr>
<td>120</td>
<td>Inter-Integrated Circuit Peripheral Ready (PRI2C)</td>
<td>0x020</td>
</tr>
<tr>
<td>119</td>
<td>Universal Serial Bus Peripheral Ready (PRUSB)</td>
<td>0x028</td>
</tr>
<tr>
<td>118</td>
<td>Controller Area Network Peripheral Ready (PRCAN)</td>
<td>0x034</td>
</tr>
<tr>
<td>117</td>
<td>Analog-to-Digital Converter Peripheral Ready (PRADC)</td>
<td>0x038</td>
</tr>
<tr>
<td>116</td>
<td>Analog Comparator Peripheral Ready (PRACMP)</td>
<td>0x03C</td>
</tr>
<tr>
<td>115</td>
<td>Quadrate Encoder Interface Peripheral Ready (PRPWM)</td>
<td>0x040</td>
</tr>
<tr>
<td>114</td>
<td>Watchdog Timer Peripheral Ready (PRWD)</td>
<td>0x048</td>
</tr>
<tr>
<td>113</td>
<td>16/32-Bit General-Purpose Timer Peripheral Ready (PRTIMER)</td>
<td>0x050</td>
</tr>
<tr>
<td>112</td>
<td>Micro Direct Memory Access Peripheral Ready (PRDMA)</td>
<td>0x058</td>
</tr>
<tr>
<td>111</td>
<td>Micro Direct Memory Access Peripheral Ready (PRDMA)</td>
<td>0x05C</td>
</tr>
<tr>
<td>110</td>
<td>Controller Area Network Deep-Sleep Mode Clock Gating Control (DCGCAN)</td>
<td>0x060</td>
</tr>
<tr>
<td>109</td>
<td>Analog-to-Digital Converter Deep-Sleep Mode Clock Gating Control (DCGCADC)</td>
<td>0x064</td>
</tr>
<tr>
<td>108</td>
<td>Analog Comparator Deep-Sleep Mode Clock Gating Control (DCGCACMP)</td>
<td>0x068</td>
</tr>
<tr>
<td>107</td>
<td>Pulse Width Modulator Deep-Sleep Mode Clock Gating Control (DCGCPWM)</td>
<td>0x070</td>
</tr>
<tr>
<td>106</td>
<td>Quadrature Encoder Interface Deep-Sleep Mode Clock Gating Control (DCGCQEI)</td>
<td>0x074</td>
</tr>
<tr>
<td>105</td>
<td>EEPROM Deep-Sleep Mode Clock Gating Control (DCGCEEPROM)</td>
<td>0x078</td>
</tr>
<tr>
<td>104</td>
<td>32/64-Bit Wide General-Purpose Timer Deep-Sleep Mode Clock Gating Control (DCGWTIMER)</td>
<td>0x080</td>
</tr>
<tr>
<td>103</td>
<td>Watchdog Timer Deep-Sleep Mode Clock Gating Control (DCGCWTIMER)</td>
<td>0x084</td>
</tr>
<tr>
<td>102</td>
<td>16/32-Bit General-Purpose Timer Deep-Sleep Mode Clock Gating Control (DCGCCAN)</td>
<td>0x088</td>
</tr>
<tr>
<td>101</td>
<td>Universal Asynchronous Receiver/Transmitter Deep-Sleep Mode Clock Gating Control (DCGCUART)</td>
<td>0x090</td>
</tr>
<tr>
<td>100</td>
<td>32/64-Bit Wide General-Purpose Timer Deep-Sleep Mode Clock Gating Control (DCGCWTIMER)</td>
<td>0x094</td>
</tr>
<tr>
<td>99</td>
<td>Watchdog Timer Deep-Sleep Mode Clock Gating Control (DCGCWTIMER)</td>
<td>0x098</td>
</tr>
</tbody>
</table>

**Notes:**
- The table lists various registers for different components of the Tiva™ TM4C123GH6PZ Microcontroller.
- Each register is identified by its offset in the memory address space.
- The registers control various functions such as clock gating, reset, and peripheral readiness.

**Additional Information:**
- The image is a page from a Texas Instruments document, indicating it is related to the Tiva™ TM4C123GH6PZ Microcontroller.
- The date on the page is June 12, 2014.
### System Exception Module

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>System Exception Raw Interrupt Status (SYSEXCRIS)</td>
<td>0x000</td>
</tr>
<tr>
<td>2</td>
<td>System Exception Interrupt Mask (SYSEXCM)</td>
<td>0x004</td>
</tr>
<tr>
<td>3</td>
<td>System Exception Masked Interrupt Status (SYSEXCMIS)</td>
<td>0x008</td>
</tr>
<tr>
<td>4</td>
<td>System Exception Interrupt Clear (SYSEXCIC)</td>
<td>0x00C</td>
</tr>
</tbody>
</table>

### Hibernation Module

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Hibernation RTC Counter (HIBRTCC)</td>
<td>0x000</td>
</tr>
<tr>
<td>2</td>
<td>Hibernation RTC Match 0 (HIBRTCM0)</td>
<td>0x004</td>
</tr>
<tr>
<td>3</td>
<td>Hibernation RTC Load (HIBRTCLD)</td>
<td>0x00C</td>
</tr>
<tr>
<td>4</td>
<td>Hibernation Control (HIBCTRL)</td>
<td>0x010</td>
</tr>
<tr>
<td>5</td>
<td>Hibernation Interrupt Mask (HIBIM)</td>
<td>0x014</td>
</tr>
<tr>
<td>6</td>
<td>Hibernation Raw Interrupt Status (HIBRIS)</td>
<td>0x018</td>
</tr>
<tr>
<td>7</td>
<td>Hibernation Masked Interrupt Status (HIBMIS)</td>
<td>0x01C</td>
</tr>
<tr>
<td>8</td>
<td>Hibernation Interrupt Clear (HIBIC)</td>
<td>0x020</td>
</tr>
<tr>
<td>9</td>
<td>Hibernation RTC Trim (HIBRTCT)</td>
<td>0x024</td>
</tr>
<tr>
<td>10</td>
<td>Hibernation RTC Sub Seconds (HIBRTCSS)</td>
<td>0x028</td>
</tr>
<tr>
<td>11</td>
<td>Hibernation Data (HIBDATA)</td>
<td>0x030-0x06F</td>
</tr>
</tbody>
</table>

### Internal Memory

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Flash Memory Address (FMA)</td>
<td>0x000</td>
</tr>
<tr>
<td>2</td>
<td>Flash Memory Data (FMD)</td>
<td>0x004</td>
</tr>
<tr>
<td>3</td>
<td>Flash Memory Control (FMC)</td>
<td>0x008</td>
</tr>
<tr>
<td>4</td>
<td>Flash Controller Raw Interrupt Status (FCRIS)</td>
<td>0x00C</td>
</tr>
<tr>
<td>5</td>
<td>Flash Controller Masked Interrupt Mask (FCMISC)</td>
<td>0x010</td>
</tr>
<tr>
<td>6</td>
<td>Flash Controller Masked Interrupt Status and Clear (FCMISC)</td>
<td>0x014</td>
</tr>
<tr>
<td>7</td>
<td>Flash Memory Control 2 (FMC2)</td>
<td>0x020</td>
</tr>
<tr>
<td>8</td>
<td>Flash Write Buffer Valid (FWBVAL)</td>
<td>0x030</td>
</tr>
<tr>
<td>9</td>
<td>Flash Write Buffer n (FWBN)</td>
<td>0x100 - 0x17C</td>
</tr>
<tr>
<td>10</td>
<td>Flash Size (FSIZE)</td>
<td>0x0FC0</td>
</tr>
<tr>
<td>11</td>
<td>SRAM Size (SSIZE)</td>
<td>0x0FC4</td>
</tr>
<tr>
<td>12</td>
<td>ROM Software Map (ROMSWMAP)</td>
<td>0xFCC</td>
</tr>
<tr>
<td>13</td>
<td>EEPROM Size Information (EESIZE)</td>
<td>0x000</td>
</tr>
<tr>
<td>14</td>
<td>EEPROM Current Block (EEBLOCK)</td>
<td>0x004</td>
</tr>
<tr>
<td>15</td>
<td>EEPROM Current Offset (EEOFFSET)</td>
<td>0x008</td>
</tr>
<tr>
<td>16</td>
<td>EEPROM Read-Write (EERDWR)</td>
<td>0x010</td>
</tr>
<tr>
<td>17</td>
<td>EEPROM Read-Write with Increment (EERDWRINC)</td>
<td>0x014</td>
</tr>
<tr>
<td>18</td>
<td>EEPROM Done Status (EEDONE)</td>
<td>0x018</td>
</tr>
<tr>
<td>19</td>
<td>EEPROM Support Control and Status (EESUPP)</td>
<td>0x01C</td>
</tr>
<tr>
<td>20</td>
<td>EEPROM Unlock (EEUNLOCK)</td>
<td>0x020</td>
</tr>
<tr>
<td>21</td>
<td>EEPROM Protection (EEPROT)</td>
<td>0x030</td>
</tr>
<tr>
<td>22</td>
<td>EEPROM Password (EEPASS0)</td>
<td>0x034</td>
</tr>
<tr>
<td>23</td>
<td>EEPROM Password (EEPASS1)</td>
<td>0x038</td>
</tr>
<tr>
<td>24</td>
<td>EEPROM Password (EEPASS2)</td>
<td>0x03C</td>
</tr>
<tr>
<td>25</td>
<td>EEPROM Interrupt (EEINT)</td>
<td>0x040</td>
</tr>
<tr>
<td>26</td>
<td>EEPROM Block Hide (EEHIDE)</td>
<td>0x050</td>
</tr>
</tbody>
</table>
Register 27: EEPROM Debug Mass Erase (EEDBGM), offset 0x080
Register 28: EEPROM Peripheral Properties (EEPROMPP), offset 0xFC0
Register 29: ROM Control (RMCTL), offset 0x0F0
Register 30: Flash Memory Protection Read Enable 0 (FMPRE0), offset 0x130 and 0x200
Register 31: Flash Memory Protection Read Enable 1 (FMPRE1), offset 0x204
Register 32: Flash Memory Protection Read Enable 2 (FMPRE2), offset 0x208
Register 33: Flash Memory Protection Read Enable 3 (FMPRE3), offset 0x20C
Register 34: Flash Memory Protection Program Enable 0 (FMPPE0), offset 0x134 and 0x400
Register 35: Flash Memory Protection Program Enable 1 (FMPPE1), offset 0x404
Register 36: Flash Memory Protection Program Enable 2 (FMPPE2), offset 0x408
Register 37: Flash Memory Protection Program Enable 3 (FMPPE3), offset 0x40C
Register 38: Boot Configuration (BOOTCFG), offset 0x1DD
Register 39: User Register 0 (USER_REG0), offset 0x1E0
Register 40: User Register 1 (USER_REG1), offset 0x1E4
Register 41: User Register 2 (USER_REG2), offset 0x1E8
Register 42: User Register 3 (USER_REG3), offset 0x1EC

Micro Direct Memory Access (μDMA)
Register 33: DMA PrimeCell Identification 1 (DMAPCelllD1), offset 0xFF4 .............................................. 656
Register 34: DMA PrimeCell Identification 2 (DMAPCelllD2), offset 0xFF8 .............................................. 657
Register 35: DMA PrimeCell Identification 3 (DMAPCelllD3), offset 0xFFC .............................................. 658

General-Purpose Input/Outputs (GPIOs) ........................................................................................................ 659
Register 1: GPIO Data (GPIODATA), offset 0x000 .................................................................................. 673
Register 2: GPIO Direction (GPIODIR), offset 0x400 ................................................................................. 675
Register 3: GPIO Interrupt Sense (GPIOIS), offset 0x404 ........................................................................... 676
Register 4: GPIO Interrupt Both Edges (GPIOIBE), offset 0x408 ............................................................... 677
Register 5: GPIO Interrupt Event (GPIOIEV), offset 0x40C ................................................................. 679
Register 6: GPIO Interrupt Mask (GPIOIM), offset 0x410 ................................................................. 680
Register 7: GPIO Raw Interrupt Status (GPIORIS), offset 0x414............................................................. 681
Register 8: GPIO Masked Interrupt Status (GPIOMIS), offset 0x418 ....................................................... 682
Register 9: GPIO Interrupt Clear (GPIOICR), offset 0x41C ...................................................................... 683
Register 10: GPIO Alternate Function Select (GPIOAFSEL), offset 0x420 .................................................. 684
Register 11: GPIO 2-mA Drive Select (GPIOD2R), offset 0x500 ................................................................. 686
Register 12: GPIO 4-mA Drive Select (GPIOD4R), offset 0x504 ................................................................. 687
Register 13: GPIO 8-mA Drive Select (GPIOD8R), offset 0x508 ................................................................. 688
Register 14: GPIO Open Drain Select (GPIOODR), offset 0x50C .............................................................. 689
Register 15: GPIO Pull-Up Select (GPIOPUR), offset 0x510 ................................................................. 690
Register 16: GPIO Pull-Down Select (GPIOPDR), offset 0x514 ................................................................. 692
Register 17: GPIO Slew Rate Control Select (GPIOSLR), offset 0x518 .................................................... 694
Register 18: GPIO Digital Enable (GPIODEN), offset 0x51C ................................................................. 695
Register 19: GPIO Lock (GPIOLOCK), offset 0x520 .................................................................................. 697
Register 20: GPIO Commit (GPIOCR), offset 0x524 .................................................................................. 698
Register 21: GPIO Analog Mode Select (GPIOAMSEL), offset 0x528 ..................................................... 700
Register 22: GPIO Port Control (GPIOPCTL), offset 0x52C ................................................................. 702
Register 23: GPIO ADC Control (GPIOADCCCTL), offset 0x530 .......................................................... 704
Register 24: GPIO DMA Control (GPIODMACCTL), offset 0x534 .......................................................... 705
Register 25: GPIO Peripheral Identification 4 (GPIOPeriphID4), offset 0xFD0 .............................................. 706
Register 26: GPIO Peripheral Identification 5 (GPIOPeriphID5), offset 0xFD4 .............................................. 707
Register 27: GPIO Peripheral Identification 6 (GPIOPeriphID6), offset 0xFD8 .............................................. 708
Register 28: GPIO Peripheral Identification 7 (GPIOPeriphID7), offset 0xFDc .............................................. 709
Register 29: GPIO Peripheral Identification 0 (GPIOPeriphID0), offset 0xFE0 ........................................... 710
Register 30: GPIO Peripheral Identification 1 (GPIOPeriphID1), offset 0xFE4 ........................................... 711
Register 31: GPIO Peripheral Identification 2 (GPIOPeriphID2), offset 0xFE8 ........................................... 712
Register 32: GPIO Peripheral Identification 3 (GPIOPeriphID3), offset 0xFEC ........................................... 713
Register 33: GPIO PrimeCell Identification 0 (GPIOPCelllD0), offset 0xFF0 ............................................. 714
Register 34: GPIO PrimeCell Identification 1 (GPIOPCelllD1), offset 0xFF4 ............................................. 715
Register 35: GPIO PrimeCell Identification 2 (GPIOPCelllD2), offset 0xFF8 ............................................. 716
Register 36: GPIO PrimeCell Identification 3 (GPIOPCelllD3), offset 0xFFC ............................................. 717

General-Purpose Timers ............................................................................................................................... 718
Register 1: GPTM Configuration (GPTMCFG), offset 0x000 ................................................................. 741
Register 2: GPTM Timer A Mode (GPTMTAMR), offset 0x004 ................................................................. 743
Register 3: GPTM Timer B Mode (GPTMTBMR), offset 0x008 ................................................................. 747
Register 4: GPTM Control (GPTMCTL), offset 0x00C ................................................................. 751
Register 5: GPTM Synchronize (GPTMSYNC), offset 0x010 ................................................................. 755
Register 6: GPTM Interrupt Mask (GPTMIMR), offset 0x018 ................................................................. 759
Register 7: GPTM Raw Interrupt Status (GPTMRIS), offset 0x01C ............................................................... 762
Register 8: GPTM Masked Interrupt Status (GPTMMIS), offset 0x020 ............................................................ 765
Register 9: GPTM Interrupt Clear (GPTMICR), offset 0x024 ...................................................................... 768
Register 10: GPTM Timer A Interval Load (GPTMTAILR), offset 0x028 ........................................................... 770
Register 11: GPTM Timer B Interval Load (GPTMTBILR), offset 0x02C ........................................................... 771
Register 12: GPTM Timer A Match (GPTMTAMATCHR), offset 0x030 ........................................................... 772
Register 13: GPTM Timer B Match (GPTMTBMATCHR), offset 0x034 ........................................................... 773
Register 14: GPTM Timer A Prescale (GPTMTAPR), offset 0x038 ............................................................... 774
Register 15: GPTM Timer B Prescale (GPTMTBPR), offset 0x03C ............................................................... 775
Register 16: GPTM TimerA Prescale Match (GPTMTAPMR), offset 0x040 ................................................... 776
Register 17: GPTM TimerB Prescale Match (GPTMTBPMR), offset 0x044 ................................................... 777
Register 18: GPTM Timer A (GPTMTAR), offset 0x048 .............................................................................. 778
Register 19: GPTM Timer B (GPTMTBR), offset 0x04C .............................................................................. 779
Register 20: GPTM Timer A Value (GPTMTAV), offset 0x050 ....................................................................... 780
Register 21: GPTM Timer B Value (GPTMTBV), offset 0x054 ....................................................................... 781
Register 22: GPTM RTC Predivide (GPTMRTCPD), offset 0x058 ................................................................. 782
Register 23: GPTM Timer A Prescale Snapshot (GPTMTAPS), offset 0x05C ................................................... 783
Register 24: GPTM Timer B Prescale Snapshot (GPTMTBPS), offset 0x060 ................................................... 784
Register 25: GPTM Timer A Prescale Value (GPTMTAPV), offset 0x064 ...................................................... 785
Register 26: GPTM Timer B Prescale Value (GPTMTBPV), offset 0x068 ...................................................... 786
Register 27: GPTM Peripheral Properties (GPTMPP), offset 0xFC0 ............................................................. 787

Watchdog Timers ........................................................................................................................................... 788
Register 1: Watchdog Load (WDTLOAD), offset 0x000 ................................................................................. 792
Register 2: Watchdog Value (WDTVALUE), offset 0x004 .......................................................................... 793
Register 3: Watchdog Control (WDTCTL), offset 0x008 .......................................................................... 794
Register 4: Watchdog Interrupt Clear (WDTICR), offset 0x00C ................................................................. 796
Register 5: Watchdog Raw Interrupt Status (WDRIS), offset 0x010 ............................................................ 797
Register 6: Watchdog Masked Interrupt Status (WDMIS), offset 0x014 ..................................................... 798
Register 7: Watchdog Test (WDTTEST), offset 0x418 ................................................................................. 799
Register 8: Watchdog Lock (WDTLOCK), offset 0xC00 ............................................................................. 800
Register 9: Watchdog Peripheral Identification 4 (WDTPeriphID4), offset 0xFD0 ....................................... 801
Register 10: Watchdog Peripheral Identification 5 (WDTPeriphID5), offset 0xFD4 ..................................... 802
Register 11: Watchdog Peripheral Identification 6 (WDTPeriphID6), offset 0xFD8 ..................................... 803
Register 12: Watchdog Peripheral Identification 7 (WDTPeriphID7), offset 0xFD ........................................ 804
Register 13: Watchdog Peripheral Identification 0 (WDTPeriphID0), offset 0xFE0 ........................................ 805
Register 14: Watchdog Peripheral Identification 1 (WDTPeriphID1), offset 0xFE4 ........................................ 806
Register 15: Watchdog Peripheral Identification 2 (WDTPeriphID2), offset 0xFE8 ........................................ 807
Register 16: Watchdog Peripheral Identification 3 (WDTPeriphID3), offset 0xFEC ........................................ 808
Register 17: Watchdog PrimeCell Identification 0 (WDTPCellID0), offset 0xFF0 ........................................ 809
Register 18: Watchdog PrimeCell Identification 1 (WDTPCellID1), offset 0xFF4 ........................................ 810
Register 19: Watchdog PrimeCell Identification 2 (WDTPCellID2), offset 0xFF8 ........................................ 811
Register 20: Watchdog PrimeCell Identification 3 (WDTPCellID3 ), offset 0xFFC ........................................ 812

Analog-to-Digital Converter (ADC) ............................................................................................................. 813
Register 1: ADC Active Sample Sequencer (ADCACTSS), offset 0x000 ..................................................... 835
Register 2: ADC Raw Interrupt Status (ADCRIS), offset 0x004 ................................................................. 837
Register 3: ADC Interrupt Mask (ADCIM), offset 0x008 .......................................................................... 839
Register 4: ADC Interrupt Status and Clear (ADCSIC), offset 0x00C ......................................................... 842
Register 5: ADC Overflow Status (ADCOSTAT), offset 0x010 ............................................................... 845
Register 6: ADC Event Multiplexer Select (ADCEMUX), offset 0x014 .............................................................. 887
Register 7: ADC Underflow Status (ADCUSTAT), offset 0x018 ................................................................. 882
Register 8: ADC Trigger Source Select (ADCTSSSEL), offset 0x01C ............................................................ 883
Register 9: ADC Sample Sequencer Priority (ADCSSPRI), offset 0x020 ...................................................... 885
Register 10: ADC Sample Phase Control (ADCSPC), offset 0x024 .............................................................. 887
Register 11: ADC Processor Sample Sequence Initiate (ADCPSSI), offset 0x028 ............................................ 889
Register 12: ADC Sample Averaging Control (ADCSAC), offset 0x030 ...................................................... 881
Register 13: ADC Digital Comparator Interrupt Status and Clear (ADCDCISC), offset 0x034 ..................... 882
Register 14: ADC Control (ADCCTL), offset 0x038 ..................................................................................... 884
Register 15: ADC Sample Sequence Input Multiplexer Select 0 (ADCSSMUX0), offset 0x040 ................. 885
Register 16: ADC Sample Sequence Control 0 (ADCSSCTL0), offset 0x044 .................................................. 887
Register 17: ADC Sample Sequence Result FIFO 0 (ADCSSFIFO0), offset 0x048 ........................................ 874
Register 18: ADC Sample Sequence Result FIFO 1 (ADCSSFIFO1), offset 0x068 ........................................ 874
Register 19: ADC Sample Sequence Result FIFO 2 (ADCSSFIFO2), offset 0x088 ........................................ 874
Register 20: ADC Sample Sequence Result FIFO 3 (ADCSSFIFO3), offset 0x0A8 ........................................ 874
Register 21: ADC Sample Sequence FIFO 0 Status (ADCSSFSTAT0), offset 0x0C ........................................ 876
Register 22: ADC Sample Sequence FIFO 1 Status (ADCSSFSTAT1), offset 0x0E ........................................ 876
Register 23: ADC Sample Sequence FIFO 2 Status (ADCSSFSTAT2), offset 0x0E ........................................ 876
Register 24: ADC Sample Sequence FIFO 3 Status (ADCSSFSTAT3), offset 0x0F ........................................ 876
Register 25: ADC Sample Sequence FIFO 0 Operation (ADCSSFOP0), offset 0x050 .............................. 877
Register 26: ADC Sample Sequence FIFO 1 Digital Comparator Select (ADCSSFDC0), offset 0x054 ...... 879
Register 27: ADC Sample Sequence FIFO 1 Digital Comparator Select (ADCSSFDC1), offset 0x054 ...... 879
Register 28: ADC Sample Sequence FIFO 2 Digital Comparator Select (ADCSSFDC2), offset 0x054 ...... 879
Register 29: ADC Sample Sequence FIFO 3 Digital Comparator Select (ADCSSFDC3), offset 0x054 ...... 879
Register 30: ADC Sample Sequence FIFO 0 Operation (ADCSSFOP0), offset 0x050 .............................. 877
Register 31: ADC Sample Sequence FIFO 1 Operation (ADCSSFOP1), offset 0x070 .............................. 888
Register 32: ADC Sample Sequence FIFO 2 Operation (ADCSSFOP2), offset 0x090 .............................. 888
Register 33: ADC Sample Sequence FIFO 3 Operation (ADCSSFOP3), offset 0x0B0 .............................. 896
Register 34: ADC Sample Sequence FIFO 1 Digital Comparator Select (ADCSSFDC1), offset 0x074 ...... 889
Register 35: ADC Sample Sequence FIFO 2 Digital Comparator Select (ADCSSFDC2), offset 0x094 ...... 889
Register 36: ADC Sample Sequence FIFO 3 Digital Comparator Select (ADCSSFDC3), offset 0x0B4 ...... 897
Register 37: ADC Sample Sequence FIFO 1 Digital Comparator Select (ADCSSFDC0), offset 0x054 ...... 879
Register 38: ADC Sample Sequence FIFO 2 Digital Comparator Select (ADCSSFDC2), offset 0x054 ...... 879
Register 39: ADC Sample Sequence FIFO 3 Digital Comparator Select (ADCSSFDC3), offset 0x054 ...... 879
Register 40: ADC Sample Sequence FIFO 0 Operation (ADCSSFOP0), offset 0x050 .............................. 877
Register 41: ADC Sample Sequence FIFO 1 Operation (ADCSSFOP1), offset 0x070 .............................. 888
Register 42: ADC Sample Sequence FIFO 2 Operation (ADCSSFOP2), offset 0x090 .............................. 888
Register 43: ADC Sample Sequence FIFO 3 Operation (ADCSSFOP3), offset 0x0B0 .............................. 896
Register 44: ADC Sample Sequence FIFO 0 Operation (ADCSSFOP0), offset 0x050 .............................. 877
Register 45: ADC Sample Sequence FIFO 1 Operation (ADCSSFOP1), offset 0x070 .............................. 888
Register 46: ADC Sample Sequence FIFO 2 Operation (ADCSSFOP2), offset 0x090 .............................. 888
Register 47: ADC Sample Sequence FIFO 3 Operation (ADCSSFOP3), offset 0x0B0 .............................. 896
Register 48: ADC Sample Sequence FIFO 3 Operation (ADCSSFOP3), offset 0x0B0 .............................. 896
Register 49: ADC Sample Sequence FIFO 0 Operation (ADCSSFOP0), offset 0x050 .............................. 877
Register 50: ADC Sample Sequence FIFO 1 Operation (ADCSSFOP1), offset 0x070 .............................. 888
Register 51: ADC Sample Sequence FIFO 2 Operation (ADCSSFOP2), offset 0x090 .............................. 888
Register 52: ADC Sample Sequence FIFO 3 Operation (ADCSSFOP3), offset 0x0B0 .............................. 896
Register 53: ADC Sample Sequence FIFO 0 Operation (ADCSSFOP0), offset 0x050 .............................. 877
Register 54: ADC Sample Sequence FIFO 1 Operation (ADCSSFOP1), offset 0x070 .............................. 888
Register 55: ADC Sample Sequence FIFO 2 Operation (ADCSSFOP2), offset 0x090 .............................. 888
Register 56: ADC Sample Sequence FIFO 3 Operation (ADCSSFOP3), offset 0x0B0 .............................. 896
Register 57: ADC Sample Sequence FIFO 0 Operation (ADCSSFOP0), offset 0x050 .............................. 877
Register 58: ADC Sample Sequence FIFO 1 Operation (ADCSSFOP1), offset 0x070 .............................. 888
Register 59: ADC Sample Sequence FIFO 2 Operation (ADCSSFOP2), offset 0x090 .............................. 888
Register 60: ADC Sample Sequence FIFO 3 Operation (ADCSSFOP3), offset 0x0B0 .............................. 896
Register 61: ADC Sample Sequence FIFO 0 Operation (ADCSSFOP0), offset 0x050 .............................. 877
Register 62: ADC Sample Sequence FIFO 1 Operation (ADCSSFOP1), offset 0x070 .............................. 888
Register 63: ADC Sample Sequence FIFO 2 Operation (ADCSSFOP2), offset 0x090 .............................. 888
Register 64: ADC Sample Sequence FIFO 3 Operation (ADCSSFOP3), offset 0x0B0 .............................. 896

Texas Instruments-Production Data
Register 51: ADC Digital Comparator Control 7 (ADCDCTL7), offset 0xE1C .................................................. 904
Register 52: ADC Digital Comparator Range 0 (ADCDCCMP0), offset 0xE40 ............................................. 907
Register 53: ADC Digital Comparator Range 1 (ADCDCCMP1), offset 0xE44 .................................................. 907
Register 54: ADC Digital Comparator Range 2 (ADCDCCMP2), offset 0xE48 .................................................. 907
Register 55: ADC Digital Comparator Range 3 (ADCDCCMP3), offset 0xE4C .................................................. 907
Register 56: ADC Digital Comparator Range 4 (ADCDCCMP4), offset 0xE50 .................................................. 907
Register 57: ADC Digital Comparator Range 5 (ADCDCCMP5), offset 0xE54 .................................................. 907
Register 58: ADC Digital Comparator Range 6 (ADCDCCMP6), offset 0xE58 .................................................. 907
Register 59: ADC Digital Comparator Range 7 (ADCDCCMP7), offset 0xE5C .................................................. 907
Register 60: ADC Peripheral Properties (ADCPP), offset 0xFC0 ................................................................. 908
Register 61: ADC Peripheral Configuration (ADCCP), offset 0xFC4 ............................................................. 910
Register 62: ADC Clock Configuration (ADCCC), offset 0xFC8 ................................................................. 911

Universal Asynchronous Receivers/Transmitters (UARTs) ............................................................................... 912
Register 1: UART Data (UARTDR), offset 0x000 ...................................................................................... 926
Register 2: UART Receive Status/Error Clear (UARTRSR/UARTECR), offset 0x004 ................................. 928
Register 3: UART Flag (UARTFR), offset 0x018 ...................................................................................... 931
Register 4: UART IrDA Low-Power Register (UARTILPR), offset 0x020 ..................................................... 934
Register 5: UART Integer Baud-Rate Divisor (UARTIBRD), offset 0x024 ..................................................... 935
Register 6: UART Fractional Baud-Rate Divisor (UARTFBRD), offset 0x028 .................................................. 936
Register 7: UART Line Control (UARTRCRL), offset 0x02C ................................................................. 937
Register 8: UART Control (UARTCTL), offset 0x030 .................................................................................. 939
Register 9: UART Interrupt FIFO Level Select (UARTIFLS), offset 0x034 ..................................................... 943
Register 10: UART Interrupt Mask (UARTIM), offset 0x038 ....................................................................... 945
Register 11: UART Raw Interrupt Status (UARTRIS), offset 0x03C ............................................................ 948
Register 12: UART Masked Interrupt Status (UARTMIS), offset 0x040 ....................................................... 951
Register 13: UART Interrupt Clear (UARTICR), offset 0x044 ................................................................. 954
Register 14: UART DMA Control (UARTDMACTL), offset 0x048 ............................................................. 956
Register 15: UART 9-Bit Self Address (UART9BITADDR), offset 0x0A4 ..................................................... 957
Register 16: UART 9-Bit Self Address Mask (UART9BITAMASK), offset 0x0A8 .............................................. 958
Register 17: UART Peripheral Properties (UARTPP), offset 0xFC0 ........................................................ 959
Register 18: UART Clock Configuration (UARTCC), offset 0xFC8 .......................................................... 960
Register 19: UART Peripheral Identification 4 (UARTPeriphID4), offset 0xFD0 .............................................. 961
Register 20: UART Peripheral Identification 5 (UARTPeriphID5), offset 0xFD4 .............................................. 962
Register 21: UART Peripheral Identification 6 (UARTPeriphID6), offset 0xFD8 .............................................. 963
Register 22: UART Peripheral Identification 7 (UARTPeriphID7), offset 0xFD9 .............................................. 964
Register 23: UART Peripheral Identification 0 (UARTPeriphID0), offset 0xFE0 .............................................. 965
Register 24: UART Peripheral Identification 1 (UARTPeriphID1), offset 0xFE4 .............................................. 966
Register 25: UART Peripheral Identification 2 (UARTPeriphID2), offset 0xFE8 .............................................. 967
Register 26: UART Peripheral Identification 3 (UARTPeriphID3), offset 0xFEC .............................................. 968
Register 27: UART PrimeCell Identification 0 (UARTPrimeCellID0), offset 0xFFF0 ........................................ 969
Register 28: UART PrimeCell Identification 1 (UARTPrimeCellID1), offset 0xFFF4 ........................................ 970
Register 29: UART PrimeCell Identification 2 (UARTPrimeCellID2), offset 0xFFF8 ........................................ 971
Register 30: UART PrimeCell Identification 3 (UARTPrimeCellID3), offset 0xFFC ........................................ 972

Synchronous Serial Interface (SSI) ................................................................................................................ 973
Register 1: SSI Control 0 (SSICR0), offset 0x000 ...................................................................................... 990
Register 2: SSI Control 1 (SSICR1), offset 0x004 ...................................................................................... 992
Register 3: SSI Data (SSIDR), offset 0x008 .......................................................................................... 994
Register 4: SSI Status (SSISR), offset 0x00C ...................................................................................... 995
### Controller Area Network (CAN) Module

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CAN Control (CANCTL), offset 0x000</td>
<td>1091</td>
</tr>
<tr>
<td>2</td>
<td>CAN Status (CANSTS), offset 0x004</td>
<td>1093</td>
</tr>
<tr>
<td>3</td>
<td>CAN Error Counter (CANERR), offset 0x008</td>
<td>1096</td>
</tr>
<tr>
<td>4</td>
<td>CAN Masked Interrupt Status (CANMIS), offset 0x014</td>
<td>1001</td>
</tr>
<tr>
<td>5</td>
<td>CAN Raw Interrupt Status (CANRIS), offset 0x018</td>
<td>999</td>
</tr>
<tr>
<td>6</td>
<td>CAN Interrupt Clear (CANICR), offset 0x020</td>
<td>1003</td>
</tr>
<tr>
<td>7</td>
<td>CAN Masked Interrupt Clear (CANMCLR), offset 0x024</td>
<td>1004</td>
</tr>
<tr>
<td>8</td>
<td>CAN Raw Interrupt Clear (CANNCLR), offset 0x028</td>
<td>1005</td>
</tr>
<tr>
<td>9</td>
<td>CAN Interrupt Mask (CANIM), offset 0x030</td>
<td>1006</td>
</tr>
<tr>
<td>10</td>
<td>CAN Masked Interrupt Mask (CANMIM), offset 0x034</td>
<td>1008</td>
</tr>
<tr>
<td>11</td>
<td>CAN Raw Interrupt Mask (CANRMK), offset 0x038</td>
<td>1009</td>
</tr>
<tr>
<td>12</td>
<td>CAN Error Mask (CANE), offset 0x040</td>
<td>1010</td>
</tr>
<tr>
<td>13</td>
<td>CAN Masked Error (CANME), offset 0x044</td>
<td>1011</td>
</tr>
<tr>
<td>14</td>
<td>CAN Error Counter 2 (CANER2), offset 0x048</td>
<td>1012</td>
</tr>
<tr>
<td>15</td>
<td>CAN Error Counter 1 (CANER1), offset 0x050</td>
<td>1013</td>
</tr>
<tr>
<td>16</td>
<td>CAN Error Counter 0 (CANER0), offset 0x052</td>
<td>1014</td>
</tr>
</tbody>
</table>

### Inter-Integrated Circuit (I²C) Interface

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I²C Master Slave Address (I2CMSA), offset 0x000</td>
<td>1040</td>
</tr>
<tr>
<td>2</td>
<td>I²C Master Control/Status (I2CMCS), offset 0x004</td>
<td>1041</td>
</tr>
<tr>
<td>3</td>
<td>I²C Master Data (I2CMDR), offset 0x008</td>
<td>1046</td>
</tr>
<tr>
<td>4</td>
<td>I²C Master Timer Period (I2CMTPR), offset 0x00C</td>
<td>1047</td>
</tr>
<tr>
<td>5</td>
<td>I²C Master Interrupt Mask (I2CMIMR), offset 0x010</td>
<td>1048</td>
</tr>
<tr>
<td>6</td>
<td>I²C Master Raw Interrupt Status (I2CMRIS), offset 0x014</td>
<td>1049</td>
</tr>
<tr>
<td>7</td>
<td>I²C Master Masked Interrupt Status (I2CMMIS), offset 0x018</td>
<td>1050</td>
</tr>
<tr>
<td>8</td>
<td>I²C Master Interrupt Clear (I2CMICR), offset 0x01C</td>
<td>1051</td>
</tr>
<tr>
<td>9</td>
<td>I²C Master Configuration (I2CMCR), offset 0x020</td>
<td>1052</td>
</tr>
<tr>
<td>10</td>
<td>I²C Master Clock Low Timeout Count (I2CMCLKOCNT), offset 0x024</td>
<td>1054</td>
</tr>
<tr>
<td>11</td>
<td>I²C Master Bus Monitor (I2CMBMON), offset 0x02C</td>
<td>1055</td>
</tr>
<tr>
<td>12</td>
<td>I²C Master Configuration 2 (I2CMCR2), offset 0x038</td>
<td>1056</td>
</tr>
<tr>
<td>13</td>
<td>I²C Slave Own Address (I2CSOAR), offset 0x800</td>
<td>1057</td>
</tr>
<tr>
<td>14</td>
<td>I²C Slave Control/Status (I2CSCSR), offset 0x804</td>
<td>1058</td>
</tr>
<tr>
<td>15</td>
<td>I²C Slave Data (I2CSDR), offset 0x808</td>
<td>1060</td>
</tr>
<tr>
<td>16</td>
<td>I²C Slave Interrupt Mask (I2CSIMR), offset 0x80C</td>
<td>1061</td>
</tr>
<tr>
<td>17</td>
<td>I²C Slave Raw Interrupt Status (I2CSRIS), offset 0x810</td>
<td>1062</td>
</tr>
<tr>
<td>18</td>
<td>I²C Slave Masked Interrupt Status (I2CSMIS), offset 0x814</td>
<td>1063</td>
</tr>
<tr>
<td>19</td>
<td>I²C Slave Interrupt Clear (I2CSTCLR), offset 0x818</td>
<td>1064</td>
</tr>
<tr>
<td>20</td>
<td>I²C Slave Own Address 2 (I2CSOAR2), offset 0x81C</td>
<td>1065</td>
</tr>
<tr>
<td>21</td>
<td>I²C Slave ACK Control (I2CSACKCTL), offset 0x820</td>
<td>1066</td>
</tr>
<tr>
<td>22</td>
<td>I²C Peripheral Properties (I2CPP), offset 0xFD0</td>
<td>1067</td>
</tr>
<tr>
<td>23</td>
<td>I²C Peripheral Configuration (I2CPC), offset 0xFFC</td>
<td>1068</td>
</tr>
</tbody>
</table>

---

**Texas Instruments-Production Data**

June 12, 2014
<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>CAN Baud Rate Prescaler Extension (CANBRPE),</td>
<td>0x014</td>
</tr>
<tr>
<td>0x001</td>
<td>CAN Message 1 Valid (CANIF1MSK1),</td>
<td>0x028</td>
</tr>
<tr>
<td>0x002</td>
<td>CAN Message 1 Interrupt Pending (CANIF1MCTL),</td>
<td>0x030</td>
</tr>
<tr>
<td>0x003</td>
<td>CAN New Data 1 (CANIF1DA1),</td>
<td>0x038</td>
</tr>
<tr>
<td>0x004</td>
<td>CAN Transmission Request 1 (CANIF1CRQ),</td>
<td>0x040</td>
</tr>
<tr>
<td>0x005</td>
<td>CAN Transmission Request 2 (CANIF1CRQ),</td>
<td>0x044</td>
</tr>
<tr>
<td>0x006</td>
<td>CAN Message 1 Valid (CANIF1MSK1),</td>
<td>0x048</td>
</tr>
<tr>
<td>0x007</td>
<td>CAN Test (CANTST),</td>
<td>0x052</td>
</tr>
<tr>
<td>0x008</td>
<td>CAN Interrupt (CANINT),</td>
<td>0x060</td>
</tr>
<tr>
<td>0x009</td>
<td>CAN Bit Timing (CANBIT),</td>
<td>0x064</td>
</tr>
<tr>
<td>0x00A</td>
<td>CAN Power (USBPOWER),</td>
<td>0x070</td>
</tr>
<tr>
<td>0x00B</td>
<td>CAN Transmit Interrupt Status (USBTXIS),</td>
<td>0x074</td>
</tr>
<tr>
<td>0x00C</td>
<td>CAN Receive Interrupt Status (USBRXIS),</td>
<td>0x078</td>
</tr>
<tr>
<td>0x00D</td>
<td>CAN Transmit Interrupt Enable (USBTXIE),</td>
<td>0x080</td>
</tr>
<tr>
<td>0x00E</td>
<td>CAN Receive Interrupt Enable (USBRXIE),</td>
<td>0x084</td>
</tr>
<tr>
<td>0x00F</td>
<td>CAN General Interrupt Status (USBIS),</td>
<td>0x088</td>
</tr>
<tr>
<td>0x010</td>
<td>CAN Interrupt Enable (USBIE),</td>
<td>0x090</td>
</tr>
<tr>
<td>0x011</td>
<td>CAN Frame Value (USBFRAME),</td>
<td>0x094</td>
</tr>
<tr>
<td>0x012</td>
<td>CAN Endpoint Index (USBEPIDX),</td>
<td>0x098</td>
</tr>
<tr>
<td>0x013</td>
<td>CAN Test Mode (USBTEST),</td>
<td>0x0A0</td>
</tr>
<tr>
<td>0x014</td>
<td>CAN FIFO Endpoint 0 (USBFIFO0),</td>
<td>0x0A4</td>
</tr>
<tr>
<td>0x015</td>
<td>CAN FIFO Endpoint 1 (USBFIFO1),</td>
<td>0x0A8</td>
</tr>
<tr>
<td>0x016</td>
<td>CAN FIFO Endpoint 2 (USBFIFO2),</td>
<td>0x0B0</td>
</tr>
<tr>
<td>0x017</td>
<td>CAN FIFO Endpoint 3 (USBFIFO3),</td>
<td>0x0B4</td>
</tr>
<tr>
<td>0x018</td>
<td>CAN FIFO Endpoint 4 (USBFIFO4),</td>
<td>0x0B8</td>
</tr>
<tr>
<td>0x019</td>
<td>CAN FIFO Endpoint 5 (USBFIFO5),</td>
<td>0x0C0</td>
</tr>
<tr>
<td>0x01A</td>
<td>CAN FIFO Endpoint 6 (USBFIFO6),</td>
<td>0x0C4</td>
</tr>
<tr>
<td>0x01B</td>
<td>CAN FIFO Endpoint 7 (USBFIFO7),</td>
<td>0x0C8</td>
</tr>
<tr>
<td>0x01C</td>
<td>CAN FIFO Endpoint 8 (USBFIFO8),</td>
<td>0x0D0</td>
</tr>
<tr>
<td>0x01D</td>
<td>CAN FIFO Endpoint 9 (USBFIFO9),</td>
<td>0x0D4</td>
</tr>
<tr>
<td>0x01E</td>
<td>CAN FIFO Endpoint 10 (USBFIFO10),</td>
<td>0x0D8</td>
</tr>
<tr>
<td>0x01F</td>
<td>CAN FIFO Endpoint 11 (USBFIFO11),</td>
<td>0x0E0</td>
</tr>
<tr>
<td>0x020</td>
<td>CAN FIFO Endpoint 0 (USBFIFO0),</td>
<td>0x0E4</td>
</tr>
<tr>
<td>0x021</td>
<td>CAN FIFO Endpoint 1 (USBFIFO1),</td>
<td>0x0E8</td>
</tr>
<tr>
<td>0x022</td>
<td>CAN FIFO Endpoint 2 (USBFIFO2),</td>
<td>0x0F0</td>
</tr>
<tr>
<td>0x023</td>
<td>CAN FIFO Endpoint 3 (USBFIFO3),</td>
<td>0x0F4</td>
</tr>
<tr>
<td>0x024</td>
<td>CAN FIFO Endpoint 4 (USBFIFO4),</td>
<td>0x0F8</td>
</tr>
<tr>
<td>0x025</td>
<td>CAN FIFO Endpoint 5 (USBFIFO5),</td>
<td>0x100</td>
</tr>
<tr>
<td>0x026</td>
<td>CAN FIFO Endpoint 6 (USBFIFO6),</td>
<td>0x104</td>
</tr>
<tr>
<td>0x027</td>
<td>CAN FIFO Endpoint 7 (USBFIFO7),</td>
<td>0x108</td>
</tr>
<tr>
<td>0x028</td>
<td>CAN FIFO Endpoint 8 (USBFIFO8),</td>
<td>0x110</td>
</tr>
<tr>
<td>0x029</td>
<td>CAN FIFO Endpoint 9 (USBFIFO9),</td>
<td>0x114</td>
</tr>
<tr>
<td>0x02A</td>
<td>CAN FIFO Endpoint 10 (USBFIFO10),</td>
<td>0x118</td>
</tr>
<tr>
<td>0x02B</td>
<td>CAN FIFO Endpoint 11 (USBFIFO11),</td>
<td>0x120</td>
</tr>
<tr>
<td>0x02C</td>
<td>CAN FIFO Endpoint 12 (USBFIFO12),</td>
<td>0x124</td>
</tr>
<tr>
<td>0x02D</td>
<td>CAN FIFO Endpoint 13 (USBFIFO13),</td>
<td>0x128</td>
</tr>
<tr>
<td>0x02E</td>
<td>CAN FIFO Endpoint 14 (USBFIFO14),</td>
<td>0x130</td>
</tr>
<tr>
<td>0x02F</td>
<td>CAN FIFO Endpoint 15 (USBFIFO15),</td>
<td>0x134</td>
</tr>
</tbody>
</table>

**Universal Serial Bus (USB) Controller**

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>USB Device Functional Address (USBFADDR),</td>
<td>0x000</td>
</tr>
<tr>
<td>0x001</td>
<td>USB Power (USBPOWER),</td>
<td>0x001</td>
</tr>
<tr>
<td>0x002</td>
<td>USB Transmit Interrupt Status (USBTXIS),</td>
<td>0x002</td>
</tr>
<tr>
<td>0x003</td>
<td>USB Receive Interrupt Status (USBRXIS),</td>
<td>0x004</td>
</tr>
<tr>
<td>0x004</td>
<td>USB Transmit Interrupt Enable (USBTXIE),</td>
<td>0x006</td>
</tr>
<tr>
<td>0x005</td>
<td>USB Receive Interrupt Enable (USBRXIE),</td>
<td>0x008</td>
</tr>
<tr>
<td>0x006</td>
<td>USB General Interrupt Status (USBIS),</td>
<td>0x00A</td>
</tr>
<tr>
<td>0x007</td>
<td>USB Interrupt Enable (USBIE),</td>
<td>0x00B</td>
</tr>
<tr>
<td>0x008</td>
<td>USB Frame Value (USBFRAME),</td>
<td>0x00C</td>
</tr>
<tr>
<td>0x009</td>
<td>USB Endpoint Index (USBEPIDX),</td>
<td>0x00E</td>
</tr>
<tr>
<td>0x00A</td>
<td>USB Test Mode (USBTEST),</td>
<td>0x00F</td>
</tr>
<tr>
<td>0x00B</td>
<td>USB FIFO Endpoint 0 (USBFIFO0),</td>
<td>0x020</td>
</tr>
<tr>
<td>0x00C</td>
<td>USB FIFO Endpoint 1 (USBFIFO1),</td>
<td>0x024</td>
</tr>
<tr>
<td>0x00D</td>
<td>USB FIFO Endpoint 2 (USBFIFO2),</td>
<td>0x028</td>
</tr>
<tr>
<td>0x00E</td>
<td>USB FIFO Endpoint 3 (USBFIFO3),</td>
<td>0x02C</td>
</tr>
<tr>
<td>0x00F</td>
<td>USB FIFO Endpoint 4 (USBFIFO4),</td>
<td>0x030</td>
</tr>
</tbody>
</table>

---

*Texas Instruments-Production Data*

June 12, 2014
<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>USB FIFO Endpoint 2 (USBFIFO2)</td>
<td>0x028</td>
</tr>
<tr>
<td>15</td>
<td>USB FIFO Endpoint 3 (USBFIFO3)</td>
<td>0x02C</td>
</tr>
<tr>
<td>16</td>
<td>USB FIFO Endpoint 4 (USBFIFO4)</td>
<td>0x030</td>
</tr>
<tr>
<td>17</td>
<td>USB FIFO Endpoint 5 (USBFIFO5)</td>
<td>0x034</td>
</tr>
<tr>
<td>18</td>
<td>USB FIFO Endpoint 6 (USBFIFO6)</td>
<td>0x038</td>
</tr>
<tr>
<td>19</td>
<td>USB FIFO Endpoint 7 (USBFIFO7)</td>
<td>0x03C</td>
</tr>
<tr>
<td>20</td>
<td>USB Device Control (USBDVECTL)</td>
<td>0x060</td>
</tr>
<tr>
<td>21</td>
<td>USB Transmit Dynamic FIFO Sizing (USBTXFIFOSZ)</td>
<td>0x062</td>
</tr>
<tr>
<td>22</td>
<td>USB Receive Dynamic FIFO Sizing (USBRXFIFOSZ)</td>
<td>0x063</td>
</tr>
<tr>
<td>23</td>
<td>USB Transmit FIFO Start Address (USBTXIFOADD)</td>
<td>0x064</td>
</tr>
<tr>
<td>24</td>
<td>USB Receive FIFO Start Address (USBRXIFOADD)</td>
<td>0x066</td>
</tr>
<tr>
<td>25</td>
<td>USB Connect Timing (USBCONTIM)</td>
<td>0x07A</td>
</tr>
<tr>
<td>26</td>
<td>USB OTG VBUS Pulse Timing (USBVPLEN)</td>
<td>0x07B</td>
</tr>
<tr>
<td>27</td>
<td>USB Full-Speed Last Transaction to End of Frame Timing (USBFSEOF)</td>
<td>0x07D</td>
</tr>
<tr>
<td>28</td>
<td>USB Low-Speed Last Transaction to End of Frame Timing (USBLSEOF)</td>
<td>0x07E</td>
</tr>
<tr>
<td>29</td>
<td>USB Transmit Functional Address Endpoint 0 (USBTXFUNCADDR0)</td>
<td>0x080</td>
</tr>
<tr>
<td>30</td>
<td>USB Transmit Functional Address Endpoint 1 (USBTXFUNCADDR1)</td>
<td>0x088</td>
</tr>
<tr>
<td>31</td>
<td>USB Transmit Functional Address Endpoint 2 (USBTXFUNCADDR2)</td>
<td>0x090</td>
</tr>
<tr>
<td>32</td>
<td>USB Transmit Functional Address Endpoint 3 (USBTXFUNCADDR3)</td>
<td>0x098</td>
</tr>
<tr>
<td>33</td>
<td>USB Transmit Functional Address Endpoint 4 (USBTXFUNCADDR4)</td>
<td>0x0A0</td>
</tr>
<tr>
<td>34</td>
<td>USB Transmit Functional Address Endpoint 5 (USBTXFUNCADDR5)</td>
<td>0x0A8</td>
</tr>
<tr>
<td>35</td>
<td>USB Transmit Functional Address Endpoint 6 (USBTXFUNCADDR6)</td>
<td>0x0B0</td>
</tr>
<tr>
<td>36</td>
<td>USB Transmit Functional Address Endpoint 7 (USBTXFUNCADDR7)</td>
<td>0x0B8</td>
</tr>
<tr>
<td>37</td>
<td>USB Transmit Hub Address Endpoint 0 (USBTXHUBADDRO)</td>
<td>0x082</td>
</tr>
<tr>
<td>38</td>
<td>USB Transmit Hub Address Endpoint 1 (USBTXHUBADDR1)</td>
<td>0x08A</td>
</tr>
<tr>
<td>39</td>
<td>USB Transmit Hub Address Endpoint 2 (USBTXHUBADDR2)</td>
<td>0x092</td>
</tr>
<tr>
<td>40</td>
<td>USB Transmit Hub Address Endpoint 3 (USBTXHUBADDR3)</td>
<td>0x09A</td>
</tr>
<tr>
<td>41</td>
<td>USB Transmit Hub Address Endpoint 4 (USBTXHUBADDR4)</td>
<td>0x0A2</td>
</tr>
<tr>
<td>42</td>
<td>USB Transmit Hub Address Endpoint 5 (USBTXHUBADDR5)</td>
<td>0x0AA</td>
</tr>
<tr>
<td>43</td>
<td>USB Transmit Hub Address Endpoint 6 (USBTXHUBADDR6)</td>
<td>0x0B2</td>
</tr>
<tr>
<td>44</td>
<td>USB Transmit Hub Address Endpoint 7 (USBTXHUBADDR7)</td>
<td>0x0BA</td>
</tr>
<tr>
<td>45</td>
<td>USB Transmit Hub Port Endpoint 0 (USBTXHUBPORT0)</td>
<td>0x083</td>
</tr>
<tr>
<td>46</td>
<td>USB Transmit Hub Port Endpoint 1 (USBTXHUBPORT1)</td>
<td>0x08B</td>
</tr>
<tr>
<td>47</td>
<td>USB Transmit Hub Port Endpoint 2 (USBTXHUBPORT2)</td>
<td>0x093</td>
</tr>
<tr>
<td>48</td>
<td>USB Transmit Hub Port Endpoint 3 (USBTXHUBPORT3)</td>
<td>0x09B</td>
</tr>
<tr>
<td>49</td>
<td>USB Transmit Hub Port Endpoint 4 (USBTXHUBPORT4)</td>
<td>0x0A3</td>
</tr>
<tr>
<td>50</td>
<td>USB Transmit Hub Port Endpoint 5 (USBTXHUBPORT5)</td>
<td>0x0AB</td>
</tr>
<tr>
<td>51</td>
<td>USB Transmit Hub Port Endpoint 6 (USBTXHUBPORT6)</td>
<td>0x0B3</td>
</tr>
<tr>
<td>52</td>
<td>USB Transmit Hub Port Endpoint 7 (USBTXHUBPORT7)</td>
<td>0x0BB</td>
</tr>
<tr>
<td>53</td>
<td>USB Receive Functional Address Endpoint 1 (USBRXFUNCADDR1)</td>
<td>0x08C</td>
</tr>
<tr>
<td>54</td>
<td>USB Receive Functional Address Endpoint 2 (USBRXFUNCADDR2)</td>
<td>0x094</td>
</tr>
<tr>
<td>55</td>
<td>USB Receive Functional Address Endpoint 3 (USBRXFUNCADDR3)</td>
<td>0x09C</td>
</tr>
<tr>
<td>56</td>
<td>USB Receive Functional Address Endpoint 4 (USBRXFUNCADDR4)</td>
<td>0x0A4</td>
</tr>
<tr>
<td>57</td>
<td>USB Receive Functional Address Endpoint 5 (USBRXFUNCADDR5)</td>
<td>0x0AC</td>
</tr>
<tr>
<td>58</td>
<td>USB Receive Functional Address Endpoint 6 (USBRXFUNCADDR6)</td>
<td>0x0B4</td>
</tr>
<tr>
<td>59</td>
<td>USB Receive Functional Address Endpoint 7 (USBRXFUNCADDR7)</td>
<td>0x0BC</td>
</tr>
<tr>
<td>60</td>
<td>USB Receive Hub Address Endpoint 1 (USBRXHUBADDR1)</td>
<td>0x08E</td>
</tr>
<tr>
<td>61</td>
<td>USB Receive Hub Address Endpoint 2 (USBRXHUBADDR2)</td>
<td>0x096</td>
</tr>
<tr>
<td>Register</td>
<td>Description</td>
<td>Offset</td>
</tr>
<tr>
<td>------------</td>
<td>--------------------------------------------------</td>
<td>----------</td>
</tr>
<tr>
<td>62</td>
<td>USB Receive Hub Address Endpoint 3 (USBRXHUBADDR3), offset 0x09E</td>
<td>1176</td>
</tr>
<tr>
<td>63</td>
<td>USB Receive Hub Address Endpoint 4 (USBRXHUBADDR4), offset 0x0A6</td>
<td>1176</td>
</tr>
<tr>
<td>64</td>
<td>USB Receive Hub Address Endpoint 5 (USBRXHUBADDR5), offset 0x0AE</td>
<td>1176</td>
</tr>
<tr>
<td>65</td>
<td>USB Receive Hub Address Endpoint 6 (USBRXHUBADDR6), offset 0x0B6</td>
<td>1176</td>
</tr>
<tr>
<td>66</td>
<td>USB Receive Hub Address Endpoint 7 (USBRXHUBADDR7), offset 0x0BE</td>
<td>1176</td>
</tr>
<tr>
<td>67</td>
<td>USB Receive Hub Port Endpoint 1 (USBRXHUBPORT1), offset 0x08F</td>
<td>1177</td>
</tr>
<tr>
<td>68</td>
<td>USB Receive Hub Port Endpoint 2 (USBRXHUBPORT2), offset 0x097</td>
<td>1177</td>
</tr>
<tr>
<td>69</td>
<td>USB Receive Hub Port Endpoint 3 (USBRXHUBPORT3), offset 0x09F</td>
<td>1177</td>
</tr>
<tr>
<td>70</td>
<td>USB Receive Hub Port Endpoint 4 (USBRXHUBPORT4), offset 0x0A7</td>
<td>1177</td>
</tr>
<tr>
<td>71</td>
<td>USB Receive Hub Port Endpoint 5 (USBRXHUBPORT5), offset 0x0AF</td>
<td>1177</td>
</tr>
<tr>
<td>72</td>
<td>USB Receive Hub Port Endpoint 6 (USBRXHUBPORT6), offset 0x0B7</td>
<td>1177</td>
</tr>
<tr>
<td>73</td>
<td>USB Receive Hub Port Endpoint 7 (USBRXHUBPORT7), offset 0x0BF</td>
<td>1177</td>
</tr>
<tr>
<td>74</td>
<td>USB Maximum Transmit Data Endpoint 1 (USBTXMAXP1), offset 0x110</td>
<td>1178</td>
</tr>
<tr>
<td>75</td>
<td>USB Maximum Transmit Data Endpoint 2 (USBTXMAXP2), offset 0x120</td>
<td>1178</td>
</tr>
<tr>
<td>76</td>
<td>USB Maximum Transmit Data Endpoint 3 (USBTXMAXP3), offset 0x130</td>
<td>1178</td>
</tr>
<tr>
<td>77</td>
<td>USB Maximum Transmit Data Endpoint 4 (USBTXMAXP4), offset 0x140</td>
<td>1178</td>
</tr>
<tr>
<td>78</td>
<td>USB Maximum Transmit Data Endpoint 5 (USBTXMAXP5), offset 0x150</td>
<td>1178</td>
</tr>
<tr>
<td>79</td>
<td>USB Maximum Transmit Data Endpoint 6 (USBTXMAXP6), offset 0x160</td>
<td>1178</td>
</tr>
<tr>
<td>80</td>
<td>USB Maximum Transmit Data Endpoint 7 (USBTXMAXP7), offset 0x170</td>
<td>1178</td>
</tr>
<tr>
<td>81</td>
<td>USB Control and Status Endpoint 0 Low (USBCSRLO), offset 0x102</td>
<td>1179</td>
</tr>
<tr>
<td>82</td>
<td>USB Control and Status Endpoint 0 High (USBCSRH0), offset 0x103</td>
<td>1183</td>
</tr>
<tr>
<td>83</td>
<td>USB Receive Byte Count Endpoint 0 (USBCOUNT0), offset 0x108</td>
<td>1185</td>
</tr>
<tr>
<td>84</td>
<td>USB Type Endpoint 0 (USBTYPE0), offset 0x10A</td>
<td>1186</td>
</tr>
<tr>
<td>85</td>
<td>USB NAK Limit (USBNAKLMT), offset 0x10B</td>
<td>1187</td>
</tr>
<tr>
<td>86</td>
<td>USB Transmit Control and Status Endpoint 1 Low (USBTXCSRL1), offset 0x112</td>
<td>1188</td>
</tr>
<tr>
<td>87</td>
<td>USB Transmit Control and Status Endpoint 2 Low (USBTXCSRL2), offset 0x122</td>
<td>1188</td>
</tr>
<tr>
<td>88</td>
<td>USB Transmit Control and Status Endpoint 3 Low (USBTXCSRL3), offset 0x132</td>
<td>1188</td>
</tr>
<tr>
<td>89</td>
<td>USB Transmit Control and Status Endpoint 4 Low (USBTXCSRL4), offset 0x142</td>
<td>1188</td>
</tr>
<tr>
<td>90</td>
<td>USB Transmit Control and Status Endpoint 5 Low (USBTXCSRL5), offset 0x152</td>
<td>1188</td>
</tr>
<tr>
<td>91</td>
<td>USB Transmit Control and Status Endpoint 6 Low (USBTXCSRL6), offset 0x162</td>
<td>1188</td>
</tr>
<tr>
<td>92</td>
<td>USB Transmit Control and Status Endpoint 7 Low (USBTXCSRL7), offset 0x172</td>
<td>1188</td>
</tr>
<tr>
<td>93</td>
<td>USB Transmit Control and Status Endpoint 1 High (USBTXCSRHL), offset 0x113</td>
<td>1192</td>
</tr>
<tr>
<td>94</td>
<td>USB Transmit Control and Status Endpoint 2 High (USBTXCSRHL2), offset 0x123</td>
<td>1192</td>
</tr>
<tr>
<td>95</td>
<td>USB Transmit Control and Status Endpoint 3 High (USBTXCSRHL3), offset 0x133</td>
<td>1192</td>
</tr>
<tr>
<td>96</td>
<td>USB Transmit Control and Status Endpoint 4 High (USBTXCSRHL4), offset 0x143</td>
<td>1192</td>
</tr>
<tr>
<td>97</td>
<td>USB Transmit Control and Status Endpoint 5 High (USBTXCSRHL5), offset 0x153</td>
<td>1192</td>
</tr>
<tr>
<td>98</td>
<td>USB Transmit Control and Status Endpoint 6 High (USBTXCSRHL6), offset 0x163</td>
<td>1192</td>
</tr>
<tr>
<td>99</td>
<td>USB Transmit Control and Status Endpoint 7 High (USBTXCSRHL7), offset 0x173</td>
<td>1192</td>
</tr>
<tr>
<td>100</td>
<td>USB Maximum Receive Data Endpoint 1 (USBRXMAXP1), offset 0x114</td>
<td>1196</td>
</tr>
<tr>
<td>101</td>
<td>USB Maximum Receive Data Endpoint 2 (USBRXMAXP2), offset 0x124</td>
<td>1196</td>
</tr>
<tr>
<td>102</td>
<td>USB Maximum Receive Data Endpoint 3 (USBRXMAXP3), offset 0x134</td>
<td>1196</td>
</tr>
<tr>
<td>103</td>
<td>USB Maximum Receive Data Endpoint 4 (USBRXMAXP4), offset 0x144</td>
<td>1196</td>
</tr>
<tr>
<td>104</td>
<td>USB Maximum Receive Data Endpoint 5 (USBRXMAXP5), offset 0x154</td>
<td>1196</td>
</tr>
<tr>
<td>105</td>
<td>USB Maximum Receive Data Endpoint 6 (USBRXMAXP6), offset 0x164</td>
<td>1196</td>
</tr>
<tr>
<td>106</td>
<td>USB Maximum Receive Data Endpoint 7 (USBRXMAXP7), offset 0x174</td>
<td>1196</td>
</tr>
<tr>
<td>107</td>
<td>USB Receive Control and Status Endpoint 1 Low (USBRXCSRSL1), offset 0x116</td>
<td>1197</td>
</tr>
<tr>
<td>108</td>
<td>USB Receive Control and Status Endpoint 2 Low (USBRXCSRSL2), offset 0x126</td>
<td>1197</td>
</tr>
<tr>
<td>109</td>
<td>USB Receive Control and Status Endpoint 3 Low (USBRXCSRSL3), offset 0x136</td>
<td>1197</td>
</tr>
</tbody>
</table>
Register 110: USB Receive Control and Status Endpoint 4 Low (USBRXCSRL4), offset 0x146 .......... 1197
Register 111: USB Receive Control and Status Endpoint 5 Low (USBRXCSRL5), offset 0x156 .......... 1197
Register 112: USB Receive Control and Status Endpoint 6 Low (USBRXCSRL6), offset 0x166 .......... 1197
Register 113: USB Receive Control and Status Endpoint 7 Low (USBRXCSRL7), offset 0x176 .......... 1197
Register 114: USB Receive Control and Status Endpoint 1 High (USBRXCSRH1), offset 0x117 .......... 1202
Register 115: USB Receive Control and Status Endpoint 2 High (USBRXCSRH2), offset 0x127 .......... 1202
Register 116: USB Receive Control and Status Endpoint 3 High (USBRXCSRH3), offset 0x137 .......... 1202
Register 117: USB Receive Control and Status Endpoint 4 High (USBRXCSRH4), offset 0x147 .......... 1202
Register 118: USB Receive Control and Status Endpoint 5 High (USBRXCSRH5), offset 0x157 .......... 1202
Register 119: USB Receive Control and Status Endpoint 6 High (USBRXCSRH6), offset 0x167 .......... 1202
Register 120: USB Receive Control and Status Endpoint 7 High (USBRXCSRH7), offset 0x177 .......... 1202
Register 121: USB Receive Byte Count Endpoint 1 (USBRXCOUNT1), offset 0x118 ......................... 1206
Register 122: USB Receive Byte Count Endpoint 2 (USBRXCOUNT2), offset 0x128 ......................... 1206
Register 123: USB Receive Byte Count Endpoint 3 (USBRXCOUNT3), offset 0x138 ......................... 1206
Register 124: USB Receive Byte Count Endpoint 4 (USBRXCOUNT4), offset 0x148 ......................... 1206
Register 125: USB Receive Byte Count Endpoint 5 (USBRXCOUNT5), offset 0x158 ......................... 1206
Register 126: USB Receive Byte Count Endpoint 6 (USBRXCOUNT6), offset 0x168 ......................... 1206
Register 127: USB Receive Byte Count Endpoint 7 (USBRXCOUNT7), offset 0x178 ......................... 1206
Register 128: USB Host Transmit Configure Type Endpoint 1 (USBTXTYPE1), offset 0x11A ............. 1207
Register 129: USB Host Transmit Configure Type Endpoint 2 (USBTXTYPE2), offset 0x12A ............. 1207
Register 130: USB Host Transmit Configure Type Endpoint 3 (USBTXTYPE3), offset 0x13A ............. 1207
Register 131: USB Host Transmit Configure Type Endpoint 4 (USBTXTYPE4), offset 0x14A ............. 1207
Register 132: USB Host Transmit Configure Type Endpoint 5 (USBTXTYPE5), offset 0x15A ............. 1207
Register 133: USB Host Transmit Configure Type Endpoint 6 (USBTXTYPE6), offset 0x16A ............. 1207
Register 134: USB Host Transmit Configure Type Endpoint 7 (USBTXTYPE7), offset 0x17A ............. 1207
Register 135: USB Host Transmit Interval Endpoint 1 (USBTXINTERVAL1), offset 0x11B ................. 1209
Register 136: USB Host Transmit Interval Endpoint 2 (USBTXINTERVAL2), offset 0x12B ................. 1209
Register 137: USB Host Transmit Interval Endpoint 3 (USBTXINTERVAL3), offset 0x13B ................. 1209
Register 138: USB Host Transmit Interval Endpoint 4 (USBTXINTERVAL4), offset 0x14B ................. 1209
Register 139: USB Host Transmit Interval Endpoint 5 (USBTXINTERVAL5), offset 0x15B ................. 1209
Register 140: USB Host Transmit Interval Endpoint 6 (USBTXINTERVAL6), offset 0x16B ................. 1209
Register 141: USB Host Transmit Interval Endpoint 7 (USBTXINTERVAL7), offset 0x17B ................. 1209
Register 142: USB Host Configure Receive Type Endpoint 1 (USBRXTYPE1), offset 0x11C ............... 1210
Register 143: USB Host Configure Receive Type Endpoint 2 (USBRXTYPE2), offset 0x12C ............... 1210
Register 144: USB Host Configure Receive Type Endpoint 3 (USBRXTYPE3), offset 0x13C ............... 1210
Register 145: USB Host Configure Receive Type Endpoint 4 (USBRXTYPE4), offset 0x14C ............... 1210
Register 146: USB Host Configure Receive Type Endpoint 5 (USBRXTYPE5), offset 0x15C ............... 1210
Register 147: USB Host Configure Receive Type Endpoint 6 (USBRXTYPE6), offset 0x16C ............... 1210
Register 148: USB Host Configure Receive Type Endpoint 7 (USBRXTYPE7), offset 0x17C ............... 1210
Register 149: USB Host Receive Polling Interval Endpoint 1 (USBRXINTERVAL1), offset 0x11D ........... 1212
Register 150: USB Host Receive Polling Interval Endpoint 2 (USBRXINTERVAL2), offset 0x12D ........... 1212
Register 151: USB Host Receive Polling Interval Endpoint 3 (USBRXINTERVAL3), offset 0x13D ........... 1212
Register 152: USB Host Receive Polling Interval Endpoint 4 (USBRXINTERVAL4), offset 0x14D ........... 1212
Register 153: USB Host Receive Polling Interval Endpoint 5 (USBRXINTERVAL5), offset 0x15D ........... 1212
Register 154: USB Host Receive Polling Interval Endpoint 6 (USBRXINTERVAL6), offset 0x16D ........... 1212
Register 155: USB Host Receive Polling Interval Endpoint 7 (USBRXINTERVAL7), offset 0x17D ........... 1212
Register 156: USB Request Packet Count in Block Transfer Endpoint 1 (USBREQPKTCOUNT1), offset 0x304 .......................................................... 1213
Register 157: USB Request Packet Count in Block Transfer Endpoint 2 (USBRPKTCOUNT2), offset 0x308
Register 158: USB Request Packet Count in Block Transfer Endpoint 3 (USBRPKTCOUNT3), offset 0x30C
Register 159: USB Request Packet Count in Block Transfer Endpoint 4 (USBRPKTCOUNT4), offset 0x310
Register 160: USB Request Packet Count in Block Transfer Endpoint 5 (USBRPKTCOUNT5), offset 0x314
Register 161: USB Request Packet Count in Block Transfer Endpoint 6 (USBRPKTCOUNT6), offset 0x318
Register 162: USB Request Packet Count in Block Transfer Endpoint 7 (USBRPKTCOUNT7), offset 0x31C
Register 163: USB Receive Double Packet Buffer Disable (USBRXPDKTBUDIS), offset 0x340
Register 164: USB Transmit Double Packet Buffer Disable (USBTXDPKTBUDIS), offset 0x342
Register 165: USB External Power Control (USBEPC), offset 0x400
Register 166: USB External Power Control Raw Interrupt Status (USBEPCRIS), offset 0x404
Register 167: USB External Power Control Interrupt Mask (USBEPCIM), offset 0x408
Register 168: USB External Power Control Interrupt Status and Clear (USBEPCISC), offset 0x40C
Register 169: USB Device RESUME Raw Interrupt Status (USBDRRIS), offset 0x410
Register 170: USB Device RESUME Interrupt Mask (USBDRIM), offset 0x414
Register 171: USB Device RESUME Interrupt Status and Clear (USBDRISC), offset 0x418
Register 172: USB General-Purpose Control and Status (USBGPCS), offset 0x41C
Register 173: USB VBUS Droop Control (USBVDC), offset 0x430
Register 174: USB VBUS Droop Control Raw Interrupt Status (USBVDCRIS), offset 0x434
Register 175: USB VBUS Droop Control Interrupt Mask (USBVDCIM), offset 0x438
Register 176: USB VBUS Droop Control Interrupt Status and Clear (USBVDCISC), offset 0x43C
Register 177: USB ID Valid Detect Raw Interrupt Status (USBIDVRIS), offset 0x444
Register 178: USB ID Valid Detect Interrupt Mask (USBIDVIM), offset 0x448
Register 179: USB ID Valid Detect Interrupt Status and Clear (USBIDVISC), offset 0x44C
Register 180: USB DMA Select (USBDMASEL), offset 0x450
Register 181: USB Peripheral Properties (USBPP), offset 0x4C0

**Analog Comparators**

Register 1: Analog Comparator Masked Interrupt Status (ACMIS), offset 0x000
Register 2: Analog Comparator Raw Interrupt Status (ACRIS), offset 0x004
Register 3: Analog Comparator Interrupt Enable (ACINTEN), offset 0x008
Register 4: Analog Comparator Reference Voltage Control (ACREFCTL), offset 0x010
Register 5: Analog Comparator Status 0 (ACSTAT0), offset 0x020
Register 6: Analog Comparator Status 1 (ACSTAT1), offset 0x040
Register 7: Analog Comparator Status 2 (ACSTAT2), offset 0x060
Register 8: Analog Comparator Control 0 (ACCTL0), offset 0x024
Register 9: Analog Comparator Control 1 (ACCTL1), offset 0x044
Register 10: Analog Comparator Control 2 (ACCTL2), offset 0x064
Register 11: Analog Comparator Peripheral Properties (ACMPPP), offset 0xFC0

**Pulse Width Modulator (PWM)**

Register 1: PWM Master Control (PWMCTL), offset 0x000
Register 2: PWM Time Base Sync (PWMSYNC), offset 0x004
Register 3: PWM Output Enable (PWMEMABLE), offset 0x008
Register 4: PWM Output Inversion (PWMINVERT), offset 0x00C
<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Offset</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>PWM Output Fault (PWMFAULT), offset 0x010</td>
<td></td>
<td>1273</td>
</tr>
<tr>
<td>6</td>
<td>PWM Interrupt Enable (PWMINTEN), offset 0x014</td>
<td></td>
<td>1275</td>
</tr>
<tr>
<td>7</td>
<td>PWM Raw Interrupt Status (PWMRIS), offset 0x018</td>
<td></td>
<td>1277</td>
</tr>
<tr>
<td>8</td>
<td>PWM Interrupt Status and Clear (PWMISC), offset 0x01C</td>
<td></td>
<td>1280</td>
</tr>
<tr>
<td>9</td>
<td>PWM Status (PWMSTATUS), offset 0x020</td>
<td></td>
<td>1283</td>
</tr>
<tr>
<td>10</td>
<td>PWM Fault Condition Value (PWMFAULTVAL), offset 0x024</td>
<td></td>
<td>1285</td>
</tr>
<tr>
<td>11</td>
<td>PWM Enable Update (PWMENUPD), offset 0x028</td>
<td></td>
<td>1287</td>
</tr>
<tr>
<td>12</td>
<td>PWM0 Control (PWM0CTL), offset 0x040</td>
<td></td>
<td>1291</td>
</tr>
<tr>
<td>13</td>
<td>PWM1 Control (PWM1CTL), offset 0x080</td>
<td></td>
<td>1291</td>
</tr>
<tr>
<td>14</td>
<td>PWM2 Control (PWM2CTL), offset 0x0C0</td>
<td></td>
<td>1291</td>
</tr>
<tr>
<td>15</td>
<td>PWM3 Control (PWM3CTL), offset 0x100</td>
<td></td>
<td>1291</td>
</tr>
<tr>
<td>16</td>
<td>PWM0 Interrupt and Trigger Enable (PWM0INTEN), offset 0x044</td>
<td></td>
<td>1296</td>
</tr>
<tr>
<td>17</td>
<td>PWM1 Interrupt and Trigger Enable (PWM1INTEN), offset 0x084</td>
<td></td>
<td>1296</td>
</tr>
<tr>
<td>18</td>
<td>PWM2 Interrupt and Trigger Enable (PWM2INTEN), offset 0x0C4</td>
<td></td>
<td>1296</td>
</tr>
<tr>
<td>19</td>
<td>PWM3 Interrupt and Trigger Enable (PWM3INTEN), offset 0x104</td>
<td></td>
<td>1296</td>
</tr>
<tr>
<td>20</td>
<td>PWM0 Raw Interrupt Status (PWM0RIS), offset 0x048</td>
<td></td>
<td>1299</td>
</tr>
<tr>
<td>21</td>
<td>PWM1 Raw Interrupt Status (PWM1RIS), offset 0x088</td>
<td></td>
<td>1299</td>
</tr>
<tr>
<td>22</td>
<td>PWM2 Raw Interrupt Status (PWM2RIS), offset 0x0C8</td>
<td></td>
<td>1299</td>
</tr>
<tr>
<td>23</td>
<td>PWM3 Raw Interrupt Status (PWM3RIS), offset 0x108</td>
<td></td>
<td>1299</td>
</tr>
<tr>
<td>24</td>
<td>PWM0 Interrupt Status and Clear (PWM0ISC), offset 0x04C</td>
<td></td>
<td>1301</td>
</tr>
<tr>
<td>25</td>
<td>PWM1 Interrupt Status and Clear (PWM1ISC), offset 0x08C</td>
<td></td>
<td>1301</td>
</tr>
<tr>
<td>26</td>
<td>PWM2 Interrupt Status and Clear (PWM2ISC), offset 0x0CC</td>
<td></td>
<td>1301</td>
</tr>
<tr>
<td>27</td>
<td>PWM3 Interrupt Status and Clear (PWM3ISC), offset 0x10C</td>
<td></td>
<td>1301</td>
</tr>
<tr>
<td>28</td>
<td>PWM0 Load (PWM0LOAD), offset 0x050</td>
<td></td>
<td>1303</td>
</tr>
<tr>
<td>29</td>
<td>PWM1 Load (PWM1LOAD), offset 0x090</td>
<td></td>
<td>1303</td>
</tr>
<tr>
<td>30</td>
<td>PWM2 Load (PWM2LOAD), offset 0x0D0</td>
<td></td>
<td>1303</td>
</tr>
<tr>
<td>31</td>
<td>PWM3 Load (PWM3LOAD), offset 0x110</td>
<td></td>
<td>1303</td>
</tr>
<tr>
<td>32</td>
<td>PWM0 Counter (PWM0COUNT), offset 0x054</td>
<td></td>
<td>1304</td>
</tr>
<tr>
<td>33</td>
<td>PWM1 Counter (PWM1COUNT), offset 0x094</td>
<td></td>
<td>1304</td>
</tr>
<tr>
<td>34</td>
<td>PWM2 Counter (PWM2COUNT), offset 0x0D4</td>
<td></td>
<td>1304</td>
</tr>
<tr>
<td>35</td>
<td>PWM3 Counter (PWM3COUNT), offset 0x114</td>
<td></td>
<td>1304</td>
</tr>
<tr>
<td>36</td>
<td>PWM0 Compare A (PWM0CMPA), offset 0x058</td>
<td></td>
<td>1305</td>
</tr>
<tr>
<td>37</td>
<td>PWM1 Compare A (PWM1CMPA), offset 0x098</td>
<td></td>
<td>1305</td>
</tr>
<tr>
<td>38</td>
<td>PWM2 Compare A (PWM2CMPA), offset 0x0D8</td>
<td></td>
<td>1305</td>
</tr>
<tr>
<td>39</td>
<td>PWM3 Compare A (PWM3CMPA), offset 0x118</td>
<td></td>
<td>1305</td>
</tr>
<tr>
<td>40</td>
<td>PWM0 Compare B (PWM0CMPB), offset 0x05C</td>
<td></td>
<td>1306</td>
</tr>
<tr>
<td>41</td>
<td>PWM1 Compare B (PWM1CMPB), offset 0x09C</td>
<td></td>
<td>1306</td>
</tr>
<tr>
<td>42</td>
<td>PWM2 Compare B (PWM2CMPB), offset 0x0DC</td>
<td></td>
<td>1306</td>
</tr>
<tr>
<td>43</td>
<td>PWM3 Compare B (PWM3CMPB), offset 0x11C</td>
<td></td>
<td>1306</td>
</tr>
<tr>
<td>44</td>
<td>PWM0 Generator A Control (PWM0GENA), offset 0x060</td>
<td></td>
<td>1307</td>
</tr>
<tr>
<td>45</td>
<td>PWM1 Generator A Control (PWM1GENA), offset 0xA0</td>
<td></td>
<td>1307</td>
</tr>
<tr>
<td>46</td>
<td>PWM2 Generator A Control (PWM2GENA), offset 0xE0</td>
<td></td>
<td>1307</td>
</tr>
<tr>
<td>47</td>
<td>PWM3 Generator A Control (PWM3GENA), offset 0x120</td>
<td></td>
<td>1307</td>
</tr>
<tr>
<td>48</td>
<td>PWM0 Generator B Control (PWM0GENB), offset 0x64</td>
<td></td>
<td>1310</td>
</tr>
<tr>
<td>49</td>
<td>PWM1 Generator B Control (PWM1GENB), offset 0xA4</td>
<td></td>
<td>1310</td>
</tr>
<tr>
<td>50</td>
<td>PWM2 Generator B Control (PWM2GENB), offset 0xE4</td>
<td></td>
<td>1310</td>
</tr>
<tr>
<td>51</td>
<td>PWM3 Generator B Control (PWM3GENB), offset 0x124</td>
<td></td>
<td>1310</td>
</tr>
<tr>
<td>52</td>
<td>PWM0 Dead-Band Control (PWM0DBCTL), offset 0x068</td>
<td></td>
<td>1313</td>
</tr>
</tbody>
</table>
Register 53: PWM1 Dead-Band Control (PWM1DBCTL), offset 0x0A8 .................................................. 1313
Register 54: PWM2 Dead-Band Control (PWM2DBCTL), offset 0x0E8 .................................................. 1313
Register 55: PWM3 Dead-Band Control (PWM3DBCTL), offset 0x128 .................................................. 1313
Register 56: PWM0 Dead-Band Rising-Edge Delay (PWM0DBRISE), offset 0x06C ............................ 1314
Register 57: PWM1 Dead-Band Rising-Edge Delay (PWM1DBRISE), offset 0x0AC ............................ 1314
Register 58: PWM2 Dead-Band Rising-Edge Delay (PWM2DBRISE), offset 0x0EC ............................ 1314
Register 59: PWM3 Dead-Band Rising-Edge Delay (PWM3DBRISE), offset 0x12C ............................ 1314
Register 60: PWM0 Dead-Band Falling-Edge Delay (PWM0DFALL), offset 0x070 ............................ 1315
Register 61: PWM1 Dead-Band Falling-Edge Delay (PWM1DFALL), offset 0x0B0 ............................ 1315
Register 62: PWM2 Dead-Band Falling-Edge Delay (PWM2DFALL), offset 0x0F0 ............................ 1315
Register 63: PWM3 Dead-Band Falling-Edge Delay (PWM3DFALL), offset 0x130 ............................ 1315
Register 64: PWM0 Fault Source 0 (PWM0FLTSRC0), offset 0x074 .................................................. 1316
Register 65: PWM1 Fault Source 0 (PWM1FLTSRC0), offset 0x0B4 .................................................. 1316
Register 66: PWM2 Fault Source 0 (PWM2FLTSRC0), offset 0x0F4 .................................................. 1316
Register 67: PWM3 Fault Source 0 (PWM3FLTSRC0), offset 0x134 .................................................. 1316
Register 68: PWM0 Fault Source 1 (PWM0FLTSRC1), offset 0x078 .................................................. 1318
Register 69: PWM1 Fault Source 1 (PWM1FLTSRC1), offset 0x0B8 .................................................. 1318
Register 70: PWM2 Fault Source 1 (PWM2FLTSRC1), offset 0x0F8 .................................................. 1318
Register 71: PWM3 Fault Source 1 (PWM3FLTSRC1), offset 0x138 .................................................. 1318
Register 72: PWM0 Minimum Fault Period (PWM0MINFLTPER), offset 0x07C ............................ 1321
Register 73: PWM1 Minimum Fault Period (PWM1MINFLTPER), offset 0x0BC ............................ 1321
Register 74: PWM2 Minimum Fault Period (PWM2MINFLTPER), offset 0x0FC ............................ 1321
Register 75: PWM3 Minimum Fault Period (PWM3MINFLTPER), offset 0x13C ............................ 1321
Register 76: PWM0 Fault Pin Logic Sense (PWM0FLTSEN), offset 0x800 .......................................... 1322
Register 77: PWM1 Fault Pin Logic Sense (PWM1FLTSEN), offset 0x880 .......................................... 1322
Register 78: PWM2 Fault Pin Logic Sense (PWM2FLTSEN), offset 0x900 .......................................... 1322
Register 79: PWM3 Fault Pin Logic Sense (PWM3FLTSEN), offset 0x980 .......................................... 1322
Register 80: PWM0 Fault Status 0 (PWM0FLTSTAT0), offset 0x804 .................................................. 1323
Register 81: PWM1 Fault Status 0 (PWM1FLTSTAT0), offset 0x884 .................................................. 1323
Register 82: PWM2 Fault Status 0 (PWM2FLTSTAT0), offset 0x904 .................................................. 1323
Register 83: PWM3 Fault Status 0 (PWM3FLTSTAT0), offset 0x984 .................................................. 1323
Register 84: PWM0 Fault Status 1 (PWM0FLTSTAT1), offset 0x808 .................................................. 1325
Register 85: PWM1 Fault Status 1 (PWM1FLTSTAT1), offset 0x888 .................................................. 1325
Register 86: PWM2 Fault Status 1 (PWM2FLTSTAT1), offset 0x908 .................................................. 1325
Register 87: PWM3 Fault Status 1 (PWM3FLTSTAT1), offset 0x988 .................................................. 1325
Register 88: PWM Peripheral Properties (PWMPP), offset 0xFC0 ...................................................... 1328

Quadrature Encoder Interface (QEI) ........................................................................................................ 1330
Register 1: QEI Control (QEICCTL), offset 0x000 ............................................................................... 1337
Register 2: QEI Status (QEISTAT), offset 0x004 ................................................................................. 1340
Register 3: QEI Position (QEIPOS), offset 0x008 ................................................................................. 1341
Register 4: QEI Maximum Position (QEIMAXPOS), offset 0x00C .................................................. 1342
Register 5: QEI Timer Load (QEILOAD), offset 0x010 ........................................................................ 1343
Register 6: QEI Timer (QEIITIME), offset 0x014 ................................................................................. 1344
Register 7: QEI Velocity Counter (QEICOUNT), offset 0x018 .......................................................... 1345
Register 8: QEI Velocity (QEISPEED), offset 0x01C ........................................................................... 1346
Register 9: QEI Interrupt Enable (QEINTE), offset 0x020 ................................................................. 1347
Register 10: QEI Raw Interrupt Status (QEIRIS), offset 0x024 ......................................................... 1349
Register 11: QEI Interrupt Status and Clear (QEISC), offset 0x028 .................................................... 1351
# Revision History

The revision history table notes changes made between the indicated revisions of the TM4C123GH6PZ data sheet.

## Table 1. Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
</tr>
</thead>
</table>
| June 2014  | 15842.2741| ■ In System Control Chapter, corrected description for MINSYSDIV bitfield in **Device Capabilities 1 (DC1)** legacy register.  
■ In Timers chapter, removed erroneous references to TCACT bit field.  
■ In SSI chapter, corrected that during idle periods the transmit data line SSInTx is tristated.  
■ In Electrical Characteristics chapter, added Data Retention parameter for extended temperature devices to Flash Memory Characteristics table.  
■ In Package Information appendix:  
  – Corrected Key to Part Numbers diagram.  
  – Moved Orderable Part Numbers table to addendum.  
  – Deleted Packaging Materials section and put into separate packaging document.  
■ Additional minor data sheet clarifications and corrections. |
| March 2014 | 15741.2722| ■ In the Internal Memory chapter, in the EEPROM section:  
  – Added section on soft reset handling.  
  – Added important information on EEPROM initialization and configuration.  
■ In the DMA chapter, added information regarding interrupts and transfers from the UART or SSI modules.  
■ In the Hibernation chapter, noted that the EXTW bit is set in the **HIBRIS** register regardless of the PINWEN setting in the **HIBCTL** register.  
■ In the GPIO chapter:  
  – Corrected table GPIO Pins with Special Considerations.  
  – Added information on preventing false interrupts.  
■ In the Timer chapter:  
  – Clarified initialization and configuration for Input-Edge Count mode.  
  – Clarified behavior of TnMIE and TnCINTD bits in the **GPTM Timer n Mode (GPTMTnMR)** register.  
■ In the USB chapter, added note to SUSPEND section regarding bus-powered devices.  
■ In the Electrical Characteristics chapter:  
  – In table Reset Characteristics, clarified internal reset time parameter values.  
  – In table Hibernation Oscillator Input Characteristics, added parameter CINSE Input capacitance.  
  – In tables Hibernation Oscillator Input Characteristics and Main Oscillator Input Characteristics, removed parameter C0 Crystal shunt capacitance.  
  – Updated table Crystal Parameters.  
  – In table GPIO Module Characteristics, added parameter CGPIO GPIO Digital Input Capacitance.  
  – Added table PWM Timing Characteristics.  
■ In the Package Information appendix:  
  – Updated Orderable Devices section to reflect silicon revision 7 part numbers.  
  – Added Tape and Reel pin 1 location.  
■ Additional minor data sheet clarifications and corrections. |
| November 2013 | 15553.2700 | ■ In System Control chapter, clarified PIOSC features and accuracy. |

---

*Texas Instruments-Production Data*  
*June 12, 2014*
Table 1. Revision History (continued)

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>June 12, 2014</td>
<td></td>
<td>In Hibernation Module chapter:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Corrected figures &quot;Using a Crystal as the Hibernation Clock Source with a Single Battery Source&quot; and &quot;Using a Regulator for Both VDD and VBAT&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Replaced RTC Trim tables with two new figures &quot;Counter Behavior with a TRIM Value of 0x8002&quot; and &quot;Counter Behavior with a TRIM Value of 0x7FFC&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clarified Hibernation Data (HIBDATA) register description.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In Watchdog Timers chapter, clarified Watchdog Control (WDTCTL) register description.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In ADC chapter:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clarified functionality when using an ADC digital comparator as a fault source.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clarified signals used for ADC voltage reference.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clarified ADC Trigger Source Select (ADCTSSEL) register description.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Corrected VREF bit in ADC Control (ADCCCTL) register from 2-bit field [1:0] to 1-bit field [0].</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In UART chapter, clarified DMA operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In SSI chapter:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Corrected timing guidelines in figures &quot;Freescale SPI Frame Format (Continuous Transfer) with SPO=1 and SPH=0&quot; and &quot;Freescale SPI Frame Format (Continuous Transfer) with SPO=0 and SPH=0&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clarified SSI Initialization and Configuration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Corrected bit 3 in SSI Control 1 (SSICR1) register from SO (SSI Slave Mode Output Disable) to reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In PWM chapter, added clarifications to PWM0 Control (PWM0CTL), PWM0 Interrupt Status and Clear (PWM0ISC), PWM0 Counter (PWM0COUNT), PWM0 Fault Status 0 (PWM0FLTSTAT0), and PWM0 Fault Status 1 (PWM0FLTSTAT1) registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In Signal Tables chapter:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In Unused Signals table, corrected preferred and acceptable practices for RST pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clarified GNDX pin description.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In Electrical Characteristics chapter:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In Power-On and Brown-Out Levels table, corrected TVDD,RISE parameter min and max values.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In PIOSC Clock Characteristics table, clarified F_PIOSC parameter values by defining values for both factory calibration and recalibration. Also added PIOSC startup time parameter to table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In Main Oscillator Specifications section, corrected minimum value for External load capacitance on OSC0, OSC1 pins. Also added two 25-MHz crystals to Crystal Parameters table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Corrected figure &quot;Master Mode SSI Timing for SPI Frame Format (FRF=00), with SPH=1&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In I²C Characteristics table, clarified T_DH data hold time parameter values by defining values for both slave and master. In addition, added parameter I10 T_DV data valid.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Modified figure &quot;I2C Timing&quot; to add new parameter I10.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In Packaging Information appendix, added Packaging Materials figures.</td>
</tr>
<tr>
<td>July 16, 2013</td>
<td>15033.2672</td>
<td>In the Electrical Characteristics chapter:</td>
</tr>
</tbody>
</table>
Table 1. Revision History (continued)

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>July 2013</td>
<td>14995.2667</td>
<td>- Added maximum junction temperature to Maximum Ratings table. Also moved Unpowered storage temperature range parameter to this table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- In SSI Characteristics table, corrected values for $T_{RXDMs}$, $T_{RXDMH}$, and $T_{RXDSSU}$. Also clarified footnotes to the table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Corrected parameter numbers in figures &quot;Master Mode SSI Timing for SPI Frame Format (FRF=00), with SPH=1&quot; and &quot;Slave Mode SSI Timing for SPI Frame Format (FRF=00), with SPH=1&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Additional minor data sheet clarifications and corrections.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Deleted erroneous references to the PWM Peripheral Configuration (PWMPC) register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the Hibernation Module chapter:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Corrected figures &quot;Using a Crystal as the Hibernation Clock Source with a Single Battery Source&quot; and &quot;Using a Dedicated Oscillator as the Hibernation Clock Source with VDD3ON Mode&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clarified when the Hibernation module can generate interrupts.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the Internal Memory chapter, removed the INVPIL bit from the EEPROM Done Status (EEDONE) register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the uDMA chapter, in the µDMA Channel Assignments table, corrected names of timers 6-11 to wide timers 0-5.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the Timers chapter:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Clarified that the timer must be configured for one-shot or periodic time-out mode to produce an ADC trigger assertion and that the GPTM does not generate triggers for match, compare events or compare match events.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Added a step in the RTC Mode initialization and configuration: If the timer has been operating in a different mode prior to this, clear any residual set bits in the GPTM Timer n Mode (GPTMTnMR) register before reconfiguring.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the Watchdog Timer chapter, added a note that locking the watchdog registers using the WDTLOCK register does not affect the WDTICR register and allows interrupts to always be serviced.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the SSI chapter, clarified note in Bit Rate Generation section to indicate that the System Clock or the PIOSC can be used as the source for SSIClk. Also corrected to indicate maximum SSIClk limit in SSI slave mode as well as the fact that SYSCLK has to be at least 12 times that of SSIClk.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the PWM chapter, clarified that the PWM has two clock sources, selected by the USPWMDIV bit in the Run-Mode Clock Configuration (RCC) register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the QEI chapter, noted that the INTERROR bit is only applicable when the QEI is operating in quadrature phase mode (SIGMODE=0) and should be masked when SIGMODE=1. Similarly, the INTDIR bit is only applicable when the QEI is operating in clock/direction mode (SIGMODE=1) and should be masked when SIGMODE=0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the Electrical Characteristics chapter:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Moved Maximum Ratings and ESD Absolute Maximum Ratings to the front of the chapter.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Added $V_{BATRMP}$ parameter to Maximum Ratings and Hibernation Module Battery Characteristics tables.</td>
</tr>
</tbody>
</table>
Table 1. Revision History (continued)

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>• Added ambient and junction temperatures to Temperature Characteristics table and clarified values in Thermal Characteristics table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added clarifying footnote to $V_{VDD_POK}$ parameter in Power-On and Brown-Out Levels table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Corrected GPIO Package Side Assignments table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In the Flash Memory and EEPROM Characteristics tables, added a parameter for page/mass erase times for 10k cycles and corrected existing values for all page and mass erase parameters.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Corrected DNL max value in ADC Electrical Characteristics table.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In the SSI Characteristics table, changed parameter names for S7-S14, provided a max number instead of a min for S7, and corrected values for S9-S14.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Replaced figure “SSI Timing for SPI Frame Format (FRF=00), with SPH=1” with two figures, one for Master Mode and one for Slave Mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated and added values to the table Table 24-41 on page 1437.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ In the Package Information appendix, moved orderable devices table from addendum to appendix, clarified part markings and moved packaging diagram from addendum to appendix.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Additional minor data sheet clarifications and corrections.</td>
</tr>
</tbody>
</table>
About This Document

This data sheet provides reference information for the TM4C123GH6PZ microcontroller, describing the functional blocks of the system-on-chip (SoC) device designed around the ARM® Cortex™-M4F core.

Audience

This manual is intended for system software developers, hardware designers, and application developers.

About This Manual

This document is organized into sections that correspond to each major feature.

Related Documents

The following related documents are available on the Tiva™ C Series web site at http://www.ti.com/tiva-c:

- Tiva™ C Series TM4C123x Silicon Errata (literature number SPMZ849)
- TivaWare™ Boot Loader for C Series User’s Guide (literature number SPMU301)
- TivaWare™ Graphics Library for C Series User’s Guide (literature number SPMU300)
- TivaWare™ for C Series Release Notes (literature number SPMU299)
- TivaWare™ Peripheral Driver Library for C Series User’s Guide (literature number SPMU298)
- TivaWare™ USB Library for C Series User’s Guide (literature number SPMU297)
- Tiva™ C Series TM4C123x ROM User’s Guide (literature number SPMU367)

The following related documents may also be useful:

- ARM® Cortex™-M4 Errata (literature number SPMZ637)
- ARM® Debug Interface V5 Architecture Specification
- ARM® Embedded Trace Macrocell Architecture Specification
- Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A)
- IEEE Standard 1149.1-Test Access Port and Boundary-Scan Architecture

This documentation list was current as of publication date. Please check the web site for additional documentation, including application notes and white papers.
Documentation Conventions

This document uses the conventions shown in Table 2 on page 43.

Table 2. Documentation Conventions

<table>
<thead>
<tr>
<th>Notation</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>REGISTER</strong></td>
<td>APB registers are indicated in uppercase bold. For example, PBORCTL is the Power-On and Brown-Out Reset Control register. If a register name contains a lowercase n, it represents more than one register. For example, SSCRn represents any (or all) of the three Software Reset Control registers: SSCR0, SSCR1, and SSCR2.</td>
</tr>
<tr>
<td>bit</td>
<td>A single bit in a register.</td>
</tr>
<tr>
<td>bit field</td>
<td>Two or more consecutive and related bits.</td>
</tr>
<tr>
<td>offset 0xnnn</td>
<td>A hexadecimal increment to a register's address, relative to that module's base address as specified in Table 2-4 on page 92.</td>
</tr>
<tr>
<td>Register N</td>
<td>Registers are numbered consecutively throughout the document to aid in referencing them. The register number has no meaning to software.</td>
</tr>
<tr>
<td>reserved</td>
<td>Register bits marked reserved are reserved for future use. In most cases, reserved bits are set to 0; however, user software should not rely on the value of a reserved bit. To provide software compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>yy:xx</td>
<td>The range of register bits inclusive from xx to yy. For example, 31:15 means bits 15 through 31 in that register.</td>
</tr>
<tr>
<td><strong>Register Bit/Field Types</strong></td>
<td>This value in the register bit diagram indicates whether software running on the controller can change the value of the bit field.</td>
</tr>
<tr>
<td>RC</td>
<td>Software can read this field. The bit or field is cleared by hardware after reading the bit/field.</td>
</tr>
<tr>
<td>RO</td>
<td>Software can read this field. Always write the chip reset value.</td>
</tr>
<tr>
<td>RW</td>
<td>Software can read or write this field.</td>
</tr>
<tr>
<td>RWC</td>
<td>Software can read or write this field. Writing to it with any value clears the register.</td>
</tr>
<tr>
<td>RW1C</td>
<td>Software can read or write this field. A write of a 0 to a W1C bit does not affect the bit value in the register. A write of a 1 clears the value of the bit in the register; the remaining bits remain unchanged. This register type is primarily used for clearing interrupt status bits where the read operation provides the interrupt status and the write of the read value clears only the interrupts being reported at the time the register was read.</td>
</tr>
<tr>
<td>RW1S</td>
<td>Software can read or write a 1 to this field. A write of a 0 to a RW1S bit does not affect the bit value in the register.</td>
</tr>
<tr>
<td>W1C</td>
<td>Software can write this field. A write of a 0 to a W1C bit does not affect the bit value in the register. A read of the register returns no meaningful data. This register is typically used to clear the corresponding bit in an interrupt register.</td>
</tr>
<tr>
<td>WO</td>
<td>Only a write by software is valid; a read of the register returns no meaningful data.</td>
</tr>
<tr>
<td><strong>Register Bit/Field Reset Value</strong></td>
<td>This value in the register bit diagram shows the bit/field value after any reset, unless noted.</td>
</tr>
<tr>
<td>0</td>
<td>Bit cleared to 0 on chip reset.</td>
</tr>
<tr>
<td>1</td>
<td>Bit set to 1 on chip reset.</td>
</tr>
<tr>
<td>-</td>
<td>Nondeterministic.</td>
</tr>
<tr>
<td><strong>Pin/Signal Notation</strong></td>
<td></td>
</tr>
<tr>
<td>[]</td>
<td>Pin alternate function; a pin defaults to the signal without the brackets.</td>
</tr>
<tr>
<td>pin</td>
<td>Refers to the physical connection on the package.</td>
</tr>
<tr>
<td>signal</td>
<td>Refers to the electrical signal encoding of a pin.</td>
</tr>
</tbody>
</table>
### Table 2. Documentation Conventions (continued)

<table>
<thead>
<tr>
<th>Notation</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>assert a signal</td>
<td>Change the value of the signal from the logically False state to the logically True state. For active High signals, the asserted signal value is 1 (High); for active Low signals, the asserted signal value is 0 (Low). The active polarity (High or Low) is defined by the signal name (see SIGNAL and SIGNAL below).</td>
</tr>
<tr>
<td>deassert a signal</td>
<td>Change the value of the signal from the logically True state to the logically False state.</td>
</tr>
<tr>
<td>SIGNAL</td>
<td>Signal names are in uppercase and in the Courier font. An overbar on a signal name indicates that it is active Low. To assert SIGNAL is to drive it Low; to deassert SIGNAL is to drive it High.</td>
</tr>
<tr>
<td>SIGNAL</td>
<td>Signal names are in uppercase and in the Courier font. An active High signal has no overbar. To assert SIGNAL is to drive it High; to deassert SIGNAL is to drive it Low.</td>
</tr>
</tbody>
</table>

### Numbers

<table>
<thead>
<tr>
<th>X</th>
<th>An uppercase X indicates any of several values is allowed, where X can be any legal pattern. For example, a binary value of 0X00 can be either 0100 or 0000, a hex value of 0xX is 0x0 or 0x1, and so on.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x</td>
<td>Hexadecimal numbers have a prefix of 0x. For example, 0x00FF is the hexadecimal number FF. All other numbers within register tables are assumed to be binary. Within conceptual information, binary numbers are indicated with a b suffix, for example, 1011b, and decimal numbers are written without a prefix or suffix.</td>
</tr>
</tbody>
</table>
1 Architectural Overview

Texas Instrument's Tiva™ C Series microcontrollers provide designers a high-performance ARM® Cortex™-M-based architecture with a broad set of integration capabilities and a strong ecosystem of software and development tools. Targeting performance and flexibility, the Tiva™ C Series architecture offers a 80 MHz Cortex-M with FPU, a variety of integrated memories and multiple programmable GPIO. Tiva™ C Series devices offer consumers compelling cost-effective solutions by integrating application-specific peripherals and providing a comprehensive library of software tools which minimize board costs and design-cycle time. Offering quicker time-to-market and cost savings, the Tiva™ C Series microcontrollers are the leading choice in high-performance 32-bit applications.

This chapter contains an overview of the Tiva™ C Series microcontrollers as well as details on the TM4C123GH6PZ microcontroller:

- “Tiva™ C Series Overview” on page 45
- “TM4C123GH6PZ Microcontroller Overview” on page 46
- “TM4C123GH6PZ Microcontroller Features” on page 49
- “TM4C123GH6PZ Microcontroller Hardware Details” on page 68
- “Kits” on page 68
- “Support Information” on page 68

1.1 Tiva™ C Series Overview

The Tiva™ C Series ARM Cortex-M4 microcontrollers provide top performance and advanced integration. The product family is positioned for cost-conscious applications requiring significant control processing and connectivity capabilities such as:

- Low power, hand-held smart devices
- Gaming equipment
- Home and commercial site monitoring and control
- Motion control
- Medical instrumentation
- Test and measurement equipment
- Factory automation
- Fire and security
- Smart Energy/Smart Grid solutions
- Intelligent lighting control
- Transportation

For applications requiring extreme conservation of power, the TM4C123GH6PZ microcontroller features a battery-backed Hibernation module to efficiently power down the TM4C123GH6PZ to a low-power state during extended periods of inactivity. With a power-up/power-down sequencer, a real-time counter (RTC), multiple wake-from-hibernate options, and dedicated battery-backed memory, the Hibernation module positions the TM4C123GH6PZ microcontroller perfectly for battery applications.

In addition, the TM4C123GH6PZ microcontroller offers the advantages of ARM's widely available development tools, System-on-Chip (SoC) infrastructure IP applications, and a large user community. Additionally, the microcontroller uses ARM's Thumb®-compatible Thumb-2 instruction set to reduce memory requirements and, thereby, cost. Finally, much of the TM4C123GH6PZ microcontroller code is compatible to the Tiva™ C Series product line, providing flexibility across designs.
Texas Instruments offers a complete solution to get to market quickly, with evaluation and development boards, white papers and application notes, an easy-to-use peripheral driver library, and a strong support, sales, and distributor network.

1.2 TM4C123GH6PZ Microcontroller Overview

The TM4C123GH6PZ microcontroller combines complex integration and high performance with the features shown in Table 1-1.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Performance</strong></td>
<td></td>
</tr>
<tr>
<td>Core</td>
<td>ARM Cortex-M4F processor core</td>
</tr>
<tr>
<td>Performance</td>
<td>80-MHz operation; 100 DMIPS performance</td>
</tr>
<tr>
<td>Flash</td>
<td>256 KB single-cycle Flash memory</td>
</tr>
<tr>
<td>System SRAM</td>
<td>32 KB single-cycle SRAM</td>
</tr>
<tr>
<td>EEPROM</td>
<td>2KB of EEPROM</td>
</tr>
<tr>
<td>Internal ROM</td>
<td>Internal ROM loaded with TivaWare™ for C Series software</td>
</tr>
<tr>
<td><strong>Security</strong></td>
<td></td>
</tr>
<tr>
<td><strong>Communication Interfaces</strong></td>
<td></td>
</tr>
<tr>
<td>Universal Asynchronous Receivers/Transmitter (UART)</td>
<td>Eight UARTs</td>
</tr>
<tr>
<td>Synchronous Serial Interface (SSI)</td>
<td>Four SSI modules</td>
</tr>
<tr>
<td>Inter-Integrated Circuit (I2C)</td>
<td>Six I2C modules with four transmission speeds including high-speed mode</td>
</tr>
<tr>
<td>Controller Area Network (CAN)</td>
<td>Two CAN 2.0 A/B controllers</td>
</tr>
<tr>
<td>Universal Serial Bus (USB)</td>
<td>USB 2.0 OTG/Host/Device</td>
</tr>
<tr>
<td><strong>System Integration</strong></td>
<td></td>
</tr>
<tr>
<td>Micro Direct Memory Access (µDMA)</td>
<td>ARM® PrimeCell® 32-channel configurable µDMA controller</td>
</tr>
<tr>
<td>General-Purpose Timer (GPTM)</td>
<td>Six 16/32-bit GPTM blocks and six 32/64-bit Wide GPTM blocks</td>
</tr>
<tr>
<td>Watchdog Timer (WDT)</td>
<td>Two watchdog timers</td>
</tr>
<tr>
<td>Hibernation Module (HIB)</td>
<td>Low-power battery-backed Hibernation module</td>
</tr>
<tr>
<td>General-Purpose Input/Output (GPIO)</td>
<td>10 physical GPIO blocks</td>
</tr>
<tr>
<td><strong>Advanced Motion Control</strong></td>
<td></td>
</tr>
<tr>
<td>Pulse Width Modulator (PWM)</td>
<td>Two PWM modules, each with four PWM generator blocks and a control block, for a total of 16 PWM outputs.</td>
</tr>
<tr>
<td>Quadrature Encoder Interface (QEI)</td>
<td>Two QEI modules</td>
</tr>
<tr>
<td><strong>Analog Support</strong></td>
<td></td>
</tr>
<tr>
<td>Analog-to-Digital Converter (ADC)</td>
<td>Two 12-bit ADC modules, each with a maximum sample rate of one million samples/second</td>
</tr>
<tr>
<td>Analog Comparator Controller</td>
<td>Three independent integrated analog comparators</td>
</tr>
<tr>
<td>Digital Comparator</td>
<td>16 digital comparators</td>
</tr>
<tr>
<td>JTAG and Serial Wire Debug (SWD)</td>
<td>One JTAG module with integrated ARM SWD</td>
</tr>
<tr>
<td><strong>Package Information</strong></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td>100-pin LQFP</td>
</tr>
<tr>
<td>Operating Range (Ambient)</td>
<td>Industrial (-40°C to 85°C) temperature range</td>
</tr>
<tr>
<td>Operating Range (Extended)</td>
<td>Extended (-40°C to 105°C) temperature range</td>
</tr>
</tbody>
</table>
Figure 1-1 on page 48 shows the features on the TM4C123GH6PZ microcontroller. Note that there are two on-chip buses that connect the core to the peripherals. The Advanced Peripheral Bus (APB) bus is the legacy bus. The Advanced High-Performance Bus (AHB) bus provides better back-to-back access performance than the APB bus.
Figure 1-1. Tiva™ TM4C123GH6PZ Microcontroller High-Level Block Diagram
1.3 **TM4C123GH6PZ Microcontroller Features**

The TM4C123GH6PZ microcontroller component features and general function are discussed in more detail in the following section.

### 1.3.1 ARM Cortex-M4F Processor Core

All members of the Tiva™ C Series, including the TM4C123GH6PZ microcontroller, are designed around an ARM Cortex-M processor core. The ARM Cortex-M processor provides the core for a high-performance, low-cost platform that meets the needs of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

#### 1.3.1.1 Processor Core (see page 69)

- 32-bit ARM Cortex-M4F architecture optimized for small-footprint embedded applications
- 80-MHz operation; 100 DMIPS performance
- Outstanding processing performance combined with fast interrupt handling
- Thumb-2 mixed 16-/32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- IEEE754-compliant single-precision Floating-Point Unit (FPU)
- 16-bit SIMD vector processing unit
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system and memories
- Hardware division and fast digital-signal-processing orientated multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Memory protection unit (MPU) to provide a privileged mode for protected operating system functionality
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging and tracing
Migration from the ARM7™ processor family for better performance and power efficiency

- Optimized for single-cycle Flash memory usage up to specific frequencies; see “Internal Memory” on page 534 for more information.

- Ultra-low power consumption with integrated sleep modes

1.3.1.2 System Timer (SysTick) (see page 123)

ARM Cortex-M4F includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit, clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer that fires at a programmable rate (for example, 100 Hz) and invokes a SysTick routine

- A high-speed alarm timer using the system clock

- A variable rate alarm or signal timer—the duration is range-dependent on the reference clock used and the dynamic range of the counter

- A simple counter used to measure time to completion and time used

- An internal clock-source control based on missing/meeting durations

1.3.1.3 Nested Vectored Interrupt Controller (NVIC) (see page 124)

The TM4C123GH6PZ controller includes the ARM Nested Vectored Interrupt Controller (NVIC). The NVIC and Cortex-M4F prioritize and handle all exceptions in Handler Mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the Interrupt Service Routine (ISR). The interrupt vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining, meaning that back-to-back interrupts can be performed without the overhead of state saving and restoration. Software can set eight priority levels on 7 exceptions (system handlers) and 85 interrupts.

- Deterministic, fast interrupt processing: always 12 cycles, or just 6 cycles with tail-chaining (these values reflect no FPU stacking)

- External non-maskable interrupt signal (NMI) available for immediate execution of NMI handler for safety critical applications

- Dynamically reprioritizable interrupts

- Exceptional interrupt handling via hardware implementation of required register manipulations

1.3.1.4 System Control Block (SCB) (see page 125)

The SCB provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

1.3.1.5 Memory Protection Unit (MPU) (see page 125)

The MPU supports the standard ARM7 Protected Memory System Architecture (PMSA) model. The MPU provides full support for protection regions, overlapping protection regions, access permissions, and exporting memory attributes to the system.
1.3.1.6 Floating-Point Unit (FPU) (see page 130)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

- 32-bit instructions for single-precision (C float) data-processing operations
- Combined multiply and accumulate instructions for increased precision (Fused MAC)
- Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
- Hardware support for denormals and all IEEE rounding modes
- 32 dedicated 32-bit single-precision registers, also addressable as 16 double-word registers
- Decoupled three stage pipeline

1.3.2 On-Chip Memory

The TM4C123GH6PZ microcontroller is integrated with the following set of on-chip memory and features:

- 32 KB single-cycle SRAM
- 256 KB Flash memory
- 2KB EEPROM
- Internal ROM loaded with TivaWare™ for C Series software:
  - TivaWare™ Peripheral Driver Library
  - TivaWare Boot Loader
  - Advanced Encryption Standard (AES) cryptography tables
  - Cyclic Redundancy Check (CRC) error detection functionality

1.3.2.1 SRAM (see page 535)

The TM4C123GH6PZ microcontroller provides 32 KB of single-cycle on-chip SRAM. The internal SRAM of the device is located at offset 0x2000.0000 of the device memory map.

Because read-modify-write (RMW) operations are very time consuming, ARM has introduced bit-banding technology in the Cortex-M4F processor. With a bit-band-enabled processor, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in a single, atomic operation.

Data can be transferred to and from SRAM by the following masters:

- µDMA
- USB

1.3.2.2 Flash Memory (see page 538)

The TM4C123GH6PZ microcontroller provides 256 KB of single-cycle on-chip Flash memory. The Flash memory is organized as a set of 1-KB blocks that can be individually erased. Erasing a block causes the entire contents of the block to be reset to all 1s. These blocks are paired into a set of
2-KB blocks that can be individually protected. The blocks can be marked as read-only or execute-only, providing different levels of code protection. Read-only blocks cannot be erased or programmed, protecting the contents of those blocks from being modified. Execute-only blocks cannot be erased or programmed, and can only be read by the controller instruction fetch mechanism, protecting the contents of those blocks from being read by either the controller or by a debugger.

1.3.2.3 ROM (see page 536)
The TM4C123GH6PZ ROM is preprogrammed with the following software and programs:

- TivaWare Peripheral Driver Library
- TivaWare Boot Loader
- Advanced Encryption Standard (AES) cryptography tables
- Cyclic Redundancy Check (CRC) error-detection functionality

The TivaWare Peripheral Driver Library is a royalty-free software library for controlling on-chip peripherals with a boot-loader capability. The library performs both peripheral initialization and control functions, with a choice of polled or interrupt-driven peripheral support. In addition, the library is designed to take full advantage of the stellar interrupt performance of the ARM Cortex-M4F core. No special pragmas or custom assembly code prologue/epilogue functions are required. For applications that require in-field programmability, the royalty-free TivaWare Boot Loader can act as an application loader and support in-field firmware updates.

The Advanced Encryption Standard (AES) is a publicly defined encryption standard used by the U.S. Government. AES is a strong encryption method with reasonable performance and size. In addition, it is fast in both hardware and software, is fairly easy to implement, and requires little memory. The Texas Instruments encryption package is available with full source code, and is based on Lesser General Public License (LGPL) source. An LGPL means that the code can be used within an application without any copyleft implications for the application (the code does not automatically become open source). Modifications to the package source, however, must be open source.

CRC (Cyclic Redundancy Check) is a technique to validate a span of data has the same contents as when previously checked. This technique can be used to validate correct receipt of messages (nothing lost or modified in transit), to validate data after decompression, to validate that Flash memory contents have not been changed, and for other cases where the data needs to be validated. A CRC is preferred over a simple checksum (for example, XOR all bits) because it catches changes more readily.

1.3.2.4 EEPROM (see page 544)
The TM4C123GH6PZ microcontroller includes an EEPROM with the following features:

- 2Kbytes of memory accessible as 512 32-bit words
- 32 blocks of 16 words (64 bytes) each
- Built-in wear leveling
- Access protection per block
- Lock protection option for the whole peripheral as well as per block using 32-bit to 96-bit unlock codes (application selectable)
Interrupt support for write completion to avoid polling

Endurance of 500K writes (when writing at fixed offset in every alternate page in circular fashion) to 15M operations (when cycling through two pages) per each 2-page block.

1.3.3 Serial Communications Peripherals

The TM4C123GH6PZ controller supports both asynchronous and synchronous serial communications with:

- Two CAN 2.0 A/B controllers
- USB 2.0 OTG/Host/Device
- Eight UARTs with IrDA, 9-bit and ISO 7816 support.
- Six I2C modules with four transmission speeds including high-speed mode
- Four Synchronous Serial Interface modules (SSI)

The following sections provide more detail on each of these communications functions.

1.3.3.1 Controller Area Network (CAN) (see page 1069)

Controller Area Network (CAN) is a multicast shared serial-bus standard for connecting electronic control units (ECUs). CAN was specifically designed to be robust in electromagnetically noisy environments and can utilize a differential balanced line like RS-485 or twisted-pair wire. Originally created for automotive purposes, it is now used in many embedded control applications (for example, industrial or medical). Bit rates up to 1 Mbps are possible at network lengths below 40 meters. Decreased bit rates allow longer network distances (for example, 125 Kbps at 500m).

A transmitter sends a message to all CAN nodes (broadcasting). Each node decides on the basis of the identifier received whether it should process the message. The identifier also determines the priority that the message enjoys in competition for bus access. Each CAN message can transmit from 0 to 8 bytes of user information.

The TM4C123GH6PZ microcontroller includes two CAN units with the following features:

- CAN protocol version 2.0 part A/B
- Bit rates up to 1 Mbps
- 32 message objects with individual identifier masks
- Maskable interrupt
- Disable Automatic Retransmission mode for Time-Triggered CAN (TTCAN) applications
- Programmable loopback mode for self-test operation
- Programmable FIFO mode enables storage of multiple message objects
- Gluelessly attaches to an external CAN transceiver through the CANnTX and CANnRX signals
1.3.3.2 **Universal Serial Bus (USB) (see page 1120)**

Universal Serial Bus (USB) is a serial bus standard designed to allow peripherals to be connected and disconnected using a standardized interface without rebooting the system.

The TM4C123GH6PZ microcontroller supports three configurations in USB 2.0 full and low speed: USB Device, USB Host, and USB On-The-Go (negotiated on-the-go as host or device when connected to other USB-enabled systems).

The USB module has the following features:

- Complies with USB-IF (Implementer's Forum) certification standards
- USB 2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps) operation with integrated PHY
- 4 transfer types: Control, Interrupt, Bulk, and Isochronous
- 16 endpoints
  - 1 dedicated control IN endpoint and 1 dedicated control OUT endpoint
  - 7 configurable IN endpoints and 7 configurable OUT endpoints
- 4 KB dedicated endpoint memory: one endpoint may be defined for double-buffered 1023-byte isochronous packet size
- VBUS droop and valid ID detection and interrupt
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive for up to three IN endpoints and three OUT endpoints
  - Channel requests asserted when FIFO contains required amount of data

1.3.3.3 **UART (see page 912)**

A Universal Asynchronous Receiver/Transmitter (UART) is an integrated circuit used for RS-232C serial communications, containing a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter), each clocked separately.

The TM4C123GH6PZ microcontroller includes eight fully programmable 16C550-type UARTs. Although the functionality is similar to a 16C550 UART, this UART design is not register compatible. The UART can generate individually masked interrupts from the Rx, Tx, modem flow control, modem status, and error conditions. The module generates a single combined interrupt when any of the interrupts are asserted and are unmasked.

The eight UARTs have the following features:

- Programmable baud-rate generator allowing speeds up to 5 Mbps for regular speed (divide by 16) and 10 Mbps for high speed (divide by 8)
- Separate 16x8 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation/detection
  - 1 or 2 stop bit generation
- IrDA serial-IR (SIR) encoder/decoder providing
  - Programmable use of IrDA Serial Infrared (SIR) or UART input/output
  - Support of IrDA SIR encoder/decoder functions for data rates up to 115.2 Kbps half-duplex
  - Support of normal 3/16 and low-power (1.41-2.23 μs) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power mode bit duration
- Support for communication with ISO 7816 smart cards
- Modem flow control and status (on UART1)
- EIA-485 9-bit support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
  - Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level

1.3.3.4 I²C (see page 1018)

The Inter-Integrated Circuit (I²C) bus provides bi-directional data transfer through a two-wire design (a serial data line SDA and a serial clock line SCL). The I²C bus interfaces to external I²C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on. The I²C bus may also be used for system testing and diagnostic purposes in product development and manufacture.

Each device on the I²C bus can be designated as either a master or a slave. I²C module supports both sending and receiving data as either a master or a slave and can operate simultaneously as both a master and a slave. Both the I²C master and slave can generate interrupts.

The TM4C123GH6PZ microcontroller includes six I²C modules with the following features:

- Devices on the I²C bus can be designated as either a master or a slave
– Supports both transmitting and receiving data as either a master or a slave
– Supports simultaneous master and slave operation

■ Four I²C modes
  – Master transmit
  – Master receive
  – Slave transmit
  – Slave receive

■ Four transmission speeds:
  – Standard (100 Kbps)
  – Fast-mode (400 Kbps)
  – Fast-mode plus (1 Mbps)
  – High-speed mode (3.33 Mbps)

■ Clock low timeout interrupt

■ Dual slave address capability

■ Glitch suppression

■ Master and slave interrupt generation
  – Master generates interrupts when a transmit or receive operation completes (or aborts due to an error)
  – Slave generates interrupts when data has been transferred or requested by a master or when a START or STOP condition is detected

■ Master with arbitration and clock synchronization, multimaster support, and 7-bit addressing mode

1.3.3.5 SSI (see page 973)

Synchronous Serial Interface (SSI) is a four-wire bi-directional communications interface that converts data between parallel and serial. The SSI module performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data transmitted to a peripheral device. The SSI module can be configured as either a master or slave device. As a slave device, the SSI module can also be configured to disable its output, which allows a master device to be coupled with multiple slave devices. The TX and RX paths are buffered with separate internal FIFOs.

The SSI module also includes a programmable bit rate clock divider and prescaler to generate the output serial clock derived from the SSI module’s input clock. Bit rates are generated based on the input clock and the maximum bit rate is determined by the connected peripheral.

The TM4C123GH6PZ microcontroller includes four SSI modules with the following features:
Programmable interface operation for Freescale SPI, MICROWIRE, or Texas Instruments synchronous serial interfaces

- Master or slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive FIFOs, each 16 bits wide and 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Internal loopback test mode for diagnostic/debug testing
- Standard FIFO-based interrupts and End-of-Transmission interrupt
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains 4 entries
  - Transmit single request asserted when there is space in the FIFO; burst request asserted when four or more entries are available to be written in the FIFO

1.3.4 System Integration

The TM4C123GH6PZ microcontroller provides a variety of standard system functions integrated into the device, including:

- Direct Memory Access Controller (DMA)
- System control and clocks including on-chip precision 16-MHz oscillator
- Six 32-bit timers (up to twelve 16-bit)
- Six wide 64-bit timers (up to twelve 32-bit)
- Twelve 32/64-bit Capture Compare PWM (CCP) pins
- Lower-power battery-backed Hibernation module
- Real-Time Clock in Hibernation module
- Two Watchdog Timers
  - One timer runs off the main oscillator
  - One timer runs off the precision internal oscillator
- Up to 69 GPIOs, depending on configuration
  - Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
  - Independently configurable to 2-, 4- or 8-mA drive capability
  - Up to 4 GPIOs can have 18-mA drive capability

The following sections provide more detail on each of these functions.
1.3.4.1 Direct Memory Access (see page 595)

The TM4C123GH6PZ microcontroller includes a Direct Memory Access (DMA) controller, known as micro-DMA (μDMA). The μDMA controller provides a way to offload data transfer tasks from the Cortex-M4F processor, allowing for more efficient use of the processor and the available bus bandwidth. The μDMA controller can perform transfers between memory and peripherals. It has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data. The μDMA controller provides the following features:

- ARM PrimeCell® 32-channel configurable μDMA controller
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes
  - Basic for simple transfer scenarios
  - Ping-pong for continuous data flow
  - Scatter-gather for a programmable list of up to 256 arbitrary transfers initiated from a single request
- Highly flexible and configurable channel operation
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules
  - Flexible channel assignments
  - One channel each for receive and transmit path for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable priority scheme
  - Optional software-initiated requests for any channel
- Two levels of priority
- Design optimizations for improved bus access performance between μDMA controller and the processor core
  - μDMA controller access is subordinate to core access
  - RAM striping
  - Peripheral bus segmentation
- Data sizes of 8, 16, and 32 bits
- Transfer size is programmable in binary steps from 1 to 1024
- Source and destination address increment size of byte, half-word, word, or no increment
- Maskable peripheral requests
Interrupt on transfer completion, with a separate interrupt per channel

1.3.4.2 System Control and Clocks (see page 212)

System control determines the overall operation of the device. It provides information about the device, controls power-saving features, controls the clocking of the device and individual peripherals, and handles reset detection and reporting.

- Device identification information: version, part number, SRAM size, Flash memory size, and so on
- Power control
  - On-chip fixed Low Drop-Out (LDO) voltage regulator
  - Hibernation module handles the power-up/down 3.3 V sequencing and control for the core digital logic and analog circuits
  - Low-power options for microcontroller: Sleep and Deep-Sleep modes with clock gating
  - Low-power options for on-chip modules: software controls shutdown of individual peripherals and memory
  - 3.3-V supply brown-out detection and reporting via interrupt or reset
- Multiple clock sources for microcontroller system clock. The following clock sources are provided to the TM4C123GH6PZ microcontroller:
  - Precision Internal Oscillator (PIOSC) providing a 16-MHz frequency
    - 16 MHz ±3% across temperature and voltage
    - Can be recalibrated with 7-bit trim resolution to achieve better accuracy (16 MHz ±1%)
    - Software power down control for low power modes
  - Main Oscillator (MOSC): A frequency-accurate clock source by one of two means: an external single-ended clock source is connected to the \( \text{OSC}_0 \) input pin, or an external crystal is connected across the \( \text{OSC}_0 \) input and \( \text{OSC}_1 \) output pins.
  - Low Frequency Internal Oscillator (LFIOSC): On-chip resource used during power-saving modes
  - Hibernate RTC oscillator (RTCOSC) clock that can be configured to be the 32.768-kHz external oscillator source from the Hibernation (HIB) module or the HIB Low Frequency clock source (HIB LFIOSC), which is located within the Hibernation Module.
- Flexible reset sources
  - Power-on reset (POR)
  - Reset pin assertion
  - Brown-out reset (BOR) detector alerts to system power drops
  - Software reset
  - Watchdog timer reset
Programmable Timers (see page 718)

Programmable timers can be used to count or time external events that drive the Timer input pins. Each 16/32-bit GPTM block provides two 16-bit timers/counters that can be configured to operate independently as timers or event counters, or configured to operate as one 32-bit timer or one 32-bit Real-Time Clock (RTC). Each 32/64-bit Wide GPTM block provides two 32-bit timers/counters that can be configured to operate independently as timers or event counters, or configured to operate as one 64-bit timer or one 64-bit Real-Time Clock (RTC). Timers can also be used to trigger analog-to-digital (ADC) conversions and DMA transfers.

The General-Purpose Timer Module (GPTM) contains six 16/32-bit GPTM blocks and six 32/64-bit Wide GPTM blocks with the following functional options:

- 16/32-bit operating modes:
  - 16- or 32-bit programmable one-shot timer
  - 16- or 32-bit programmable periodic timer
  - 16-bit general-purpose timer with an 8-bit prescaler
  - 32-bit Real-Time Clock (RTC) when using an external 32.768-KHz clock as the input
  - 16-bit input-edge count- or time-capture modes with an 8-bit prescaler
  - 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal

- 32/64-bit operating modes:
  - 32- or 64-bit programmable one-shot timer
  - 32- or 64-bit programmable periodic timer
  - 32-bit general-purpose timer with a 16-bit prescaler
  - 64-bit Real-Time Clock (RTC) when using an external 32.768-KHz clock as the input
  - 32-bit input-edge count- or time-capture modes with a16-bit prescaler
  - 32-bit PWM mode with a 16-bit prescaler and software-programmable output inversion of the PWM signal

- Count up or down

- Twelve 16/32-bit Capture Compare PWM pins (CCP)

- Twelve 32/64-bit Capture Compare PWM pins (CCP)

- Daisy chaining of timer modules to allow a single timer to initiate multiple timing events

- Timer synchronization allows selected timers to start counting on the same clock cycle

- ADC event trigger
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug (excluding RTC mode)

- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine

- Efficient transfers using Micro Direct Memory Access Controller (μDMA)
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt

### 1.3.4.4 CCP Pins (see page 727)

Capture Compare PWM pins (CCP) can be used by the General-Purpose Timer Module to time/count external events using the CCP pin as an input. Alternatively, the GPTM can generate a simple PWM output on the CCP pin.

The TM4C123GH6PZ microcontroller includes twelve 16/32-bit CCP pins that can be programmed to operate in the following modes:

- **Capture:** The GP Timer is incremented/decremented by programmed events on the CCP input. The GP Timer captures and stores the current timer value when a programmed event occurs.

- **Compare:** The GP Timer is incremented/decremented by programmed events on the CCP input. The GP Timer compares the current value with a stored value and generates an interrupt when a match occurs.

- **PWM:** The GP Timer is incremented/decremented by the system clock. A PWM signal is generated based on a match between the counter value and a value stored in a match register and is output on the CCP pin.

### 1.3.4.5 Hibernation Module (HIB) (see page 503)

The Hibernation module provides logic to switch power off to the main processor and peripherals and to wake on external or time-based events. The Hibernation module includes power-sequencing logic and has the following features:

- **32-bit real-time seconds counter (RTC) with 1/32,768 second resolution and a 15-bit sub-seconds counter**
  - 32-bit RTC seconds match register and a 15-bit sub seconds match for timed wake-up and interrupt generation with 1/32,768 second resolution
  - RTC predivider trim for making fine adjustments to the clock rate

- **Two mechanisms for power control**
  - System power control using discrete external regulator
  - On-chip power control using internal switches under register control

- **Dedicated pin for waking using an external signal**

- **RTC operational and hibernation memory valid as long as \( V_{DD} \) or \( V_{BAT} \) is valid**

- **Low-battery detection, signaling, and interrupt generation, with optional wake on low battery**
- GPIO pin state can be retained during hibernation
- Clock source from a 32.768-kHz external crystal or oscillator
- Sixteen 32-bit words of battery-backed memory to save state during hibernation
- Programmable interrupts for:
  - RTC match
  - External wake
  - Low battery

### 1.3.4.6 Watchdog Timers (see page 788)

A watchdog timer is used to regain control when a system has failed due to a software error or to the failure of an external device to respond in the expected way. The TM4C123GH6PZ Watchdog Timer can generate an interrupt, a non-maskable interrupt, or a reset when a time-out value is reached. In addition, the Watchdog Timer is ARM FiRM-compliant and can be configured to generate an interrupt to the microcontroller on its first time-out, and to generate a reset signal on its second timeout. Once the Watchdog Timer has been configured, the lock register can be written to prevent the timer configuration from being inadvertently altered.

The TM4C123GH6PZ microcontroller has two Watchdog Timer modules: Watchdog Timer 0 uses the system clock for its timer clock; Watchdog Timer 1 uses the PIOSC as its timer clock. The Watchdog Timer module has the following features:

- 32-bit down counter with a programmable load register
- Separate watchdog clock with an enable
- Programmable interrupt generation logic with interrupt masking and optional NMI function
- Lock register protection from runaway software
- Reset generation logic with an enable/disable
- User-enabled stalling when the microcontroller asserts the CPU Halt flag during debug

### 1.3.4.7 Programmable GPIOs (see page 659)

General-purpose input/output (GPIO) pins offer flexibility for a variety of connections. The TM4C123GH6PZ GPIO module is comprised of ten physical GPIO blocks, each corresponding to an individual GPIO port. The GPIO module is FiRM-compliant (compliant to the ARM Foundation IP for Real-Time Microcontrollers specification) and supports 0-69 programmable input/output pins. The number of GPIOs available depends on the peripherals being used (see "Signal Tables" on page 1354 for the signals available to each GPIO pin).

- Up to 69 GPIOs, depending on configuration
- Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
- 5-V-tolerant in input configuration
- Fast toggle capable of a change every clock cycle for ports on AHB, every two clock cycles for ports on APB
■ Programmable control for GPIO interrupts
  – Interrupt generation masking
  – Edge-triggered on rising, falling, or both
  – Level-sensitive on High or Low values
■ Bit masking in both read and write operations through address lines
■ Can be used to initiate an ADC sample sequence or a μDMA transfer
■ Pin state can be retained during Hibernation mode
■ Pins configured as digital inputs are Schmitt-triggered
■ Programmable control for GPIO pad configuration
  – Weak pull-up or pull-down resistors
  – 2-mA, 4-mA, and 8-mA pad drive for digital communication; up to four pads can sink 18-mA for high-current applications
  – Slew rate control for 8-mA pad drive
  – Open drain enables
  – Digital input enables

1.3.5 Advanced Motion Control

The TM4C123GH6PZ microcontroller provides motion control functions integrated into the device, including:

■ Two PWM modules, with a total of 16 advanced PWM outputs for motion and energy applications
■ Eight fault inputs to promote low-latency shutdown
■ Two Quadrature Encoder Inputs (QEI)

The following provides more detail on these motion control functions.

1.3.5.1 PWM (see page 1252)

The TM4C123GH6PZ microcontroller contains two PWM modules, each with four PWM generator blocks and a control block, for a total of 16 PWM outputs. Pulse width modulation (PWM) is a powerful technique for digitally encoding analog signal levels. High-resolution counters are used to generate a square wave, and the duty cycle of the square wave is modulated to encode an analog signal. Typical applications include switching power supplies and motor control. Each TM4C123GH6PZ PWM module consists of four PWM generator block and a control block. Each PWM generator block contains one timer (16-bit down or up/down counter), two comparators, a PWM signal generator, a dead-band generator, and an interrupt/ADC-trigger selector. Each PWM generator block produces two PWM signals that can either be independent signals or a single pair of complementary signals with dead-band delays inserted.

Each PWM generator has the following features:
- Four fault-condition handling inputs to quickly provide low-latency shutdown and prevent damage to the motor being controlled, for a total of eight inputs

- One 16-bit counter
  - Runs in Down or Up/Down mode
  - Output frequency controlled by a 16-bit load value
  - Load value updates can be synchronized
  - Produces output signals at zero and load value

- Two PWM comparators
  - Comparator value updates can be synchronized
  - Produces output signals on match

- PWM signal generator
  - Output PWM signal is constructed based on actions taken as a result of the counter and PWM comparator output signals
  - Produces two independent PWM signals

- Dead-band generator
  - Produces two PWM signals with programmable dead-band delays suitable for driving a half-H bridge
  - Can be bypassed, leaving input PWM signals unmodified

- Can initiate an ADC sample sequence

The control block determines the polarity of the PWM signals and which signals are passed through to the pins. The output of the PWM generation blocks are managed by the output control block before being passed to the device pins. The PWM control block has the following options:

- PWM output enable of each PWM signal
- Optional output inversion of each PWM signal (polarity control)
- Optional fault handling for each PWM signal
- Synchronization of timers in the PWM generator blocks
- Synchronization of timer/comparator updates across the PWM generator blocks
- Extended PWM synchronization of timer/comparator updates across the PWM generator blocks
- Interrupt status summary of the PWM generator blocks
- Extended PWM fault handling, with multiple fault signals, programmable polarities, and filtering
- PWM generators can be operated independently or synchronized with other generators
1.3.5.2 **QEI (see page 1330)**

A quadrature encoder, also known as a 2-channel incremental encoder, converts linear displacement into a pulse signal. By monitoring both the number of pulses and the relative phase of the two signals, the position, direction of rotation, and speed can be tracked. In addition, a third channel, or index signal, can be used to reset the position counter. The TM4C123GH6PZ quadrature encoder with index (QEI) module interprets the code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture a running estimate of the velocity of the encoder wheel. The input frequency of the QEI inputs may be as high as 1/4 of the processor frequency (for example, 20 MHz for a 80-MHz system).

The TM4C123GH6PZ microcontroller includes two QEI modules providing control of two motors at the same time with the following features:

- Position integrator that tracks the encoder position
- Programmable noise filter on the inputs
- Velocity capture using built-in timer
- The input frequency of the QEI inputs may be as high as 1/4 of the processor frequency (for example, 12.5 MHz for a 50-MHz system)
- Interrupt generation on:
  - Index pulse
  - Velocity-timer expiration
  - Direction change
  - Quadrature error detection

1.3.6 **Analog**

The TM4C123GH6PZ microcontroller provides analog functions integrated into the device, including:

- Two 12-bit Analog-to-Digital Converters (ADC), with a total of 22 analog input channels and each with a sample rate of one million samples/second
- Three analog comparators
- On-chip voltage regulator

The following provides more detail on these analog functions.

1.3.6.1 **ADC (see page 813)**

An analog-to-digital converter (ADC) is a peripheral that converts a continuous analog voltage to a discrete digital number. The TM4C123GH6PZ ADC module features 12-bit conversion resolution and supports 22 input channels plus an internal temperature sensor. Four buffered sample sequencers allow rapid sampling of up to 22 analog input sources without controller intervention. Each sample sequencer provides flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority. Each ADC module has a digital comparator function that allows the conversion value to be diverted to a comparison unit that provides eight digital comparators.
The TM4C123GH6PZ microcontroller provides two ADC modules, each with the following features:

- 22 shared analog input channels
- 12-bit precision ADC
- Single-ended and differential-input configurations
- On-chip internal temperature sensor
- Maximum sample rate of one million samples/second
- Optional phase shift in sample time programmable from 22.5° to 337.5°
- Four programmable sample conversion sequencers from one to eight entries long, with corresponding conversion result FIFOs
- Flexible trigger control
  - Controller (software)
  - Timers
  - Analog Comparators
  - PWM
  - GPIO
- Hardware averaging of up to 64 samples
- Eight digital comparators
- Converter uses two external reference signals (VREFA+ and VREFA−) or VDDA and GNDA as the voltage reference
- Power and ground for the analog circuitry is separate from the digital power and ground
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Dedicated channel for each sample sequencer
  - ADC module uses burst requests for DMA

1.3.6.2 Analog Comparators (see page 1236)

An analog comparator is a peripheral that compares two analog voltages and provides a logical output that signals the comparison result. The TM4C123GH6PZ microcontroller provides three independent integrated analog comparators that can be configured to drive an output or generate an interrupt or ADC event.

The comparator can provide its output to a device pin, acting as a replacement for an analog comparator on the board, or it can be used to signal the application via interrupts or triggers to the ADC to cause it to start capturing a sample sequence. The interrupt generation and ADC triggering logic is separate. This means, for example, that an interrupt can be generated on a rising edge and the ADC triggered on a falling edge.
The TM4C123GH6PZ microcontroller provides three independent integrated analog comparators with the following functions:

- Compare external pin input to external pin input or to internal programmable voltage reference
- Compare a test voltage against any one of the following voltages:
  - An individual external reference voltage
  - A shared single external reference voltage
  - A shared internal reference voltage

1.3.7 JTAG and ARM Serial Wire Debug (see page 200)

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a Test Access Port and Boundary Scan Architecture for digital integrated circuits and provides a standardized serial interface for controlling the associated test logic. The TAP, Instruction Register (IR), and Data Registers (DR) can be used to test the interconnections of assembled printed circuit boards and obtain manufacturing information on the components. The JTAG Port also provides a means of accessing and controlling design-for-test features such as I/O pin observation and control, scan testing, and debugging. Texas Instruments replaces the ARM SW-DP and JTAG-DP with the ARM Serial Wire JTAG Debug Port (SWJ-DP) interface. The SWJ-DP interface combines the SWD and JTAG debug ports into one module providing all the normal JTAG debug and test functionality plus real-time access to system memory without halting the core or requiring any target resident code. The SWJ-DP interface has the following features:

- IEEE 1149.1-1990 compatible Test Access Port (TAP) controller
- Four-bit Instruction Register (IR) chain for storing JTAG instructions
- IEEE standard instructions: BYPASS, IDCODE, SAMPLE/PRELOAD, and EXTEST
- ARM additional instructions: APACC, DPACC and ABORT
- Integrated ARM Serial Wire Debug (SWD)
  - Serial Wire JTAG Debug Port (SWJ-DP)
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
  - Data Watchpoint and Trace (DWT) unit for implementing watchpoints, trigger resources, and system profiling
  - Instrumentation Trace Macrocell (ITM) for support of printf style debugging
  - Embedded Trace Macrocell (ETM) for instruction trace capture
  - Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

1.3.8 Packaging and Temperature

- 100-pin RoHS-compliant LQFP package
- Industrial (−40°C to 85°C) ambient temperature range
Extended (-40°C to 105°C) ambient temperature range

1.4 TM4C123GH6PZ Microcontroller Hardware Details
Details on the pins and package can be found in the following sections:
- “Pin Diagram” on page 1353
- “Signal Tables” on page 1354
- “Electrical Characteristics” on page 1395
- “Package Information” on page 1440

1.5 Kits
The Tiva™ C Series provides the hardware and software tools that engineers need to begin development quickly.
- Reference Design Kits accelerate product development by providing ready-to-run hardware and comprehensive documentation including hardware design files
- Evaluation Kits provide a low-cost and effective means of evaluating TM4C123GH6PZ microcontrollers before purchase
- Development Kits provide you with all the tools you need to develop and prototype embedded applications right out of the box

See the Tiva series website at http://www.ti.com/tiva-c for the latest tools available, or ask your distributor.

1.6 Support Information
For support on Tiva™ C Series products, contact the TI Worldwide Product Information Center nearest you.
2 The Cortex-M4F Processor

The ARM® Cortex™-M4F processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, reduced pin count, and low power consumption, while delivering outstanding computational performance and exceptional system response to interrupts. Features include:

- 32-bit ARM® Cortex™-M4F architecture optimized for small-footprint embedded applications
- 80-MHz operation; 100 DMIPS performance
- Outstanding processing performance combined with fast interrupt handling
- Thumb-2 mixed 16-/32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory utilization and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- IEEE754-compliant single-precision Floating-Point Unit (FPU)
- 16-bit SIMD vector processing unit
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system and memories
- Hardware division and fast digital-signal-processing orientated multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Memory protection unit (MPU) to provide a privileged mode for protected operating system functionality
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle Flash memory usage up to specific frequencies; see “Internal Memory” on page 534 for more information.
- Ultra-low power consumption with integrated sleep modes
The Tiva™ C Series microcontrollers build on this core to bring high-performance 32-bit computing to

This chapter provides information on the Tiva™ C Series implementation of the Cortex-M4F processor, including the programming model, the memory model, the exception model, fault handling, and power management.

For technical details on the instruction set, see the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A).

### 2.1 Block Diagram

The Cortex-M4F processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division.

To facilitate the design of cost-sensitive devices, the Cortex-M4F processor implements tightly coupled system components that reduce processor area while significantly improving interrupt handling and system debug capabilities. The Cortex-M4F processor implements a version of the Thumb® instruction set based on Thumb-2 technology, ensuring high code density and reduced program memory requirements. The Cortex-M4F instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers.

The Cortex-M4F processor closely integrates a nested interrupt controller (NVIC), to deliver industry-leading interrupt performance. The TM4C123GH6PZ NVIC includes a non-maskable interrupt (NMI) and provides eight interrupt priority levels. The tight integration of the processor core and NVIC provides fast execution of interrupt service routines (ISRs), dramatically reducing interrupt latency. The hardware stacking of registers and the ability to suspend load-multiple and store-multiple operations further reduce interrupt latency. Interrupt handlers do not require any assembler stubs which removes code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another. To optimize low-power designs, the NVIC integrates with the sleep modes, including Deep-sleep mode, which enables the entire device to be rapidly powered down.
2.2 Overview

2.2.1 System-Level Interface

The Cortex-M4F processor provides multiple interfaces using AMBA® technology to provide high-speed, low-latency memory accesses. The core supports unaligned data accesses and implements atomic bit manipulation that enables faster peripheral controls, system spinlocks, and thread-safe Boolean data handling.

The Cortex-M4F processor has a memory protection unit (MPU) that provides fine-grain memory control, enabling applications to implement security privilege levels and separate code, data and stack on a task-by-task basis.

2.2.2 Integrated Configurable Debug

The Cortex-M4F processor implements a complete hardware debug solution, providing high system visibility of the processor and memory through either a traditional JTAG port or a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices. The Tiva™ C Series implementation replaces the ARM SW-DP and JTAG-DP with the ARM CoreSight™-compliant Serial Wire JTAG Debug Port (SWJ-DP) interface. The SWJ-DP interface combines the SWD and JTAG debug ports into one module. See the ARM® Debug Interface V5 Architecture Specification for details on SWJ-DP.

For system trace, the processor integrates an Instrumentation Trace Macrocell (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system trace events, a Serial Wire Viewer (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.
The Embedded Trace Macrocell (ETM) delivers unrivaled instruction trace capture in an area smaller than traditional trace units, enabling full instruction trace. For more details on the ARM ETM, see the ARM® Embedded Trace Macrocell Architecture Specification.

The Flash Patch and Breakpoint Unit (FPB) provides up to eight hardware breakpoint comparators that debuggers can use. The comparators in the FPB also provide remap functions for up to eight words of program code in the code memory region. This FPB enables applications stored in a read-only area of Flash memory to be patched in another area of on-chip SRAM or Flash memory. If a patch is required, the application programs the FPB to remap a number of addresses. When those addresses are accessed, the accesses are redirected to a remap table specified in the FPB configuration.

For more information on the Cortex-M4F debug capabilities, see the ARM® Debug Interface V5 Architecture Specification.

### 2.2.3 Trace Port Interface Unit (TPIU)

The TPIU acts as a bridge between the Cortex-M4F trace data from the ITM, and an off-chip Trace Port Analyzer, as shown in Figure 2-2 on page 72.

**Figure 2-2. TPIU Block Diagram**

---

#### 2.2.4 Cortex-M4F System Component Details

The Cortex-M4F includes the following system components:

- **SysTick**
  
  A 24-bit count-down timer that can be used as a Real-Time Operating System (RTOS) tick timer or as a simple counter (see “System Timer (SysTick)” on page 123).

- **Nested Vectored Interrupt Controller (NVIC)**
An embedded interrupt controller that supports low latency interrupt processing (see “Nested Vectored Interrupt Controller (NVIC)” on page 124).

- **System Control Block (SCB)**
  The programming model interface to the processor. The SCB provides system implementation information and system control, including configuration, control, and reporting of system exceptions (see “System Control Block (SCB)” on page 125).

- **Memory Protection Unit (MPU)**
  Improves system reliability by defining the memory attributes for different memory regions. The MPU provides up to eight different regions and an optional predefined background region (see “Memory Protection Unit (MPU)” on page 125).

- **Floating-Point Unit (FPU)**
  Fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square-root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions (see “Floating-Point Unit (FPU)” on page 130).

### 2.3 Programming Model

This section describes the Cortex-M4F programming model. In addition to the individual core register descriptions, information about the processor modes and privilege levels for software execution and stacks is included.

#### 2.3.1 Processor Mode and Privilege Levels for Software Execution

The Cortex-M4F has two modes of operation:

- **Thread mode**
  Used to execute application software. The processor enters Thread mode when it comes out of reset.

- **Handler mode**
  Used to handle exceptions. When the processor has finished exception processing, it returns to Thread mode.

In addition, the Cortex-M4F has two privilege levels:

- **Unprivileged**
  In this mode, software has the following restrictions:
  - Limited access to the MSR and MRS instructions and no use of the CPS instruction
  - No access to the system timer, NVIC, or system control block
  - Possibly restricted access to memory or peripherals

- **Privileged**
  In this mode, software can use all the instructions and has access to all resources.

In Thread mode, the **CONTROL** register (see page 88) controls whether software execution is privileged or unprivileged. In Handler mode, software execution is always privileged.
Only privileged software can write to the **CONTROL** register to change the privilege level for software execution in Thread mode. Unprivileged software can use the **SVC** instruction to make a supervisor call to transfer control to privileged software.

### 2.3.2 Stacks

The processor uses a full descending stack, meaning that the stack pointer indicates the last stacked item on the memory. When the processor pushes a new item onto the stack, it decrements the stack pointer and then writes the item to the new memory location. The processor implements two stacks: the main stack and the process stack, with a pointer for each held in independent registers (see the **SP** register on page 78).

In Thread mode, the **CONTROL** register (see page 88) controls whether the processor uses the main stack or the process stack. In Handler mode, the processor always uses the main stack. The options for processor operations are shown in Table 2-1 on page 74.

<table>
<thead>
<tr>
<th>Processor Mode</th>
<th>Use</th>
<th>Privilege Level</th>
<th>Stack Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thread</td>
<td>Applications</td>
<td>Privileged or unprivileged</td>
<td>Main stack or process stack</td>
</tr>
<tr>
<td>Handler</td>
<td>Exception handlers</td>
<td>Always privileged</td>
<td>Main stack</td>
</tr>
</tbody>
</table>

a. See **CONTROL** (page 88).

### 2.3.3 Register Map

Figure 2-3 on page 75 shows the Cortex-M4F register set. Table 2-2 on page 75 lists the Core registers. The core registers are not memory mapped and are accessed by register name, so the base address is n/a (not applicable) and there is no offset.
**Figure 2-3. Cortex-M4F Register Set**

Low registers:
- R0
- R1
- R2
- R3
- R4
- R5
- R6
- R7
- R8
- R9
- R10
- R11
- R12

High registers:
- SP (R13)
- LR (R14)
- PC (R15)

General-purpose registers:
- PSP
- MSP

Stack Pointer
- SP (R13)

Link Register
- LR (R14)

Program Counter
- PC (R15)

Program status register
- PSR
- PRIMASK
- FAULTMASK
- BASEPRI
- CONTROL

Exception mask registers

Special registers

‡ Banked version of SP

**Table 2-2. Processor Register Map**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>R0</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 0</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R1</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 1</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R2</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 2</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R3</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 3</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R4</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 4</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R5</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 5</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R6</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 6</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R7</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 7</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R8</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 8</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R9</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 9</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R10</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 10</td>
<td>77</td>
</tr>
<tr>
<td>-</td>
<td>R11</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 11</td>
<td>77</td>
</tr>
</tbody>
</table>
Table 2-2. Processor Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R12</td>
<td>RW</td>
<td>-</td>
<td>Cortex General-Purpose Register 12</td>
<td>77</td>
</tr>
<tr>
<td></td>
<td>SP</td>
<td>RW</td>
<td>-</td>
<td>Stack Pointer</td>
<td>78</td>
</tr>
<tr>
<td></td>
<td>LR</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Link Register</td>
<td>79</td>
</tr>
<tr>
<td></td>
<td>PC</td>
<td>RW</td>
<td>-</td>
<td>Program Counter</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td>PSR</td>
<td>RW</td>
<td>0x0100.0000</td>
<td>Program Status Register</td>
<td>81</td>
</tr>
<tr>
<td></td>
<td>PRIMASK</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Priority Mask Register</td>
<td>85</td>
</tr>
<tr>
<td></td>
<td>FAULTMASK</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Fault Mask Register</td>
<td>86</td>
</tr>
<tr>
<td></td>
<td>BASEPRI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Base Priority Mask Register</td>
<td>87</td>
</tr>
<tr>
<td></td>
<td>CONTROL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Control Register</td>
<td>88</td>
</tr>
<tr>
<td></td>
<td>FPSC</td>
<td>RW</td>
<td>-</td>
<td>Floating-Point Status Control</td>
<td>90</td>
</tr>
</tbody>
</table>

2.3.4  Register Descriptions

This section lists and describes the Cortex-M4F registers, in the order shown in Figure 2-3 on page 75. The core registers are not memory mapped and are accessed by register name rather than offset.

**Note:** The register type shown in the register descriptions refers to type during program execution in Thread mode and Handler mode. Debug access can differ.
Register 1: Cortex General-Purpose Register 0 (R0)
Register 2: Cortex General-Purpose Register 1 (R1)
Register 3: Cortex General-Purpose Register 2 (R2)
Register 4: Cortex General-Purpose Register 3 (R3)
Register 5: Cortex General-Purpose Register 4 (R4)
Register 6: Cortex General-Purpose Register 5 (R5)
Register 7: Cortex General-Purpose Register 6 (R6)
Register 8: Cortex General-Purpose Register 7 (R7)
Register 9: Cortex General-Purpose Register 8 (R8)
Register 10: Cortex General-Purpose Register 9 (R9)
Register 11: Cortex General-Purpose Register 10 (R10)
Register 12: Cortex General-Purpose Register 11 (R11)
Register 13: Cortex General-Purpose Register 12 (R12)

The \( R_n \) registers are 32-bit general-purpose registers for data operations and can be accessed from either privileged or unprivileged mode.

Cortex General-Purpose Register 0 (R0)

Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:0      | DATA  | RW   | -     | Register data.
Register 14: Stack Pointer (SP)

The Stack Pointer (SP) is register R13. In Thread mode, the function of this register changes depending on the ASP bit in the Control Register (CONTROL) register. When the ASP bit is clear, this register is the Main Stack Pointer (MSP). When the ASP bit is set, this register is the Process Stack Pointer (PSP). On reset, the ASP bit is clear, and the processor loads the MSP with the value from address 0x0000.0000. The MSP can only be accessed in privileged mode; the PSP can be accessed in either privileged or unprivileged mode.

Stack Pointer (SP)
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>SP</td>
<td>RW</td>
<td>-</td>
<td>This field is the address of the stack pointer.</td>
</tr>
</tbody>
</table>
Register 15: Link Register (LR)

The Link Register (LR) is register R14, and it stores the return information for subroutines, function calls, and exceptions. The Link Register can be accessed from either privileged or unprivileged mode.

EXC_RETURN is loaded into the LR on exception entry. See Table 2-10 on page 111 for the values and description.

Link Register (LR)
Type RW, reset 0xFFFF.FFFF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>LINK</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>This field is the return address.</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
Register 16: Program Counter (PC)

The Program Counter (PC) is register R15, and it contains the current program address. On reset, the processor loads the PC with the value of the reset vector, which is at address 0x0000.0004. Bit 0 of the reset vector is loaded into the THUMB bit of the EPSR at reset and must be 1. The PC register can be accessed in either privileged or unprivileged mode.

<table>
<thead>
<tr>
<th>Type/RW</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC</td>
<td>RW</td>
<td>This field is the current program address.</td>
</tr>
</tbody>
</table>
Register 17: Program Status Register (PSR)

Note: This register is also referred to as xPSR.

The Program Status Register (PSR) has three functions, and the register bits are assigned to the different functions:

- **Application Program Status Register (APSR)**, bits 31:27, bits 19:16
- **Execution Program Status Register (EPSR)**, bits 26:24, 15:10
- **Interrupt Program Status Register (IPSR)**, bits 7:0

The PSR, IPSR, and EPSR registers can only be accessed in privileged mode; the APSR register can be accessed in either privileged or unprivileged mode.

APSR contains the current state of the condition flags from previous instruction executions.

EPSR contains the Thumb state bit and the execution state bits for the If-Then (IT) instruction or the Interruptible-Continuable Instruction (ICI) field for an interrupted load multiple or store multiple instruction. Attempts to read the EPSR directly through application software using the MSR instruction always return zero. Attempts to write the EPSR using the MSR instruction in application software are always ignored. Fault handlers can examine the EPSR value in the stacked PSR to determine the operation that faulted (see "Exception Entry and Return" on page 108).

IPSR contains the exception type number of the current Interrupt Service Routine (ISR).

These registers can be accessed individually or as a combination of any two or all three registers, using the register name as an argument to the MSR or MRS instructions. For example, all of the registers can be read using PSR with the MRS instruction, or APSR only can be written to using APSR with the MSR instruction. page 81 shows the possible register combinations for the PSR. See the MRS and MSR instruction descriptions in the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A) for more information about how to access the program status registers.

Table 2-3. PSR Register Combinations

<table>
<thead>
<tr>
<th>Register</th>
<th>Type</th>
<th>Combination</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSR</td>
<td>RW&lt;sup&gt;a&lt;/sup&gt;, &lt;sup&gt;b&lt;/sup&gt;</td>
<td>APSR, EPSR, and IPSR</td>
</tr>
<tr>
<td>EPSR</td>
<td>RO</td>
<td>EPSR and IPSR</td>
</tr>
<tr>
<td>APSR</td>
<td>RW&lt;sup&gt;c&lt;/sup&gt;</td>
<td>APSR and IPSR</td>
</tr>
<tr>
<td>IPSR</td>
<td>RW&lt;sup&gt;d&lt;/sup&gt;</td>
<td>APSR and EPSR</td>
</tr>
</tbody>
</table>

a. The processor ignores writes to the IPSR bits.
b. Reads of the EPSR bits return zero, and the processor ignores writes to these bits.

Program Status Register (PSR)

Type RW, reset 0x0100.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>1</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
</tbody>
</table>

Tiva™ TM4C123GH6PZ Microcontroller

June 12, 2014

Texas Instruments-Production Data
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>N</td>
<td>RW</td>
<td>0</td>
<td><strong>APSR Negative or Less Flag</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The previous operation result was negative or less than.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The previous operation result was positive, zero, greater than, or equal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value of this bit is only meaningful when accessing <strong>PSR</strong> or <strong>APSR</strong>.</td>
</tr>
<tr>
<td>30</td>
<td>Z</td>
<td>RW</td>
<td>0</td>
<td><strong>APSR Zero Flag</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The previous operation result was zero.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The previous operation result was non-zero.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value of this bit is only meaningful when accessing <strong>PSR</strong> or <strong>APSR</strong>.</td>
</tr>
<tr>
<td>29</td>
<td>C</td>
<td>RW</td>
<td>0</td>
<td><strong>APSR Carry or Borrow Flag</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The previous add operation resulted in a carry bit or the previous subtract operation did not result in a borrow bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The previous add operation did not result in a carry bit or the previous subtract operation resulted in a borrow bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value of this bit is only meaningful when accessing <strong>PSR</strong> or <strong>APSR</strong>.</td>
</tr>
<tr>
<td>28</td>
<td>V</td>
<td>RW</td>
<td>0</td>
<td><strong>APSR Overflow Flag</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The previous operation resulted in an overflow.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The previous operation did not result in an overflow.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value of this bit is only meaningful when accessing <strong>PSR</strong> or <strong>APSR</strong>.</td>
</tr>
<tr>
<td>27</td>
<td>Q</td>
<td>RW</td>
<td>0</td>
<td><strong>APSR DSP Overflow and Saturation Flag</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  DSP Overflow or saturation has occurred when using a SIMD instruction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  DSP overflow or saturation has not occurred since reset or since the bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value of this bit is only meaningful when accessing <strong>PSR</strong> or <strong>APSR</strong>. This bit is cleared by software using an <strong>MRS</strong> instruction.</td>
</tr>
</tbody>
</table>
These bits, along with bits 15:10, contain the Interruptible-Continuable Instruction (ICI) field for an interrupted load multiple or store multiple instruction or the execution state bits of the IT instruction.

When EPSR holds the ICI execution state, bits 26:25 are zero.

The If-Then block contains up to four instructions following an IT instruction. Each instruction in the block is conditional. The conditions for the instructions are either all the same, or some can be the inverse of others. See the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A) for more information.

The value of this field is only meaningful when accessing PSR or EPSR. Note that these EPSR bits cannot be accessed using MSR and MRS instructions but the definitions are provided to allow the stacked (E)PSR value to be decoded within an exception handler.

The value of this bit is only meaningful when accessing PSR or EPSR.

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

See the description of the SEL instruction in the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A) for more information.

The value of this field is only meaningful when accessing PSR or APSR.
These bits, along with bits 26:25, contain the Interruptible-Continuable Instruction (ICI) field for an interrupted load multiple or store multiple instruction or the execution state bits of the IT instruction.

When an interrupt occurs during the execution of an LDM, STM, PUSH, POP, VLDM, VSTM, VPUSH, or VPOP instruction, the processor stops the load multiple or store multiple instruction operation temporarily and stores the next register operand in the multiple load or store instruction. When EPSR holds the ICI execution state, bits 11:10 are zero.

The If-Then block contains up to four instructions following a 16-bit IT instruction. Each instruction in the block is conditional. The conditions for the instructions are either all the same, or some can be the inverse of others. See the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A) for more information.

The value of this field is only meaningful when accessing PSR or EPSR.

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

This field contains the exception type number of the current Interrupt Service Routine (ISR).

See “Exception Types” on page 102 for more information.

The value of this field is only meaningful when accessing PSR or IPSR.
Register 18: Priority Mask Register (PRIMASK)

The **PRIMASK** register prevents activation of all exceptions with programmable priority. Reset, non-maskable interrupt (NMI), and hard fault are the only exceptions with fixed priority. Exceptions should be disabled when they might impact the timing of critical tasks. This register is only accessible in privileged mode. The **MSR** and **MRS** instructions are used to access the **PRIMASK** register, and the **CPS** instruction may be used to change the value of the **PRIMASK** register. See the Cortex™-M4 instruction set chapter in the *ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A)* for more information on these instructions. For more information on exception priority levels, see “Exception Types” on page 102.

Priority Mask Register (PRIMASK)

Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>PRIMASK</td>
<td>RW</td>
<td>0</td>
<td>Priority Mask</td>
</tr>
</tbody>
</table>

- **Value** Description
  - 1 Prevents the activation of all exceptions with configurable priority.
  - 0 No effect.
Register 19: Fault Mask Register (FAULTMASK)

The **FAULTMASK** register prevents activation of all exceptions except for the Non-Maskable Interrupt (NMI). Exceptions should be disabled when they might impact the timing of critical tasks. This register is only accessible in privileged mode. The **MSR** and **MRS** instructions are used to access the **FAULTMASK** register, and the **CPS** instruction may be used to change the value of the **FAULTMASK** register. See the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number **ARM DUI 0553A**) for more information on these instructions. For more information on exception priority levels, see “Exception Types” on page 102.

Fault Mask Register (FAULTMASK)
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>FAULTMASK</td>
<td>RW</td>
<td>0</td>
<td>Fault Mask</td>
</tr>
</tbody>
</table>

The processor clears the **FAULTMASK** bit on exit from any exception handler except the NMI handler.
Register 20: Base Priority Mask Register (BASEPRI)

The BASEPRI register defines the minimum priority for exception processing. When BASEPRI is set to a nonzero value, it prevents the activation of all exceptions with the same or lower priority level as the BASEPRI value. Exceptions should be disabled when they might impact the timing of critical tasks. This register is only accessible in privileged mode. For more information on exception priority levels, see “Exception Types” on page 102.

Base Priority Mask Register (BASEPRI)
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RW</td>
<td>0x0</td>
<td>Base Priority</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Any exception that has a programmable priority level with the same or lower priority as the value of this field is masked. The PRIMASK register can be used to mask all exceptions with programmable priority levels. Higher priority exceptions have lower priority levels.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:5</td>
<td>BASEPRI</td>
<td>RW</td>
<td>0x0</td>
<td>Base Priority</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Any exception that has a programmable priority level with the same or lower priority as the value of this field is masked. The PRIMASK register can be used to mask all exceptions with programmable priority levels. Higher priority exceptions have lower priority levels.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 All exceptions are unmasked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 All exceptions with priority level 1-7 are masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 All exceptions with priority level 2-7 are masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 All exceptions with priority level 3-7 are masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x4 All exceptions with priority level 4-7 are masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x5 All exceptions with priority level 5-7 are masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x6 All exceptions with priority level 6-7 are masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x7 All exceptions with priority level 7 are masked.</td>
</tr>
<tr>
<td>4:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 21: Control Register (CONTROL)

The CONTROL register controls the stack used and the privilege level for software execution when the processor is in Thread mode, and indicates whether the FPU state is active. This register is only accessible in privileged mode.

Handler mode always uses the MSP, so the processor ignores explicit writes to the ASP bit of the CONTROL register when in Handler mode. The exception entry and return mechanisms automatically update the CONTROL register based on the EXC_RETURN value (see Table 2-10 on page 111). In an OS environment, threads running in Thread mode should use the process stack and the kernel and exception handlers should use the main stack. By default, Thread mode uses the MSP. To switch the stack pointer used in Thread mode to the PSP, either use the MSR instruction to set the ASP bit, as detailed in the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A), or perform an exception return to Thread mode with the appropriate EXC_RETURN value, as shown in Table 2-10 on page 111.

Note: When changing the stack pointer, software must use an ISB instruction immediately after the MSR instruction, ensuring that instructions after the ISB execute use the new stack pointer. See the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A).

Control Register (CONTROL)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>FPCA</td>
<td>RW</td>
<td>0</td>
<td>Floating-Point Context Active</td>
</tr>
</tbody>
</table>

Important: Two bits control when FPCA can be enabled: the ASPEN bit in the Floating-Point Context Control (FPCC) register and the DISFPCA bit in the Auxiliary Control (ACTLR) register.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ASP</td>
<td>RW</td>
<td>0</td>
<td>Active Stack Pointer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>The <strong>PSP</strong> is the current stack pointer.</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The <strong>MSP</strong> is the current stack pointer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>In Handler mode, this bit reads as zero and ignores writes. The Cortex-M4F updates this bit automatically on exception return.</td>
</tr>
<tr>
<td>0</td>
<td>TMPL</td>
<td>RW</td>
<td>0</td>
<td>Thread Mode Privilege Level</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>Unprivileged software can be executed in Thread mode.</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>Only privileged software can be executed in Thread mode.</td>
</tr>
</tbody>
</table>
Register 22: Floating-Point Status Control (FPSC)

The FPSC register provides all necessary user-level control of the floating-point system.

### Floating-Point Status Control (FPSC)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>N</td>
<td>RW</td>
<td>-</td>
<td>Negative Condition Code Flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Floating-point comparison operations update this condition code flag.</td>
</tr>
<tr>
<td>30</td>
<td>Z</td>
<td>RW</td>
<td>-</td>
<td>Zero Condition Code Flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Floating-point comparison operations update this condition code flag.</td>
</tr>
<tr>
<td>29</td>
<td>C</td>
<td>RW</td>
<td>-</td>
<td>Carry Condition Code Flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Floating-point comparison operations update this condition code flag.</td>
</tr>
<tr>
<td>28</td>
<td>V</td>
<td>RW</td>
<td>-</td>
<td>Overflow Condition Code Flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Floating-point comparison operations update this condition code flag.</td>
</tr>
<tr>
<td>27</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>26</td>
<td>AHP</td>
<td>RW</td>
<td>-</td>
<td>Alternative Half-Precision</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, alternative half-precision format is selected. When clear, IEEE half-precision format is selected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The AHP bit in the FPDSC register holds the default value for this bit.</td>
</tr>
<tr>
<td>25</td>
<td>DN</td>
<td>RW</td>
<td>-</td>
<td>Default NaN Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, any operation involving one or more NaNs returns the Default NaN. When clear, NaN operands propagate through to the output of a floating-point operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The DN bit in the FPDSC register holds the default value for this bit.</td>
</tr>
<tr>
<td>24</td>
<td>FZ</td>
<td>RW</td>
<td>-</td>
<td>Flush-to-Zero Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, Flush-to-Zero mode is enabled. When clear, Flush-to-Zero mode is disabled and the behavior of the floating-point system is fully compliant with the IEEE 754 standard.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The FZ bit in the FPDSC register holds the default value for this bit.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>23:22</td>
<td>RMODE</td>
<td>RW</td>
<td>-</td>
<td>Rounding Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The specified rounding mode is used by almost all floating-point instructions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The RMODE bit in the FPDSC register holds the default value for this bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Round to Nearest (RN) mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 Round towards Plus Infinity (RP) mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 Round towards Minus Infinity (RM) mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 Round towards Zero (RZ) mode</td>
</tr>
<tr>
<td>21:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>IDC</td>
<td>RW</td>
<td>-</td>
<td>Input Denormal Cumulative Exception</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates this exception has occurred since 0 was last written to this bit.</td>
</tr>
<tr>
<td>6:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>IXC</td>
<td>RW</td>
<td>-</td>
<td>Inexact Cumulative Exception</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates this exception has occurred since 0 was last written to this bit.</td>
</tr>
<tr>
<td>3</td>
<td>UFC</td>
<td>RW</td>
<td>-</td>
<td>Underflow Cumulative Exception</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates this exception has occurred since 0 was last written to this bit.</td>
</tr>
<tr>
<td>2</td>
<td>OFC</td>
<td>RW</td>
<td>-</td>
<td>Overflow Cumulative Exception</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates this exception has occurred since 0 was last written to this bit.</td>
</tr>
<tr>
<td>1</td>
<td>DZC</td>
<td>RW</td>
<td>-</td>
<td>Division by Zero Cumulative Exception</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates this exception has occurred since 0 was last written to this bit.</td>
</tr>
<tr>
<td>0</td>
<td>IOC</td>
<td>RW</td>
<td>-</td>
<td>Invalid Operation Cumulative Exception</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates this exception has occurred since 0 was last written to this bit.</td>
</tr>
</tbody>
</table>
2.3.5 Exceptions and Interrupts

The Cortex-M4F processor supports interrupts and system exceptions. The processor and the Nested Vectored Interrupt Controller (NVIC) prioritize and handle all exceptions. An exception changes the normal flow of software control. The processor uses Handler mode to handle all exceptions except for reset. See “Exception Entry and Return” on page 108 for more information.

The NVIC registers control interrupt handling. See “Nested Vectored Interrupt Controller (NVIC)” on page 124 for more information.

2.3.6 Data Types

The Cortex-M4F supports 32-bit words, 16-bit halfwords, and 8-bit bytes. The processor also supports 64-bit data transfer instructions. All instruction and data memory accesses are little endian. See “Memory Regions, Types and Attributes” on page 95 for more information.

2.4 Memory Model

This section describes the processor memory map, the behavior of memory accesses, and the bit-banding features. The processor has a fixed memory map that provides up to 4 GB of addressable memory.

The memory map for the TM4C123GH6PZ controller is provided in Table 2-4 on page 92. In this manual, register addresses are given as a hexadecimal increment, relative to the module’s base address as shown in the memory map.

The regions for SRAM and peripherals include bit-band regions. Bit-banding provides atomic operations to bit data (see “Bit-Banding” on page 97).

The processor reserves regions of the Private peripheral bus (PPB) address range for core peripheral registers (see “Cortex-M4 Peripherals” on page 122).

**Note:** Within the memory map, attempts to read or write addresses in reserved spaces result in a bus fault. In addition, attempts to write addresses in the flash range also result in a bus fault.

Table 2-4. Memory Map

<table>
<thead>
<tr>
<th>Start</th>
<th>End</th>
<th>Description</th>
<th>For details, see page...</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0000.0000</td>
<td>0x0003.FFFF</td>
<td>On-chip Flash</td>
<td>550</td>
</tr>
<tr>
<td>0x0004.0000</td>
<td>0x1FFF.FFFF</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x2000.0000</td>
<td>0x2000.7FFF</td>
<td>Bit-banded on-chip SRAM</td>
<td>535</td>
</tr>
<tr>
<td>0x2000.8000</td>
<td>0x21FF.FFFF</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x2200.0000</td>
<td>0x220F.FFFF</td>
<td>Bit-band alias of bit-banded on-chip SRAM starting at 0x2000.0000</td>
<td>535</td>
</tr>
<tr>
<td>0x2210.0000</td>
<td>0x3FFF.FFFF</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>Peripherals</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x4000.0000</td>
<td>0x4000.0FFF</td>
<td>Watchdog timer 0</td>
<td>790</td>
</tr>
<tr>
<td>0x4000.1000</td>
<td>0x4000.1FFF</td>
<td>Watchdog timer 1</td>
<td>790</td>
</tr>
<tr>
<td>0x4000.2000</td>
<td>0x4000.3FFF</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0x4000.4000</td>
<td>0x4000.4FFF</td>
<td>GPIO Port A</td>
<td>669</td>
</tr>
<tr>
<td>0x4000.5000</td>
<td>0x4000.5FFF</td>
<td>GPIO Port B</td>
<td>669</td>
</tr>
</tbody>
</table>
### Table 2-4. Memory Map (continued)

<table>
<thead>
<tr>
<th>Start</th>
<th>End</th>
<th>Description</th>
<th>For details, see page ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4000.6000</td>
<td>0x4000.6FFF</td>
<td>GPIO Port C</td>
<td>669</td>
</tr>
<tr>
<td>0x4000.7000</td>
<td>0x4000.7FFF</td>
<td>GPIO Port D</td>
<td>669</td>
</tr>
<tr>
<td>0x4000.8000</td>
<td>0x4000.8FFF</td>
<td>SSI0</td>
<td>988</td>
</tr>
<tr>
<td>0x4000.9000</td>
<td>0x4000.9FFF</td>
<td>SSI1</td>
<td>988</td>
</tr>
<tr>
<td>0x4000.A000</td>
<td>0x4000.AFFF</td>
<td>SSI2</td>
<td>988</td>
</tr>
<tr>
<td>0x4000.B000</td>
<td>0x4000.BFFF</td>
<td>SSI3</td>
<td>988</td>
</tr>
<tr>
<td>0x4000.C000</td>
<td>0x4000.CFFF</td>
<td>UART0</td>
<td>923</td>
</tr>
<tr>
<td>0x4000.D000</td>
<td>0x4000.DFFF</td>
<td>UART1</td>
<td>923</td>
</tr>
<tr>
<td>0x4000.E000</td>
<td>0x4000.EFFF</td>
<td>UART2</td>
<td>923</td>
</tr>
<tr>
<td>0x4000.F000</td>
<td>0x4000.FFFF</td>
<td>UART3</td>
<td>923</td>
</tr>
<tr>
<td>0x4001.0000</td>
<td>0x4001.0FFF</td>
<td>UART4</td>
<td>923</td>
</tr>
<tr>
<td>0x4001.1000</td>
<td>0x4001.1FFF</td>
<td>UART5</td>
<td>923</td>
</tr>
<tr>
<td>0x4001.2000</td>
<td>0x4001.2FFF</td>
<td>UART6</td>
<td>923</td>
</tr>
<tr>
<td>0x4001.3000</td>
<td>0x4001.3FFF</td>
<td>UART7</td>
<td>923</td>
</tr>
<tr>
<td>0x4001.4000</td>
<td>0x4001.FFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
</tbody>
</table>

**Peripherals**

<table>
<thead>
<tr>
<th>Start</th>
<th>End</th>
<th>Description</th>
<th>For details, see page ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4002.0000</td>
<td>0x4002.0FFF</td>
<td>I²C 0</td>
<td>1038</td>
</tr>
<tr>
<td>0x4002.1000</td>
<td>0x4002.1FFF</td>
<td>I²C 1</td>
<td>1038</td>
</tr>
<tr>
<td>0x4002.2000</td>
<td>0x4002.2FFF</td>
<td>I²C 2</td>
<td>1038</td>
</tr>
<tr>
<td>0x4002.3000</td>
<td>0x4002.3FFF</td>
<td>I²C 3</td>
<td>1038</td>
</tr>
<tr>
<td>0x4002.4000</td>
<td>0x4002.4FFF</td>
<td>GPIO Port E</td>
<td>669</td>
</tr>
<tr>
<td>0x4002.5000</td>
<td>0x4002.5FFF</td>
<td>GPIO Port F</td>
<td>669</td>
</tr>
<tr>
<td>0x4002.6000</td>
<td>0x4002.6FFF</td>
<td>GPIO Port G</td>
<td>669</td>
</tr>
<tr>
<td>0x4002.7000</td>
<td>0x4002.7FFF</td>
<td>GPIO Port H</td>
<td>669</td>
</tr>
<tr>
<td>0x4002.8000</td>
<td>0x4002.8FFF</td>
<td>PWM 0</td>
<td>1262</td>
</tr>
<tr>
<td>0x4002.9000</td>
<td>0x4002.9FFF</td>
<td>PWM 1</td>
<td>1262</td>
</tr>
<tr>
<td>0x4002.A000</td>
<td>0x4002.BFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x4002.C000</td>
<td>0x4002.CFFF</td>
<td>QEI0</td>
<td>1336</td>
</tr>
<tr>
<td>0x4002.D000</td>
<td>0x4002.DFFF</td>
<td>QEI1</td>
<td>1336</td>
</tr>
<tr>
<td>0x4002.E000</td>
<td>0x4002.FFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x4003.0000</td>
<td>0x4003.0FFF</td>
<td>16/32-bit Timer 0</td>
<td>739</td>
</tr>
<tr>
<td>0x4003.1000</td>
<td>0x4003.1FFF</td>
<td>16/32-bit Timer 1</td>
<td>739</td>
</tr>
<tr>
<td>0x4003.2000</td>
<td>0x4003.2FFF</td>
<td>16/32-bit Timer 2</td>
<td>739</td>
</tr>
<tr>
<td>0x4003.3000</td>
<td>0x4003.3FFF</td>
<td>16/32-bit Timer 3</td>
<td>739</td>
</tr>
<tr>
<td>0x4003.4000</td>
<td>0x4003.4FFF</td>
<td>16/32-bit Timer 4</td>
<td>739</td>
</tr>
<tr>
<td>0x4003.5000</td>
<td>0x4003.5FFF</td>
<td>16/32-bit Timer 5</td>
<td>739</td>
</tr>
<tr>
<td>0x4003.6000</td>
<td>0x4003.6FFF</td>
<td>32/64-bit Timer 0</td>
<td>739</td>
</tr>
<tr>
<td>0x4003.7000</td>
<td>0x4003.7FFF</td>
<td>32/64-bit Timer 1</td>
<td>739</td>
</tr>
<tr>
<td>0x4003.8000</td>
<td>0x4003.8FFF</td>
<td>ADC0</td>
<td>832</td>
</tr>
<tr>
<td>0x4003.9000</td>
<td>0x4003.9FFF</td>
<td>ADC1</td>
<td>832</td>
</tr>
<tr>
<td>0x4003.A000</td>
<td>0x4003.BFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
</tbody>
</table>
Table 2-4. Memory Map (continued)

<table>
<thead>
<tr>
<th>Start</th>
<th>End</th>
<th>Description</th>
<th>For details, see page ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4003.C000</td>
<td>0x4003.CFFF</td>
<td>Analog Comparators</td>
<td>1242</td>
</tr>
<tr>
<td>0x4003.D000</td>
<td>0x4003.DFFF</td>
<td>GPIO Port J</td>
<td>669</td>
</tr>
<tr>
<td>0x4003.E000</td>
<td>0x4003.FFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x4004.0000</td>
<td>0x4004.0FFF</td>
<td>CAN0 Controller</td>
<td>1088</td>
</tr>
<tr>
<td>0x4004.1000</td>
<td>0x4004.1FFF</td>
<td>CAN1 Controller</td>
<td>1088</td>
</tr>
<tr>
<td>0x4004.2000</td>
<td>0x4004.BFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x4004.C000</td>
<td>0x4004.CFFF</td>
<td>32/64-bit Timer 2</td>
<td>739</td>
</tr>
<tr>
<td>0x4004.D000</td>
<td>0x4004.DFFF</td>
<td>32/64-bit Timer 3</td>
<td>739</td>
</tr>
<tr>
<td>0x4004.E000</td>
<td>0x4004.EFFF</td>
<td>32/64-bit Timer 4</td>
<td>739</td>
</tr>
<tr>
<td>0x4004.F000</td>
<td>0x4004.FFFF</td>
<td>32/64-bit Timer 5</td>
<td>739</td>
</tr>
<tr>
<td>0x4005.0000</td>
<td>0x4005.0FFF</td>
<td>USB</td>
<td>1135</td>
</tr>
<tr>
<td>0x4005.1000</td>
<td>0x4005.7FFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x4005.8000</td>
<td>0x4005.8FFF</td>
<td>GPIO Port A (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4005.9000</td>
<td>0x4005.9FFF</td>
<td>GPIO Port B (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4005.A000</td>
<td>0x4005.AFFF</td>
<td>GPIO Port C (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4005.B000</td>
<td>0x4005.BFFF</td>
<td>GPIO Port D (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4005.C000</td>
<td>0x4005.CFFF</td>
<td>GPIO Port E (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4005.D000</td>
<td>0x4005.DFFF</td>
<td>GPIO Port F (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4005.E000</td>
<td>0x4005.EFFF</td>
<td>GPIO Port G (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4005.F000</td>
<td>0x4005.FFFF</td>
<td>GPIO Port H (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4006.0000</td>
<td>0x4006.0FFF</td>
<td>GPIO Port J (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4006.1000</td>
<td>0x4006.1FFF</td>
<td>GPIO Port K (AHB aperture)</td>
<td>669</td>
</tr>
<tr>
<td>0x4006.2000</td>
<td>0x400A.EFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x400A.F000</td>
<td>0x400A.FFFF</td>
<td>EEPROM and Key Locker</td>
<td>550</td>
</tr>
<tr>
<td>0x400B.0000</td>
<td>0x400B.FFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x400C.0000</td>
<td>0x400C.0FFF</td>
<td>I²C 4</td>
<td>1038</td>
</tr>
<tr>
<td>0x400C.1000</td>
<td>0x400C.1FFF</td>
<td>I²C 5</td>
<td>1038</td>
</tr>
<tr>
<td>0x400C.2000</td>
<td>0x400F.8FFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x400F.9000</td>
<td>0x400F.9FFF</td>
<td>System Exception Module</td>
<td>495</td>
</tr>
<tr>
<td>0x400F.A000</td>
<td>0x400F.BFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x400F.C000</td>
<td>0x400F.CFFF</td>
<td>Hibernation Module</td>
<td>515</td>
</tr>
<tr>
<td>0x400F.D000</td>
<td>0x400F.DFFF</td>
<td>Flash memory control</td>
<td>550</td>
</tr>
<tr>
<td>0x400F.E000</td>
<td>0x400F.EFFF</td>
<td>System control</td>
<td>231</td>
</tr>
<tr>
<td>0x400F.F000</td>
<td>0x400F.FFFF</td>
<td>µDMA</td>
<td>616</td>
</tr>
<tr>
<td>0x4010.0000</td>
<td>0x41FF.FFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x4200.0000</td>
<td>0x43FF.FFFF</td>
<td>Bit-banded alias of 0x4000.0000 through 0x400F.FFFF</td>
<td>-</td>
</tr>
<tr>
<td>0x4400.0000</td>
<td>0xFFFF.FFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
</tbody>
</table>

**Private Peripheral Bus**

<table>
<thead>
<tr>
<th>Start</th>
<th>End</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000.0000</td>
<td>0xE000.0FFF</td>
<td>Instrumentation Trace Macrocell (ITM)</td>
</tr>
<tr>
<td>0xE000.1000</td>
<td>0xE000.1FFF</td>
<td>Data Watchpoint and Trace (DWT)</td>
</tr>
<tr>
<td>0xE000.2000</td>
<td>0xE000.2FFF</td>
<td>Flash Patch and Breakpoint (FPB)</td>
</tr>
</tbody>
</table>
Table 2-4. Memory Map (continued)

<table>
<thead>
<tr>
<th>Start</th>
<th>End</th>
<th>Description</th>
<th>For details, see page ...</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000.3000</td>
<td>0xE000.DFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0xE000.E000</td>
<td>0xE000.EFFF</td>
<td>Cortex-M4F Peripherals (SysTick, NVIC, MPU, FPU and SCB)</td>
<td>134</td>
</tr>
<tr>
<td>0xE000.F000</td>
<td>0xE003.FFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
<tr>
<td>0xE004.0000</td>
<td>0xE004.0FFF</td>
<td>Trace Port Interface Unit (TPIU)</td>
<td>72</td>
</tr>
<tr>
<td>0xE004.1000</td>
<td>0xE004.1FFF</td>
<td>Embedded Trace Macrocell (ETM)</td>
<td>71</td>
</tr>
<tr>
<td>0xE004.2000</td>
<td>0xFFFF.FFFF</td>
<td>Reserved</td>
<td>-</td>
</tr>
</tbody>
</table>

2.4.1 Memory Regions, Types and Attributes

The memory map and the programming of the MPU split the memory map into regions. Each region has a defined memory type, and some regions have additional memory attributes. The memory type and attributes determine the behavior of accesses to the region.

The memory types are:

- Normal: The processor can re-order transactions for efficiency and perform speculative reads.
- Device: The processor preserves transaction order relative to other transactions to Device or Strongly Ordered memory.
- Strongly Ordered: The processor preserves transaction order relative to all other transactions.

The different ordering requirements for Device and Strongly Ordered memory mean that the memory system can buffer a write to Device memory but must not buffer a write to Strongly Ordered memory.

An additional memory attribute is Execute Never (XN), which means the processor prevents instruction accesses. A fault exception is generated only on execution of an instruction executed from an XN region.

2.4.2 Memory System Ordering of Memory Accesses

For most memory accesses caused by explicit memory access instructions, the memory system does not guarantee that the order in which the accesses complete matches the program order of the instructions, providing the order does not affect the behavior of the instruction sequence. Normally, if correct program execution depends on two memory accesses completing in program order, software must insert a memory barrier instruction between the memory access instructions (see "Software Ordering of Memory Accesses" on page 96).

However, the memory system does guarantee ordering of accesses to Device and Strongly Ordered memory. For two memory access instructions A1 and A2, if both A1 and A2 are accesses to either Device or Strongly Ordered memory, and if A1 occurs before A2 in program order, A1 is always observed before A2.

2.4.3 Behavior of Memory Accesses

Table 2-5 on page 96 shows the behavior of accesses to each region in the memory map. See “Memory Regions, Types and Attributes” on page 95 for more information on memory types and the XN attribute. Tiva™ C Series devices may have reserved memory areas within the address ranges shown below (refer to Table 2-4 on page 92 for more information).
Table 2-5. Memory Access Behavior

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Memory Region</th>
<th>Memory Type</th>
<th>ExecuteNever (XN)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000.0000 - 0x1FFF.FFFF</td>
<td>Code</td>
<td>Normal</td>
<td>-</td>
<td>This executable region is for program code. Data can also be stored here.</td>
</tr>
<tr>
<td>0x2000.0000 - 0x3FFF.FFFF</td>
<td>SRAM</td>
<td>Normal</td>
<td>-</td>
<td>This executable region is for data. Code can also be stored here. This region includes bit band and bit band alias areas (see Table 2-6 on page 98).</td>
</tr>
<tr>
<td>0x4000.0000 - 0x5FFF.FFFF</td>
<td>Peripheral</td>
<td>Device</td>
<td>XN</td>
<td>This region includes bit band and bit band alias areas (see Table 2-7 on page 98).</td>
</tr>
<tr>
<td>0x6000.0000 - 0x9FFF.FFFF</td>
<td>External RAM</td>
<td>Normal</td>
<td>-</td>
<td>This executable region is for data.</td>
</tr>
<tr>
<td>0xA000.0000 - 0xDFFF.FFFF</td>
<td>External device</td>
<td>Device</td>
<td>XN</td>
<td>This region is for external device memory.</td>
</tr>
<tr>
<td>0xE000.0000- 0xE00F.FFFF</td>
<td>Private peripheral bus</td>
<td>Strongly Ordered</td>
<td>XN</td>
<td>This region includes the NVIC, system timer, and system control block.</td>
</tr>
<tr>
<td>0xE010.0000- 0xFFFF.FFFF</td>
<td>Reserved</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

The Code, SRAM, and external RAM regions can hold programs. However, it is recommended that programs always use the Code region because the Cortex-M4F has separate buses that can perform instruction fetches and data accesses simultaneously.

The MPU can override the default memory access behavior described in this section. For more information, see “Memory Protection Unit (MPU)” on page 125.

The Cortex-M4F prefetches instructions ahead of execution and speculatively prefetches from branch target addresses.

2.4.4 Software Ordering of Memory Accesses

The order of instructions in the program flow does not always guarantee the order of the corresponding memory transactions for the following reasons:

- The processor can reorder some memory accesses to improve efficiency, providing this does not affect the behavior of the instruction sequence.
- The processor has multiple bus interfaces.
- Memory or devices in the memory map have different wait states.
- Some memory accesses are buffered or speculative.

“Memory System Ordering of Memory Accesses” on page 95 describes the cases where the memory system guarantees the order of memory accesses. Otherwise, if the order of memory accesses is critical, software must include memory barrier instructions to force that ordering. The Cortex-M4F has the following memory barrier instructions:

- The Data Memory Barrier (DMB) instruction ensures that outstanding memory transactions complete before subsequent memory transactions.
- The Data Synchronization Barrier (DSB) instruction ensures that outstanding memory transactions complete before subsequent instructions execute.
- The Instruction Synchronization Barrier (ISB) instruction ensures that the effect of all completed memory transactions is recognizable by subsequent instructions.
Memory barrier instructions can be used in the following situations:

- **MPU programming**
  - If the MPU settings are changed and the change must be effective on the very next instruction, use a **DSB** instruction to ensure the effect of the MPU takes place immediately at the end of context switching.
  - Use an **ISB** instruction to ensure the new MPU setting takes effect immediately after programming the MPU region or regions, if the MPU configuration code was accessed using a branch or call. If the MPU configuration code is entered using exception mechanisms, then an **ISB** instruction is not required.

- **Vector table**
  If the program changes an entry in the vector table and then enables the corresponding exception, use a **DMB** instruction between the operations. The **DMB** instruction ensures that if the exception is taken immediately after being enabled, the processor uses the new exception vector.

- **Self-modifying code**
  If a program contains self-modifying code, use an **ISB** instruction immediately after the code modification in the program. The **ISB** instruction ensures subsequent instruction execution uses the updated program.

- **Memory map switching**
  If the system contains a memory map switching mechanism, use a **DSB** instruction after switching the memory map in the program. The **DSB** instruction ensures subsequent instruction execution uses the updated memory map.

- **Dynamic exception priority change**
  When an exception priority has to change when the exception is pending or active, use **DSB** instructions after the change. The change then takes effect on completion of the **DSB** instruction.

Memory accesses to Strongly Ordered memory, such as the System Control Block, do not require the use of **DMB** instructions.

For more information on the memory barrier instructions, see the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A).

### 2.4.5 Bit-Banding

A bit-band region maps each word in a bit-band alias region to a single bit in the bit-band region. The bit-band regions occupy the lowest 1 MB of the SRAM and peripheral memory regions. Accesses to the 32-MB SRAM alias region map to the 1-MB SRAM bit-band region, as shown in Table 2-6 on page 98. Accesses to the 32-MB peripheral alias region map to the 1-MB peripheral bit-band region, as shown in Table 2-7 on page 98. For the specific address range of the bit-band regions, see Table 2-4 on page 92.

**Note:** A word access to the SRAM or the peripheral bit-band alias region maps to a single bit in the SRAM or peripheral bit-band region.

A word access to a bit band address results in a word access to the underlying memory, and similarly for halfword and byte accesses. This allows bit band accesses to match the access requirements of the underlying peripheral.
Table 2-6. SRAM Memory Bit-Banding Regions

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Memory Region</th>
<th>Instruction and Data Accesses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start</td>
<td>End</td>
<td></td>
</tr>
<tr>
<td>0x2000.0000</td>
<td>0x2000.7FFF</td>
<td>SRAM bit-band region</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Direct accesses to this memory range behave as SRAM memory accesses, but this region is also bit addressable through bit-band alias.</td>
</tr>
<tr>
<td>0x2200.0000</td>
<td>0x220F.FFFF</td>
<td>SRAM bit-band alias</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data accesses to this region are remapped to bit band region. A write operation is performed as read-modify-write. Instruction accesses are not remapped.</td>
</tr>
</tbody>
</table>

Table 2-7. Peripheral Memory Bit-Banding Regions

<table>
<thead>
<tr>
<th>Address Range</th>
<th>Memory Region</th>
<th>Instruction and Data Accesses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start</td>
<td>End</td>
<td></td>
</tr>
<tr>
<td>0x4000.0000</td>
<td>0x400F.FFFF</td>
<td>Peripheral bit-band region</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Direct accesses to this memory range behave as peripheral memory accesses, but this region is also bit addressable through bit-band alias.</td>
</tr>
<tr>
<td>0x4200.0000</td>
<td>0x43FF.FFFF</td>
<td>Peripheral bit-band alias</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data accesses to this region are remapped to bit band region. A write operation is performed as read-modify-write. Instruction accesses are not permitted.</td>
</tr>
</tbody>
</table>

The following formula shows how the alias region maps onto the bit-band region:

\[
\text{bit\_word\_offset} = (\text{byte\_offset} \times 32) + (\text{bit\_number} \times 4)
\]

\[
\text{bit\_word\_addr} = \text{bit\_band\_base} + \text{bit\_word\_offset}
\]

where:

- \( \text{bit\_word\_offset} \) The position of the target bit in the bit-band memory region.
- \( \text{bit\_word\_addr} \) The address of the word in the alias memory region that maps to the targeted bit.
- \( \text{bit\_band\_base} \) The starting address of the alias region.
- \( \text{byte\_offset} \) The number of the byte in the bit-band region that contains the targeted bit.
- \( \text{bit\_number} \) The bit position, 0-7, of the targeted bit.

Figure 2-4 on page 99 shows examples of bit-band mapping between the SRAM bit-band alias region and the SRAM bit-band region:

- The alias word at 0x23FF.FFE0 maps to bit 0 of the bit-band byte at 0x200F.FFFF:
  \[
  0x23FF.FFE0 = 0x2200.0000 + (0x000F.FFFF \times 32) + (0 \times 4)
  \]

- The alias word at 0x23FF.FFFC maps to bit 7 of the bit-band byte at 0x200F.FFFF:
  \[
  0x23FF.FFFC = 0x2200.0000 + (0x000F.FFFF \times 32) + (7 \times 4)
  \]
The alias word at 0x2200.0000 maps to bit 0 of the bit-band byte at 0x2000.0000:

\[
0x2200.0000 = 0x2200.0000 + (0*32) + (0*4)
\]

The alias word at 0x2200.001C maps to bit 7 of the bit-band byte at 0x2000.0000:

\[
0x2200.001C = 0x2200.0000 + (0*32) + (7*4)
\]

Figure 2-4. Bit-Band Mapping

2.4.5.1 Directly Accessing an Alias Region

Writing to a word in the alias region updates a single bit in the bit-band region.

Bit 0 of the value written to a word in the alias region determines the value written to the targeted bit in the bit-band region. Writing a value with bit 0 set writes a 1 to the bit-band bit, and writing a value with bit 0 clear writes a 0 to the bit-band bit.

Bits 31:1 of the alias word have no effect on the bit-band bit. Writing 0x01 has the same effect as writing 0xFF. Writing 0x00 has the same effect as writing 0x0E.

When reading a word in the alias region, 0x0000.0000 indicates that the targeted bit in the bit-band region is clear and 0x0000.0001 indicates that the targeted bit in the bit-band region is set.

2.4.5.2 Directly Accessing a Bit-Band Region

“Behavior of Memory Accesses” on page 95 describes the behavior of direct byte, halfword, or word accesses to the bit-band regions.

2.4.6 Data Storage

The processor views memory as a linear collection of bytes numbered in ascending order from zero. For example, bytes 0-3 hold the first stored word, and bytes 4-7 hold the second stored word. Data is stored in little-endian format, with the least-significant byte (lsbyte) of a word stored at the
lowest-numbered byte, and the most-significant byte (msbyte) stored at the highest-numbered byte. Figure 2-5 on page 100 illustrates how data is stored.

**Figure 2-5. Data Storage**

<table>
<thead>
<tr>
<th>Memory</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address A</td>
<td>B0</td>
</tr>
<tr>
<td>A+1</td>
<td>B1</td>
</tr>
<tr>
<td>A+2</td>
<td>B2</td>
</tr>
<tr>
<td>A+3</td>
<td>B3</td>
</tr>
<tr>
<td>lsbyte</td>
<td>0</td>
</tr>
<tr>
<td>msbyte</td>
<td>31</td>
</tr>
</tbody>
</table>

### 2.4.7 Synchronization Primitives

The Cortex-M4F instruction set includes pairs of synchronization primitives which provide a non-blocking mechanism that a thread or process can use to obtain exclusive access to a memory location. Software can use these primitives to perform a guaranteed read-modify-write memory update sequence or for a semaphore mechanism.

A pair of synchronization primitives consists of:

- A Load-Exclusive instruction, which is used to read the value of a memory location and requests exclusive access to that location.
- A Store-Exclusive instruction, which is used to attempt to write to the same memory location and returns a status bit to a register. If this status bit is clear, it indicates that the thread or process gained exclusive access to the memory and the write succeeds; if this status bit is set, it indicates that the thread or process did not gain exclusive access to the memory and no write was performed.

The pairs of Load-Exclusive and Store-Exclusive instructions are:

- The word instructions **LDREX** and **STREX**
- The halfword instructions **LDREXH** and **STREXH**
- The byte instructions **LDREXB** and **STREXB**

Software must use a Load-Exclusive instruction with the corresponding Store-Exclusive instruction. To perform an exclusive read-modify-write of a memory location, software must:

1. Use a Load-Exclusive instruction to read the value of the location.
2. Modify the value, as required.
3. Use a Store-Exclusive instruction to attempt to write the new value back to the memory location.
4. Test the returned status bit.
If the status bit is clear, the read-modify-write completed successfully. If the status bit is set, no write was performed, which indicates that the value returned at step 1 might be out of date. The software must retry the entire read-modify-write sequence.

Software can use the synchronization primitives to implement a semaphore as follows:

1. Use a Load-Exclusive instruction to read from the semaphore address to check whether the semaphore is free.
2. If the semaphore is free, use a Store-Exclusive to write the claim value to the semaphore address.
3. If the returned status bit from step 2 indicates that the Store-Exclusive succeeded, then the software has claimed the semaphore. However, if the Store-Exclusive failed, another process might have claimed the semaphore after the software performed step 1.

The Cortex-M4F includes an exclusive access monitor that tags the fact that the processor has executed a Load-Exclusive instruction. The processor removes its exclusive access tag if:

- It executes a CLREX instruction.
- It executes a Store-Exclusive instruction, regardless of whether the write succeeds.
- An exception occurs, which means the processor can resolve semaphore conflicts between different threads.

For more information about the synchronization primitive instructions, see the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A).

### 2.5 Exception Model

The ARM Cortex-M4F processor and the Nested Vectored Interrupt Controller (NVIC) prioritize and handle all exceptions in Handler Mode. The processor state is automatically stored to the stack on an exception and automatically restored from the stack at the end of the Interrupt Service Routine (ISR). The vector is fetched in parallel to the state saving, enabling efficient interrupt entry. The processor supports tail-chaining, which enables back-to-back interrupts to be performed without the overhead of state saving and restoration.

Table 2-8 on page 103 lists all exception types. Software can set eight priority levels on seven of these exceptions (system handlers) as well as on 85 interrupts (listed in Table 2-9 on page 104). Priorities on the system handlers are set with the NVIC System Handler Priority n (SYSPRIn) registers. Interrupts are enabled through the NVIC Interrupt Set Enable n (ENn) register and prioritized with the NVIC Interrupt Priority n (PRIn) registers. Priorities can be grouped by splitting priority levels into preemption priorities and subpriorities. All the interrupt registers are described in “Nested Vectored Interrupt Controller (NVIC)” on page 124.

Internally, the highest user-programmable priority (0) is treated as fourth priority, after a Reset, Non-Maskable Interrupt (NMI), and a Hard Fault, in that order. Note that 0 is the default priority for all the programmable priorities.

**Important:** After a write to clear an interrupt source, it may take several processor cycles for the NVIC to see the interrupt source deassert. Thus if the interrupt clear is done as the last action in an interrupt handler, it is possible for the interrupt handler to complete while
the NVIC sees the interrupt as still asserted, causing the interrupt handler to be re-entered errantly. This situation can be avoided by either clearing the interrupt source at the beginning of the interrupt handler or by performing a read or write after the write to clear the interrupt source (and flush the write buffer).

See “Nested Vectored Interrupt Controller (NVIC)” on page 124 for more information on exceptions and interrupts.

2.5.1 Exception States

Each exception is in one of the following states:

- **Inactive.** The exception is not active and not pending.

- **Pending.** The exception is waiting to be serviced by the processor. An interrupt request from a peripheral or from software can change the state of the corresponding interrupt to pending.

- **Active.** An exception that is being serviced by the processor but has not completed.

  **Note:** An exception handler can interrupt the execution of another exception handler. In this case, both exceptions are in the active state.

- **Active and Pending.** The exception is being serviced by the processor, and there is a pending exception from the same source.

2.5.2 Exception Types

The exception types are:

- **Reset.** Reset is invoked on power up or a warm reset. The exception model treats reset as a special form of exception. When reset is asserted, the operation of the processor stops, potentially at any point in an instruction. When reset is deasserted, execution restarts from the address provided by the reset entry in the vector table. Execution restarts as privileged execution in Thread mode.

- **NMI.** A non-maskable Interrupt (NMI) can be signaled using the NMI signal or triggered by software using the **Interrupt Control and State (INTCTRL)** register. This exception has the highest priority other than reset. NMI is permanently enabled and has a fixed priority of -2. NMIs cannot be masked or prevented from activation by any other exception or preempted by any exception other than reset.

- **Hard Fault.** A hard fault is an exception that occurs because of an error during exception processing, or because an exception cannot be managed by any other exception mechanism. Hard faults have a fixed priority of -1, meaning they have higher priority than any exception with configurable priority.

- **Memory Management Fault.** A memory management fault is an exception that occurs because of a memory protection related fault, including access violation and no match. The MPU or the fixed memory protection constraints determine this fault, for both instruction and data memory transactions. This fault is used to abort instruction accesses to Execute Never (XN) memory regions, even if the MPU is disabled.

- **Bus Fault.** A bus fault is an exception that occurs because of a memory-related fault for an instruction or data memory transaction such as a prefetch fault or a memory access fault. This fault can be enabled or disabled.
- **Usage Fault.** A usage fault is an exception that occurs because of a fault related to instruction execution, such as:
  - An undefined instruction
  - An illegal unaligned access
  - Invalid state on instruction execution
  - An error on exception return
  An unaligned address on a word or halfword memory access or division by zero can cause a usage fault when the core is properly configured.

- **SVCall.** A supervisor call (SVC) is an exception that is triggered by the SVC instruction. In an OS environment, applications can use SVC instructions to access OS kernel functions and device drivers.

- **Debug Monitor.** This exception is caused by the debug monitor (when not halting). This exception is only active when enabled. This exception does not activate if it is a lower priority than the current activation.

- **PendSV.** PendSV is a pendable, interrupt-driven request for system-level service. In an OS environment, use PendSV for context switching when no other exception is active. PendSV is triggered using the **Interrupt Control and State (INTCTRL)** register.

- **SysTick.** A SysTick exception is an exception that the system timer generates when it reaches zero when it is enabled to generate an interrupt. Software can also generate a SysTick exception using the **Interrupt Control and State (INTCTRL)** register. In an OS environment, the processor can use this exception as system tick.

- **Interrupt (IRQ).** An interrupt, or IRQ, is an exception signaled by a peripheral or generated by a software request and fed through the NVIC (prioritized). All interrupts are asynchronous to instruction execution. In the system, peripherals use interrupts to communicate with the processor. Table 2-9 on page 104 lists the interrupts on the TM4C123GH6PZ controller.

For an asynchronous exception, other than reset, the processor can execute another instruction between when the exception is triggered and when the processor enters the exception handler.

Privileged software can disable the exceptions that Table 2-8 on page 103 shows as having configurable priority (see the **SYSHNDCTRL** register on page 173 and the **DIS0** register on page 144).

For more information about hard faults, memory management faults, bus faults, and usage faults, see “Fault Handling” on page 111.

### Table 2-8. Exception Types

<table>
<thead>
<tr>
<th>Exception Type</th>
<th>Vector Number</th>
<th>Priority</th>
<th>Vector Address or Offset</th>
<th>Activation</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>0</td>
<td>-</td>
<td>0x0000.0000</td>
<td>Stack top is loaded from the first entry of the vector table on reset.</td>
</tr>
<tr>
<td>Reset</td>
<td>1</td>
<td>-3 (highest)</td>
<td>0x0000.0004</td>
<td>Asynchronous</td>
</tr>
<tr>
<td>Non-Maskable Interrupt (NMI)</td>
<td>2</td>
<td>-2</td>
<td>0x0000.0008</td>
<td>Asynchronous</td>
</tr>
<tr>
<td>Hard Fault</td>
<td>3</td>
<td>-1</td>
<td>0x0000.000C</td>
<td>-</td>
</tr>
<tr>
<td>Memory Management</td>
<td>4</td>
<td>programmable</td>
<td>0x0000.0010</td>
<td>Synchronous</td>
</tr>
</tbody>
</table>
Table 2-8. Exception Types (continued)

<table>
<thead>
<tr>
<th>Exception Type</th>
<th>Vector Number</th>
<th>Priority(^\text{a})</th>
<th>Vector Address or Offset(^\text{b})</th>
<th>Activation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Fault</td>
<td>5</td>
<td>programmable(^\text{c})</td>
<td>0x0000.0014</td>
<td>Synchronous when precise and asynchronous when imprecise</td>
</tr>
<tr>
<td>Usage Fault</td>
<td>6</td>
<td>programmable(^\text{c})</td>
<td>0x0000.0018</td>
<td>Synchronous</td>
</tr>
<tr>
<td>-</td>
<td>7-10</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>SVCall</td>
<td>11</td>
<td>programmable(^\text{c})</td>
<td>0x0000.002C</td>
<td>Synchronous</td>
</tr>
<tr>
<td>Debug Monitor</td>
<td>12</td>
<td>programmable(^\text{c})</td>
<td>0x0000.0030</td>
<td>Synchronous</td>
</tr>
<tr>
<td>-</td>
<td>13</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>PendSV</td>
<td>14</td>
<td>programmable(^\text{c})</td>
<td>0x0000.0038</td>
<td>Asynchronous</td>
</tr>
<tr>
<td>SysTick</td>
<td>15</td>
<td>programmable(^\text{c})</td>
<td>0x0000.003C</td>
<td>Asynchronous</td>
</tr>
<tr>
<td>Interrupts</td>
<td>16 and above</td>
<td>programmable(^\text{d})</td>
<td>0x0000.0040 and above</td>
<td>Asynchronous</td>
</tr>
</tbody>
</table>

\( ^\text{a} \) 0 is the default priority for all the programmable priorities.
\( ^\text{b} \) See “Vector Table” on page 107.
\( ^\text{c} \) See SYSPRI1 on page 170.
\( ^\text{d} \) See PRIn registers on page 152.

Table 2-9. Interrupts

<table>
<thead>
<tr>
<th>Vector Number</th>
<th>Interrupt Number (Bit in Interrupt Registers)</th>
<th>Vector Address or Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-15</td>
<td>-</td>
<td>0x0000.0000 - 0x0000.003C</td>
<td>Processor exceptions</td>
</tr>
<tr>
<td>16</td>
<td>0</td>
<td>0x0000.0040</td>
<td>GPIO Port A</td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>0x0000.0044</td>
<td>GPIO Port B</td>
</tr>
<tr>
<td>18</td>
<td>2</td>
<td>0x0000.0048</td>
<td>GPIO Port C</td>
</tr>
<tr>
<td>19</td>
<td>3</td>
<td>0x0000.004C</td>
<td>GPIO Port D</td>
</tr>
<tr>
<td>20</td>
<td>4</td>
<td>0x0000.0050</td>
<td>GPIO Port E</td>
</tr>
<tr>
<td>21</td>
<td>5</td>
<td>0x0000.0054</td>
<td>UART0</td>
</tr>
<tr>
<td>22</td>
<td>6</td>
<td>0x0000.0058</td>
<td>UART1</td>
</tr>
<tr>
<td>23</td>
<td>7</td>
<td>0x0000.005C</td>
<td>SSI0</td>
</tr>
<tr>
<td>24</td>
<td>8</td>
<td>0x0000.0060</td>
<td>IPC0</td>
</tr>
<tr>
<td>25</td>
<td>9</td>
<td>0x0000.0064</td>
<td>PWM0 Fault</td>
</tr>
<tr>
<td>26</td>
<td>10</td>
<td>0x0000.0068</td>
<td>PWM0 Generator 0</td>
</tr>
<tr>
<td>27</td>
<td>11</td>
<td>0x0000.006C</td>
<td>PWM0 Generator 1</td>
</tr>
<tr>
<td>28</td>
<td>12</td>
<td>0x0000.0070</td>
<td>PWM0 Generator 2</td>
</tr>
<tr>
<td>29</td>
<td>13</td>
<td>0x0000.0074</td>
<td>QEI0</td>
</tr>
<tr>
<td>30</td>
<td>14</td>
<td>0x0000.0078</td>
<td>ADC0 Sequence 0</td>
</tr>
<tr>
<td>31</td>
<td>15</td>
<td>0x0000.007C</td>
<td>ADC0 Sequence 1</td>
</tr>
<tr>
<td>32</td>
<td>16</td>
<td>0x0000.0080</td>
<td>ADC0 Sequence 2</td>
</tr>
<tr>
<td>33</td>
<td>17</td>
<td>0x0000.0084</td>
<td>ADC0 Sequence 3</td>
</tr>
<tr>
<td>34</td>
<td>18</td>
<td>0x0000.0088</td>
<td>Watchdog Timers 0 and 1</td>
</tr>
<tr>
<td>35</td>
<td>19</td>
<td>0x0000.008C</td>
<td>16/32-Bit Timer 0A</td>
</tr>
<tr>
<td>36</td>
<td>20</td>
<td>0x0000.0090</td>
<td>16/32-Bit Timer 0B</td>
</tr>
<tr>
<td>37</td>
<td>21</td>
<td>0x0000.0094</td>
<td>16/32-Bit Timer 1A</td>
</tr>
</tbody>
</table>
Table 2-9. Interrupts (continued)

<table>
<thead>
<tr>
<th>Vector Number</th>
<th>Interrupt Number (Bit in Interrupt Registers)</th>
<th>Vector Address or Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>38</td>
<td>22</td>
<td>0x0000.0098</td>
<td>16/32-Bit Timer 1B</td>
</tr>
<tr>
<td>39</td>
<td>23</td>
<td>0x0000.009C</td>
<td>16/32-Bit Timer 2A</td>
</tr>
<tr>
<td>40</td>
<td>24</td>
<td>0x0000.00A0</td>
<td>16/32-Bit Timer 2B</td>
</tr>
<tr>
<td>41</td>
<td>25</td>
<td>0x0000.00A4</td>
<td>Analog Comparator 0</td>
</tr>
<tr>
<td>42</td>
<td>26</td>
<td>0x0000.00A8</td>
<td>Analog Comparator 1</td>
</tr>
<tr>
<td>43</td>
<td>27</td>
<td>0x0000.00AC</td>
<td>Analog Comparator 2</td>
</tr>
<tr>
<td>44</td>
<td>28</td>
<td>0x0000.00B0</td>
<td>System Control</td>
</tr>
<tr>
<td>45</td>
<td>29</td>
<td>0x0000.00B4</td>
<td>Flash Memory Control and EEPROM Control</td>
</tr>
<tr>
<td>46</td>
<td>30</td>
<td>0x0000.00B8</td>
<td>GPIO Port F</td>
</tr>
<tr>
<td>47</td>
<td>31</td>
<td>0x0000.00BC</td>
<td>GPIO Port G</td>
</tr>
<tr>
<td>48</td>
<td>32</td>
<td>0x0000.00C0</td>
<td>GPIO Port H</td>
</tr>
<tr>
<td>49</td>
<td>33</td>
<td>0x0000.00C4</td>
<td>UART2</td>
</tr>
<tr>
<td>50</td>
<td>34</td>
<td>0x0000.00C8</td>
<td>SSI1</td>
</tr>
<tr>
<td>51</td>
<td>35</td>
<td>0x0000.00CC</td>
<td>16/32-Bit Timer 3A</td>
</tr>
<tr>
<td>52</td>
<td>36</td>
<td>0x0000.00D0</td>
<td>16/32-Bit Timer 3B</td>
</tr>
<tr>
<td>53</td>
<td>37</td>
<td>0x0000.00D4</td>
<td>I2C1</td>
</tr>
<tr>
<td>54</td>
<td>38</td>
<td>0x0000.00D8</td>
<td>QEI1</td>
</tr>
<tr>
<td>55</td>
<td>39</td>
<td>0x0000.00DC</td>
<td>CAN0</td>
</tr>
<tr>
<td>56</td>
<td>40</td>
<td>0x0000.00E0</td>
<td>CAN1</td>
</tr>
<tr>
<td>57-58</td>
<td>41-42</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>59</td>
<td>43</td>
<td>0x0000.00EC</td>
<td>Hibernation Module</td>
</tr>
<tr>
<td>60</td>
<td>44</td>
<td>0x0000.00F0</td>
<td>USB</td>
</tr>
<tr>
<td>61</td>
<td>45</td>
<td>0x0000.00F4</td>
<td>PWM Generator 3</td>
</tr>
<tr>
<td>62</td>
<td>46</td>
<td>0x0000.00F8</td>
<td>µDMA Software</td>
</tr>
<tr>
<td>63</td>
<td>47</td>
<td>0x0000.00FC</td>
<td>µDMA Error</td>
</tr>
<tr>
<td>64</td>
<td>48</td>
<td>0x0000.0100</td>
<td>ADC1 Sequence 0</td>
</tr>
<tr>
<td>65</td>
<td>49</td>
<td>0x0000.0104</td>
<td>ADC1 Sequence 1</td>
</tr>
<tr>
<td>66</td>
<td>50</td>
<td>0x0000.0108</td>
<td>ADC1 Sequence 2</td>
</tr>
<tr>
<td>67</td>
<td>51</td>
<td>0x0000.010C</td>
<td>ADC1 Sequence 3</td>
</tr>
<tr>
<td>68-69</td>
<td>52-53</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>70</td>
<td>54</td>
<td>0x0000.0118</td>
<td>GPIO Port J</td>
</tr>
<tr>
<td>71</td>
<td>55</td>
<td>0x0000.011C</td>
<td>GPIO Port K</td>
</tr>
<tr>
<td>72</td>
<td>56</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>73</td>
<td>57</td>
<td>0x0000.0124</td>
<td>SSI2</td>
</tr>
<tr>
<td>74</td>
<td>58</td>
<td>0x0000.0128</td>
<td>SSI3</td>
</tr>
<tr>
<td>75</td>
<td>59</td>
<td>0x0000.012C</td>
<td>UART3</td>
</tr>
<tr>
<td>76</td>
<td>60</td>
<td>0x0000.0130</td>
<td>UART4</td>
</tr>
<tr>
<td>77</td>
<td>61</td>
<td>0x0000.0134</td>
<td>UART5</td>
</tr>
<tr>
<td>78</td>
<td>62</td>
<td>0x0000.0138</td>
<td>UART6</td>
</tr>
<tr>
<td>79</td>
<td>63</td>
<td>0x0000.013C</td>
<td>UART7</td>
</tr>
</tbody>
</table>
### Table 2-9. Interrupts (continued)

<table>
<thead>
<tr>
<th>Vector Number</th>
<th>Interrupt Number (Bit in Interrupt Registers)</th>
<th>Vector Address or Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>80-83</td>
<td>64-67</td>
<td>0x0000.0140 -0x0000.014C</td>
<td>Reserved</td>
</tr>
<tr>
<td>84</td>
<td>68</td>
<td>0x0000.0150</td>
<td>I^2C2</td>
</tr>
<tr>
<td>85</td>
<td>69</td>
<td>0x0000.0154</td>
<td>I^2C3</td>
</tr>
<tr>
<td>86</td>
<td>70</td>
<td>0x0000.0158</td>
<td>16/32-Bit Timer 4A</td>
</tr>
<tr>
<td>87</td>
<td>71</td>
<td>0x0000.015C</td>
<td>16/32-Bit Timer 4B</td>
</tr>
<tr>
<td>88-107</td>
<td>72-91</td>
<td>0x0000.0160 -0x0000.01AC</td>
<td>Reserved</td>
</tr>
<tr>
<td>108</td>
<td>92</td>
<td>0x0000.01B0</td>
<td>16/32-Bit Timer 5A</td>
</tr>
<tr>
<td>109</td>
<td>93</td>
<td>0x0000.01B4</td>
<td>16/32-Bit Timer 5B</td>
</tr>
<tr>
<td>110</td>
<td>94</td>
<td>0x0000.01B8</td>
<td>32/64-Bit Timer 0A</td>
</tr>
<tr>
<td>111</td>
<td>95</td>
<td>0x0000.01BC</td>
<td>32/64-Bit Timer 0B</td>
</tr>
<tr>
<td>112</td>
<td>96</td>
<td>0x0000.01C0</td>
<td>32/64-Bit Timer 1A</td>
</tr>
<tr>
<td>113</td>
<td>97</td>
<td>0x0000.01C4</td>
<td>32/64-Bit Timer 1B</td>
</tr>
<tr>
<td>114</td>
<td>98</td>
<td>0x0000.01C8</td>
<td>32/64-Bit Timer 2A</td>
</tr>
<tr>
<td>115</td>
<td>99</td>
<td>0x0000.01CC</td>
<td>32/64-Bit Timer 2B</td>
</tr>
<tr>
<td>116</td>
<td>100</td>
<td>0x0000.01D0</td>
<td>32/64-Bit Timer 3A</td>
</tr>
<tr>
<td>117</td>
<td>101</td>
<td>0x0000.01D4</td>
<td>32/64-Bit Timer 3B</td>
</tr>
<tr>
<td>118</td>
<td>102</td>
<td>0x0000.01D8</td>
<td>32/64-Bit Timer 4A</td>
</tr>
<tr>
<td>119</td>
<td>103</td>
<td>0x0000.01DC</td>
<td>32/64-Bit Timer 4B</td>
</tr>
<tr>
<td>120</td>
<td>104</td>
<td>0x0000.01E0</td>
<td>32/64-Bit Timer 5A</td>
</tr>
<tr>
<td>121</td>
<td>105</td>
<td>0x0000.01E4</td>
<td>32/64-Bit Timer 5B</td>
</tr>
<tr>
<td>122</td>
<td>106</td>
<td>0x0000.01E8</td>
<td>System Exception (imprecise)</td>
</tr>
<tr>
<td>123-124</td>
<td>107-108</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>125</td>
<td>109</td>
<td>0x0000.01F4</td>
<td>I^2C4</td>
</tr>
<tr>
<td>126</td>
<td>110</td>
<td>0x0000.01F8</td>
<td>I^2C5</td>
</tr>
<tr>
<td>127-149</td>
<td>111-133</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>150</td>
<td>134</td>
<td>0x0000.0258</td>
<td>PWM1 Generator 0</td>
</tr>
<tr>
<td>151</td>
<td>135</td>
<td>0x0000.025C</td>
<td>PWM1 Generator 1</td>
</tr>
<tr>
<td>152</td>
<td>136</td>
<td>0x0000.0260</td>
<td>PWM1 Generator 2</td>
</tr>
<tr>
<td>153</td>
<td>137</td>
<td>0x0000.0264</td>
<td>PWM1 Generator 3</td>
</tr>
<tr>
<td>154</td>
<td>138</td>
<td>0x0000.0268</td>
<td>PWM1 Fault</td>
</tr>
</tbody>
</table>

### 2.5.3 Exception Handlers

The processor handles exceptions using:

- **Interrupt Service Routines (ISRs).** Interrupts (IRQx) are the exceptions handled by ISRs.

- **Fault Handlers.** Hard fault, memory management fault, usage fault, and bus fault are fault exceptions handled by the fault handlers.

- **System Handlers.** NMI, PendSV, SVCll, SysTick, and the fault exceptions are all system exceptions that are handled by system handlers.
2.5.4 Vector Table

The vector table contains the reset value of the stack pointer and the start addresses, also called exception vectors, for all exception handlers. The vector table is constructed using the vector address or offset shown in Table 2-8 on page 103. Figure 2-6 on page 107 shows the order of the exception vectors in the vector table. The least-significant bit of each vector must be 1, indicating that the exception handler is Thumb code.

Figure 2-6. Vector Table

<table>
<thead>
<tr>
<th>Exception number</th>
<th>IRQ number</th>
<th>Offset</th>
<th>Vector</th>
</tr>
</thead>
<tbody>
<tr>
<td>154</td>
<td>138</td>
<td>0x0268</td>
<td>IRQ131</td>
</tr>
<tr>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>18</td>
<td>2</td>
<td>0x004C</td>
<td>IRQ2</td>
</tr>
<tr>
<td>17</td>
<td>1</td>
<td>0x0048</td>
<td>IRQ1</td>
</tr>
<tr>
<td>16</td>
<td>0</td>
<td>0x0044</td>
<td>IRQ0</td>
</tr>
<tr>
<td>15</td>
<td>-1</td>
<td>0x0040</td>
<td>Systick</td>
</tr>
<tr>
<td>14</td>
<td>-2</td>
<td>0x003C</td>
<td>PendSV</td>
</tr>
<tr>
<td>13</td>
<td>.</td>
<td>0x003B</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>.</td>
<td></td>
<td>Reserved for Debug</td>
</tr>
<tr>
<td>11</td>
<td>-5</td>
<td>0x002C</td>
<td>SVCalls</td>
</tr>
<tr>
<td>10</td>
<td>.</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>9</td>
<td>.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>-10</td>
<td>0x0018</td>
<td>Usage fault</td>
</tr>
<tr>
<td>5</td>
<td>-11</td>
<td>0x0014</td>
<td>Bus fault</td>
</tr>
<tr>
<td>4</td>
<td>-12</td>
<td>0x0010</td>
<td>Memory management fault</td>
</tr>
<tr>
<td>3</td>
<td>-13</td>
<td>0x000C</td>
<td>Hard fault</td>
</tr>
<tr>
<td>2</td>
<td>-14</td>
<td>0x0008</td>
<td>NMI</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>0x0004</td>
<td>Reset</td>
</tr>
<tr>
<td>.</td>
<td></td>
<td>0x0000</td>
<td>Initial SP value</td>
</tr>
</tbody>
</table>

On system reset, the vector table is fixed at address 0x0000.0000. Privileged software can write to the Vector Table Offset (VTABLE) register to relocate the vector table start address to a different memory location, in the range 0x0000.0400 to 0x3FFF.FC00 (see “Vector Table” on page 107). Note that when configuring the VTABLE register, the offset must be aligned on a 1024-byte boundary.

2.5.5 Exception Priorities

As Table 2-8 on page 103 shows, all exceptions have an associated priority, with a lower priority value indicating a higher priority and configurable priorities for all exceptions except Reset, Hard fault, and NMI. If software does not configure any priorities, then all exceptions with a configurable priority have a priority of 0. For information about configuring exception priorities, see page 170 and page 152.
**Note:** Configurable priority values for the Tiva™ C Series implementation are in the range 0-7. This means that the Reset, Hard fault, and NMI exceptions, with fixed negative priority values, always have higher priority than any other exception.

For example, assigning a higher priority value to IRQ[0] and a lower priority value to IRQ[1] means that IRQ[1] has higher priority than IRQ[0]. If both IRQ[1] and IRQ[0] are asserted, IRQ[1] is processed before IRQ[0].

If multiple pending exceptions have the same priority, the pending exception with the lowest exception number takes precedence. For example, if both IRQ[0] and IRQ[1] are pending and have the same priority, then IRQ[0] is processed before IRQ[1].

When the processor is executing an exception handler, the exception handler is preempted if a higher priority exception occurs. If an exception occurs with the same priority as the exception being handled, the handler is not preempted, irrespective of the exception number. However, the status of the new interrupt changes to pending.

### 2.5.6 Interrupt Priority Grouping

To increase priority control in systems with interrupts, the NVIC supports priority grouping. This grouping divides each interrupt priority register entry into two fields:

- An upper field that defines the group priority
- A lower field that defines a subpriority within the group

Only the group priority determines preemption of interrupt exceptions. When the processor is executing an interrupt exception handler, another interrupt with the same group priority as the interrupt being handled does not preempt the handler.

If multiple pending interrupts have the same group priority, the subpriority field determines the order in which they are processed. If multiple pending interrupts have the same group priority and subpriority, the interrupt with the lowest IRQ number is processed first.

For information about splitting the interrupt priority fields into group priority and subpriority, see page 164.

### 2.5.7 Exception Entry and Return

Descriptions of exception handling use the following terms:

- **Preemption.** When the processor is executing an exception handler, an exception can preempt the exception handler if its priority is higher than the priority of the exception being handled. See “Interrupt Priority Grouping” on page 108 for more information about preemption by an interrupt. When one exception preempts another, the exceptions are called nested exceptions. See “Exception Entry” on page 109 for more information.

- **Return.** Return occurs when the exception handler is completed, and there is no pending exception with sufficient priority to be serviced and the completed exception handler was not handling a late-arriving exception. The processor pops the stack and restores the processor state to the state it had before the interrupt occurred. See “Exception Return” on page 110 for more information.

- **Tail-Chaining.** This mechanism speeds up exception servicing. On completion of an exception handler, if there is a pending exception that meets the requirements for exception entry, the stack pop is skipped and control transfers to the new exception handler.
Late-Arriving. This mechanism speeds up preemption. If a higher priority exception occurs during state saving for a previous exception, the processor switches to handle the higher priority exception and initiates the vector fetch for that exception. State saving is not affected by late arrival because the state saved is the same for both exceptions. Therefore, the state saving continues uninterrupted. The processor can accept a late arriving exception until the first instruction of the exception handler of the original exception enters the execute stage of the processor. On return from the exception handler of the late-arriving exception, the normal tail-chaining rules apply.

2.5.7.1 Exception Entry

Exception entry occurs when there is a pending exception with sufficient priority and either the processor is in Thread mode or the new exception is of higher priority than the exception being handled, in which case the new exception preempts the original exception.

When one exception preempts another, the exceptions are nested.

Sufficient priority means the exception has more priority than any limits set by the mask registers (see PRIMASK on page 85, FAULTMASK on page 86, and BASEPRI on page 87). An exception with less priority than this is pending but is not handled by the processor.

When the processor takes an exception, unless the exception is a tail-chained or a late-arriving exception, the processor pushes information onto the current stack. This operation is referred to as stacking and the structure of eight data words is referred to as stack frame.

When using floating-point routines, the Cortex-M4F processor automatically stacks the architected floating-point state on exception entry. Figure 2-7 on page 110 shows the Cortex-M4F stack frame layout when floating-point state is preserved on the stack as the result of an interrupt or an exception.

Note: Where stack space for floating-point state is not allocated, the stack frame is the same as that of ARMv7-M implementations without an FPU. Figure 2-7 on page 110 shows this stack frame also.
Immediately after stacking, the stack pointer indicates the lowest address in the stack frame. The stack frame includes the return address, which is the address of the next instruction in the interrupted program. This value is restored to the PC at exception return so that the interrupted program resumes.

In parallel with the stacking operation, the processor performs a vector fetch that reads the exception handler start address from the vector table. When stacking is complete, the processor starts executing the exception handler. At the same time, the processor writes an EXC_RETURN value to the LR, indicating which stack pointer corresponds to the stack frame and what operation mode the processor was in before the entry occurred.

If no higher-priority exception occurs during exception entry, the processor starts executing the exception handler and automatically changes the status of the corresponding pending interrupt to active.

If another higher-priority exception occurs during exception entry, known as late arrival, the processor starts executing the exception handler for this exception and does not change the pending status of the earlier exception.

### 2.5.7.2 Exception Return

Exception return occurs when the processor is in Handler mode and executes one of the following instructions to load the EXC_RETURN value into the PC:
An LDM or POP instruction that loads the PC

A BX instruction using any register

An LDR instruction with the PC as the destination

EXC RETURN is the value loaded into the LR on exception entry. The exception mechanism relies on this value to detect when the processor has completed an exception handler. The lowest five bits of this value provide information on the return stack and processor mode. Table 2-10 on page 111 shows the EXC RETURN values with a description of the exception return behavior.

EXC RETURN bits 31:5 are all set. When this value is loaded into the PC, it indicates to the processor that the exception is complete, and the processor initiates the appropriate exception return sequence.

Table 2-10. Exception Return Behavior

<table>
<thead>
<tr>
<th>EXC_RETURN[31:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFFFF.FFE0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFFFF.FFE1</td>
<td>Return to Handler mode. Exception return uses floating-point state from MSP. Execution uses MSP after return.</td>
</tr>
<tr>
<td>0xFFFF.FFE2 - 0xFFFF.FFE8</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFFFF.FFE9</td>
<td>Return to Thread mode. Exception return uses floating-point state from MSP. Execution uses MSP after return.</td>
</tr>
<tr>
<td>0xFFFF.FFEA - 0xFFFF.FFEC</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFFFF.FFED</td>
<td>Return to Thread mode. Exception return uses floating-point state from PSP. Execution uses PSP after return.</td>
</tr>
<tr>
<td>0xFFFF.FFEF - 0xFFFF.FFFE0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFFFF.FFF1</td>
<td>Return to Handler mode. Exception return uses non-floating-point state from MSP. Execution uses MSP after return.</td>
</tr>
<tr>
<td>0xFFFF.FFF2 - 0xFFFF.FFF8</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFFFF.FFF9</td>
<td>Return to Thread mode. Exception return uses non-floating-point state from MSP. Execution uses MSP after return.</td>
</tr>
<tr>
<td>0xFFFF.FFFA - 0xFFFF.FFFC</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFFFF.FFFD</td>
<td>Return to Thread mode. Exception return uses non-floating-point state from PSP. Execution uses PSP after return.</td>
</tr>
<tr>
<td>0xFFFF.FFFE - 0xFFFF.FFFF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

2.6 Fault Handling

Faults are a subset of the exceptions (see "Exception Model" on page 101). The following conditions generate a fault:

- A bus error on an instruction fetch or vector table load or a data access.
- An internally detected error such as an undefined instruction or an attempt to change state with a BX instruction.

- Attempting to execute an instruction from a memory region marked as Non-Executable (XN).

- An MPU fault because of a privilege violation or an attempt to access an unmanaged region.

### 2.6.1 Fault Types

Table 2-11 on page 112 shows the types of fault, the handler used for the fault, the corresponding fault status register, and the register bit that indicates the fault has occurred. See page 177 for more information about the fault status registers.

<table>
<thead>
<tr>
<th>Fault</th>
<th>Handler</th>
<th>Fault Status Register</th>
<th>Bit Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus error on a vector read</td>
<td>Hard fault</td>
<td>Hard Fault Status (HFAULTSTAT)</td>
<td>VECT</td>
</tr>
<tr>
<td>Fault escalated to a hard fault</td>
<td>Hard fault</td>
<td>Hard Fault Status (HFAULTSTAT)</td>
<td>FORCED</td>
</tr>
<tr>
<td>MPU or default memory mismatch on instruction access</td>
<td>Memory management fault</td>
<td>Memory Management Fault Status (MFAULTSTAT)</td>
<td>IERR a</td>
</tr>
<tr>
<td>MPU or default memory mismatch on data access</td>
<td>Memory management fault</td>
<td>Memory Management Fault Status (MFAULTSTAT)</td>
<td>DERR</td>
</tr>
<tr>
<td>MPU or default memory mismatch on exception stacking</td>
<td>Memory management fault</td>
<td>Memory Management Fault Status (MFAULTSTAT)</td>
<td>MSTKE</td>
</tr>
<tr>
<td>MPU or default memory mismatch on exception unstacking</td>
<td>Memory management fault</td>
<td>Memory Management Fault Status (MFAULTSTAT)</td>
<td>MUSTKE</td>
</tr>
<tr>
<td>MPU or default memory mismatch during lazy floating-point state preservation</td>
<td>Memory management fault</td>
<td>Memory Management Fault Status (MFAULTSTAT)</td>
<td>MLSPEERR</td>
</tr>
<tr>
<td>Bus error during exception stacking</td>
<td>Bus fault</td>
<td>Bus Fault Status (BFAULTSTAT)</td>
<td>BSTKE</td>
</tr>
<tr>
<td>Bus error during exception unstacking</td>
<td>Bus fault</td>
<td>Bus Fault Status (BFAULTSTAT)</td>
<td>BUSTKE</td>
</tr>
<tr>
<td>Bus error during instruction prefetch</td>
<td>Bus fault</td>
<td>Bus Fault Status (BFAULTSTAT)</td>
<td>IBUS</td>
</tr>
<tr>
<td>Bus error during lazy floating-point state preservation</td>
<td>Bus fault</td>
<td>Bus Fault Status (BFAULTSTAT)</td>
<td>BLSPE</td>
</tr>
<tr>
<td>Precise data bus error</td>
<td>Bus fault</td>
<td>Bus Fault Status (BFAULTSTAT)</td>
<td>PRECISE</td>
</tr>
<tr>
<td>Imprecise data bus error</td>
<td>Bus fault</td>
<td>Bus Fault Status (BFAULTSTAT)</td>
<td>IMPRE</td>
</tr>
<tr>
<td>Attempt to access a coprocessor</td>
<td>Usage fault</td>
<td>Usage Fault Status (UFAULTSTAT)</td>
<td>NOCP</td>
</tr>
<tr>
<td>Undefined instruction</td>
<td>Usage fault</td>
<td>Usage Fault Status (UFAULTSTAT)</td>
<td>UNDEF</td>
</tr>
<tr>
<td>Attempt to enter an invalid instruction set state b</td>
<td>Usage fault</td>
<td>Usage Fault Status (UFAULTSTAT)</td>
<td>INVSTAT</td>
</tr>
<tr>
<td>Invalid EXC_RETURN value</td>
<td>Usage fault</td>
<td>Usage Fault Status (UFAULTSTAT)</td>
<td>INVPC</td>
</tr>
<tr>
<td>Illegal unaligned load or store</td>
<td>Usage fault</td>
<td>Usage Fault Status (UFAULTSTAT)</td>
<td>UNALIGN</td>
</tr>
<tr>
<td>Divide by 0</td>
<td>Usage fault</td>
<td>Usage Fault Status (UFAULTSTAT)</td>
<td>DIV0</td>
</tr>
</tbody>
</table>

a. Occurs on an access to an XN region even if the MPU is disabled.

b. Attempting to use an instruction set other than the Thumb instruction set, or returning to a non load-store-multiply instruction with ICI continuation.

### 2.6.2 Fault Escalation and Hard Faults

All fault exceptions except for hard fault have configurable exception priority (see SYSPRI1 on page 170). Software can disable execution of the handlers for these faults (see SYSHNDCTRL on page 173).
Usually, the exception priority, together with the values of the exception mask registers, determines whether the processor enters the fault handler, and whether a fault handler can preempt another fault handler as described in “Exception Model” on page 101.

In some situations, a fault with configurable priority is treated as a hard fault. This process is called priority escalation, and the fault is described as *escalated to hard fault*. Escalation to hard fault occurs when:

- A fault handler causes the same kind of fault as the one it is servicing. This escalation to hard fault occurs because a fault handler cannot preempt itself because it must have the same priority as the current priority level.

- A fault handler causes a fault with the same or lower priority as the fault it is servicing. This situation happens because the handler for the new fault cannot preempt the currently executing fault handler.

- An exception handler causes a fault for which the priority is the same as or lower than the currently executing exception.

- A fault occurs and the handler for that fault is not enabled.

If a bus fault occurs during a stack push when entering a bus fault handler, the bus fault does not escalate to a hard fault. Thus if a corrupted stack causes a fault, the fault handler executes even though the stack push for the handler failed. The fault handler operates but the stack contents are corrupted.

**Note:** Only Reset and NMI can preempt the fixed priority hard fault. A hard fault can preempt any exception other than Reset, NMI, or another hard fault.

### 2.6.3 Fault Status Registers and Fault Address Registers

The fault status registers indicate the cause of a fault. For bus faults and memory management faults, the fault address register indicates the address accessed by the operation that caused the fault, as shown in Table 2-12 on page 113.

**Table 2-12. Fault Status and Fault Address Registers**

<table>
<thead>
<tr>
<th>Handler</th>
<th>Status Register Name</th>
<th>Address Register Name</th>
<th>Register Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hard fault</td>
<td>Hard Fault Status (HFAULTSTAT)</td>
<td>-</td>
<td>page 183</td>
</tr>
<tr>
<td>Memory management fault</td>
<td>Memory Management Fault Status (MFAULTSTAT)</td>
<td>Memory Management Fault Address (MMADDR)</td>
<td>page 177 page 184</td>
</tr>
<tr>
<td>Bus fault</td>
<td>Bus Fault Status (BFAULTSTAT)</td>
<td>Bus Fault Address (FAULTADDR)</td>
<td>page 177 page 185</td>
</tr>
<tr>
<td>Usage fault</td>
<td>Usage Fault Status (UFAULTSTAT)</td>
<td>-</td>
<td>page 177</td>
</tr>
</tbody>
</table>

### 2.6.4 Lockup

The processor enters a lockup state if a hard fault occurs when executing the NMI or hard fault handlers. When the processor is in the lockup state, it does not execute any instructions. The processor remains in lockup state until it is reset, an NMI occurs, or it is halted by a debugger.

**Note:** If the lockup state occurs from the NMI handler, a subsequent NMI does not cause the processor to leave the lockup state.
2.7 Power Management

The Cortex-M4F processor sleep modes reduce power consumption:

- Sleep mode stops the processor clock.
- Deep-sleep mode stops the system clock and switches off the PLL and Flash memory.

The SLEEPDEEP bit of the System Control (SYSCTRL) register selects which sleep mode is used (see page 166). For more information about the behavior of the sleep modes, see “System Control” on page 227.

This section describes the mechanisms for entering sleep mode and the conditions for waking up from sleep mode, both of which apply to Sleep mode and Deep-sleep mode.

2.7.1 Entering Sleep Modes

This section describes the mechanisms software can use to put the processor into one of the sleep modes.

The system can generate spurious wake-up events, for example a debug operation wakes up the processor. Therefore, software must be able to put the processor back into sleep mode after such an event. A program might have an idle loop to put the processor back to sleep mode.

2.7.1.1 Wait for Interrupt

The wait for interrupt instruction, WFI, causes immediate entry to sleep mode unless the wake-up condition is true (see “Wake Up from WFI or Sleep-on-Exit” on page 115). When the processor executes a WFI instruction, it stops executing instructions and enters sleep mode. See the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A) for more information.

2.7.1.2 Wait for Event

The wait for event instruction, WFE, causes entry to sleep mode conditional on the value of a one-bit event register. When the processor executes a WFE instruction, it checks the event register. If the register is 0, the processor stops executing instructions and enters sleep mode. If the register is 1, the processor clears the register and continues executing instructions without entering sleep mode.

If the event register is 1, the processor must not enter sleep mode on execution of a WFE instruction. Typically, this situation occurs if an SEV instruction has been executed. Software cannot access this register directly.

See the Cortex™-M4 instruction set chapter in the ARM® Cortex™-M4 Devices Generic User Guide (literature number ARM DUI 0553A) for more information.

2.7.1.3 Sleep-on-Exit

If the SLEEPEXIT bit of the SYSCTRL register is set, when the processor completes the execution of all exception handlers, it returns to Thread mode and immediately enters sleep mode. This mechanism can be used in applications that only require the processor to run when an exception occurs.

2.7.2 Wake Up from Sleep Mode

The conditions for the processor to wake up depend on the mechanism that caused it to enter sleep mode.
2.7.2.1 Wake Up from WFI or Sleep-on-Exit

Normally, the processor wakes up only when the NVIC detects an exception with sufficient priority to cause exception entry. Some embedded systems might have to execute system restore tasks after the processor wakes up and before executing an interrupt handler. Entry to the interrupt handler can be delayed by setting the PRIMASK bit and clearing the FAULTMASK bit. If an interrupt arrives that is enabled and has a higher priority than current exception priority, the processor wakes up but does not execute the interrupt handler until the processor clears PRIMASK. For more information about PRIMASK and FAULTMASK, see page 85 and page 86.

2.7.2.2 Wake Up from WFE

The processor wakes up if it detects an exception with sufficient priority to cause exception entry. In addition, if the SEVONPEND bit in the SYSCTRL register is set, any new pending interrupt triggers an event and wakes up the processor, even if the interrupt is disabled or has insufficient priority to cause exception entry. For more information about SYSCTRL, see page 166.

2.8 Instruction Set Summary

The processor implements a version of the Thumb instruction set. Table 2-13 on page 115 lists the supported instructions.

Note: In Table 2-13 on page 115:

- Angle brackets, <>, enclose alternative forms of the operand
- Braces, {}, enclose optional operands
- The Operands column is not exhaustive
- Op2 is a flexible second operand that can be either a register or a constant
- Most instructions can use an optional condition code suffix

For more information on the instructions and operands, see the instruction descriptions in the ARM® Cortex™-M4 Technical Reference Manual.

Table 2-13. Cortex-M4F Instruction Summary

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Operands</th>
<th>Brief Description</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC, ADCS</td>
<td>(Rd,) Rn, Op2</td>
<td>Add with carry</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>ADD, ADDS</td>
<td>(Rd,) Rn, Op2</td>
<td>Add</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>ADD, ADDW</td>
<td>(Rd,) Rn, #imm12</td>
<td>Add</td>
<td></td>
</tr>
<tr>
<td>ADR</td>
<td>Rd, label</td>
<td>Load PC-relative address</td>
<td></td>
</tr>
<tr>
<td>AND, ANDS</td>
<td>(Rd,) Rn, Op2</td>
<td>Logical AND</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>ASR, ASRS</td>
<td>Rd, Rm, &lt;Rs</td>
<td>#n&gt;</td>
<td>Arithmetic shift right</td>
</tr>
<tr>
<td>B</td>
<td>label</td>
<td>Branch</td>
<td></td>
</tr>
<tr>
<td>BFC</td>
<td>Rd, #lsb, #width</td>
<td>Bit field clear</td>
<td></td>
</tr>
<tr>
<td>BFI</td>
<td>Rd, Rn, #lsb, #width</td>
<td>Bit field insert</td>
<td></td>
</tr>
<tr>
<td>BIC, BICS</td>
<td>(Rd,) Rn, Op2</td>
<td>Bit clear</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>BKPT</td>
<td>#imm</td>
<td>Breakpoint</td>
<td></td>
</tr>
<tr>
<td>BL</td>
<td>label</td>
<td>Branch with link</td>
<td></td>
</tr>
<tr>
<td>BLX</td>
<td>Rm</td>
<td>Branch indirect with link</td>
<td></td>
</tr>
<tr>
<td>BX</td>
<td>Rm</td>
<td>Branch indirect</td>
<td></td>
</tr>
<tr>
<td>CBNZ</td>
<td>Rn, label</td>
<td>Compare and branch if non-zero</td>
<td></td>
</tr>
</tbody>
</table>
Table 2-13. Cortex-M4F Instruction Summary (continued)

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Operands</th>
<th>Brief Description</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>CBZ</td>
<td>Rn, label</td>
<td>Compare and branch if zero</td>
<td>-</td>
</tr>
<tr>
<td>CLR</td>
<td>-</td>
<td>Clear exclusive</td>
<td>-</td>
</tr>
<tr>
<td>CLZ</td>
<td>Rd, Rm</td>
<td>Count leading zeros</td>
<td>-</td>
</tr>
<tr>
<td>CMN</td>
<td>Rn, Op2</td>
<td>Compare negative</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>CMP</td>
<td>Rn, Op2</td>
<td>Compare</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>CPSID</td>
<td>i</td>
<td>Change processor state, disable interrupts</td>
<td>-</td>
</tr>
<tr>
<td>CPSIE</td>
<td>i</td>
<td>Change processor state, enable interrupts</td>
<td>-</td>
</tr>
<tr>
<td>DMB</td>
<td>-</td>
<td>Data memory barrier</td>
<td>-</td>
</tr>
<tr>
<td>DSB</td>
<td>-</td>
<td>Data synchronization barrier</td>
<td>-</td>
</tr>
<tr>
<td>EOR, EORS</td>
<td>(Rd,) Rn, Op2</td>
<td>Exclusive OR</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>ISB</td>
<td>-</td>
<td>Instruction synchronization barrier</td>
<td>-</td>
</tr>
<tr>
<td>IT</td>
<td>-</td>
<td>If-Then condition block</td>
<td>-</td>
</tr>
<tr>
<td>LDM</td>
<td>Rn{}, reglist</td>
<td>Load multiple registers, increment after</td>
<td>-</td>
</tr>
<tr>
<td>LDMDB, LDMEA</td>
<td>Rn{}, reglist</td>
<td>Load multiple registers, decrement before</td>
<td>-</td>
</tr>
<tr>
<td>LDMFD, LDMA</td>
<td>Rn{}, reglist</td>
<td>Load multiple registers, increment after</td>
<td>-</td>
</tr>
<tr>
<td>LDR</td>
<td>Rt, [Rn, #offset]</td>
<td>Load register with word</td>
<td>-</td>
</tr>
<tr>
<td>LDRB, LDRBT</td>
<td>Rt, [Rn, #offset]</td>
<td>Load register with byte</td>
<td>-</td>
</tr>
<tr>
<td>LDRD</td>
<td>Rt, Rt2, [Rn, #offset]</td>
<td>Load register with two bytes</td>
<td>-</td>
</tr>
<tr>
<td>LDREX</td>
<td>Rt, [Rn, #offset]</td>
<td>Load register exclusive</td>
<td>-</td>
</tr>
<tr>
<td>LDREXB</td>
<td>Rt, [Rn]</td>
<td>Load register exclusive with byte</td>
<td>-</td>
</tr>
<tr>
<td>LDREXH</td>
<td>Rt, [Rn]</td>
<td>Load register exclusive with halfword</td>
<td>-</td>
</tr>
<tr>
<td>LDRH, LDRHT</td>
<td>Rt, [Rn, #offset]</td>
<td>Load register with halfword</td>
<td>-</td>
</tr>
<tr>
<td>LDRSB, LDRSBT</td>
<td>Rt, [Rn, #offset]</td>
<td>Load register with signed byte</td>
<td>-</td>
</tr>
<tr>
<td>LDRSH, LDRSHT</td>
<td>Rt, [Rn, #offset]</td>
<td>Load register with signed halfword</td>
<td>-</td>
</tr>
<tr>
<td>LDRT</td>
<td>Rt, [Rn, #offset]</td>
<td>Load register with word</td>
<td>-</td>
</tr>
<tr>
<td>LSL, LSLS</td>
<td>Rd, Rm, &lt;Rs</td>
<td>n&gt;</td>
<td>Logical shift left</td>
</tr>
<tr>
<td>LSR, LSRS</td>
<td>Rd, Rm, &lt;Rs</td>
<td>n&gt;</td>
<td>Logical shift right</td>
</tr>
<tr>
<td>MLA</td>
<td>Rd, Rn, Rm, Ra</td>
<td>Multiply with accumulate, 32-bit result</td>
<td>-</td>
</tr>
<tr>
<td>MLS</td>
<td>Rd, Rn, Rm, Ra</td>
<td>Multiply and subtract, 32-bit result</td>
<td>-</td>
</tr>
<tr>
<td>MOV, MOVS</td>
<td>Rd, Op2</td>
<td>Move</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>MOV, MOVN</td>
<td>Rd, #imm16</td>
<td>Move 16-bit constant</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>MOVT</td>
<td>Rd, #imm16</td>
<td>Move top</td>
<td>-</td>
</tr>
<tr>
<td>MRS</td>
<td>Rd, spec_reg</td>
<td>Move from special register to general</td>
<td>-</td>
</tr>
<tr>
<td>MSR</td>
<td>spec_reg, Rm</td>
<td>Move from general register to special</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>MUL, MULS</td>
<td>(Rd,) Rn, Rm</td>
<td>Multiply, 32-bit result</td>
<td>N, Z</td>
</tr>
<tr>
<td>MVN, MVNS</td>
<td>Rd, Op2</td>
<td>Move NOT</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>NOP</td>
<td>-</td>
<td>No operation</td>
<td>-</td>
</tr>
<tr>
<td>ORN, ORNS</td>
<td>(Rd,) Rn, Op2</td>
<td>Logical OR NOT</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>Mnemonic</td>
<td>Operands</td>
<td>Brief Description</td>
<td>Flags</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>------------------</td>
<td>-------</td>
</tr>
<tr>
<td>ORR, ORRS</td>
<td>(Rd,) Rn, Op2</td>
<td>Logical OR</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>PKHTB, PKHBT</td>
<td>(Rd,) Rn, Rm, Op2</td>
<td>Pack halfword</td>
<td>-</td>
</tr>
<tr>
<td>POP</td>
<td>reglist</td>
<td>Pop registers from stack</td>
<td>-</td>
</tr>
<tr>
<td>PUSH</td>
<td>reglist</td>
<td>Push registers onto stack</td>
<td>-</td>
</tr>
<tr>
<td>QADD</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating add</td>
<td>Q</td>
</tr>
<tr>
<td>QADD16</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating add 16</td>
<td>-</td>
</tr>
<tr>
<td>QADD8</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating add 8</td>
<td>-</td>
</tr>
<tr>
<td>QASX</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating add and subtract with exchange</td>
<td>-</td>
</tr>
<tr>
<td>QDADD</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating double and add</td>
<td>Q</td>
</tr>
<tr>
<td>QDSUB</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating double and subtract</td>
<td>Q</td>
</tr>
<tr>
<td>QSAX</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating subtract and add with exchange</td>
<td>-</td>
</tr>
<tr>
<td>QSUB</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating subtract</td>
<td>Q</td>
</tr>
<tr>
<td>QSUB16</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating subtract 16</td>
<td>-</td>
</tr>
<tr>
<td>QSUB8</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating subtract 8</td>
<td>-</td>
</tr>
<tr>
<td>RBIT</td>
<td>Rd, Rn</td>
<td>Reverse bits</td>
<td>-</td>
</tr>
<tr>
<td>REV</td>
<td>Rd, Rn</td>
<td>Reverse byte order in a word</td>
<td>-</td>
</tr>
<tr>
<td>REV16</td>
<td>Rd, Rn</td>
<td>Reverse byte order in each halfword</td>
<td>-</td>
</tr>
<tr>
<td>REVSH</td>
<td>Rd, Rn</td>
<td>Reverse byte order in bottom halfword and sign extend</td>
<td>-</td>
</tr>
<tr>
<td>ROR, RORS</td>
<td>Rd, Rm, &lt;Rs</td>
<td>#n&gt;</td>
<td>Rotate right</td>
</tr>
<tr>
<td>RRX, RRXS</td>
<td>Rd, Rm</td>
<td>Rotate right with extend</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>RSB, RSBS</td>
<td>(Rd,) Rn, Op2</td>
<td>Reverse subtract</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>SADD16</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed add 16</td>
<td>GE</td>
</tr>
<tr>
<td>SADD8</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed add 8</td>
<td>GE</td>
</tr>
<tr>
<td>SASX</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed add and subtract with exchange</td>
<td>GE</td>
</tr>
<tr>
<td>SBC, SBCS</td>
<td>(Rd,) Rn, Op2</td>
<td>Subtract with carry</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>SBFX</td>
<td>Rd, Rn, #lsb, #width</td>
<td>Signed bit field extract</td>
<td>-</td>
</tr>
<tr>
<td>SDIV</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed divide</td>
<td>-</td>
</tr>
<tr>
<td>SEL</td>
<td>(Rd,) Rn, Rm</td>
<td>Select bytes</td>
<td>-</td>
</tr>
<tr>
<td>SEV</td>
<td>-</td>
<td>Send event</td>
<td>-</td>
</tr>
<tr>
<td>SHADD16</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed halving add 16</td>
<td>-</td>
</tr>
<tr>
<td>SHADD8</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed halving add 8</td>
<td>-</td>
</tr>
<tr>
<td>SHASX</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed halving add and subtract with exchange</td>
<td>-</td>
</tr>
<tr>
<td>SHSAX</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed halving add and subtract with exchange</td>
<td>-</td>
</tr>
<tr>
<td>SHSUB16</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed halving subtract 16</td>
<td>-</td>
</tr>
<tr>
<td>SHSUB8</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed halving subtract 8</td>
<td>-</td>
</tr>
<tr>
<td>Mnemonic</td>
<td>Operands</td>
<td>Brief Description</td>
<td>Flags</td>
</tr>
<tr>
<td>----------------</td>
<td>---------------------------</td>
<td>-------------------------------------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>SMLABB,</td>
<td>Rd, Rn, Rm, Ra</td>
<td>Signed multiply accumulate long (halfwords)</td>
<td>Q</td>
</tr>
<tr>
<td>SMLABT,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMLATB,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMLATT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMLAD,</td>
<td>Rd, Rn, Rm, Ra</td>
<td>Signed multiply accumulate dual</td>
<td>Q</td>
</tr>
<tr>
<td>SMLADX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMLAL</td>
<td>RdLo, RdHi, Rn, Rm</td>
<td>Signed multiply with accumulate (32x32+64), 64-bit result</td>
<td>-</td>
</tr>
<tr>
<td>SMLALBB,</td>
<td>RdLo, RdHi, Rn, Rm</td>
<td>Signed multiply accumulate long (halfwords)</td>
<td>-</td>
</tr>
<tr>
<td>SMLALBT,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMLALTB,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMLALTT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMLALDX</td>
<td>RdLo, RdHi, Rn, Rm</td>
<td>Signed multiply accumulate long dual</td>
<td>-</td>
</tr>
<tr>
<td>SMLAWB, SMLAWT</td>
<td>Rd, Rn, Rm, Ra</td>
<td>Signed multiply accumulate, word by halfword</td>
<td>Q</td>
</tr>
<tr>
<td>SMLSD</td>
<td>Rd, Rn, Rm, Ra</td>
<td>Signed multiply subtract dual</td>
<td>Q</td>
</tr>
<tr>
<td>SMLSDX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMLSLD</td>
<td>RdLo, RdHi, Rn, Rm</td>
<td>Signed multiply subtract long dual</td>
<td></td>
</tr>
<tr>
<td>SMLSLDX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMMMA</td>
<td>Rd, Rn, Rm, Ra</td>
<td>Signed most significant word multiply accumulate</td>
<td>-</td>
</tr>
<tr>
<td>SMMMLS,</td>
<td>Rd, Rn, Rm, Ra</td>
<td>Signed most significant word multiply subtract</td>
<td>-</td>
</tr>
<tr>
<td>SMMUL,</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed most significant word multiply</td>
<td>-</td>
</tr>
<tr>
<td>SMMULR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMUAD</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed dual multiply add</td>
<td>Q</td>
</tr>
<tr>
<td>SMUADX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMULBB,</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed multiply halfwords</td>
<td>-</td>
</tr>
<tr>
<td>SMULBT,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMULTB,</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMULTT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMULL</td>
<td>RdLo, RdHi, Rn, Rm</td>
<td>Signed multiply (32x32), 64-bit result</td>
<td>-</td>
</tr>
<tr>
<td>SMULWB,</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed multiply by halfword</td>
<td>-</td>
</tr>
<tr>
<td>SMULWT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SMUSD,</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed dual multiply subtract</td>
<td>-</td>
</tr>
<tr>
<td>SMUSDX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSAT</td>
<td>Rd, #n, Rm {}, shift #s</td>
<td>Signed saturate</td>
<td>Q</td>
</tr>
<tr>
<td>SSAT16</td>
<td>Rd, #n, Rm</td>
<td>Signed saturate 16</td>
<td>Q</td>
</tr>
<tr>
<td>SSAX</td>
<td>(Rd,) Rn, Rm</td>
<td>Saturating subtract and add with exchange</td>
<td>GE</td>
</tr>
<tr>
<td>SSUBL6</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed subtract 16</td>
<td>-</td>
</tr>
<tr>
<td>SSUB8</td>
<td>(Rd,) Rn, Rm</td>
<td>Signed subtract 8</td>
<td>-</td>
</tr>
<tr>
<td>STM</td>
<td>Rn{}, reglist</td>
<td>Store multiple registers, increment after</td>
<td>-</td>
</tr>
<tr>
<td>Mnemonic</td>
<td>Operands</td>
<td>Brief Description</td>
<td>Flags</td>
</tr>
<tr>
<td>------------</td>
<td>----------</td>
<td>--------------------------------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>STMDB, STMBA</td>
<td>Rn{!}, reglist</td>
<td>Store multiple registers, decrement before</td>
<td>-</td>
</tr>
<tr>
<td>STMFD, STMFIA</td>
<td>Rn{!}, reglist</td>
<td>Store multiple registers, increment after</td>
<td>-</td>
</tr>
<tr>
<td>STR</td>
<td>Rt, [Rn {, #offset}]</td>
<td>Store register word</td>
<td>-</td>
</tr>
<tr>
<td>STRB, STRBT</td>
<td>Rt, [Rn {, #offset}]</td>
<td>Store register byte</td>
<td>-</td>
</tr>
<tr>
<td>STRD</td>
<td>Rt, Rt2, [Rn {, #offset}]</td>
<td>Store register two words</td>
<td>-</td>
</tr>
<tr>
<td>STREX</td>
<td>Rt, Rt, [Rn {, #offset}]</td>
<td>Store register exclusive</td>
<td>-</td>
</tr>
<tr>
<td>STREXB</td>
<td>Rd, Rt, [Rn]</td>
<td>Store register exclusive byte</td>
<td>-</td>
</tr>
<tr>
<td>STREXH</td>
<td>Rd, Rt, [Rn]</td>
<td>Store register exclusive halfword</td>
<td>-</td>
</tr>
<tr>
<td>STRH, STRHT</td>
<td>Rt, [Rn {, #offset}]</td>
<td>Store register halfword</td>
<td>-</td>
</tr>
<tr>
<td>STRSB, STRSBT</td>
<td>Rt, [Rn {, #offset}]</td>
<td>Store register signed byte</td>
<td>-</td>
</tr>
<tr>
<td>STRSH, STRSHT</td>
<td>Rt, [Rn {, #offset}]</td>
<td>Store register signed halfword</td>
<td>-</td>
</tr>
<tr>
<td>STRT</td>
<td>Rt, [Rn {, #offset}]</td>
<td>Store register word</td>
<td>-</td>
</tr>
<tr>
<td>SUB, SUBS</td>
<td>(Rd,) Rn, Op2</td>
<td>Subtract</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>SUB, SUBW</td>
<td>(Rd,) Rn, #imm12</td>
<td>Subtract 12-bit constant</td>
<td>N, Z, C, V</td>
</tr>
<tr>
<td>SVC</td>
<td>#imm</td>
<td>Supervisor call</td>
<td>-</td>
</tr>
<tr>
<td>SXTAB</td>
<td>(Rd,) Rn, Rm, (ROR #)</td>
<td>Extend 8 bits to 32 and add</td>
<td>-</td>
</tr>
<tr>
<td>SXTAB16</td>
<td>(Rd,) Rn, Rm,(ROR #)</td>
<td>Dual extend 8 bits to 16 and add</td>
<td>-</td>
</tr>
<tr>
<td>SXTAH</td>
<td>(Rd,) Rn, Rm,(ROR #)</td>
<td>Extend 16 bits to 32 and add</td>
<td>-</td>
</tr>
<tr>
<td>SXTB16</td>
<td>(Rd,) Rm,(ROR #n)</td>
<td>Signed extend byte 16</td>
<td>-</td>
</tr>
<tr>
<td>SXTB</td>
<td>(Rd,) Rm,(ROR #n)</td>
<td>Sign extend a byte</td>
<td>-</td>
</tr>
<tr>
<td>SXTH</td>
<td>(Rd,) Rm,(ROR #n)</td>
<td>Sign extend a halfword</td>
<td>-</td>
</tr>
<tr>
<td>TBB</td>
<td>[Rn, Rm]</td>
<td>Table branch byte</td>
<td>-</td>
</tr>
<tr>
<td>TBH</td>
<td>[Rn, Rm, LSL #1]</td>
<td>Table branch halfword</td>
<td>-</td>
</tr>
<tr>
<td>TEQ</td>
<td>Rn, Op2</td>
<td>Test equivalence</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>TST</td>
<td>Rn, Op2</td>
<td>Test</td>
<td>N, Z, C</td>
</tr>
<tr>
<td>UADD16</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned add 16</td>
<td>GE</td>
</tr>
<tr>
<td>UADD8</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned add 8</td>
<td>GE</td>
</tr>
<tr>
<td>UASX</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned add and subtract with exchange</td>
<td>GE</td>
</tr>
<tr>
<td>UNADD16</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned halving add 16</td>
<td>-</td>
</tr>
<tr>
<td>UNADD8</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned halving add 8</td>
<td>-</td>
</tr>
<tr>
<td>UHASX</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned halving add and subtract with exchange</td>
<td>-</td>
</tr>
<tr>
<td>UHSAX</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned halving subtract and add with exchange</td>
<td>-</td>
</tr>
<tr>
<td>UHSUB16</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned halving subtract 16</td>
<td>-</td>
</tr>
<tr>
<td>UHSUB8</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned halving subtract 8</td>
<td>-</td>
</tr>
<tr>
<td>UBFX</td>
<td>Rd, Rn, #lsb, #width</td>
<td>Unsigned bit field extract</td>
<td>-</td>
</tr>
<tr>
<td>UDIV</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned divide</td>
<td>-</td>
</tr>
<tr>
<td>UMAAL</td>
<td>RdLo, RdHi, Rn, Rm</td>
<td>Unsigned multiply accumulate accumulate long (32x32+64), 64-bit result</td>
<td>-</td>
</tr>
</tbody>
</table>
### Table 2-13. Cortex-M4F Instruction Summary (continued)

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Operands</th>
<th>Brief Description</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>UMLAL</td>
<td>RdLo, RdHi, Rn, Rm</td>
<td>Unsigned multiply with accumulate (32x32+32+32, 64-bit result)</td>
<td>-</td>
</tr>
<tr>
<td>UMULL</td>
<td>RdLo, RdHi, Rn, Rm</td>
<td>Unsigned multiply (32x 2), 64-bit result</td>
<td>-</td>
</tr>
<tr>
<td>UQADD16</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Saturating Add 16</td>
<td>-</td>
</tr>
<tr>
<td>UQADD8</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Saturating Add 8</td>
<td>-</td>
</tr>
<tr>
<td>UQASX</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Saturating Add and Subtract with Exchange</td>
<td>-</td>
</tr>
<tr>
<td>UQAX</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Saturating Subtract and Add with Exchange</td>
<td>-</td>
</tr>
<tr>
<td>UQSUB16</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Saturating Subtract 16</td>
<td>-</td>
</tr>
<tr>
<td>UQSUB8</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Saturating Subtract 8</td>
<td>-</td>
</tr>
<tr>
<td>USA8</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Sum of Absolute Differences</td>
<td>-</td>
</tr>
<tr>
<td>USADA8</td>
<td>(Rd,) Rn, Rm, Ra</td>
<td>Unsigned Sum of Absolute Differences and Accumulate</td>
<td>-</td>
</tr>
<tr>
<td>USAT</td>
<td>Rd, #n, Rm {,shift #s}</td>
<td>Unsigned Saturate</td>
<td>Q</td>
</tr>
<tr>
<td>USAT16</td>
<td>Rd, #n, Rm</td>
<td>Unsigned Saturate 16</td>
<td>Q</td>
</tr>
<tr>
<td>USAX</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Subtract and add with Exchange</td>
<td>GE</td>
</tr>
<tr>
<td>USUB16</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Subtract 16</td>
<td>GE</td>
</tr>
<tr>
<td>USUB8</td>
<td>(Rd,) Rn, Rm</td>
<td>Unsigned Subtract 8</td>
<td>GE</td>
</tr>
<tr>
<td>UXTAB</td>
<td>(Rd,) Rn, Rm, {,ROR #}</td>
<td>Rotate, extend 8 bits to 32 and Add</td>
<td>-</td>
</tr>
<tr>
<td>UXTAB16</td>
<td>(Rd,) Rn, Rm, {,ROR #}</td>
<td>Rotate, dual extend 8 bits to 16 and Add</td>
<td>-</td>
</tr>
<tr>
<td>UXTAH</td>
<td>(Rd,) Rn, Rm, {,ROR #}</td>
<td>Rotate, unsigned extend and Add Halfword</td>
<td>-</td>
</tr>
<tr>
<td>UXTB</td>
<td>(Rd,) Rm, {,ROR #n}</td>
<td>Zero extend a Byte</td>
<td>-</td>
</tr>
<tr>
<td>UXTB16</td>
<td>(Rd,) Rm, {,ROR #n}</td>
<td>Unsigned Extend Byte 16</td>
<td>-</td>
</tr>
<tr>
<td>UXTBH</td>
<td>(Rd,) Rm, {,ROR #n}</td>
<td>Zero extend a Halfword</td>
<td>-</td>
</tr>
<tr>
<td>VABS.F32</td>
<td>Sd, Sm</td>
<td>Floating-point Absolute</td>
<td>-</td>
</tr>
<tr>
<td>VADD.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Add</td>
<td>-</td>
</tr>
<tr>
<td>VCMPE.F32</td>
<td>Sd, &lt;Sm</td>
<td>#0.0&gt;</td>
<td>Compare two floating-point registers, or one floating-point register and zero</td>
</tr>
<tr>
<td>VCMPE.F32</td>
<td>Sd, &lt;Sm</td>
<td>#0.0&gt;</td>
<td>Compare two floating-point registers, or one floating-point register and zero with Invalid Operation check</td>
</tr>
<tr>
<td>VCVT.S32.F32</td>
<td>Sd, Sm</td>
<td>Convert between floating-point and integer</td>
<td>-</td>
</tr>
<tr>
<td>VCVT.S16.F32</td>
<td>Sd, Sd, #fbits</td>
<td>Convert between floating-point and fixed point</td>
<td>-</td>
</tr>
<tr>
<td>VCVTR.S32.F32</td>
<td>Sd, Sm</td>
<td>Convert between floating-point and integer with rounding</td>
<td>-</td>
</tr>
<tr>
<td>VCVT&lt;:B</td>
<td>H&gt;.F32.F16</td>
<td>Sd, Sm</td>
<td>Converts half-precision value to single-precision</td>
</tr>
<tr>
<td>VCVT&lt;T:B</td>
<td>T&gt;.F32.F16</td>
<td>Sd, Sm</td>
<td>Converts single-precision register to half-precision</td>
</tr>
<tr>
<td>VDIV.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Divide</td>
<td>-</td>
</tr>
<tr>
<td>VFMA.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Fused Multiply Accumulate</td>
<td>-</td>
</tr>
</tbody>
</table>
Table 2-13. Cortex-M4F Instruction Summary (continued)

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Operands</th>
<th>Brief Description</th>
<th>Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>VFNMA.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Fused Negate Multiply Accumulate</td>
<td>-</td>
</tr>
<tr>
<td>VFMS.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Fused Multiply Subtract</td>
<td>-</td>
</tr>
<tr>
<td>VFNMS.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Fused Negate Multiply Subtract</td>
<td>-</td>
</tr>
<tr>
<td>VLDM.F&lt;32</td>
<td>64&gt;</td>
<td>Rn[]!, list</td>
<td>Load Multiple extension registers</td>
</tr>
<tr>
<td>VLDR.F&lt;32</td>
<td>64&gt;</td>
<td>&lt;Dd</td>
<td>Sd&gt;, [Rn]</td>
</tr>
<tr>
<td>VLM.A.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Multiply Accumulate</td>
<td>-</td>
</tr>
<tr>
<td>VLM.S.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Multiply Subtract</td>
<td>-</td>
</tr>
<tr>
<td>VMOV.F32</td>
<td>Sd, #imm</td>
<td>Floating-point Move immediate</td>
<td>-</td>
</tr>
<tr>
<td>VMV</td>
<td>Sd, Sm</td>
<td>Floating-point Move register</td>
<td>-</td>
</tr>
<tr>
<td>VMV</td>
<td>Sn, Rt</td>
<td>Copy ARM core register to single precision</td>
<td>-</td>
</tr>
<tr>
<td>VMV</td>
<td>Sm, Sm1, Rt, Rt2</td>
<td>Copy 2 ARM core registers to 2 single precision</td>
<td>-</td>
</tr>
<tr>
<td>VMV</td>
<td>Dd[x], Rt</td>
<td>Copy ARM core register to scalar</td>
<td>-</td>
</tr>
<tr>
<td>VMV</td>
<td>Rt, Dn[x]</td>
<td>Copy scalar to ARM core register</td>
<td>-</td>
</tr>
<tr>
<td>VMRS</td>
<td>Rt, FPSCR</td>
<td>Move FPSCR to ARM core register or APSCR</td>
<td>N,Z,C,V</td>
</tr>
<tr>
<td>VMSR</td>
<td>FPSCR, Rt</td>
<td>Move to FPSCR from ARM Core register</td>
<td>FPSCR</td>
</tr>
<tr>
<td>VMUL.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Multiply</td>
<td>-</td>
</tr>
<tr>
<td>VNEG.F32</td>
<td>Sd, Sm</td>
<td>Floating-point Negate</td>
<td>-</td>
</tr>
<tr>
<td>VNMLA.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Multiply and Add</td>
<td>-</td>
</tr>
<tr>
<td>VNMLS.F32</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Multiply and Subtract</td>
<td>-</td>
</tr>
<tr>
<td>VNMUL</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Multiply</td>
<td>-</td>
</tr>
<tr>
<td>VPOP</td>
<td>list</td>
<td>Pop extension registers</td>
<td>-</td>
</tr>
<tr>
<td>VPOUSH</td>
<td>list</td>
<td>Push extension registers</td>
<td>-</td>
</tr>
<tr>
<td>VSQRT.F32</td>
<td>Sd, Sm</td>
<td>Calculates floating-point Square Root</td>
<td>-</td>
</tr>
<tr>
<td>VSTM</td>
<td>Rn[]!, list</td>
<td>Floating-point register Store Multiple</td>
<td>-</td>
</tr>
<tr>
<td>VSTR.F&lt;32</td>
<td>64&gt;</td>
<td>Sd, [Rn]</td>
<td>Stores an extension register to memory</td>
</tr>
<tr>
<td>VSUB.F&lt;32</td>
<td>64&gt;</td>
<td>(Sd,) Sn, Sm</td>
<td>Floating-point Subtract</td>
</tr>
<tr>
<td>WFE</td>
<td>-</td>
<td>Wait for event</td>
<td>-</td>
</tr>
<tr>
<td>WFI</td>
<td>-</td>
<td>Wait for interrupt</td>
<td>-</td>
</tr>
</tbody>
</table>
3 Cortex-M4 Peripherals

This chapter provides information on the Tiva™ C Series implementation of the Cortex-M4 processor peripherals, including:

- **SysTick (see page 123)**
  Provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism.

- **Nested Vectored Interrupt Controller (NVIC) (see page 124)**
  - Facilitates low-latency exception and interrupt handling
  - Controls power management
  - Implements system control registers

- **System Control Block (SCB) (see page 125)**
  Provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

- **Memory Protection Unit (MPU) (see page 125)**
  Supports the standard ARMv7 Protected Memory System Architecture (PMSA) model. The MPU provides full support for protection regions, overlapping protection regions, access permissions, and exporting memory attributes to the system.

- **Floating-Point Unit (FPU) (see page 130)**
  Fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

Table 3-1 on page 122 shows the address map of the Private Peripheral Bus (PPB). Some peripheral register regions are split into two address regions, as indicated by two addresses listed.

**Table 3-1. Core Peripheral Register Regions**

<table>
<thead>
<tr>
<th>Address</th>
<th>Core Peripheral</th>
<th>Description (see page ...)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000.E010-0xE000.E01F</td>
<td>System Timer</td>
<td>123</td>
</tr>
<tr>
<td>0xE000.E100-0xE000.E4EF</td>
<td>Nested Vectored Interrupt Controller</td>
<td>124</td>
</tr>
<tr>
<td>0xE000.EF00-0xE000.EF03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xE000.E008-0xE000.E00F</td>
<td>System Control Block</td>
<td>125</td>
</tr>
<tr>
<td>0xE000.ED00-0xE000.ED3F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xE000.ED90-0xE000.EDB8</td>
<td>Memory Protection Unit</td>
<td>125</td>
</tr>
<tr>
<td>0xE000.EF30-0xE000.EF44</td>
<td>Floating Point Unit</td>
<td>130</td>
</tr>
</tbody>
</table>

3.1 Functional Description

This chapter provides information on the Tiva™ C Series implementation of the Cortex-M4 processor peripherals: SysTick, NVIC, SCB, MPU, FPU.
3.1.1 System Timer (SysTick)

Cortex-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example as:

- An RTOS tick timer that fires at a programmable rate (for example, 100 Hz) and invokes a SysTick routine.
- A high-speed alarm timer using the system clock.
- A variable rate alarm or signal timer—the duration is range-dependent on the reference clock used and the dynamic range of the counter.
- A simple counter used to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNT bit in the STCTRL control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

The timer consists of three registers:

- **SysTick Control and Status (STCTRL):** A control and status counter to configure its clock, enable the counter, enable the SysTick interrupt, and determine counter status.

- **SysTick Reload Value (STRELOAD):** The reload value for the counter, used to provide the counter's wrap value.

- **SysTick Current Value (STCURRENT):** The current value of the counter.

When enabled, the timer counts down on each clock from the reload value to zero, reloads (wraps) to the value in the STRELOAD register on the next clock edge, then decrements on subsequent clocks. Clearing the STRELOAD register disables the counter on the next wrap. When the counter reaches zero, the COUNT status bit is set. The COUNT bit clears on reads.

Writing to the STCURRENT register clears the register and the COUNT status bit. The write does not trigger the SysTick exception logic. On a read, the current value is the value of the register at the time the register is accessed.

The SysTick counter runs on either the system clock or the precision internal oscillator (PIOSC) divided by 4. If this clock signal is stopped for low power mode, the SysTick counter stops. SysTick can be kept running during Deep-sleep mode by setting the CLK_SRC bit in the SysTick Control and Status Register (STCTRL) register and ensuring that the PIOSCPD bit in the Deep Sleep Clock Configuration (DSLPCLKCFG) register is clear. Ensure software uses aligned word accesses to access the SysTick registers.

The SysTick counter reload and current value are undefined at reset; the correct initialization sequence for the SysTick counter is:

1. Program the value in the STRELOAD register.
2. Clear the STCURRENT register by writing to it with any value.
3. Configure the STCTRL register for the required operation.

**Note:** When the processor is halted for debugging, the counter does not decrement.
3.1.2 Nested Vectored Interrupt Controller (NVIC)

This section describes the Nested Vectored Interrupt Controller (NVIC) and the registers it uses. The NVIC supports:

- 85 interrupts.
- A programmable priority level of 0-7 for each interrupt. A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Low-latency exception and interrupt handling.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non-maskable interrupt (NMI).

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead, providing low latency exception handling.

3.1.2.1 Level-Sensitive and Pulse Interrupts

The processor supports both level-sensitive and pulse interrupts. Pulse interrupts are also described as edge-triggered interrupts.

A level-sensitive interrupt is held asserted until the peripheral deasserts the interrupt signal. Typically this happens because the ISR accesses the peripheral, causing it to clear the interrupt request. A pulse interrupt is an interrupt signal sampled synchronously on the rising edge of the processor clock. To ensure the NVIC detects the interrupt, the peripheral must assert the interrupt signal for at least one clock cycle, during which the NVIC detects the pulse and latches the interrupt.

When the processor enters the ISR, it automatically removes the pending state from the interrupt (see “Hardware and Software Control of Interrupts” on page 124 for more information). For a level-sensitive interrupt, if the signal is not deasserted before the processor returns from the ISR, the interrupt becomes pending again, and the processor must execute its ISR again. As a result, the peripheral can hold the interrupt signal asserted until it no longer needs servicing.

3.1.2.2 Hardware and Software Control of Interrupts

The Cortex-M4 latches all interrupts. A peripheral interrupt becomes pending for one of the following reasons:

- The NVIC detects that the interrupt signal is High and the interrupt is not active.
- The NVIC detects a rising edge on the interrupt signal.

- Software writes to the corresponding interrupt set-pending register bit, or to the Software Trigger Interrupt (SWTRIG) register to make a Software-Generated Interrupt pending. See the INT bit in the PEND0 register on page 146 or SWTRIG on page 156.

A pending interrupt remains pending until one of the following:
The processor enters the ISR for the interrupt, changing the state of the interrupt from pending to active. Then:

- For a level-sensitive interrupt, when the processor returns from the ISR, the NVIC samples the interrupt signal. If the signal is asserted, the state of the interrupt changes to pending, which might cause the processor to immediately re-enter the ISR. Otherwise, the state of the interrupt changes to inactive.

- For a pulse interrupt, the NVIC continues to monitor the interrupt signal, and if this is pulsed the state of the interrupt changes to pending and active. In this case, when the processor returns from the ISR the state of the interrupt changes to pending, which might cause the processor to immediately re-enter the ISR.

If the interrupt signal is not pulsed while the processor is in the ISR, when the processor returns from the ISR the state of the interrupt changes to inactive.

Software writes to the corresponding interrupt clear-pending register bit

- For a level-sensitive interrupt, if the interrupt signal is still asserted, the state of the interrupt does not change. Otherwise, the state of the interrupt changes to inactive.

- For a pulse interrupt, the state of the interrupt changes to inactive, if the state was pending or to active, if the state was active and pending.

### 3.1.3 System Control Block (SCB)

The System Control Block (SCB) provides system implementation information and system control, including configuration, control, and reporting of the system exceptions.

### 3.1.4 Memory Protection Unit (MPU)

This section describes the Memory protection unit (MPU). The MPU divides the memory map into a number of regions and defines the location, size, access permissions, and memory attributes of each region. The MPU supports independent attribute settings for each region, overlapping regions, and export of memory attributes to the system.

The memory attributes affect the behavior of memory accesses to the region. The Cortex-M4 MPU defines eight separate memory regions, 0-7, and a background region.

When memory regions overlap, a memory access is affected by the attributes of the region with the highest number. For example, the attributes for region 7 take precedence over the attributes of any region that overlaps region 7.

The background region has the same memory access attributes as the default memory map, but is accessible from privileged software only.

The Cortex-M4 MPU memory map is unified, meaning that instruction accesses and data accesses have the same region settings.

If a program accesses a memory location that is prohibited by the MPU, the processor generates a memory management fault, causing a fault exception and possibly causing termination of the process in an OS environment. In an OS environment, the kernel can update the MPU region setting dynamically based on the process to be executed. Typically, an embedded OS uses the MPU for memory protection.

Configuration of MPU regions is based on memory types (see "Memory Regions, Types and Attributes" on page 95 for more information).
Table 3-2 on page 126 shows the possible MPU region attributes. See the section called “MPU Configuration for a Tiva™ C Series Microcontroller” on page 130 for guidelines for programming a microcontroller implementation.

### Table 3-2. Memory Attributes Summary

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strongly Ordered</td>
<td>All accesses to Strongly Ordered memory occur in program order.</td>
</tr>
<tr>
<td>Device</td>
<td>Memory-mapped peripherals</td>
</tr>
<tr>
<td>Normal</td>
<td>Normal memory</td>
</tr>
</tbody>
</table>

To avoid unexpected behavior, disable the interrupts before updating the attributes of a region that the interrupt handlers might access.

Ensure software uses aligned accesses of the correct size to access MPU registers:

- Except for the MPU Region Attribute and Size (MPUATTR) register, all MPU registers must be accessed with aligned word accesses.
- The MPUATTR register can be accessed with byte or aligned halfword or word accesses.

The processor does not support unaligned accesses to MPU registers.

When setting up the MPU, and if the MPU has previously been programmed, disable unused regions to prevent any previous region settings from affecting the new MPU setup.

#### 3.1.4.1 Updating an MPU Region

To update the attributes for an MPU region, the MPU Region Number (MPUNUMBER), MPU Region Base Address (MPUBASE) and MPUATTR registers must be updated. Each register can be programmed separately or with a multiple-word write to program all of these registers. You can use the MPUBASEx and MPUATTRx aliases to program up to four regions simultaneously using an STM instruction.

**Updating an MPU Region Using Separate Words**

This example simple code configures one region:

```asm
; R1 = region number
; R2 = size/enable
; R3 = attributes
; R4 = address
LDR R0,=MPUNUMBER        ; 0xE000ED98, MPU region number register
STR R1, [R0, #0x0]       ; Region Number
STR R4, [R0, #0x4]       ; Region Base Address
STRH R2, [R0, #0x8]      ; Region Size and Enable
STRH R3, [R0, #0xA]      ; Region Attribute
```

Disable a region before writing new region settings to the MPU if you have previously enabled the region being changed. For example:

```asm
; R1 = region number
; R2 = size/enable
; R3 = attributes
; R4 = address
LDR R0,=MPUNUMBER        ; 0xE000ED98, MPU region number register
```
软件必须使用内存屏障指令:

- 在 MPU 设置之前，如果有未完成的内存转移，如缓冲写入，这些转移可能会受到 MPU 设置变化的影响。
- 在 MPU 设置之后，如果包括必须使用新 MPU 设置的内存转移。

然而，如果 MPU 设置过程开始于进入异常处理程序或异常返回，因为异常处理和异常返回机制会导致内存屏障行为，所以不需要使用内存屏障指令。

软件在 MPU 设置期间不需要任何内存屏障指令，因为它通过私有外围总线 (PPB) 访问 MPU，这是一个强序内存区域。

例如，如果所有的内存访问行为都被设计为在编程序列结束时立即生效，那么应使用 DSBr 指令和 ISBr 指令。DSBr 指令在改变 MPU 设置后，如在上下文切换结束时，是必需的。ISBr 指令在使用分支或调用的代码编程 MPU 区域或区域时是必需的。如果程序是通过异常返回或异常处理进入的，那么 ISBr 指令是不必需的。

**更新 MPU 区域使用多字写入**

MPU 可以直接使用多字写入来编程，这取决于信息是如何划分的。考虑以下重编程:

```assembly
LDR R0, =MPUNUMBER ; 0xE000ED98, MPU region number register
STR R1, [R0, #0x0] ; Region Number
STR R2, [R0, #0x4] ; Region Base Address
STR R3, [R0, #0x8] ; Region Attribute, Size and Enable
```

使用 STM 指令可以优化这个过程:

```assembly
LDR R0, =MPUNUMBER ; 0xE000ED98, MPU region number register
STM R0, {R1-R3} ; Region number, address, attribute, size and enable
```

此操作可以在两字中完成，这意味着 MPU Region Base Address (MPUBASE) 寄存器（见第 190 页）包含所需的区域编号，并且 VALID 标志已设置。此方法可以用于静态打包的数据，例如在引导加载器中。
; R1 = address and region number in one
; R2 = size and attributes in one
LDR R0, =MPUBASE ; 0xE000ED9C, MPU Region Base register
STR R1, [R0, #0x0] ; Region base address and region number combined
; with VALID (bit 4) set
STR R2, [R0, #0x4] ; Region Attribute, Size and Enable

**Subregions**

Regions of 256 bytes or more are divided into eight equal-sized subregions. Set the corresponding bit in the **SRD** field of the **MPU Region Attribute and Size (MPUATTR)** register (see page 192) to disable a subregion. The least-significant bit of the **SRD** field controls the first subregion, and the most-significant bit controls the last subregion. Disabling a subregion means another region overlapping the disabled range matches instead. If no other enabled region overlaps the disabled subregion, the MPU issues a fault.

Regions of 32, 64, and 128 bytes do not support subregions. With regions of these sizes, the **SRD** field must be configured to 0x00, otherwise the MPU behavior is unpredictable.

**Example of SRD Use**

Two regions with the same base address overlap. Region one is 128 KB, and region two is 512 KB. To ensure the attributes from region one apply to the first 128 KB region, configure the **SRD** field for region two to 0x03 to disable the first two subregions, as Figure 3-1 on page 128 shows.

**Figure 3-1. SRD Use Example**

![Figure 3-1. SRD Use Example](image)

**Base address of both regions**

<table>
<thead>
<tr>
<th>Region 2, with subregions</th>
<th>Offset from base address</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>512KB</td>
</tr>
<tr>
<td></td>
<td>448KB</td>
</tr>
<tr>
<td></td>
<td>384KB</td>
</tr>
<tr>
<td></td>
<td>320KB</td>
</tr>
<tr>
<td></td>
<td>256KB</td>
</tr>
<tr>
<td></td>
<td>192KB</td>
</tr>
<tr>
<td></td>
<td>128KB</td>
</tr>
<tr>
<td></td>
<td>64KB</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

**3.1.4.2 MPU Access Permission Attributes**

The access permission bits, **TEX**, **S**, **C**, **B**, **AP**, and **XN** of the **MPUATTR** register, control access to the corresponding memory region. If an access is made to an area of memory without the required permissions, then the MPU generates a permission fault.

Table 3-3 on page 128 shows the encodings for the **TEX**, **C**, **B**, and **S** access permission bits. All encodings are shown for completeness, however the current implementation of the Cortex-M4 does not support the concept of cacheability or shareability. Refer to the section called “MPU Configuration for a Tiva™ C Series Microcontroller” on page 130 for information on programming the MPU for TM4C123GH6PZ implementations.

**Table 3-3. TEX, S, C, and B Bit Field Encoding**

<table>
<thead>
<tr>
<th>TEX</th>
<th>S</th>
<th>C</th>
<th>B</th>
<th>Memory Type</th>
<th>Shareability</th>
<th>Other Attributes</th>
</tr>
</thead>
<tbody>
<tr>
<td>000b</td>
<td>x²</td>
<td>0</td>
<td>0</td>
<td>Strongly Ordered</td>
<td>Shareable</td>
<td>-</td>
</tr>
<tr>
<td>000</td>
<td>x³</td>
<td>0</td>
<td>1</td>
<td>Device</td>
<td>Shareable</td>
<td>-</td>
</tr>
</tbody>
</table>
Table 3-3. TEX, S, C, and B Bit Field Encoding (continued)

<table>
<thead>
<tr>
<th>TEX</th>
<th>S</th>
<th>C</th>
<th>B</th>
<th>Memory Type</th>
<th>Shareability</th>
<th>Other Attributes</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Normal</td>
<td>Not shareable</td>
<td>Outer and inner write-through. No write allocate.</td>
</tr>
<tr>
<td>000</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Normal</td>
<td>Shareable</td>
<td>Outer and inner non-cacheable.</td>
</tr>
<tr>
<td>000</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Normal</td>
<td>Not shareable</td>
<td>Outer and inner non-cacheable.</td>
</tr>
<tr>
<td>000</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Normal</td>
<td>Shareable</td>
<td>Outer and inner non-cacheable.</td>
</tr>
<tr>
<td>001</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Normal</td>
<td>Not shareable</td>
<td>Outer and inner non-cacheable.</td>
</tr>
<tr>
<td>001</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Normal</td>
<td>Shareable</td>
<td>Outer and inner non-cacheable.</td>
</tr>
<tr>
<td>001</td>
<td>x²</td>
<td>0</td>
<td>1</td>
<td>Reserved encoding</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>001</td>
<td>x²</td>
<td>1</td>
<td>0</td>
<td>Reserved encoding</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>001</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Normal</td>
<td>Not shareable</td>
<td>Outer and inner non-cacheable.</td>
</tr>
<tr>
<td>001</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Normal</td>
<td>Shareable</td>
<td>Outer and inner non-cacheable.</td>
</tr>
<tr>
<td>010</td>
<td>x²</td>
<td>0</td>
<td>0</td>
<td>Device</td>
<td>Not shareable</td>
<td>Nonshared Device.</td>
</tr>
<tr>
<td>010</td>
<td>x²</td>
<td>0</td>
<td>1</td>
<td>Reserved encoding</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>010</td>
<td>x²</td>
<td>1</td>
<td>x²</td>
<td>Reserved encoding</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1BB</td>
<td>0</td>
<td>A</td>
<td>A</td>
<td>Normal</td>
<td>Not shareable</td>
<td>Cached memory (BB = outer policy, AA = inner policy). See Table 3-4 for the encoding of the AA and BB bits.</td>
</tr>
<tr>
<td>1BB</td>
<td>1</td>
<td>A</td>
<td>A</td>
<td>Normal</td>
<td>Shareable</td>
<td>Cached memory (BB = outer policy, AA = inner policy). See Table 3-4 for the encoding of the AA and BB bits.</td>
</tr>
</tbody>
</table>

a. The MPU ignores the value of this bit.

Table 3-4 on page 129 shows the cache policy for memory attribute encodings with a TEX value in the range of 0x4-0x7.

Table 3-4. Cache Policy for Memory Attribute Encoding

<table>
<thead>
<tr>
<th>Encoding, AA or BB</th>
<th>Corresponding Cache Policy</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Non-cacheable</td>
</tr>
<tr>
<td>01</td>
<td>Write back, write and read allocate</td>
</tr>
<tr>
<td>10</td>
<td>Write through, no write allocate</td>
</tr>
<tr>
<td>11</td>
<td>Write back, no write allocate</td>
</tr>
</tbody>
</table>

Table 3-5 on page 129 shows the AP encodings in the MPUATTR register that define the access permissions for privileged and unprivileged software.

Table 3-5. AP Bit Field Encoding

<table>
<thead>
<tr>
<th>AP Bit Field</th>
<th>Privileged Permissions</th>
<th>Unprivileged Permissions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>No access</td>
<td>No access</td>
<td>All accesses generate a permission fault.</td>
</tr>
<tr>
<td>001</td>
<td>RW</td>
<td>No access</td>
<td>Access from privileged software only.</td>
</tr>
<tr>
<td>010</td>
<td>RW</td>
<td>RO</td>
<td>Writes by unprivileged software generate a permission fault.</td>
</tr>
<tr>
<td>011</td>
<td>RW</td>
<td>RW</td>
<td>Full access.</td>
</tr>
<tr>
<td>100</td>
<td>Unpredictable</td>
<td>Unpredictable</td>
<td>Reserved.</td>
</tr>
<tr>
<td>101</td>
<td>RO</td>
<td>No access</td>
<td>Reads by privileged software only.</td>
</tr>
</tbody>
</table>
### Table 3-5. AP Bit Field Encoding (continued)

<table>
<thead>
<tr>
<th>AP Bit Field</th>
<th>Privileged Permissions</th>
<th>Unprivileged Permissions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>110</td>
<td>RO</td>
<td>RO</td>
<td>Read-only, by privileged or unprivileged software.</td>
</tr>
<tr>
<td>111</td>
<td>RO</td>
<td>RO</td>
<td>Read-only, by privileged or unprivileged software.</td>
</tr>
</tbody>
</table>

### MPU Configuration for a Tiva™ C Series Microcontroller

Tiva™ C Series microcontrollers have only a single processor and no caches. As a result, the MPU should be programmed as shown in Table 3-6 on page 130.

### Table 3-6. Memory Region Attributes for Tiva™ C Series Microcontrollers

<table>
<thead>
<tr>
<th>Memory Region</th>
<th>TEX</th>
<th>B</th>
<th>C</th>
<th>S</th>
<th>Memory Type and Attributes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash memory</td>
<td>000b</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Normal memory, non-shareable, write-through</td>
</tr>
<tr>
<td>Internal SRAM</td>
<td>000b</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>Normal memory, shareable, write-through</td>
</tr>
<tr>
<td>External SRAM</td>
<td>000b</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Normal memory, shareable, write-back, write-allocate</td>
</tr>
<tr>
<td>Peripherals</td>
<td>000b</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Device memory, shareable</td>
</tr>
</tbody>
</table>

In current Tiva™ C Series microcontroller implementations, the shareability and cache policy attributes do not affect the system behavior. However, using these settings for the MPU regions can make the application code more portable. The values given are for typical situations.

#### 3.1.4.3 MPU Mismatch

When an access violates the MPU permissions, the processor generates a memory management fault (see “Exceptions and Interrupts” on page 92 for more information). The **MFAULTSTAT** register indicates the cause of the fault. See page 177 for more information.

#### 3.1.5 Floating-Point Unit (FPU)

This section describes the Floating-Point Unit (FPU) and the registers it uses. The FPU provides:

- 32-bit instructions for single-precision (C float) data-processing operations
- Combined multiply and accumulate instructions for increased precision (Fused MAC)
- Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
- Hardware support for denormals and all IEEE rounding modes
- 32 dedicated 32-bit single-precision registers, also addressable as 16 double-word registers
- Decoupled three stage pipeline

The Cortex-M4F FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions. The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard. The FPU’s single-precision extension registers can also be accessed as 16 doubleword registers for load, store, and move operations.
3.1.5.1 FPU Views of the Register Bank

The FPU provides an extension register file containing 32 single-precision registers. These can be viewed as:

- Sixteen 64-bit doubleword registers, D0-D15
- Thirty-two 32-bit single-word registers, S0-S31
- A combination of registers from the above views

**Figure 3-2. FPU Register Bank**

The mapping between the registers is as follows:

- S<2n> maps to the least significant half of D<n>
- S<2n+1> maps to the most significant half of D<n>

For example, you can access the least significant half of the value in D6 by accessing S12, and the most significant half of the elements by accessing S13.

3.1.5.2 Modes of Operation

The FPU provides three modes of operation to accommodate a variety of applications.

**Full-Compliance mode.** In Full-Compliance mode, the FPU processes all operations according to the IEEE 754 standard in hardware.

**Flush-to-Zero mode.** Setting the FZ bit of the Floating-Point Status and Control (FPSC) register enables Flush-to-Zero mode. In this mode, the FPU treats all subnormal input operands of arithmetic CDP operations as zeros in the operation. Exceptions that result from a zero operand are signalled appropriately. VABS, VNEG, and VMOV are not considered arithmetic CDP operations and are not affected by Flush-to-Zero mode. A result that is tiny, as described in the IEEE 754 standard, where the destination precision is smaller in magnitude than the minimum normal value before rounding, is replaced with a zero. The IDC bit in FPSC indicates when an input flush occurs. The UFC bit in FPSC indicates when a result flush occurs.

**Default NaN mode.** Setting the DN bit in the FPSC register enables default NaN mode. In this mode, the result of any arithmetic data processing operation that involves an input NaN, or that generates a NaN result, returns the default NaN. Propagation of the fraction bits is maintained only by VABS,
VNEG, and VMOV operations. All other CDP operations ignore any information in the fraction bits of an input NaN.

3.1.5.3 Compliance with the IEEE 754 standard

When Default NaN (DN) and Flush-to-Zero (FZ) modes are disabled, FPv4 functionality is compliant with the IEEE 754 standard in hardware. No support code is required to achieve this compliance.

3.1.5.4 Complete Implementation of the IEEE 754 standard

The Cortex-M4F floating point instruction set does not support all operations defined in the IEEE 754-2008 standard. Unsupported operations include, but are not limited to the following:

- Remainder
- Round floating-point number to integer-valued floating-point number
- Binary-to-decimal conversions
- Decimal-to-binary conversions
- Direct comparison of single-precision and double-precision values

The Cortex-M4 FPU supports fused MAC operations as described in the IEEE standard. For complete implementation of the IEEE 754-2008 standard, floating-point functionality must be augmented with library functions.

3.1.5.5 IEEE 754 standard implementation choices

**NaN handling**

All single-precision values with the maximum exponent field value and a nonzero fraction field are valid NaNs. A most-significant fraction bit of zero indicates a Signaling NaN (SNaN). A one indicates a Quiet NaN (QNaN). Two NaN values are treated as different NaNs if they differ in any bit. The below table shows the default NaN values.

<table>
<thead>
<tr>
<th>Sign</th>
<th>Fraction</th>
<th>Fraction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0xFF</td>
<td>bit [22] = 1, bits [21:0] are all zeros</td>
</tr>
</tbody>
</table>

Processing of input NaNs for ARM floating-point functionality and libraries is defined as follows:

- In full-compliance mode, NaNs are handled as described in the ARM Architecture Reference Manual. The hardware processes the NaNs directly for arithmetic CDP instructions. For data transfer operations, NaNs are transferred without raising the Invalid Operation exception. For the non-arithmetic CDP instructions, VABS, VNEG, and VMOV, NaNs are copied, with a change of sign if specified in the instructions, without causing the Invalid Operation exception.

- In default NaN mode, arithmetic CDP instructions involving NaN operands return the default NaN regardless of the fractions of any NaN operands. SNaNs in an arithmetic CDP operation set the IOC flag, FPSCR[0]. NaN handling by data transfer and non-arithmetic CDP instructions is the same as in full-compliance mode.
Table 3-7. QNaN and SNaN Handling

<table>
<thead>
<tr>
<th>Instruction Type</th>
<th>Default NaN Mode</th>
<th>With QNaN Operand</th>
<th>With SNaN Operand</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arithmetic CDP</td>
<td>Off</td>
<td>The QNaN or one of the QNaN operands, if there is more than one, is returned according to the rules given in the ARM Architecture Reference Manual.</td>
<td>IOC(^a) set. The SNaN is quieted and the result NaN is determined by the rules given in the ARM Architecture Reference Manual.</td>
</tr>
<tr>
<td></td>
<td>On</td>
<td>Default NaN returns.</td>
<td>IOC(^a) set. Default NaN returns.</td>
</tr>
<tr>
<td>Non-arithmetic CDP</td>
<td>Off/On</td>
<td>NaN passes to destination with sign changed as appropriate.</td>
<td></td>
</tr>
<tr>
<td>FCMP(Z)</td>
<td>-</td>
<td>Unordered compare.</td>
<td>IOC set. Unordered compare.</td>
</tr>
<tr>
<td>Load/store</td>
<td>Off/On</td>
<td>All NaNs transferred.</td>
<td></td>
</tr>
</tbody>
</table>

\(^a\) IOC is the Invalid Operation exception flag, FPSCR[0].

Comparison results modify the flags in the FPSCR. You can use the MVRS APSR, nzcv instruction (formerly FMSTAT) to transfer the current flags from the FPSCR to the APSR. See the ARM Architecture Reference Manual for mapping of IEEE 754-2008 standard predicates to ARM conditions. The flags used are chosen so that subsequent conditional execution of ARM instructions can test the predicates defined in the IEEE standard.

Underflow

The Cortex-M4F FPU uses the before rounding form of tininess and the inexact result form of loss of accuracy as described in the IEEE 754-2008 standard to generate Underflow exceptions.

In flush-to-zero mode, results that are tiny before rounding, as described in the IEEE standard, are flushed to a zero, and the UFC flag, FPSCR[3], is set. See the ARM Architecture Reference Manual for information on flush-to-zero mode.

When the FPU is not in flush-to-zero mode, operations are performed on subnormal operands. If the operation does not produce a tiny result, it returns the computed result, and the UFC flag, FPSCR[3], is not set. The IXC flag, FPSCR[4], is set if the operation is inexact. If the operation produces a tiny result, the result is a subnormal or zero value, and the UFC flag, FPSCR[3], is set if the result was also inexact.

3.1.5.6 Exceptions

The FPU sets the cumulative exception status flag in the FPSCR register as required for each instruction, in accordance with the FPv4 architecture. The FPU does not support user-mode traps. The exception enable bits in the FPSCR read-as-zero, and writes are ignored. The processor also has six output pins, FPIXC, FPUFC, FPOFC, FPDZC, FPIDC, and FPIOC, that each reflect the status of one of the cumulative exception flags. For a description of these outputs, see the ARM Cortex-M4 Integration and Implementation Manual (ARM DII 0239, available from ARM).

The processor can reduce the exception latency by using lazy stacking. See Auxiliary Control Register, ACTLR on page 4-5. This means that the processor reserves space on the stack for the FP state, but does not save that state information to the stack. See the ARMv7-M Architecture Reference Manual (available from ARM) for more information.

3.1.5.7 Enabling the FPU

The FPU is disabled from reset. You must enable it before you can use any floating-point instructions. The processor must be in privileged mode to read from and write to the Coprocessor Access.
Control (CPAC) register. The below example code sequence enables the FPU in both privileged and user modes.

```assembly
; CPACR is located at address 0xE000ED88
LDR.W R0, =0xE000ED88
; Read CPACR
LDR R1, [R0]
; Set bits 20-23 to enable CP10 and CP11 coprocessors
ORR R1, R1, #(0xF << 20)
; Write back the modified value to the CPACR
STR R1, [R0]; wait for store to complete
DSB
; reset pipeline now the FPU is enabled
ISB
```

### 3.2 Register Map

Table 3-8 on page 134 lists the Cortex-M4 Peripheral SysTick, NVIC, MPU, FPU and SCB registers. The offset listed is a hexadecimal increment to the register's address, relative to the Core Peripherals base address of 0xE000.E000.

**Note:** Register spaces that are not used are reserved for future or internal use. Software should not modify any reserved memory address.

#### Table 3-8. Peripherals Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x010</td>
<td>STCTRL</td>
<td>RW</td>
<td>0x0000.0004</td>
<td>SysTick Control and Status Register</td>
<td>138</td>
</tr>
<tr>
<td>0x014</td>
<td>STRELOAD</td>
<td>RW</td>
<td>-</td>
<td>SysTick Reload Value Register</td>
<td>140</td>
</tr>
<tr>
<td>0x018</td>
<td>STCURRENT</td>
<td>RWC</td>
<td>-</td>
<td>SysTick Current Value Register</td>
<td>141</td>
</tr>
<tr>
<td>0x100</td>
<td>EN0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 0-31 Set Enable</td>
<td>142</td>
</tr>
<tr>
<td>0x104</td>
<td>EN1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 32-63 Set Enable</td>
<td>142</td>
</tr>
<tr>
<td>0x108</td>
<td>EN2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 64-95 Set Enable</td>
<td>142</td>
</tr>
<tr>
<td>0x10C</td>
<td>EN3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 96-127 Set Enable</td>
<td>142</td>
</tr>
<tr>
<td>0x110</td>
<td>EN4</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 128-138 Set Enable</td>
<td>143</td>
</tr>
<tr>
<td>0x180</td>
<td>DIS0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 0-31 Clear Enable</td>
<td>144</td>
</tr>
<tr>
<td>0x184</td>
<td>DIS1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 32-63 Clear Enable</td>
<td>144</td>
</tr>
<tr>
<td>0x188</td>
<td>DIS2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 64-95 Clear Enable</td>
<td>144</td>
</tr>
<tr>
<td>0x18C</td>
<td>DIS3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 96-127 Clear Enable</td>
<td>144</td>
</tr>
<tr>
<td>0x190</td>
<td>DIS4</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 128-138 Clear Enable</td>
<td>145</td>
</tr>
<tr>
<td>0x200</td>
<td>PEND0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 0-31 Set Pending</td>
<td>146</td>
</tr>
<tr>
<td>0x204</td>
<td>PEND1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 32-63 Set Pending</td>
<td>146</td>
</tr>
</tbody>
</table>
## Table 3-8. Peripherals Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x208</td>
<td>PEND2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 64-95 Set Pending</td>
<td>146</td>
</tr>
<tr>
<td>0x20C</td>
<td>PEND3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 96-127 Set Pending</td>
<td>146</td>
</tr>
<tr>
<td>0x210</td>
<td>PEND4</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 128-138 Set Pending</td>
<td>147</td>
</tr>
<tr>
<td>0x280</td>
<td>UNPEND0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 0-31 Clear Pending</td>
<td>148</td>
</tr>
<tr>
<td>0x284</td>
<td>UNPEND1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 32-63 Clear Pending</td>
<td>148</td>
</tr>
<tr>
<td>0x288</td>
<td>UNPEND2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 64-95 Clear Pending</td>
<td>148</td>
</tr>
<tr>
<td>0x28C</td>
<td>UNPEND3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 96-127 Clear Pending</td>
<td>148</td>
</tr>
<tr>
<td>0x290</td>
<td>UNPEND4</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 128-138 Clear Pending</td>
<td>149</td>
</tr>
<tr>
<td>0x300</td>
<td>ACTIVE0</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Interrupt 0-31 Active Bit</td>
<td>150</td>
</tr>
<tr>
<td>0x304</td>
<td>ACTIVE1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Interrupt 32-63 Active Bit</td>
<td>150</td>
</tr>
<tr>
<td>0x308</td>
<td>ACTIVE2</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Interrupt 64-95 Active Bit</td>
<td>150</td>
</tr>
<tr>
<td>0x30C</td>
<td>ACTIVE3</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Interrupt 96-127 Active Bit</td>
<td>150</td>
</tr>
<tr>
<td>0x310</td>
<td>ACTIVE4</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Interrupt 128-138 Active Bit</td>
<td>151</td>
</tr>
<tr>
<td>0x400</td>
<td>PRI0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 0-3 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x404</td>
<td>PRI1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 4-7 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x408</td>
<td>PRI2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 8-11 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x40C</td>
<td>PRI3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 12-15 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x410</td>
<td>PRI4</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 16-19 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x414</td>
<td>PRI5</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 20-23 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x418</td>
<td>PRI6</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 24-27 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x41C</td>
<td>PRI7</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 28-31 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x420</td>
<td>PRI8</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 32-35 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x424</td>
<td>PRI9</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 36-39 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x428</td>
<td>PRI10</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 40-43 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x42C</td>
<td>PRI11</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 44-47 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x430</td>
<td>PRI12</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 48-51 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x434</td>
<td>PRI13</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 52-55 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x438</td>
<td>PRI14</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 56-59 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x43C</td>
<td>PRI15</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 60-63 Priority</td>
<td>152</td>
</tr>
<tr>
<td>0x440</td>
<td>PRI16</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 64-67 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x444</td>
<td>PRI17</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 68-71 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x448</td>
<td>PRI18</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 72-75 Priority</td>
<td>154</td>
</tr>
</tbody>
</table>
Table 3-8. Peripherals Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x44C</td>
<td>PRI19</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 76-79 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x450</td>
<td>PRI20</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 80-83 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x454</td>
<td>PRI21</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 84-87 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x458</td>
<td>PRI22</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 88-91 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x45C</td>
<td>PRI23</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 92-95 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x460</td>
<td>PRI24</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 96-99 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x464</td>
<td>PRI25</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 100-103 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x468</td>
<td>PRI26</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 104-107 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x46C</td>
<td>PRI27</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 108-111 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x470</td>
<td>PRI28</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 112-115 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x474</td>
<td>PRI29</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 116-119 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x478</td>
<td>PRI30</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 120-123 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x47C</td>
<td>PRI31</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 124-127 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x480</td>
<td>PRI32</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 128-131 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x484</td>
<td>PRI33</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 132-135 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0x488</td>
<td>PRI34</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt 136-138 Priority</td>
<td>154</td>
</tr>
<tr>
<td>0xF00</td>
<td>SWTRIG</td>
<td>WO</td>
<td>0x0000.0000</td>
<td>Software Trigger Interrupt</td>
<td>156</td>
</tr>
</tbody>
</table>

System Control Block (SCB) Registers

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x008</td>
<td>ACTLR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Auxiliary Control</td>
<td>157</td>
</tr>
<tr>
<td>0xD00</td>
<td>CPUID</td>
<td>RO</td>
<td>0x410F.C241</td>
<td>CPU ID Base</td>
<td>159</td>
</tr>
<tr>
<td>0xD04</td>
<td>INTCtrl</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt Control and State</td>
<td>160</td>
</tr>
<tr>
<td>0xD08</td>
<td>VTABLE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Vector Table Offset</td>
<td>163</td>
</tr>
<tr>
<td>0xD0C</td>
<td>APINT</td>
<td>RW</td>
<td>0xF0A5.0000</td>
<td>Application Interrupt and Reset Control</td>
<td>164</td>
</tr>
<tr>
<td>0xD10</td>
<td>SYSCTRL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>System Control</td>
<td>166</td>
</tr>
<tr>
<td>0xD14</td>
<td>CFGCTRL</td>
<td>RW</td>
<td>0x0000.0200</td>
<td>Configuration and Control</td>
<td>168</td>
</tr>
<tr>
<td>0xD18</td>
<td>SYSPRI1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>System Handler Priority 1</td>
<td>170</td>
</tr>
<tr>
<td>0xD1C</td>
<td>SYSPRI2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>System Handler Priority 2</td>
<td>171</td>
</tr>
<tr>
<td>0xD20</td>
<td>SYSPRI3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>System Handler Priority 3</td>
<td>172</td>
</tr>
<tr>
<td>0xD24</td>
<td>SYSHNDCTRL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>System Handler Control and State</td>
<td>173</td>
</tr>
<tr>
<td>0xD28</td>
<td>FAULTSTAT</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>Configurable Fault Status</td>
<td>177</td>
</tr>
<tr>
<td>0xD2C</td>
<td>HFAULTSTAT</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>Hard Fault Status</td>
<td>183</td>
</tr>
<tr>
<td>0xD34</td>
<td>MMADDR</td>
<td>RW</td>
<td>-</td>
<td>Memory Management Fault Address</td>
<td>184</td>
</tr>
</tbody>
</table>
### Table 3-8. Peripherals Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xD38</td>
<td>FAULTADDR</td>
<td>RW</td>
<td>-</td>
<td>Bus Fault Address</td>
<td>185</td>
</tr>
</tbody>
</table>

#### Memory Protection Unit (MPU) Registers

- **0xD90** MPUTYPE RO 0x0000.0800 MPU Type
- **0xD94** MPUCTRL RW 0x0000.0000 MPU Control
- **0xD98** MPUNUMBER RW 0x0000.0000 MPU Region Number
- **0xD9C** MPUBASE RW 0x0000.0000 MPU Region Base Address
- **0xDA0** MPUATTR RW 0x0000.0000 MPU Region Attribute and Size
- **0xDA4** MPUBASE1 RW 0x0000.0000 MPU Region Base Address Alias 1
- **0xDA8** MPUATTR1 RW 0x0000.0000 MPU Region Attribute and Size Alias 1
- **0xDB0** MPUATTR2 RW 0x0000.0000 MPU Region Attribute and Size Alias 2
- **0xDB4** MPUBASE3 RW 0x0000.0000 MPU Region Base Address Alias 3
- **0xDB8** MPUATTR3 RW 0x0000.0000 MPU Region Attribute and Size Alias 3

#### Floating-Point Unit (FPU) Registers

- **0xD88** CPAC RW 0x0000.0000 Coprocessor Access Control
- **0xF34** FPCC RW 0xC000.0000 Floating-Point Context Control
- **0xF38** FPCA RW - Floating-Point Context Address
- **0xF3C** FPDSC RW 0x0000.0000 Floating-Point Default Status Control

### 3.3 System Timer (SysTick) Register Descriptions

This section lists and describes the System Timer registers, in numerical order by address offset.
### Register 1: SysTick Control and Status Register (STCTRL), offset 0x010

**Note:** This register can only be accessed from privileged mode.

The SysTick **STCTRL** register enables the SysTick features.

#### SysTick Control and Status Register (STCTRL)

- **Base:** 0xE000.E000
- **Offset:** 0x010
- **Type:** RW, reset 0x0000.0004

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>COUNT</td>
<td>RO</td>
<td>0</td>
<td>Count Flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>15:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>CLK_SRC</td>
<td>RW</td>
<td>1</td>
<td>Clock Source</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

This bit is cleared by a read of the register or if the STCURRENT register is written with any value.

If read by the debugger using the DAP, this bit is cleared only if the MasterType bit in the AHB-AP Control Register is clear. Otherwise, the COUNT bit is not changed by the debugger read. See the ARM® Debug Interface V5 Architecture Specification for more information on MasterType.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INTEN</td>
<td>RW</td>
<td>0</td>
<td>Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>Value</td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>Interrupt generation is disabled. Software can use the COUNT bit to determine if the counter has ever reached 0.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>An interrupt is generated to the NVIC when SysTick counts to 0.</td>
</tr>
<tr>
<td>0</td>
<td>ENABLE</td>
<td>RW</td>
<td>0</td>
<td>Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>Value</td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The counter is disabled.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>Enables SysTick to operate in a multi-shot way. That is, the counter loads the RELOAD value and begins counting down. On reaching 0, the COUNT bit is set and an interrupt is generated if enabled by INTEN. The counter then loads the RELOAD value again and begins counting.</td>
</tr>
</tbody>
</table>
Register 2: SysTick Reload Value Register (STRELOAD), offset 0x014

**Note:** This register can only be accessed from privileged mode.

The STRELOAD register specifies the start value to load into the SysTick Current Value (STCURRENT) register when the counter reaches 0. The start value can be between 0x1 and 0x00FF.FFFF. A start value of 0 is possible but has no effect because the SysTick interrupt and the COUNT bit are activated when counting from 1 to 0.

SysTick can be configured as a multi-shot timer, repeated over and over, firing every N+1 clock pulses, where N is any value from 1 to 0x00FF.FFFF. For example, if a tick interrupt is required every 100 clock pulses, 99 must be written into the RELOAD field.

Note that in order to access this register correctly, the system clock must be faster than 8 MHz.

### SysTick Reload Value Register (STRELOAD)

Base 0xE000.E000  
Offset 0x014  
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23:0</td>
<td>RELOAD</td>
<td>RW</td>
<td>0x00.0000</td>
<td>Value to load into the SysTick Current Value (STCURRENT) register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>when the counter reaches 0.</td>
</tr>
</tbody>
</table>
Register 3: SysTick Current Value Register (STCURRENT), offset 0x018

Note: This register can only be accessed from privileged mode.

The STCURRENT register contains the current value of the SysTick counter.

SysTick Current Value Register (STCURRENT)
Base 0xE000.E000
Offset 0x018
Type RWC, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23:0</td>
<td>CURRENT</td>
<td>RWC</td>
<td>0x00.0000</td>
<td>Current Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field contains the current value at the time the register is accessed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No read-modify-write protection is provided, so change with care.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This register is write-clear. Writing to it with any value clears the register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Clearing this register also clears the COUNT bit of the STCTRL register.</td>
</tr>
</tbody>
</table>

3.4 NVIC Register Descriptions

This section lists and describes the NVIC registers, in numerical order by address offset.

The NVIC registers can only be fully accessed from privileged mode, but interrupts can be pended while in unprivileged mode by enabling the Configuration and Control (CFGCTRL) register. Any other unprivileged mode access causes a bus fault.

Ensure software uses correctly aligned register accesses. The processor does not support unaligned accesses to NVIC registers.

An interrupt can enter the pending state even if it is disabled.

Before programming the VTABLE register to relocate the vector table, ensure the vector table entries of the new vector table are set up for fault handlers, NMI, and all enabled exceptions such as interrupts. For more information, see page 163.
Register 4: Interrupt 0-31 Set Enable (EN0), offset 0x100
Register 5: Interrupt 32-63 Set Enable (EN1), offset 0x104
Register 6: Interrupt 64-95 Set Enable (EN2), offset 0x108
Register 7: Interrupt 96-127 Set Enable (EN3), offset 0x10C

Note: This register can only be accessed from privileged mode.

The **ENn** registers enable interrupts and show which interrupts are enabled. Bit 0 of **EN0** corresponds to Interrupt 0; bit 31 corresponds to Interrupt 31. Bit 0 of **EN1** corresponds to Interrupt 32; bit 31 corresponds to Interrupt 63. Bit 0 of **EN2** corresponds to Interrupt 64; bit 31 corresponds to Interrupt 95. Bit 0 of **EN3** corresponds to Interrupt 96; bit 31 corresponds to Interrupt 127. Bit 0 of **EN4** (see page 143) corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138.

See Table 2-9 on page 104 for interrupt assignments.

If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority. If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, but the NVIC never activates the interrupt, regardless of its priority.

**Interrupt 0-31 Set Enable (EN0)**
Base 0x0E000.E000
Offset 0x100
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>INT</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt Enable</td>
</tr>
</tbody>
</table>

Value Description
0 On a read, indicates the interrupt is disabled.

On a write, no effect.
1 On a read, indicates the interrupt is enabled.
On a write, enables the interrupt.

A bit can only be cleared by setting the corresponding **INT[n]** bit in the **DISn** register.
Register 8: Interrupt 128-138 Set Enable (EN4), offset 0x110

**Note:** This register can only be accessed from privileged mode.

The **EN4** register enables interrupts and shows which interrupts are enabled. Bit 0 corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138. See Table 2-9 on page 104 for interrupt assignments.

If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority. If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, but the NVIC never activates the interrupt, regardless of its priority.

Interrupt 128-138 Set Enable (EN4)

Base 0xE000.E000
Offset 0x110
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:11</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10:0</td>
<td>INT</td>
<td>RW</td>
<td>0x0</td>
<td>Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>On a read, indicates the interrupt is disabled. On a write, no effect.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>On a read, indicates the interrupt is enabled. On a write, enables the interrupt.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A bit can only be cleared by setting the corresponding *INT[n]* bit in the **DIS4** register.
Register 9: Interrupt 0-31 Clear Enable (DIS0), offset 0x180
Register 10: Interrupt 32-63 Clear Enable (DIS1), offset 0x184
Register 11: Interrupt 64-95 Clear Enable (DIS2), offset 0x188
Register 12: Interrupt 96-127 Clear Enable (DIS3), offset 0x18C

Note: This register can only be accessed from privileged mode.

The DISn registers disable interrupts. Bit 0 of DIS0 corresponds to Interrupt 0; bit 31 corresponds to Interrupt 31. Bit 0 of DIS1 corresponds to Interrupt 32; bit 31 corresponds to Interrupt 63. Bit 0 of DIS2 corresponds to Interrupt 64; bit 31 corresponds to Interrupt 95. Bit 0 of DIS3 corresponds to Interrupt 96; bit 31 corresponds to Interrupt 127. Bit 0 of DIS4 (see page 145) corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138.

See Table 2-9 on page 104 for interrupt assignments.

Interrupt 0-31 Clear Enable (DIS0)
Base 0xE000.E000
Offset 0x180
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>0</td>
<td>Interrupt Disable</td>
</tr>
<tr>
<td>RW</td>
<td>0</td>
<td>On a read, indicates the interrupt is disabled. On a write, no effect.</td>
</tr>
<tr>
<td>RW</td>
<td>0</td>
<td>On a read, indicates the interrupt is enabled. On a write, clears the corresponding INT[n] bit in the EN0 register, disabling interrupt [n].</td>
</tr>
</tbody>
</table>
Register 13: Interrupt 128-138 Clear Enable (DIS4), offset 0x190

Note: This register can only be accessed from privileged mode.

The DIS4 register disables interrupts. Bit 0 corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138. See Table 2-9 on page 104 for interrupt assignments.

Interrupt Disable

On a read, indicates the interrupt is disabled.
On a write, no effect.

Value Description
0 On a read, indicates the interrupt is disabled.
1 On a read, indicates the interrupt is enabled.

On a write, clears the corresponding INT[n] bit in the EN4 register, disabling interrupt [n].
Register 14: Interrupt 0-31 Set Pending (PEND0), offset 0x200
Register 15: Interrupt 32-63 Set Pending (PEND1), offset 0x204
Register 16: Interrupt 64-95 Set Pending (PEND2), offset 0x208
Register 17: Interrupt 96-127 Set Pending (PEND3), offset 0x20C

Note: This register can only be accessed from privileged mode.

The PENDn registers force interrupts into the pending state and show which interrupts are pending. Bit 0 of PEND0 corresponds to Interrupt 0; bit 31 corresponds to Interrupt 31. Bit 0 of PEND1 corresponds to Interrupt 32; bit 31 corresponds to Interrupt 63. Bit 0 of PEND2 corresponds to Interrupt 64; bit 31 corresponds to Interrupt 95. Bit 0 of PEND3 corresponds to Interrupt 96; bit 31 corresponds to Interrupt 127. Bit 0 of PEND4 (see page 147) corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138.

See Table 2-9 on page 104 for interrupt assignments.

Interrupt 0-31 Set Pending (PEND0)
Base 0xE000.E000
Offset 0x200
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>INT</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt Set Pending</td>
</tr>
</tbody>
</table>

Value Description
0 On a read, indicates that the interrupt is not pending.
    On a write, no effect.
1 On a read, indicates that the interrupt is pending.
    On a write, the corresponding interrupt is set to pending even if it is disabled.

If the corresponding interrupt is already pending, setting a bit has no effect.
A bit can only be cleared by setting the corresponding INT[n] bit in the UNPEND0 register.
Register 18: Interrupt 128-138 Set Pending (PEND4), offset 0x210

**Note:** This register can only be accessed from privileged mode.

The **PEND4** register forces interrupts into the pending state and shows which interrupts are pending. Bit 0 corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138. See Table 2-9 on page 104 for interrupt assignments.

### Interrupt 128-138 Set Pending (PEND4)

Base 0xE000.E000  
Offset 0x210  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:11</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10:0</td>
<td>INT</td>
<td>RW</td>
<td>0x0</td>
<td>Interrupt Set Pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: On a read, indicates that the interrupt is not pending. On a write, no effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: On a read, indicates that the interrupt is pending. On a write, the corresponding interrupt is set to pending even if it is disabled.</td>
</tr>
</tbody>
</table>

If the corresponding interrupt is already pending, setting a bit has no effect.

A bit can only be cleared by setting the corresponding INT[n] bit in the **UNPEND4** register.
Register 19: Interrupt 0-31 Clear Pending (UNPEND0), offset 0x280
Register 20: Interrupt 32-63 Clear Pending (UNPEND1), offset 0x284
Register 21: Interrupt 64-95 Clear Pending (UNPEND2), offset 0x288
Register 22: Interrupt 96-127 Clear Pending (UNPEND3), offset 0x28C

Note: This register can only be accessed from privileged mode.

The **UNPENDn** registers show which interrupts are pending and remove the pending state from interrupts. Bit 0 of **UNPEND0** corresponds to Interrupt 0; bit 31 corresponds to Interrupt 31. Bit 0 of **UNPEND1** corresponds to Interrupt 32; bit 31 corresponds to Interrupt 63. Bit 0 of **UNPEND2** corresponds to Interrupt 64; bit 31 corresponds to Interrupt 95. Bit 0 of **UNPEND3** corresponds to Interrupt 96; bit 31 corresponds to Interrupt 127. Bit 0 of **UNPEND4** (see page 149) corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138.

See Table 2-9 on page 104 for interrupt assignments.

Interrupt 0-31 Clear Pending (UNPEND0)

<table>
<thead>
<tr>
<th>Bit 31-0</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>INT</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt Clear Pending</td>
</tr>
</tbody>
</table>
Register 23: Interrupt 128-138 Clear Pending (UNPEND4), offset 0x290

Note: This register can only be accessed from privileged mode.

The UNPEND4 register shows which interrupts are pending and removes the pending state from interrupts. Bit 0 corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138. See Table 2-9 on page 104 for interrupt assignments.

Interrupt 128-138 Clear Pending (UNPEND4)
Base 0xE000.E000
Offset 0x290
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:11</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10:0</td>
<td>INT</td>
<td>RW</td>
<td>0x0</td>
<td>Interrupt Clear Pending</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>On a read, indicates that the interrupt is not pending.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>On a read, indicates that the interrupt is pending. On a write, clears the corresponding INT[n] bit in the PEND4 register, so that interrupt [n] is no longer pending. Setting a bit does not affect the active state of the corresponding interrupt.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 24: Interrupt 0-31 Active Bit (ACTIVE0), offset 0x300
Register 25: Interrupt 32-63 Active Bit (ACTIVE1), offset 0x304
Register 26: Interrupt 64-95 Active Bit (ACTIVE2), offset 0x308
Register 27: Interrupt 96-127 Active Bit (ACTIVE3), offset 0x30C

Note: This register can only be accessed from privileged mode.

The UNPENDn registers indicate which interrupts are active. Bit 0 of ACTIVE0 corresponds to Interrupt 0; bit 31 corresponds to Interrupt 31. Bit 0 of ACTIVE1 corresponds to Interrupt 32; bit 31 corresponds to Interrupt 63. Bit 0 of ACTIVE2 corresponds to Interrupt 64; bit 31 corresponds to Interrupt 95. Bit 0 of ACTIVE3 corresponds to Interrupt 96; bit 31 corresponds to Interrupt 127. Bit 0 of ACTIVE4 (see page 151) corresponds to Interrupt 128; bit 10 corresponds to Interrupt 138.

See Table 2-9 on page 104 for interrupt assignments.

Caution – Do not manually set or clear the bits in this register.

### Interrupt 0-31 Active Bit (ACTIVE0)

Base 0xE000.E000
Offset 0x300
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0000</td>
<td>INT</td>
<td>Interrupt Active</td>
</tr>
<tr>
<td>RO</td>
<td>0000</td>
<td>INT</td>
<td>Value Description</td>
</tr>
<tr>
<td>RO</td>
<td>0000</td>
<td>INT</td>
<td>0: The corresponding interrupt is not active.</td>
</tr>
<tr>
<td>RO</td>
<td>0000</td>
<td>INT</td>
<td>1: The corresponding interrupt is active, or active and pending.</td>
</tr>
</tbody>
</table>

---

**Cortex-M4 Peripherals**
Register 28: Interrupt 128-138 Active Bit (ACTIVE4), offset 0x310

**Note:** This register can only be accessed from privileged mode.

The **ACTIVE4** register indicates which interrupts are active. Bit 0 corresponds to Interrupt 128; bit 10 corresponds to Interrupt 131. See Table 2-9 on page 104 for interrupt assignments.

**Caution** – Do not manually set or clear the bits in this register.

### Interrupt 128-138 Active Bit (ACTIVE4)

Base 0xE000.E000 Offset 0x310 Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:11</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10:0</td>
<td>INT</td>
<td>RO</td>
<td>0x0</td>
<td>Interrupt Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 29: Interrupt 0-3 Priority (PRI0), offset 0x400
Register 30: Interrupt 4-7 Priority (PRI1), offset 0x404
Register 31: Interrupt 8-11 Priority (PRI2), offset 0x408
Register 32: Interrupt 12-15 Priority (PRI3), offset 0x40C
Register 33: Interrupt 16-19 Priority (PRI4), offset 0x410
Register 34: Interrupt 20-23 Priority (PRI5), offset 0x414
Register 35: Interrupt 24-27 Priority (PRI6), offset 0x418
Register 36: Interrupt 28-31 Priority (PRI7), offset 0x41C
Register 37: Interrupt 32-35 Priority (PRI8), offset 0x420
Register 38: Interrupt 36-39 Priority (PRI9), offset 0x424
Register 39: Interrupt 40-43 Priority (PRI10), offset 0x428
Register 40: Interrupt 44-47 Priority (PRI11), offset 0x42C
Register 41: Interrupt 48-51 Priority (PRI12), offset 0x430
Register 42: Interrupt 52-55 Priority (PRI13), offset 0x434
Register 43: Interrupt 56-59 Priority (PRI14), offset 0x438
Register 44: Interrupt 60-63 Priority (PRI15), offset 0x43C

**Note:** This register can only be accessed from privileged mode.

The PRIn registers (see also page 154) provide 3-bit priority fields for each interrupt. These registers are byte accessible. Each register holds four priority fields that are assigned to interrupts as follows:

<table>
<thead>
<tr>
<th>PRIn Register Bit Field</th>
<th>Interrupt</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits 31:29</td>
<td>Interrupt [4n+3]</td>
</tr>
<tr>
<td>Bits 23:21</td>
<td>Interrupt [4n+2]</td>
</tr>
<tr>
<td>Bits 15:13</td>
<td>Interrupt [4n+1]</td>
</tr>
<tr>
<td>Bits 7:5</td>
<td>Interrupt [4n]</td>
</tr>
</tbody>
</table>

See Table 2-9 on page 104 for interrupt assignments.

Each priority level can be split into separate group priority and subpriority fields. The PRIGROUP field in the Application Interrupt and Reset Control (APINT) register (see page 164) indicates the position of the binary point that splits the priority and subpriority fields.

These registers can only be accessed from privileged mode.
Interrupt 0-3 Priority (PRI0)
Base 0xE000.E000
Offset 0x400
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>INTD</td>
<td>RW</td>
<td>0x0</td>
<td>Interrupt Priority for Interrupt [4n+3]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field holds a priority value, 0-7, for the interrupt with the number [4n+3], where n is the number of the Interrupt Priority register (n=0 for PRI0, and so on). The lower the value, the greater the priority of the corresponding interrupt.</td>
</tr>
<tr>
<td>28:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23:21</td>
<td>INTC</td>
<td>RW</td>
<td>0x0</td>
<td>Interrupt Priority for Interrupt [4n+2]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field holds a priority value, 0-7, for the interrupt with the number [4n+2], where n is the number of the Interrupt Priority register (n=0 for PRI0, and so on). The lower the value, the greater the priority of the corresponding interrupt.</td>
</tr>
<tr>
<td>20:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:13</td>
<td>INTB</td>
<td>RW</td>
<td>0x0</td>
<td>Interrupt Priority for Interrupt [4n+1]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field holds a priority value, 0-7, for the interrupt with the number [4n+1], where n is the number of the Interrupt Priority register (n=0 for PRI0, and so on). The lower the value, the greater the priority of the corresponding interrupt.</td>
</tr>
<tr>
<td>12:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:5</td>
<td>INTA</td>
<td>RW</td>
<td>0x0</td>
<td>Interrupt Priority for Interrupt [4n]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field holds a priority value, 0-7, for the interrupt with the number [4n], where n is the number of the Interrupt Priority register (n=0 for PRI0, and so on). The lower the value, the greater the priority of the corresponding interrupt.</td>
</tr>
<tr>
<td>4:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 45: Interrupt 64-67 Priority (PRI16), offset 0x440
Register 46: Interrupt 68-71 Priority (PRI17), offset 0x444
Register 47: Interrupt 72-75 Priority (PRI18), offset 0x448
Register 48: Interrupt 76-79 Priority (PRI19), offset 0x44C
Register 49: Interrupt 80-83 Priority (PRI20), offset 0x450
Register 50: Interrupt 84-87 Priority (PRI21), offset 0x454
Register 51: Interrupt 88-91 Priority (PRI22), offset 0x458
Register 52: Interrupt 92-95 Priority (PRI23), offset 0x45C
Register 53: Interrupt 96-99 Priority (PRI24), offset 0x460
Register 54: Interrupt 100-103 Priority (PRI25), offset 0x464
Register 55: Interrupt 104-107 Priority (PRI26), offset 0x468
Register 56: Interrupt 108-111 Priority (PRI27), offset 0x46C
Register 57: Interrupt 112-115 Priority (PRI28), offset 0x470
Register 58: Interrupt 116-119 Priority (PRI29), offset 0x474
Register 59: Interrupt 120-123 Priority (PRI30), offset 0x478
Register 60: Interrupt 124-127 Priority (PRI31), offset 0x47C
Register 61: Interrupt 128-131 Priority (PRI32), offset 0x480
Register 62: Interrupt 132-135 Priority (PRI33), offset 0x484
Register 63: Interrupt 136-138 Priority (PRI34), offset 0x488

Note: This register can only be accessed from privileged mode.

The PRIn registers (see also page 152) provide 3-bit priority fields for each interrupt. These registers are byte accessible. Each register holds four priority fields that are assigned to interrupts as follows:

<table>
<thead>
<tr>
<th>PRIn Register Bit Field</th>
<th>Interrupt</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits 31:29</td>
<td>Interrupt [4n+3]</td>
</tr>
<tr>
<td>Bits 23:21</td>
<td>Interrupt [4n+2]</td>
</tr>
<tr>
<td>Bits 15:13</td>
<td>Interrupt [4n+1]</td>
</tr>
<tr>
<td>Bits 7:5</td>
<td>Interrupt [4n]</td>
</tr>
</tbody>
</table>

See Table 2-9 on page 104 for interrupt assignments.

Each priority level can be split into separate group priority and subpriority fields. The PRIGROUP field in the Application Interrupt and Reset Control (APINT) register (see page 164) indicates the position of the binary point that splits the priority and subpriority fields.

These registers can only be accessed from privileged mode.
### Interrupt 64-67 Priority (PRI16)

**Base 0xE000.E000**  
**Offset 0x440**  
**Type RW, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:29     | INTD | RW   | 0x0   | Interrupt Priority for Interrupt [4n+3]  
This field holds a priority value, 0-7, for the interrupt with the number [4n+3], where n is the number of the Interrupt Priority register (n=0 for PRI0, and so on). The lower the value, the greater the priority of the corresponding interrupt. |
| 28:24     | reserved | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 23:21     | INTC | RW   | 0x0   | Interrupt Priority for Interrupt [4n+2]  
This field holds a priority value, 0-7, for the interrupt with the number [4n+2], where n is the number of the Interrupt Priority register (n=0 for PRI0, and so on). The lower the value, the greater the priority of the corresponding interrupt. |
| 20:16     | reserved | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 15:13     | INTB | RW   | 0x0   | Interrupt Priority for Interrupt [4n+1]  
This field holds a priority value, 0-7, for the interrupt with the number [4n+1], where n is the number of the Interrupt Priority register (n=0 for PRI0, and so on). The lower the value, the greater the priority of the corresponding interrupt. |
| 12:8      | reserved | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 7:5       | INTA | RW   | 0x0   | Interrupt Priority for Interrupt [4n]  
This field holds a priority value, 0-7, for the interrupt with the number [4n], where n is the number of the Interrupt Priority register (n=0 for PRI0, and so on). The lower the value, the greater the priority of the corresponding interrupt. |
| 4:0       | reserved | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
Register 64: Software Trigger Interrupt (SWTRIG), offset 0xF00

Note: Only privileged software can enable unprivileged access to the SWTRIG register.

Writing an interrupt number to the SWTRIG register generates a Software Generated Interrupt (SGI). See Table 2-9 on page 104 for interrupt assignments.

When the MAINPEND bit in the Configuration and Control (CFGCTRL) register (see page 168) is set, unprivileged software can access the SWTRIG register.

Software Trigger Interrupt (SWTRIG)
Base 0xE000.E000
Offset 0xF00
Type WO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>INTID</td>
<td>WO</td>
<td>0x00</td>
<td>Interrupt ID This field holds the interrupt ID of the required SGI. For example, a value of 0x3 generates an interrupt on IRQ3.</td>
</tr>
</tbody>
</table>

3.5 System Control Block (SCB) Register Descriptions

This section lists and describes the System Control Block (SCB) registers, in numerical order by address offset. The SCB registers can only be accessed from privileged mode.

All registers must be accessed with aligned word accesses except for the FAULTSTAT and SYSPRI1-SYSPRI3 registers, which can be accessed with byte or aligned halfword or word accesses. The processor does not support unaligned accesses to system control block registers.
Register 65: Auxiliary Control (ACTLR), offset 0x008

Note: This register can only be accessed from privileged mode.

The ACTLR register provides disable bits for IT folding, write buffer use for accesses to the default memory map, and interruption of multi-cycle instructions. By default, this register is set to provide optimum performance from the Cortex-M4 processor and does not normally require modification.

Auxiliary Control (ACTLR)
Base 0xE000.E000
Offset 0x008
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 9         | DISOOFP       | RW   | 0     | Disable Out-Of-Order Floating Point
Disables floating-point instructions completing out of order with respect to integer instructions. |
| 8         | DISFPCA       | RW   | 0     | Disable CONTROL.FPCA
Disable automatic update of the FPCA bit in the CONTROL register. |
| 7:3       | reserved      | RO   | 0x00  | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 2         | DISFOLD       | RW   | 0     | Disable IT Folding
Value Description
0    No effect.
1    Disables IT folding. |

Important: Two bits control when FPCA can be enabled: the ASPEN bit in the Floating-Point Context Control (FPCC) register and the DISFPCA bit in the Auxiliary Control (ACTLR) register.

In some situations, the processor can start executing the first instruction in an IT block while it is still executing the IT instruction. This behavior is called IT folding, and improves performance. However, IT folding can cause jitter in looping. If a task must avoid jitter, set the DISFOLD bit before executing the task, to disable IT folding.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DISWBUF</td>
<td>RW</td>
<td>0</td>
<td>Disable Write Buffer</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong>    <strong>Description</strong></td>
</tr>
<tr>
<td>0</td>
<td>No effect.</td>
<td></td>
<td></td>
<td>Disables write buffer use during default memory map accesses.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td>Disables write buffer use during default memory map accesses.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>In this situation, all bus faults are precise bus faults but performance is decreased because any store to memory must complete before the processor can execute the next instruction.</td>
</tr>
<tr>
<td></td>
<td><strong>Note:</strong></td>
<td></td>
<td></td>
<td>This bit only affects write buffers implemented in the Cortex-M4 processor.</td>
</tr>
<tr>
<td>0</td>
<td>DISMCYC</td>
<td>RW</td>
<td>0</td>
<td>Disable Interrupts of Multiple Cycle Instructions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong>    <strong>Description</strong></td>
</tr>
<tr>
<td>0</td>
<td>No effect.</td>
<td></td>
<td></td>
<td>Disables interruption of load multiple and store multiple instructions.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td>In this situation, the interrupt latency of the processor is increased because any LDM or STM must complete before the processor can stack the current state and enter the interrupt handler.</td>
</tr>
</tbody>
</table>
**Register 66: CPU ID Base (CPUID), offset 0xD00**

**Note:** This register can only be accessed from privileged mode.

The **CPUID** register contains the ARM® Cortex™-M4 processor part number, version, and implementation information.

**CPU ID Base (CPUID)**
Base 0xE000.E000
Offset 0xD00
Type RO, reset 0x410F.C241

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>IMP</td>
<td>RO</td>
<td>0x41</td>
<td>Implementer Code</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x41  ARM</td>
</tr>
<tr>
<td>23:20</td>
<td>VAR</td>
<td>RO</td>
<td>0x0</td>
<td>Variant Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0  The rn value in the rnpn product revision identifier, for example, the 0 in r0p0.</td>
</tr>
<tr>
<td>19:16</td>
<td>CON</td>
<td>RO</td>
<td>0xF</td>
<td>Constant</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xF  Always reads as 0xF.</td>
</tr>
<tr>
<td>15:4</td>
<td>PARTNO</td>
<td>RO</td>
<td>0xC24</td>
<td>Part Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xC24 Cortex-M4 processor.</td>
</tr>
<tr>
<td>3:0</td>
<td>REV</td>
<td>RO</td>
<td>0x1</td>
<td>Revision Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1  The pn value in the rnpn product revision identifier, for example, the 1 in r0p1.</td>
</tr>
</tbody>
</table>
Register 67: Interrupt Control and State (INTCTRL), offset 0xD04

**Note:** This register can only be accessed from privileged mode.

The **INCTRL** register provides a set-pending bit for the NMI exception, and set-pending and clear-pending bits for the PendSV and SysTick exceptions. In addition, bits in this register indicate the exception number of the exception being processed, whether there are preempted active exceptions, the exception number of the highest priority pending exception, and whether any interrupts are pending.

When writing to **INCTRL**, the effect is unpredictable when writing a 1 to both the **PENDSV** and **UNPENDSV** bits, or writing a 1 to both the **PENDSTSET** and **PENDSTCLR** bits.

---

### Interrupt Control and State (INTCTRL)

**Base 0xE000.E000**  
**Offset 0xD04**  
**Type RW, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>31:30:29</td>
<td>NMISET</td>
<td>RW</td>
<td>0</td>
<td>NMI Set Pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td>28</td>
<td>PENDSV</td>
<td>RW</td>
<td>0</td>
<td>PendSV Set Pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td>27:26:25</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>24:23:22</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>PendSV Set Pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td>21:20</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>PendSV Set Pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td>19:18:17</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>PendSV Set Pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>PendSV Set Pending</td>
</tr>
</tbody>
</table>

---

Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it registers the setting of this bit, and clears this bit on entering the interrupt handler. A read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.

Setting this bit is the only way to set the PendSV exception state to pending. This bit is cleared by writing a 1 to the **UNPENDSV** bit.
### Description

#### PendSV Clear Pending

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td>UNPENDSV</td>
<td>WO</td>
<td>0</td>
<td>PendSV Clear Pending</td>
</tr>
</tbody>
</table>

- **Value Description**
  - 0: On a write, no effect.
  - 1: On a write, removes the pending state from the PendSV exception.

- This bit is write only; on a register read, its value is unknown.

#### SysTick Set Pending

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>26</td>
<td>PENDSTSET</td>
<td>RW</td>
<td>0</td>
<td>SysTick Set Pending</td>
</tr>
</tbody>
</table>

- **Value Description**
  - 0: On a read, indicates a SysTick exception is not pending.
  - 1: On a read, indicates a SysTick exception is pending.

- On a write, changes the SysTick exception state to pending.

- This bit is cleared by writing a 1 to the `PENDSTCLR` bit.

#### SysTick Clear Pending

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>PENDSTCLR</td>
<td>WO</td>
<td>0</td>
<td>SysTick Clear Pending</td>
</tr>
</tbody>
</table>

- **Value Description**
  - 0: On a write, no effect.
  - 1: On a write, removes the pending state from the SysTick exception.

- This bit is write only; on a register read, its value is unknown.

#### Reserved

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

#### Debug Interrupt Handling

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>ISRPRE</td>
<td>RO</td>
<td>0</td>
<td>Debug Interrupt Handling</td>
</tr>
</tbody>
</table>

- **Value Description**
  - 0: The release from halt does not take an interrupt.
  - 1: The release from halt takes an interrupt.

- This bit is only meaningful in Debug mode and reads as zero when the processor is not in Debug mode.

#### Interrupt Pending

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>ISRPEND</td>
<td>RO</td>
<td>0</td>
<td>Interrupt Pending</td>
</tr>
</tbody>
</table>

- **Value Description**
  - 0: No interrupt is pending.
  - 1: An interrupt is pending.

- This bit provides status for all interrupts excluding NMI and Faults.

#### Reserved

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>21:20</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Interrupt Pending Vector Number
This field contains the exception number of the highest priority pending enabled exception. The value indicated by this field includes the effect of the BASEPRI and FAULTMASK registers, but not any effect of the PRIMASK register.

Value | Description
--- | ---
0x00 | No exceptions are pending
0x01 | Reserved
0x02 | NMI
0x03 | Hard fault
0x04 | Memory management fault
0x05 | Bus fault
0x06 | Usage fault
0x07-0x0A | Reserved
0x0B | SVCall
0x0C | Reserved for Debug
0x0D | Reserved
0x0E | PendSV
0x0F | SysTick
0x10 | Interrupt Vector 0
0x11 | Interrupt Vector 1
... | ...
0x9A | Interrupt Vector 138

Return to Base
This bit provides status for all interrupts excluding NMI and Faults. This bit only has meaning if the processor is currently executing an ISR (the Interrupt Program Status (IPSR) register is non-zero).

Value | Description
--- | ---
0 | There are preempted active exceptions to execute.
1 | There are no active exceptions, or the currently executing exception is the only active exception.

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Interrupt Pending Vector Number
This field contains the active exception number. The exception numbers can be found in the description for the VECPEND field. If this field is clear, the processor is in Thread mode. This field contains the same value as the ISRNUM field in the IPSR register.

Subtract 16 from this value to obtain the IRQ number required to index into the Interrupt Set Enable (ENn), Interrupt Clear Enable (DISn), Interrupt Set Pending (PENDn), Interrupt Clear Pending (UNPENDn), and Interrupt Priority (PRIn) registers (see page 81).
### Register 68: Vector Table Offset (VTABLE), offset 0xD08

**Note:** This register can only be accessed from privileged mode.

The **VTABLE** register indicates the offset of the vector table base address from memory address 0x0000.0000.

#### Vector Table Offset (VTABLE)

- **Base:** 0xE000.E000
- **Offset:** 0xD08
- **Type:** RW, reset 0x0000.0000

---

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:10     | OFFSET | RW   | 0x000.00 | Vector Table Offset  
When configuring the **OFFSET** field, the offset must be aligned to the number of exception entries in the vector table. Because there are 138 interrupts, the offset must be aligned on a 1024-byte boundary. |
| 9:0       | reserved | RO   | 0x00 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
Register 69: Application Interrupt and Reset Control (APINT), offset 0xD0C

**Note:** This register can only be accessed from privileged mode.

The APINT register provides priority grouping control for the exception model, endian status for data accesses, and reset control of the system. To write to this register, 0x05FA must be written to the VECTKEY field, otherwise the write is ignored.

The PRIGROUP field indicates the position of the binary point that splits the INTx fields in the Interrupt Priority (PRIx) registers into separate group priority and subpriority fields. Table 3-9 on page 164 shows how the PRIGROUP value controls this split. The bit numbers in the Group Priority Field and Subpriority Field columns in the table refer to the bits in the INTA field. For the INTB field, the corresponding bits are 15:13; for INTC, 23:21; and for INTD, 31:29.

**Note:** Determining preemption of an exception uses only the group priority field.

### Table 3-9. Interrupt Priority Levels

<table>
<thead>
<tr>
<th>PRIGROUP</th>
<th>Bit Field</th>
<th>Binary Point</th>
<th>Group Priority Field</th>
<th>Subpriority Field</th>
<th>Group Priorities</th>
<th>Subpriorities</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0 - 0x4</td>
<td>bxxxx.</td>
<td>[7:5]</td>
<td>None</td>
<td>8</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0x5</td>
<td>bxx.y</td>
<td>[7:6]</td>
<td>[5]</td>
<td>4</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>0x6</td>
<td>bx.yy</td>
<td>[7]</td>
<td>[6:5]</td>
<td>2</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>0x7</td>
<td>b.yyy</td>
<td>None</td>
<td>[7:5]</td>
<td>1</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>

a. INTx field showing the binary point. An x denotes a group priority field bit, and a y denotes a subpriority field bit.

---

**Application Interrupt and Reset Control (APINT)**

Base 0xE000.E000  
Offset 0xD0C  
Type RW, reset 0xFA05.0000

<table>
<thead>
<tr>
<th>Description</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
|             | 31:16     | VECTKEY | RW     | 0xFA05 | Register Key  
This field is used to guard against accidental writes to this register. 0x05FA must be written to this field in order to change the bits in this register. On a read, 0xFA05 is returned. |
|             | 15        | ENDIANESS | RO    | 0     | Data Endianess  
The Tiva™ C Series implementation uses only little-endian mode so this is cleared to 0. |
|             | 14:11     | reserved | RO    | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
### Bit/Field Name Type Reset Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 10:8      | PRIGROUP | RW   | 0x0   | Interrupt Priority Grouping  
This field determines the split of group priority from subpriority (see Table 3-9 on page 164 for more information). |
| 7:3       | reserved | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 2         | SYSRESREQ | WO   | 0     | System Reset Request  
Value Description  
0    No effect.  
1    Resets the core and all on-chip peripherals except the Debug interface.  
This bit is automatically cleared during the reset of the core and reads as 0. |
| 1         | VECTCLRACT | WO   | 0     | Clear Active NMI / Fault  
This bit is reserved for Debug use and reads as 0. This bit must be written as a 0, otherwise behavior is unpredictable. |
| 0         | VECTRESET  | WO   | 0     | System Reset  
This bit is reserved for Debug use and reads as 0. This bit must be written as a 0, otherwise behavior is unpredictable. |
Register 70: System Control (SYSCTRL), offset 0xD10

**Note:** This register can only be accessed from privileged mode.

The **SYSCTRL** register controls features of entry to and exit from low-power state.

### System Control (SYSCTRL)
Base 0xE000.E000
Offset 0xD10
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>SEVONPEND</td>
<td>RW</td>
<td>0</td>
<td>Wake Up on Pending</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Only enabled interrupts or events can wake up the processor; disabled interrupts are excluded.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enabled events and all interrupts, including disabled interrupts, can wake up the processor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When an event or interrupt enters the pending state, the event signal wakes up the processor from <strong>WFE</strong>. If the processor is not waiting for an event, the event is registered and affects the next <strong>WFE</strong>.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The processor also wakes up on execution of a <strong>SEV</strong> instruction or an external event.</td>
</tr>
<tr>
<td>3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>SLEEPDEEP</td>
<td>RW</td>
<td>0</td>
<td>Deep Sleep Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Use Sleep mode as the low power mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Use Deep-sleep mode as the low power mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>SLEEPEXIT</td>
<td>RW</td>
<td>0</td>
<td>Sleep on ISR Exit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 71: Configuration and Control (CFGCTRL), offset 0xD14

**Note:** This register can only be accessed from privileged mode.

The CFGCTRL register controls entry to Thread mode and enables: the handlers for NMI, hard fault and faults escalated by the FAULTMASK register to ignore bus faults; trapping of divide by zero and unaligned accesses; and access to the SWTRIG register by unprivileged software (see page 156).

### Configuration and Control (CFGCTRL)

Base 0xE000.E000
Offset 0xD14
Type RW, reset 0x0000.0200

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>STKALIGN</td>
<td>RW</td>
<td>1</td>
<td>Stack Alignment on Exception Entry</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The stack is 4-byte aligned.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The stack is 8-byte aligned.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description: On exception entry, the processor uses bit 9 of the stacked PSR to indicate the stack alignment. On return from the exception, it uses this stacked bit to restore the correct stack alignment.</td>
</tr>
<tr>
<td>8</td>
<td>BFHFNMIGN</td>
<td>RW</td>
<td>0</td>
<td>Ignore Bus Fault in NMI and Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Data bus faults caused by load and store instructions cause a lock-up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: Handlers running at priority -1 and -2 ignore data bus faults caused by load and store instructions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description: Set this bit only when the handler and its data are in absolutely safe memory. The normal use of this bit is to probe system devices and bridges to detect control path problems and fix them.</td>
</tr>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
### Trap on Divide by 0

This bit enables faulting or halting when the processor executes an SDIV or UDIV instruction with a divisor of 0.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Do not trap on divide by 0. A divide by zero returns a quotient of 0.</td>
</tr>
<tr>
<td>1</td>
<td>Trap on divide by 0.</td>
</tr>
</tbody>
</table>

### Trap on Unaligned Access

Do not trap on unaligned halfword and word accesses.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Do not trap on unaligned halfword and word accesses.</td>
</tr>
<tr>
<td>1</td>
<td>Trap on unaligned halfword and word accesses. An unaligned access generates a usage fault.</td>
</tr>
</tbody>
</table>

Unaligned LDM, STM, LDRD, and STRD instructions always fault regardless of whether UNALIGN is set.

### Software should not rely on the value of a reserved bit.

To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Disables unprivileged software access to the SWTRIG register.</td>
</tr>
<tr>
<td>1</td>
<td>Enables unprivileged software access to the SWTRIG register (see page 156).</td>
</tr>
</tbody>
</table>

### Allow Main Interrupt Trigger

The processor can enter Thread mode from any level under the control of an EXC_RETURN value (see “Exception Return” on page 110 for more information).

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The processor can enter Thread mode only when no exception is active.</td>
</tr>
<tr>
<td>1</td>
<td>The processor can enter Thread mode from any level under the control of an EXC_RETURN value (see “Exception Return” on page 110 for more information).</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>DIV0</td>
<td>RW</td>
<td>0</td>
<td>Trap on Divide by 0</td>
</tr>
<tr>
<td>3</td>
<td>UNALIGN</td>
<td>RW</td>
<td>0</td>
<td>Trap on Unaligned Access</td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>MAINPEND</td>
<td>RW</td>
<td>0</td>
<td>Allow Main Interrupt Trigger</td>
</tr>
<tr>
<td>0</td>
<td>BASETHR</td>
<td>RW</td>
<td>0</td>
<td>Thread State Control</td>
</tr>
</tbody>
</table>
Register 72: System Handler Priority 1 (SYSPRI1), offset 0xD18

Note: This register can only be accessed from privileged mode.

The SYSPRI1 register configures the priority level, 0 to 7 of the usage fault, bus fault, and memory management fault exception handlers. This register is byte-accessible.

System Handler Priority 1 (SYSPRI1)
Base 0xE000.E000
Offset 0xD18
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23:21</td>
<td>USAGE</td>
<td>RW</td>
<td>0x0</td>
<td>Usage Fault Priority</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field configures the priority level of the usage fault. Configurable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>priority values are in the range 0-7, with lower values having higher</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>priority.</td>
</tr>
<tr>
<td>20:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:13</td>
<td>BUS</td>
<td>RW</td>
<td>0x0</td>
<td>Bus Fault Priority</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field configures the priority level of the bus fault. Configurable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>priority values are in the range 0-7, with lower values having higher</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>priority.</td>
</tr>
<tr>
<td>12:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:5</td>
<td>MEM</td>
<td>RW</td>
<td>0x0</td>
<td>Memory Management Fault Priority</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field configures the priority level of the memory management fault.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Configurable priority values are in the range 0-7, with lower values</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>having higher priority.</td>
</tr>
<tr>
<td>4:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 73: System Handler Priority 2 (SYSPRI2), offset 0xD1C

Note: This register can only be accessed from privileged mode.

The SYSPRI2 register configures the priority level, 0 to 7 of the SVCall handler. This register is byte-accessible.

System Handler Priority 2 (SYSPRI2)
Base 0xE000.E000
Offset 0xD1C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:29     | SVC    | RW   | 0x0   | SVCall Priority
This field configures the priority level of SVCall. Configurable priority values are in the range 0-7, with lower values having higher priority. |
| 28:0      | reserved | RO   | 0x000.0000 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
Register 74: System Handler Priority 3 (SYSPRI3), offset 0xD20

**Note:** This register can only be accessed from privileged mode.

The **SYSPRI3** register configures the priority level, 0 to 7 of the SysTick exception and PendSV handlers. This register is byte-accessible.

System Handler Priority 3 (SYSPRI3)
Base 0xE000.E000
Offset 0xD20
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>0x0</td>
<td>SysTick Exception Priority</td>
</tr>
<tr>
<td>RW</td>
<td>0x0</td>
<td>PendSV Priority</td>
</tr>
<tr>
<td>RO</td>
<td>0x0</td>
<td>Debug Priority</td>
</tr>
</tbody>
</table>

### Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>TICK</td>
<td>RW</td>
<td>0x0</td>
<td>SysTick Exception Priority</td>
</tr>
<tr>
<td>28:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23:21</td>
<td>PENDSV</td>
<td>RW</td>
<td>0x0</td>
<td>PendSV Priority</td>
</tr>
<tr>
<td>20:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:5</td>
<td>DEBUG</td>
<td>RW</td>
<td>0x0</td>
<td>Debug Priority</td>
</tr>
<tr>
<td>4:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x0.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 75: System Handler Control and State (SYSHNDCTRL), offset 0xD24

Note: This register can only be accessed from privileged mode.

The **SYSHNDCTRL** register enables the system handlers, and indicates the pending status of the usage fault, bus fault, memory management fault, and SVC exceptions as well as the active status of the system handlers.

If a system handler is disabled and the corresponding fault occurs, the processor treats the fault as a hard fault.

This register can be modified to change the pending or active status of system exceptions. An OS kernel can write to the active bits to perform a context switch that changes the current exception type.

**Caution –** Software that changes the value of an active bit in this register without correct adjustment to the stacked content can cause the processor to generate a fault exception. Ensure software that writes to this register retains and subsequently restores the current active status.

If the value of a bit in this register must be modified after enabling the system handlers, a read-modify-write procedure must be used to ensure that only the required bit is modified.

### System Handler Control and State (SYSHNDCTRL)

<table>
<thead>
<tr>
<th>Base 0xE000.E000</th>
<th>Offset 0xD24</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RW, reset 0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Usage Fault Enable</td>
<td>Usage</td>
</tr>
<tr>
<td>Bus Fault Enable</td>
<td>Bus</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:19</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>18</td>
<td>USAGE</td>
<td>RW</td>
<td>0</td>
<td>Usage Fault Enable</td>
</tr>
<tr>
<td>17</td>
<td>BUS</td>
<td>RW</td>
<td>0</td>
<td>Bus Fault Enable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Disables the usage fault exception.</td>
</tr>
<tr>
<td>1</td>
<td>Enables the usage fault exception.</td>
</tr>
<tr>
<td>0</td>
<td>Disables the bus fault exception.</td>
</tr>
<tr>
<td>1</td>
<td>Enables the bus fault exception.</td>
</tr>
</tbody>
</table>
### Memory Management Fault Enable

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>MEM</td>
<td>RW</td>
<td>0</td>
<td>Memory Management Fault Enable</td>
</tr>
</tbody>
</table>

- **Value**
  - 0: Disables the memory management fault exception.
  - 1: Enables the memory management fault exception.

### SVC Call Pending

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>SVC</td>
<td>RW</td>
<td>0</td>
<td>SVC Call Pending</td>
</tr>
</tbody>
</table>

- **Value**
  - 0: An SVC call exception is not pending.
  - 1: An SVC call exception is pending.

This bit can be modified to change the pending status of the SVC call exception.

### Bus Fault Pending

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>BUSP</td>
<td>RW</td>
<td>0</td>
<td>Bus Fault Pending</td>
</tr>
</tbody>
</table>

- **Value**
  - 0: A bus fault exception is not pending.
  - 1: A bus fault exception is pending.

This bit can be modified to change the pending status of the bus fault exception.

### Memory Management Fault Pending

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>MEMP</td>
<td>RW</td>
<td>0</td>
<td>Memory Management Fault Pending</td>
</tr>
</tbody>
</table>

- **Value**
  - 0: A memory management fault exception is not pending.
  - 1: A memory management fault exception is pending.

This bit can be modified to change the pending status of the memory management fault exception.

### Usage Fault Pending

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>USAGEP</td>
<td>RW</td>
<td>0</td>
<td>Usage Fault Pending</td>
</tr>
</tbody>
</table>

- **Value**
  - 0: A usage fault exception is not pending.
  - 1: A usage fault exception is pending.

This bit can be modified to change the pending status of the usage fault exception.

### SysTick Exception Active

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>TICK</td>
<td>RW</td>
<td>0</td>
<td>SysTick Exception Active</td>
</tr>
</tbody>
</table>

- **Value**
  - 0: A SysTick exception is not active.
  - 1: A SysTick exception is active.

This bit can be modified to change the active status of the SysTick exception, however, see the Caution above before setting this bit.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>PNDSV</td>
<td>RW</td>
<td>0</td>
<td>PendSV Exception Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  A PendSV exception is not active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  A PendSV exception is active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit can be modified to change the active status of the PendSV exception, however, see the Caution above before setting this bit.</td>
</tr>
<tr>
<td>9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>MON</td>
<td>RW</td>
<td>0</td>
<td>Debug Monitor Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The Debug monitor is not active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The Debug monitor is active.</td>
</tr>
<tr>
<td>7</td>
<td>SVCA</td>
<td>RW</td>
<td>0</td>
<td>SVC Call Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  SVC call is not active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  SVC call is active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit can be modified to change the active status of the SVC call exception, however, see the Caution above before setting this bit.</td>
</tr>
<tr>
<td>6:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>USGA</td>
<td>RW</td>
<td>0</td>
<td>Usage Fault Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Usage fault is not active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Usage fault is active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit can be modified to change the active status of the usage fault exception, however, see the Caution above before setting this bit.</td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>BUSA</td>
<td>RW</td>
<td>0</td>
<td>Bus Fault Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Bus fault is not active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Bus fault is active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit can be modified to change the active status of the bus fault exception, however, see the Caution above before setting this bit.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>MEMA</td>
<td>RW</td>
<td>0</td>
<td>Memory Management Fault Active</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Memory management fault is not active.</td>
</tr>
<tr>
<td>1</td>
<td>Memory management fault is active.</td>
</tr>
</tbody>
</table>

This bit can be modified to change the active status of the memory management fault exception, however, see the Caution above before setting this bit.
Register 76: Configurable Fault Status (FAULTSTAT), offset 0xD28

Note: This register can only be accessed from privileged mode.

The FAULTSTAT register indicates the cause of a memory management fault, bus fault, or usage fault. Each of these functions is assigned to a subregister as follows:

- Usage Fault Status (UFAULTSTAT), bits 31:16
- Bus Fault Status (BFAULTSTAT), bits 15:8
- Memory Management Fault Status (MFAULTSTAT), bits 7:0

FAULTSTAT is byte accessible. FAULTSTAT or its subregisters can be accessed as follows:

- The complete FAULTSTAT register, with a word access to offset 0xD28
- The MFAULTSTAT, with a byte access to offset 0xD28
- The MFAULTSTAT and BFAULTSTAT, with a halfword access to offset 0xD28
- The BFAULTSTAT, with a byte access to offset 0xD29
- The UFAULTSTAT, with a halfword access to offset 0xD2A

Bits are cleared by writing a 1 to them.

In a fault handler, the true faulting address can be determined by:

1. Read and save the Memory Management Fault Address (MMADDR) or Bus Fault Address (FAULTADDR) value.
2. Read the MMARV bit in MFAULTSTAT, or the BFARV bit in BFAULTSTAT to determine if the MMADDR or FAULTADDR contents are valid.

Software must follow this sequence because another higher priority exception might change the MMADDR or FAULTADDR value. For example, if a higher priority handler preempts the current fault handler, the other fault might change the MMADDR or FAULTADDR value.

Configurable Fault Status (FAULTSTAT)

<table>
<thead>
<tr>
<th>Base 0xE000.E000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset 0xD28</td>
</tr>
<tr>
<td>Type RW1C, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Reset Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x00 RO reserved 31:26</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
</tr>
<tr>
<td>25</td>
<td>DIV0</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>UNALIGN</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>23:20</td>
<td>reserved</td>
</tr>
<tr>
<td>19</td>
<td>NOCP</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>INVPC</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>----------</td>
<td>-----------</td>
</tr>
<tr>
<td></td>
<td>INVSTAT</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>UNDEF</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>BFARV</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>reserved</td>
</tr>
<tr>
<td></td>
<td>BLSPERR</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
</tr>
<tr>
<td>12</td>
<td>BSTKE</td>
</tr>
<tr>
<td>11</td>
<td>BUSTKE</td>
</tr>
<tr>
<td>10</td>
<td>IMPRE</td>
</tr>
<tr>
<td>9</td>
<td>PRECISE</td>
</tr>
</tbody>
</table>

**Stack Bus Fault**

- **Value**: Description
  - 0: No bus fault has occurred on stacking for exception entry.
  - 1: Stacking for an exception entry has caused one or more bus faults.

When this bit is set, the SP is still adjusted but the values in the context area on the stack might be incorrect. A fault address is not written to the FAULTADDR register.

This bit is cleared by writing a 1 to it.

**Unstack Bus Fault**

- **Value**: Description
  - 0: No bus fault has occurred on unstacking for a return from exception.
  - 1: Unstacking for a return from exception has caused one or more bus faults.

This fault is chained to the handler. Thus, when this bit is set, the original return stack is still present. The SP is not adjusted from the failing return, a new save is not performed, and a fault address is not written to the FAULTADDR register.

This bit is cleared by writing a 1 to it.

**Imprecise Data Bus Error**

- **Value**: Description
  - 0: An imprecise data bus error has not occurred.
  - 1: A data bus error has occurred, but the return address in the stack frame is not related to the instruction that caused the error.

When this bit is set, a fault address is not written to the FAULTADDR register.

This fault is asynchronous. Therefore, if the fault is detected when the priority of the current process is higher than the bus fault priority, the bus fault becomes pending and becomes active only when the processor returns from all higher-priority processes. If a precise fault occurs before the processor enters the handler for the imprecise bus fault, the handler detects that both the IMPRE bit is set and one of the precise fault status bits is set.

This bit is cleared by writing a 1 to it.

**Precise Data Bus Error**

- **Value**: Description
  - 0: A precise data bus error has not occurred.
  - 1: A data bus error has occurred, and the PC value stacked for the exception return points to the instruction that caused the fault.

When this bit is set, the fault address is written to the FAULTADDR register.

This bit is cleared by writing a 1 to it.
### Bit/Field Name Type Reset Description

#### IBUS
- **Type**: RW1C
- **Reset**: 0
- **Description**: Instruction Bus Error
  - **Value Description**:
    - 0: An instruction bus error has not occurred.
    - 1: An instruction bus error has occurred.
  - The processor detects the instruction bus error on prefetching an instruction, but sets this bit only if it attempts to issue the faulting instruction.
  - When this bit is set, a fault address is not written to the $\text{FAULTADDR}$ register.
  - This bit is cleared by writing a 1 to it.

#### MMARV
- **Type**: RW1C
- **Reset**: 0
- **Description**: Memory Management Fault Address Register Valid
  - **Value Description**:
    - 0: The value in the Memory Management Fault Address (MMADDR) register is not a valid fault address.
    - 1: The MMADDR register is holding a valid fault address.
  - If a memory management fault occurs and is escalated to a hard fault because of priority, the hard fault handler must clear this bit. This action prevents problems if returning to a stacked active memory management fault handler whose MMADDR register value has been overwritten.
  - This bit is cleared by writing a 1 to it.

#### reserved
- **Type**: RO
- **Reset**: 0
- **Description**: Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

#### MLSPERR
- **Type**: RW1C
- **Reset**: 0
- **Description**: Memory Management Fault on Floating-Point Lazy State Preservation
  - **Value Description**:
    - 0: No memory management fault has occurred during floating-point lazy state preservation.
    - 1: No memory management fault has occurred during floating-point lazy state preservation.
  - This bit is cleared by writing a 1 to it.

#### MSTKE
- **Type**: RW1C
- **Reset**: 0
- **Description**: Stack Access Violation
  - **Value Description**:
    - 0: No memory management fault has occurred on stacking for exception entry.
    - 1: Stacking for an exception entry has caused one or more access violations.
  - When this bit is set, the SP is still adjusted but the values in the context area on the stack might be incorrect. A fault address is not written to the MMADDR register.
  - This bit is cleared by writing a 1 to it.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>MUSTKE</td>
<td>RW1C</td>
<td>0</td>
<td>Unstack Access Violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   No memory management fault has occurred on unstacking for a return from exception.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Unstacking for a return from exception has caused one or more access violations.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This fault is chained to the handler. Thus, when this bit is set, the original return stack is still present. The SP is not adjusted from the failing return, a new save is not performed, and a fault address is not written to the MMADDR register. This bit is cleared by writing a 1 to it.</td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>DERR</td>
<td>RW1C</td>
<td>0</td>
<td>Data Access Violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   A data access violation has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   The processor attempted a load or store at a location that does not permit the operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, the PC value stacked for the exception return points to the faulting instruction and the address of the attempted access is written to the MMADDR register. This bit is cleared by writing a 1 to it.</td>
</tr>
<tr>
<td>0</td>
<td>IERR</td>
<td>RW1C</td>
<td>0</td>
<td>Instruction Access Violation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   An instruction access violation has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   The processor attempted an instruction fetch from a location that does not permit execution.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This fault occurs on any access to an XN region, even when the MPU is disabled or not present. When this bit is set, the PC value stacked for the exception return points to the faulting instruction and the address of the attempted access is not written to the MMADDR register. This bit is cleared by writing a 1 to it.</td>
</tr>
</tbody>
</table>
Register 77: Hard Fault Status (HFAULTSTAT), offset 0xD2C

**Note:** This register can only be accessed from privileged mode.

The **HFAULTSTAT** register gives information about events that activate the hard fault handler.

Bits are cleared by writing a 1 to them.

### Hard Fault Status (HFAULTSTAT)

Base 0xE000.E000
Offset 0xD2C
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31        | DBG           | RW1C   | 0     | Debug Event
This bit is reserved for Debug use. This bit must be written as a 0, otherwise behavior is unpredictable. |
| 30        | FORCED        | RW1C   | 0     | Forced Hard Fault
Value Description
0  No forced hard fault has occurred. |
1  A forced hard fault has been generated by escalation of a fault with configurable priority that cannot be handled, either because of priority or because it is disabled. |
When this bit is set, the hard fault handler must read the other fault status registers to find the cause of the fault. This bit is cleared by writing a 1 to it. |
| 29:2      | reserved      | RO     | 0x00  | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 1         | VECT          | RW1C   | 0     | Vector Table Read Fault
Value Description
0  No bus fault has occurred on a vector table read. |
1  A bus fault occurred on a vector table read. |
This error is always handled by the hard fault handler. When this bit is set, the PC value stacked for the exception return points to the instruction that was preempted by the exception. This bit is cleared by writing a 1 to it. |
| 0         | reserved      | RO     | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
Register 78: Memory Management Fault Address (MMADDR), offset 0xD34

**Note:** This register can only be accessed from privileged mode.

The MMADDR register contains the address of the location that generated a memory management fault. When an unaligned access faults, the address in the MMADDR register is the actual address that faulted. Because a single read or write instruction can be split into multiple aligned accesses, the fault address can be any address in the range of the requested access size. Bits in the Memory Management Fault Status (MFAULTSTAT) register indicate the cause of the fault and whether the value in the MMADDR register is valid (see page 177).

Memory Management Fault Address (MMADDR)
Base 0xE000.E000
Offset 0xD34
Type RW, reset -

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>ADDR</td>
<td>RW</td>
<td>Fault Address</td>
</tr>
</tbody>
</table>

When the MMARV bit of MFAULTSTAT is set, this field holds the address of the location that generated the memory management fault.
Register 79: Bus Fault Address (FAULTADDR), offset 0xD38

**Note:** This register can only be accessed from privileged mode.

The **FAULTADDR** register contains the address of the location that generated a bus fault. When an unaligned access faults, the address in the **FAULTADDR** register is the one requested by the instruction, even if it is not the address of the fault. Bits in the **Bus Fault Status (BFAULTSTAT)** register indicate the cause of the fault and whether the value in the **FAULTADDR** register is valid (see page 177).

### Bus Fault Address (FAULTADDR)

Base 0xE000.E000
Offset 0xD38
Type RW, reset -

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>29</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>28</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>27</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>26</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>25</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>24</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>23</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>22</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>21</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>20</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>19</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>18</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>17</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>16</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>14</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>13</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>12</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>11</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>-</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

**Bit/Field**  **Name**  **Type**  **Reset**  **Description**

31:0  **ADDR**  **RW**  -  Fault Address

When the **FAULTADDRV** bit of **BFAULTSTAT** is set, this field holds the address of the location that generated the bus fault.

### 3.6 Memory Protection Unit (MPU) Register Descriptions

This section lists and describes the Memory Protection Unit (MPU) registers, in numerical order by address offset.

The MPU registers can only be accessed from privileged mode.
Register 80: MPU Type (MPUTYPE), offset 0xD90

Note: This register can only be accessed from privileged mode.

The MPUTYPE register indicates whether the MPU is present, and if so, how many regions it supports.

### MPU Type (MPUTYPE)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000.E000</td>
<td>0xD90</td>
<td>RO</td>
<td>0x0000.0800</td>
<td>RO</td>
<td></td>
</tr>
</tbody>
</table>

#### Bit/Field Name Type Reset Description

| 31:24 | reserved | RO  | 0x00 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 23:16 | IREGION  | RO  | 0x00 | Number of I Regions This field indicates the number of supported MPU instruction regions. This field always contains 0x00. The MPU memory map is unified and is described by the DREGION field. |
| 15:8  | DREGION  | RO  | 0x08 | Number of D Regions |
| 7:1   | reserved | RO  | 0x00 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 0     | SEPARATE | RO  | 0    | Separate or Unified MPU |

Value Description

0x08 Indicates there are eight supported MPU data regions.
Register 81: MPU Control (MPUCTRL), offset 0xD94

Note: This register can only be accessed from privileged mode.

The MPUCTRL register enables the MPU, enables the default memory map background region, and enables use of the MPU when in the hard fault, Non-maskable Interrupt (NMI), and Fault Mask Register (FAULTMASK) escalated handlers.

When the ENABLE and PRIVDEFEN bits are both set:

- For privileged accesses, the default memory map is as described in "Memory Model" on page 92. Any access by privileged software that does not address an enabled memory region behaves as defined by the default memory map.

- Any access by unprivileged software that does not address an enabled memory region causes a memory management fault.

Execute Never (XN) and Strongly Ordered rules always apply to the System Control Space regardless of the value of the ENABLE bit.

When the ENABLE bit is set, at least one region of the memory map must be enabled for the system to function unless the PRIVDEFEN bit is set. If the PRIVDEFEN bit is set and no regions are enabled, then only privileged software can operate.

When the ENABLE bit is clear, the system uses the default memory map, which has the same memory attributes as if the MPU is not implemented (see Table 2-5 on page 96 for more information). The default memory map applies to accesses from both privileged and unprivileged software.

When the MPU is enabled, accesses to the System Control Space and vector table are always permitted. Other areas are accessible based on regions and whether PRIVDEFEN is set.

Unless HFNMIENA is set, the MPU is not enabled when the processor is executing the handler for an exception with priority −1 or −2. These priorities are only possible when handling a hard fault or NMI exception or when FAULTMASK is enabled. Setting the HFNMIENA bit enables the MPU when operating with these two priorities.
### Cortex-M4 Peripherals

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 2         | PRIVDEFEN   | RW   | 0     | MPU Default Region  
This bit enables privileged software access to the default memory map.  

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>If the MPU is enabled, this bit disables use of the default memory map. Any memory access to a location not covered by any enabled region causes a fault.</td>
</tr>
<tr>
<td>1</td>
<td>If the MPU is enabled, this bit enables use of the default memory map as a background region for privileged software accesses.</td>
</tr>
</tbody>
</table>

When this bit is set, the background region acts as if it is region number -1. Any region that is defined and enabled has priority over this default map.  
If the MPU is disabled, the processor ignores this bit. |

| 1      | HFNMIENA    | RW   | 0     | MPU Enabled During Faults  
This bit controls the operation of the MPU during hard fault, NMI, and FAULTMASK handlers.  

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The MPU is disabled during hard fault, NMI, and FAULTMASK handlers, regardless of the value of the ENABLE bit.</td>
</tr>
<tr>
<td>1</td>
<td>The MPU is enabled during hard fault, NMI, and FAULTMASK handlers.</td>
</tr>
</tbody>
</table>

When the MPU is disabled and this bit is set, the resulting behavior is unpredictable. |

| 0      | ENABLE      | RW   | 0     | MPU Enable  
Value Description  

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The MPU is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>The MPU is enabled.</td>
</tr>
</tbody>
</table>

When the MPU is disabled and the HFNMIENA bit is set, the resulting behavior is unpredictable. |
Register 82: MPU Region Number (MPUNUMBER), offset 0xD98

Note: This register can only be accessed from privileged mode.

The MPUNUMBER register selects which memory region is referenced by the MPU Region Base Address (MPUBASE) and MPU Region Attribute and Size (MPUATTR) registers. Normally, the required region number should be written to this register before accessing the MPUBASE or the MPUATTR register. However, the region number can be changed by writing to the MPUBASE register with the VALID bit set (see page 190). This write updates the value of the REGION field.

MPU Region Number (MPUNUMBER)
Base 0xE000.E000
Offset 0xD98
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 2:0       | NUMBER        | RW   | 0x0   | MPU Region to Access
This field indicates the MPU region referenced by the MPUBASE and MPUATTR registers. The MPU supports eight memory regions. |
Register 83: MPU Region Base Address (MPUBASE), offset 0xD9C
Register 84: MPU Region Base Address Alias 1 (MPUBASE1), offset 0xDA4
Register 85: MPU Region Base Address Alias 2 (MPUBASE2), offset 0xDAC
Register 86: MPU Region Base Address Alias 3 (MPUBASE3), offset 0xDB4

**Note:** This register can only be accessed from privileged mode.

The **MPUBASE** register defines the base address of the MPU region selected by the MPU Region Number (MPUNUMBER) register and can update the value of the MPUNUMBER register. To change the current region number and update the MPUNUMBER register, write the MPUBASE register with the **VALID** bit set.

The **ADDR** field is bits 31:/N of the **MPUBASE** register. Bits (N-1):5 are reserved. The region size, as specified by the **SIZE** field in the MPU Region Attribute and Size (MPUATTR) register, defines the value of N where:

\[ N = \log_2(\text{Region size in bytes}) \]

If the region size is configured to 4 GB in the MPUATTR register, there is no valid ADDR field. In this case, the region occupies the complete memory map, and the base address is 0x0000.0000.

The base address is aligned to the size of the region. For example, a 64-KB region must be aligned on a multiple of 64 KB, for example, at 0x0001.0000 or 0x0002.0000.

### MPU Region Base Address (MPUBASE)

Base 0xE000.E000
Offset 0xD9C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>29</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>28</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>27</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>26</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>25</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>24</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>23</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>22</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>21</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>20</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>19</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>18</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>17</td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>16</td>
<td>RW</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>REGION</th>
<th>VALID</th>
<th>reserved</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>14</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>13</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>ADDR</td>
<td>RW</td>
<td>0x0000.000</td>
<td>Base Address Mask</td>
</tr>
</tbody>
</table>

Bits 31:/N in this field contain the region base address. The value of N depends on the region size, as shown above. The remaining bits (N-1):5 are reserved.

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
### Description

#### Region Number Valid

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>VALID</td>
<td>WO</td>
<td>0</td>
<td>Region Number Valid</td>
</tr>
</tbody>
</table>

#### Value Description

0  The MPNUMBER register is not changed and the processor updates the base address for the region specified in the MPNUMBER register and ignores the value of the REGION field.

1  The MPNUMBER register is updated with the value of the REGION field and the base address is updated for the region specified in the REGION field.

This bit is always read as 0.

#### Region Number

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2:0</td>
<td>REGION</td>
<td>RW</td>
<td>0x0</td>
<td>Region Number</td>
</tr>
</tbody>
</table>

On a write, contains the value to be written to the MPNUMBER register. On a read, returns the current region number in the MPNUMBER register.
Register 87: MPU Region Attribute and Size (MPUATTR), offset 0xDA0
Register 88: MPU Region Attribute and Size Alias 1 (MPUATTR1), offset 0xDA8
Register 89: MPU Region Attribute and Size Alias 2 (MPUATTR2), offset 0xDB0
Register 90: MPU Region Attribute and Size Alias 3 (MPUATTR3), offset 0xDB8

**Note:** This register can only be accessed from privileged mode.

The MPUATTR register defines the region size and memory attributes of the MPU region specified by the MPU Region Number (MPUNUMBER) register and enables that region and any subregions.

The MPUATTR register is accessible using word or halfword accesses with the most-significant halfword holding the region attributes and the least-significant halfword holds the region size and the region and subregion enable bits.

The MPU access permission attribute bits, XN, AP, TEX, S, C, and B, control access to the corresponding memory region. If an access is made to an area of memory without the required permissions, then the MPU generates a permission fault.

The SIZE field defines the size of the MPU memory region specified by the MPUNUMBER register as follows:

\[(\text{Region size in bytes}) = 2^{\text{SIZE}+1}\]

The smallest permitted region size is 32 bytes, corresponding to a SIZE value of 4. Table 3-10 on page 192 gives example SIZE values with the corresponding region size and value of N in the MPU Region Base Address (MPUBASE) register.

### Table 3-10. Example SIZE Field Values

<table>
<thead>
<tr>
<th>SIZE Encoding</th>
<th>Region Size</th>
<th>Value of N^a</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>00100b (0x4)</td>
<td>32 B</td>
<td>5</td>
<td>Minimum permitted size</td>
</tr>
<tr>
<td>01001b (0x9)</td>
<td>1 KB</td>
<td>10</td>
<td>-</td>
</tr>
<tr>
<td>10011b (0x13)</td>
<td>1 MB</td>
<td>20</td>
<td>-</td>
</tr>
<tr>
<td>11101b (0x1D)</td>
<td>1 GB</td>
<td>30</td>
<td>-</td>
</tr>
<tr>
<td>11111b (0x1F)</td>
<td>4 GB</td>
<td>No valid ADDR field in MPUBASE; the region occupies the complete memory map.</td>
<td>Maximum possible size</td>
</tr>
</tbody>
</table>

^a. Refers to the N parameter in the MPUBASE register (see page 190).

---

**MPU Region Attribute and Size (MPUATTR)**

Base 0xE000.E000
Offset 0xDA0
Type RW, reset 0x0000.0000

---

**MPU Region Attribute and Size (MPUATTR)**

Base 0xE000.E000
Offset 0xDA0
Type RW, reset 0x0000.0000

---

**Texas Instruments-Production Data**

June 12, 2014
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>28</td>
<td>XN</td>
<td>RW</td>
<td>0</td>
<td>Instruction Access Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Instruction fetches are enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Instruction fetches are disabled.</td>
</tr>
<tr>
<td>27</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>26:24</td>
<td>AP</td>
<td>RW</td>
<td>0</td>
<td>Access Privilege</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For information on using this bit field, see Table 3-5 on page 129.</td>
</tr>
<tr>
<td>23:22</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>21:19</td>
<td>TEX</td>
<td>RW</td>
<td>0x0</td>
<td>Type Extension Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For information on using this bit field, see Table 3-3 on page 128.</td>
</tr>
<tr>
<td>18</td>
<td>S</td>
<td>RW</td>
<td>0</td>
<td>Shareable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For information on using this bit, see Table 3-3 on page 128.</td>
</tr>
<tr>
<td>17</td>
<td>C</td>
<td>RW</td>
<td>0</td>
<td>Cacheable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For information on using this bit, see Table 3-3 on page 128.</td>
</tr>
<tr>
<td>16</td>
<td>B</td>
<td>RW</td>
<td>0</td>
<td>Bufferable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For information on using this bit, see Table 3-3 on page 128.</td>
</tr>
<tr>
<td>15:8</td>
<td>SRD</td>
<td>RW</td>
<td>0x00</td>
<td>Subregion Disable Bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The corresponding subregion is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The corresponding subregion is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Region sizes of 128 bytes and less do not support subregions. When writing the attributes for such a region, configure the SRD field as 0x00. Refer to the section called “Subregions” on page 128 for more information.</td>
</tr>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5:1</td>
<td>SIZE</td>
<td>RW</td>
<td>0x0</td>
<td>Region Size Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The SIZE field defines the size of the MPU memory region specified by the MPUNUMBER register. Refer to Table 3-10 on page 192 for more information.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------</td>
</tr>
<tr>
<td>0</td>
<td>ENABLE</td>
<td>RW</td>
<td>0</td>
<td>Region Enable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The region is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>The region is enabled.</td>
</tr>
</tbody>
</table>

### 3.7 Floating-Point Unit (FPU) Register Descriptions

This section lists and describes the Floating-Point Unit (FPU) registers, in numerical order by address offset.
# Register 91: Coprocessor Access Control (CPAC), offset 0xD88

The **CPAC** register specifies the access privileges for coprocessors.

### Coprocessor Access Control (CPAC)

Base 0xE000.E000  
Offset 0xD88  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23:22</td>
<td>CP11</td>
<td>RW</td>
<td>0x00</td>
<td>CP11 Coprocessor Access Privilege</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0  Access Denied</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Any attempted access generates a NOCP Usage Fault.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1  Privileged Access Only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>An unprivileged access generates a NOCP fault.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2  Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The result of any access is unpredictable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3  Full Access</td>
</tr>
<tr>
<td>21:20</td>
<td>CP10</td>
<td>RW</td>
<td>0x00</td>
<td>CP10 Coprocessor Access Privilege</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0  Access Denied</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Any attempted access generates a NOCP Usage Fault.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1  Privileged Access Only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>An unprivileged access generates a NOCP fault.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2  Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The result of any access is unpredictable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3  Full Access</td>
</tr>
<tr>
<td>19:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

---

**June 12, 2014**  
*Texas Instruments-Production Data*
Register 92: Floating-Point Context Control (FPCC), offset 0xF34

The FPCC register sets or returns FPU control data.

Floating-Point Context Control (FPCC)

Base 0xE000.E000
Offset 0xF34
Type RW, reset 0xC000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ASPEN</td>
<td>RW</td>
<td>1</td>
<td>Automatic State Preservation Enable</td>
</tr>
<tr>
<td>30</td>
<td>LSPEN</td>
<td>RW</td>
<td>1</td>
<td>Lazy State Preservation Enable</td>
</tr>
<tr>
<td>29:9</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>MONRDY</td>
<td>RW</td>
<td>0</td>
<td>Monitor Ready</td>
</tr>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6</td>
<td>BFRDY</td>
<td>RW</td>
<td>0</td>
<td>Bus Fault Ready</td>
</tr>
<tr>
<td>5</td>
<td>MMRDY</td>
<td>RW</td>
<td>0</td>
<td>Memory Management Fault Ready</td>
</tr>
</tbody>
</table>

Important: Two bits control when FPCA can be enabled: the ASPEN bit in the Floating-Point Context Control (FPCC) register and the DISFPCA bit in the Auxiliary Control (ACTLR) register.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 4        | HFRDY    | RW   | 0     | Hard Fault Ready  
When set, priority permitted setting the HardFault handler to the pending state when the floating-point stack frame was allocated. |
| 3        | THREAD   | RW   | 0     | Thread Mode  
When set, mode was Thread Mode when the floating-point stack frame was allocated. |
| 2        | reserved | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 1        | USER     | RW   | 0     | User Privilege Level  
When set, privilege level was user when the floating-point stack frame was allocated. |
| 0        | LSPACT   | RW   | 0     | Lazy State Preservation Active  
When set, Lazy State preservation is active. Floating-point stack frame has been allocated but saving state to it has been deferred. |
Register 93: Floating-Point Context Address (FPCA), offset 0xF38

The **FPCA** register holds the location of the unpopulated floating-point register space allocated on an exception stack frame.

Floating-Point Context Address (FPCA)

Base 0xE000.E000
Offset 0xF38
Type RW, reset -

---

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>ADDRESS</td>
<td>RW</td>
<td>-</td>
<td>Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The location of the unpopulated floating-point register space allocated on an exception stack frame.</td>
</tr>
<tr>
<td>2:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 94: Floating-Point Default Status Control (FPDSC), offset 0xF3C

The FPDSC register holds the default values for the Floating-Point Status Control (FPSC) register.

Floating-Point Default Status Control (FPDSC)

Base 0xE000.E000
Offset 0xF3C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>26</td>
<td>AHP</td>
<td>RW</td>
<td>-</td>
<td>AHP Bit Default</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit holds the default value for the AHP bit in the FPSC register.</td>
</tr>
<tr>
<td>25</td>
<td>DN</td>
<td>RW</td>
<td>-</td>
<td>DN Bit Default</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit holds the default value for the DN bit in the FPSC register.</td>
</tr>
<tr>
<td>24</td>
<td>FZ</td>
<td>RW</td>
<td>-</td>
<td>FZ Bit Default</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit holds the default value for the FZ bit in the FPSC register.</td>
</tr>
<tr>
<td>23:22</td>
<td>RMODE</td>
<td>RW</td>
<td>-</td>
<td>RMODE Bit Default</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit holds the default value for the RMODE bit field in the FPSC register.</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x0</td>
<td>Round to Nearest (RN) mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>Round towards Plus Infinity (RP) mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2</td>
<td>Round towards Minus Infinity (RM) mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x3</td>
<td>Round towards Zero (RZ) mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
4 JTAG Interface

The Joint Test Action Group (JTAG) port is an IEEE standard that defines a Test Access Port and Boundary Scan Architecture for digital integrated circuits and provides a standardized serial interface for controlling the associated test logic. The TAP, Instruction Register (IR), and Data Registers (DR) can be used to test the interconnections of assembled printed circuit boards and obtain manufacturing information on the components. The JTAG Port also provides a means of accessing and controlling design-for-test features such as I/O pin observation and control, scan testing, and debugging.

The JTAG port is comprised of four pins: TCK, TMS, TDI, and TDO. Data is transmitted serially into the controller on TDI and out of the controller on TDO. The interpretation of this data is dependent on the current state of the TAP controller. For detailed information on the operation of the JTAG port and TAP controller, please refer to the IEEE Standard 1149.1-Test Access Port and Boundary-Scan Architecture.

The TM4C123GH6PZ JTAG controller works with the ARM JTAG controller built into the Cortex-M4F core by multiplexing the TDO outputs from both JTAG controllers. ARM JTAG instructions select the ARM TDO output while JTAG instructions select the TDO output. The multiplexer is controlled by the JTAG controller, which has comprehensive programming for the ARM, Tiva™ C Series microcontroller, and unimplemented JTAG instructions.

The TM4C123GH6PZ JTAG module has the following features:

- IEEE 1149.1-1990 compatible Test Access Port (TAP) controller
- Four-bit Instruction Register (IR) chain for storing JTAG instructions
- IEEE standard instructions: BYPASS, IDCODE, SAMPLE/PRELOAD, and EXTEST
- ARM additional instructions: APACC, DPACC and ABORT
- Integrated ARM Serial Wire Debug (SWD)
  - Serial Wire JTAG Debug Port (SWJ-DP)
  - Flash Patch and Breakpoint (FPB) unit for implementing breakpoints
  - Data Watchpoint and Trace (DWT) unit for implementing watchpoints, trigger resources, and system profiling
  - Instrumentation Trace Macrocell (ITM) for support of printf style debugging
  - Embedded Trace Macrocell (ETM) for instruction trace capture
  - Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer

See the ARM® Debug Interface V5 Architecture Specification for more information on the ARM JTAG controller.
4.1 Block Diagram

Figure 4-1. JTAG Module Block Diagram

4.2 Signal Description

The following table lists the external signals of the JTAG/SWD controller and describes the function of each. The JTAG/SWD controller signals are alternate functions for some GPIO signals, however note that the reset state of the pins is for the JTAG/SWD function. The JTAG/SWD controller signals are under commit protection and require a special process to be configured as GPIOs, see “Commit Control” on page 667. The column in the table below titled "Pin Mux/Pin Assignment" lists the GPIO pin placement for the JTAG/SWD controller signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) is set to choose the JTAG/SWD function. The number in parentheses is the encoding that must be programmed into the PMCn field in the GPIO Port Control (GPIOPCTL) register (page 702) to assign the JTAG/SWD controller signals to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659.

Table 4-1. JTAG_SWD_SWO Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWCLK</td>
<td>85</td>
<td>PC0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>JTAG/SWD CLK.</td>
</tr>
<tr>
<td>SWDO</td>
<td>84</td>
<td>PC1 (1)</td>
<td>I/O</td>
<td>TTL</td>
<td>JTAG TMS and SWDO.</td>
</tr>
<tr>
<td>SWO</td>
<td>82</td>
<td>PC3 (1)</td>
<td>O</td>
<td>TTL</td>
<td>JTAG TDO and SWO.</td>
</tr>
<tr>
<td>TCK</td>
<td>85</td>
<td>PC0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>JTAG/SWD CLK.</td>
</tr>
<tr>
<td>TDI</td>
<td>83</td>
<td>PC2 (1)</td>
<td>I</td>
<td>TTL</td>
<td>JTAG TDI.</td>
</tr>
<tr>
<td>TDO</td>
<td>82</td>
<td>PC3 (1)</td>
<td>O</td>
<td>TTL</td>
<td>JTAG TDO and SWO.</td>
</tr>
</tbody>
</table>
### 4.3 Functional Description

A high-level conceptual drawing of the JTAG module is shown in Figure 4-1 on page 201. The JTAG module is composed of the Test Access Port (TAP) controller and serial shift chains with parallel update registers. The TAP controller is a simple state machine controlled by the \text{TCK} and \text{TMS} inputs. The current state of the TAP controller depends on the sequence of values captured on \text{TMS} at the rising edge of \text{TCK}. The TAP controller determines when the serial shift chains capture new data, shift data from \text{TDI} towards \text{TDO}, and update the parallel load registers. The current state of the TAP controller also determines whether the Instruction Register (IR) chain or one of the Data Register (DR) chains is being accessed.

The serial shift chains with parallel load registers are comprised of a single Instruction Register (IR) chain and multiple Data Register (DR) chains. The current instruction loaded in the parallel load register determines which DR chain is captured, shifted, or updated during the sequencing of the TAP controller.

Some instructions, like \text{EXTEST}, operate on data currently in a DR chain and do not capture, shift, or update any of the chains. Instructions that are not implemented decode to the \text{BYPASS} instruction to ensure that the serial path between \text{TDI} and \text{TDO} is always connected (see Table 4-3 on page 208 for a list of implemented instructions).

See “JTAG and Boundary Scan” on page 1400 for JTAG timing diagrams.

**Note:** Of all the possible reset sources, only Power-On reset (POR) and the assertion of the \text{RST} input have any effect on the JTAG module. The pin configurations are reset by both the \text{RST} input and POR, whereas the internal JTAG logic is only reset with POR. See “Reset Sources” on page 213 for more information on reset.

### 4.3.1 JTAG Interface Pins

The JTAG interface consists of four standard pins: \text{TCK}, \text{TMS}, \text{TDI}, and \text{TDO}. These pins and their associated state after a power-on reset or reset caused by the \text{RST} input are given in Table 4-2. Detailed information on each pin follows.

**Note:** The following pins are configured as JTAG port pins out of reset. Refer to “General-Purpose Input/Outputs (GPIOs)” on page 659 for information on how to reprogram the configuration of these pins.

#### Table 4-2. JTAG Port Pins State after Power-On Reset or \text{RST} assertion

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Data Direction</th>
<th>Internal Pull-Up</th>
<th>Internal Pull-Down</th>
<th>Drive Strength</th>
<th>Drive Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>\text{TCK}</td>
<td>Input</td>
<td>Enabled</td>
<td>Disabled</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>\text{TMS}</td>
<td>Input</td>
<td>Enabled</td>
<td>Disabled</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>\text{TDI}</td>
<td>Input</td>
<td>Enabled</td>
<td>Disabled</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>\text{TDO}</td>
<td>Output</td>
<td>Enabled</td>
<td>Disabled</td>
<td>2-mA driver</td>
<td>High-Z</td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.
4.3.1.1 Test Clock Input (TCK)

The TCK pin is the clock for the JTAG module. This clock is provided so the test logic can operate independently of any other system clocks and to ensure that multiple JTAG TAP controllers that are daisy-chained together can synchronously communicate serial test data between components. During normal operation, TCK is driven by a free-running clock with a nominal 50% duty cycle. When necessary, TCK can be stopped at 0 or 1 for extended periods of time. While TCK is stopped at 0 or 1, the state of the TAP controller does not change and data in the JTAG Instruction and Data Registers is not lost.

By default, the internal pull-up resistor on the TCK pin is enabled after reset, assuring that no clocking occurs if the pin is not driven from an external source. The internal pull-up and pull-down resistors can be turned off to save internal power as long as the TCK pin is constantly being driven by an external source (see page 690 and page 692).

4.3.1.2 Test Mode Select (TMS)

The TMS pin selects the next state of the JTAG TAP controller. TMS is sampled on the rising edge of TCK. Depending on the current TAP state and the sampled value of TMS, the next state may be entered. Because the TMS pin is sampled on the rising edge of TCK, the IEEE Standard 1149.1 expects the value on TMS to change on the falling edge of TCK.

Holding TMS high for five consecutive TCK cycles drives the TAP controller state machine to the Test-Logic-Reset state. When the TAP controller enters the Test-Logic-Reset state, the JTAG module and associated registers are reset to their default values. This procedure should be performed to initialize the JTAG controller. The JTAG Test Access Port state machine can be seen in its entirety in Figure 4-2 on page 204.

By default, the internal pull-up resistor on the TMS pin is enabled after reset. Changes to the pull-up resistor settings on GPIO Port C should ensure that the internal pull-up resistor remains enabled on PC1/TMS; otherwise JTAG communication could be lost (see page 690).

4.3.1.3 Test Data Input (TDI)

The TDI pin provides a stream of serial information to the IR chain and the DR chains. TDI is sampled on the rising edge of TCK and, depending on the current TAP state and the current instruction, may present this data to the proper shift register chain. Because the TDI pin is sampled on the rising edge of TCK, the IEEE Standard 1149.1 expects the value on TDI to change on the falling edge of TCK.

By default, the internal pull-up resistor on the TDI pin is enabled after reset. Changes to the pull-up resistor settings on GPIO Port C should ensure that the internal pull-up resistor remains enabled on PC2/TDI; otherwise JTAG communication could be lost (see page 690).

4.3.1.4 Test Data Output (TDO)

The TDO pin provides an output stream of serial information from the IR chain or the DR chains. The value of TDO depends on the current TAP state, the current instruction, and the data in the chain being accessed. In order to save power when the JTAG port is not being used, the TDO pin is placed in an inactive drive state when not actively shifting out data. Because TDO can be connected to the TDI of another controller in a daisy-chain configuration, the IEEE Standard 1149.1 expects the value on TDO to change on the falling edge of TCK.

By default, the internal pull-up resistor on the TDO pin is enabled after reset, assuring that the pin remains at a constant logic level when the JTAG port is not being used. The internal pull-up and
pull-down resistors can be turned off to save internal power if a High-Z output value is acceptable during certain TAP controller states (see page 690 and page 692).

### 4.3.2 JTAG TAP Controller

The JTAG TAP controller state machine is shown in Figure 4-2. The TAP controller state machine is reset to the Test-Logic-Reset state on the assertion of a Power-On-Reset (POR). In order to reset the JTAG module after the microcontroller has been powered on, the TMS input must be held HIGH for five TCK clock cycles, resetting the TAP controller and all associated JTAG chains. Asserting the correct sequence on the TMS pin allows the JTAG module to shift in new instructions, shift in data, or idle during extended testing sequences. For detailed information on the function of the TAP controller and the operations that occur in each state, please refer to IEEE Standard 1149.1.

![Figure 4-2. Test Access Port State Machine](image)

### 4.3.3 Shift Registers

The Shift Registers consist of a serial shift register chain and a parallel load register. The serial shift register chain samples specific information during the TAP controller's CAPTURE states and allows this information to be shifted out on TDO during the TAP controller's SHIFT states. While the sampled data is being shifted out of the chain on TDO, new data is being shifted into the serial shift register on TDI. This new data is stored in the parallel load register during the TAP controller's UPDATE states. Each of the shift registers is discussed in detail in “Register Descriptions” on page 208.
4.3.4 Operational Considerations

Certain operational parameters must be considered when using the JTAG module. Because the JTAG pins can be programmed to be GPIOs, board configuration and reset conditions on these pins must be considered. In addition, because the JTAG module has integrated ARM Serial Wire Debug, the method for switching between these two operational modes is described below.

4.3.4.1 GPIO Functionality

When the microcontroller is reset with either a POR or RST, the JTAG/SWD port pins default to their JTAG/SWD configurations. The default configuration includes enabling digital functionality (DEN[3:0] set in the Port C GPIO Digital Enable (GPIODEN) register), enabling the pull-up resistors (PUE[3:0] set in the Port C GPIO Pull-Up Select (GPIOPUR) register), disabling the pull-down resistors (PDE[3:0] cleared in the Port C GPIO Pull-Down Select (GPIOPDR) register) and enabling the alternate hardware function (AFSEL[3:0] set in the Port C GPIO Alternate Function Select (GPIOAFSEL) register) on the JTAG/SWD pins. See page 684, page 690, page 692, and page 695.

It is possible for software to configure these pins as GPIOs after reset by clearing AFSEL[3:0] in the Port C GPIOAFSEL register. If the user does not require the JTAG/SWD port for debugging or board-level testing, this provides four more GPIOs for use in the design.

Caution – It is possible to create a software sequence that prevents the debugger from connecting to the TM4C123GH6PZ microcontroller. If the program code loaded into flash immediately changes the JTAG pins to their GPIO functionality, the debugger may not have enough time to connect and halt the controller before the JTAG pin functionality switches. As a result, the debugger may be locked out of the part. This issue can be avoided with a software routine that restores JTAG functionality based on an external or software trigger. In the case that the software routine is not implemented and the device is locked out of the part, this issue can be solved by using the TM4C123GH6PZ Flash Programmer "Unlock" feature. Please refer to LMFLASHPROGRAMMER on the TI web for more information.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is provided for the GPIO pins that can be used as the four JTAG/SWD pins and the NMI pin (see “Signal Tables” on page 1354 for pin numbers). Writes to protected bits of the GPIO Alternate Function Select (GPIOAFSEL) register (see page 684), GPIO Pull Up Select (GPIOPUR) register (see page 690), GPIO Pull-Down Select (GPIOPDR) register (see page 692), and GPIO Digital Enable (GPIODEN) register (see page 695) are not committed to storage unless the GPIO Lock (GPIOLOCK) register (see page 697) has been unlocked and the appropriate bits of the GPIO Commit (GPIOCR) register (see page 698) have been set.

4.3.4.2 Communication with JTAG/SWD

Because the debug clock and the system clock can be running at different frequencies, care must be taken to maintain reliable communication with the JTAG/SWD interface. In the Capture-DR state, the result of the previous transaction, if any, is returned, together with a 3-bit ACK response. Software should check the ACK response to see if the previous operation has completed before initiating a new transaction. Alternatively, if the system clock is at least 8 times faster than the debug clock (TCK or SWCLK), the previous operation has enough time to complete and the ACK bits do not have to be checked.

4.3.4.3 Recovering a "Locked" Microcontroller

Note: Performing the sequence below restores the non-volatile registers discussed in “Non-Volatile Register Programming” on page 542 to their factory default values. The mass erase of the Flash memory caused by the sequence below occurs prior to the non-volatile registers being restored.
In addition, the EEPROM is erased and its wear-leveling counters are returned to factory default values when performing the sequence below.

If software configures any of the JTAG/SWD pins as GPIO and loses the ability to communicate with the debugger, there is a debug port unlock sequence that can be used to recover the microcontroller. Performing a total of ten JTAG-to-SWD and SWD-to-JTAG switch sequences while holding the microcontroller in reset mass erases the Flash memory. The debug port unlock sequence is:

1. Assert and hold the RST signal.
2. Apply power to the device.
3. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence on the section called “JTAG-to-SWD Switching” on page 207.
4. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence on the section called “SWD-to-JTAG Switching” on page 207.
5. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence.
6. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence.
7. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence.
8. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence.
9. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence.
10. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence.
11. Perform steps 1 and 2 of the JTAG-to-SWD switch sequence.
12. Perform steps 1 and 2 of the SWD-to-JTAG switch sequence.
13. Release the RST signal.
14. Wait 400 ms.
15. Power-cycle the microcontroller.

4.3.4.4 ARM Serial Wire Debug (SWD)

In order to seamlessly integrate the ARM Serial Wire Debug (SWD) functionality, a serial-wire debugger must be able to connect to the Cortex-M4F core without having to perform, or have any knowledge of, JTAG cycles. This integration is accomplished with a SWD preamble that is issued before the SWD session begins.

The switching preamble used to enable the SWD interface of the SWJ-DP module starts with the TAP controller in the Test-Logic-Reset state. From here, the preamble sequences the TAP controller through the following states: Run Test Idle, Select DR, Select IR, Test Logic Reset, Test Logic Reset, Run Test Idle, Run Test Idle, Select DR, Select IR, Test Logic Reset, Test Logic Reset, Run Test Idle, Run Test Idle, Select DR, Select IR, and Test Logic Reset states.

Stepping through this sequence of the TAP state machine enables the SWD interface and disables the JTAG interface. For more information on this operation and the SWD interface, see the ARM® Debug Interface V5 Architecture Specification.
Because this sequence is a valid series of JTAG operations that could be issued, the ARM JTAG TAP controller is not fully compliant to the IEEE Standard 1149.1. This instance is the only one where the ARM JTAG TAP controller does not meet full compliance with the specification. Due to the low probability of this sequence occurring during normal operation of the TAP controller, it should not affect normal performance of the JTAG interface.

**JTAG-to-SWD Switching**

To switch the operating mode of the Debug Access Port (DAP) from JTAG to SWD mode, the external debug hardware must send the switching preamble to the microcontroller. The 16-bit TMS/SWDIO command for switching to SWD mode is defined as b1110.0111.1001.1110, transmitted LSB first. This command can also be represented as 0xE79E when transmitted LSB first. The complete switch sequence should consist of the following transactions on the TCK/SWCLK and TMS/SWDIO signals:

1. Send at least 50 TCK/SWCLK cycles with TMS/SWDIO High to ensure that both JTAG and SWD are in their reset states.
2. Send the 16-bit JTAG-to-SWD switch command, 0xE79E, on TMS/SWDIO.
3. Send at least 50 TCK/SWCLK cycles with TMS/SWDIO High to ensure that if SWJ-DP was already in SWD mode before sending the switch sequence, the SWD goes into the line reset state.

To verify that the Debug Access Port (DAP) has switched to the Serial Wire Debug (SWD) operating mode, perform a SWD READID operation. The ID value can be compared against the device's known ID to verify the switch.

**SWD-to-JTAG Switching**

To switch the operating mode of the Debug Access Port (DAP) from SWD to JTAG mode, the external debug hardware must send a switch command to the microcontroller. The 16-bit TMS/SWDIO command for switching to JTAG mode is defined as b1110.0111.0011.1100, transmitted LSB first. This command can also be represented as 0xE73C when transmitted LSB first. The complete switch sequence should consist of the following transactions on the TCK/SWCLK and TMS/SWDIO signals:

1. Send at least 50 TCK/SWCLK cycles with TMS/SWDIO High to ensure that both JTAG and SWD are in their reset states.
2. Send the 16-bit SWD-to-JTAG switch command, 0xE73C, on TMS/SWDIO.
3. Send at least 50 TCK/SWCLK cycles with TMS/SWDIO High to ensure that if SWJ-DP was already in JTAG mode before sending the switch sequence, the JTAG goes into the Test Logic Reset state.

To verify that the Debug Access Port (DAP) has switched to the JTAG operating mode, set the JTAG Instruction Register (IR) to the IDCODE instruction and shift out the Data Register (DR). The DR value can be compared against the device's known IDCODE to verify the switch.

### 4.4 Initialization and Configuration

After a Power-On-Reset or an external reset (RST), the JTAG pins are automatically configured for JTAG communication. No user-defined initialization or configuration is needed. However, if the user application changes these pins to their GPIO function, they must be configured back to their JTAG functionality before JTAG communication can be restored. To return the pins to their JTAG functions, enable the four JTAG pins (PC[3:0]) for their alternate function using the GPIOAFSEL register.
In addition to enabling the alternate functions, any other changes to the GPIO pad configurations on the four JTAG pins ($PC[3:0]$) should be returned to their default settings.

### 4.5 Register Descriptions

The registers in the JTAG TAP Controller or Shift Register chains are not memory mapped and are not accessible through the on-chip Advanced Peripheral Bus (APB). Instead, the registers within the JTAG controller are all accessed serially through the TAP Controller. These registers include the Instruction Register and the six Data Registers.

#### 4.5.1 Instruction Register (IR)

The JTAG TAP Instruction Register (IR) is a four-bit serial scan chain connected between the JTAG TDI and TDO pins with a parallel load register. When the TAP Controller is placed in the correct states, bits can be shifted into the IR. Once these bits have been shifted into the chain and updated, they are interpreted as the current instruction. The decode of the IR bits is shown in Table 4-3. A detailed explanation of each instruction, along with its associated Data Register, follows.

<table>
<thead>
<tr>
<th>IR[3:0]</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>EXTEST</td>
<td>Drives the values preloaded into the Boundary Scan Chain by the SAMPLE/PRELOAD instruction onto the pads.</td>
</tr>
<tr>
<td>0x2</td>
<td>SAMPLE / PRELOAD</td>
<td>Captures the current I/O values and shifts the sampled values out of the Boundary Scan Chain while new preload data is shifted in.</td>
</tr>
<tr>
<td>0x8</td>
<td>ABORT</td>
<td>Shifts data into the ARM Debug Port Abort Register.</td>
</tr>
<tr>
<td>0xA</td>
<td>DPACC</td>
<td>Shifts data into and out of the ARM DP Access Register.</td>
</tr>
<tr>
<td>0xB</td>
<td>APACC</td>
<td>Shifts data into and out of the ARM AC Access Register.</td>
</tr>
<tr>
<td>0xE</td>
<td>IDCODE</td>
<td>Loads manufacturing information defined by the IEEE Standard 1149.1 into the IDCODE chain and shifts it out.</td>
</tr>
<tr>
<td>0xF</td>
<td>BYPASS</td>
<td>Connects TDI to TDO through a single Shift Register chain.</td>
</tr>
<tr>
<td>All Others</td>
<td>Reserved</td>
<td>Defaults to the BYPASS instruction to ensure that TDI is always connected to TDO.</td>
</tr>
</tbody>
</table>

#### 4.5.1.1 EXTEST Instruction

The EXTEST instruction is not associated with its own Data Register chain. Instead, the EXTEST instruction uses the data that has been preloaded into the Boundary Scan Data Register using the SAMPLE/PRELOAD instruction. When the EXTEST instruction is present in the Instruction Register, the preloaded data in the Boundary Scan Data Register associated with the outputs and output enables are used to drive the GPIO pads rather than the signals coming from the core. With tests that drive known values out of the controller, this instruction can be used to verify connectivity. While the EXTEST instruction is present in the Instruction Register, the Boundary Scan Data Register can be accessed to sample and shift out the current data and load new data into the Boundary Scan Data Register.

#### 4.5.1.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction connects the Boundary Scan Data Register chain between TDI and TDO. This instruction samples the current state of the pad pins for observation and preloads new test data. Each GPIO pad has an associated input, output, and output enable signal. When the TAP controller enters the Capture DR state during this instruction, the input, output, and output-enable signals to each of the GPIO pads are captured. These samples are serially shifted out on TDO while
the TAP controller is in the Shift DR state and can be used for observation or comparison in various tests.

While these samples of the inputs, outputs, and output enables are being shifted out of the Boundary Scan Data Register, new data is being shifted into the Boundary Scan Data Register from TDI. Once the new data has been shifted into the Boundary Scan Data Register, the data is saved in the parallel load registers when the TAP controller enters the Update DR state. This update of the parallel load register preloads data into the Boundary Scan Data Register that is associated with each input, output, and output enable. This preloaded data can be used with the EXTEST instruction to drive data into or out of the controller. See “Boundary Scan Data Register” on page 210 for more information.

4.5.1.3 ABORT Instruction

The ABORT instruction connects the associated ABORT Data Register chain between TDI and TDO. This instruction provides read and write access to the ABORT Register of the ARM Debug Access Port (DAP). Shifting the proper data into this Data Register clears various error bits or initiates a DAP abort of a previous request. See the “ABORT Data Register” on page 211 for more information.

4.5.1.4 DPACC Instruction

The DPACC instruction connects the associated DPACC Data Register chain between TDI and TDO. This instruction provides read and write access to the DPACC Register of the ARM Debug Access Port (DAP). Shifting the proper data into this register and reading the data output from this register allows read and write access to the ARM debug and status registers. See “DPACC Data Register” on page 211 for more information.

4.5.1.5 APACC Instruction

The APACC instruction connects the associated APACC Data Register chain between TDI and TDO. This instruction provides read and write access to the APACC Register of the ARM Debug Access Port (DAP). Shifting the proper data into this register and reading the data output from this register allows read and write access to internal components and buses through the Debug Port. See “APACC Data Register” on page 211 for more information.

4.5.1.6 IDCODE Instruction

The IDCODE instruction connects the associated IDCODE Data Register chain between TDI and TDO. This instruction provides information on the manufacturer, part number, and version of the ARM core. This information can be used by testing equipment and debuggers to automatically configure input and output data streams. IDCODE is the default instruction loaded into the JTAG Instruction Register when a Power-On-Reset (POR) is asserted, or the Test-Logic-Reset state is entered. See “IDCODE Data Register” on page 210 for more information.

4.5.1.7 BYPASS Instruction

The BYPASS instruction connects the associated BYPASS Data Register chain between TDI and TDO. This instruction is used to create a minimum length serial path between the TDI and TDO ports. The BYPASS Data Register is a single-bit shift register. This instruction improves test efficiency by allowing components that are not needed for a specific test to be bypassed in the JTAG scan chain by loading them with the BYPASS instruction. See “BYPASS Data Register” on page 210 for more information.
4.5.2 Data Registers

The JTAG module contains six Data Registers. These serial Data Register chains include: IDCODE, BYPASS, Boundary Scan, APACC, DPACC, and ABORT and are discussed in the following sections.

4.5.2.1 IDCODE Data Register

The format for the 32-bit IDCODE Data Register defined by the *IEEE Standard 1149.1* is shown in Figure 4-3. The standard requires that every JTAG-compliant microcontroller implement either the IDCODE instruction or the BYPASS instruction as the default instruction. The LSB of the IDCODE Data Register is defined to be a 1 to distinguish it from the BYPASS instruction, which has an LSB of 0. This definition allows auto-configuration test tools to determine which instruction is the default instruction.

The major uses of the JTAG port are for manufacturer testing of component assembly and program development and debug. To facilitate the use of auto-configuration debug tools, the IDCODE instruction outputs a value of 0x4BA0.0477. This value allows the debuggers to automatically configure themselves to work correctly with the Cortex-M4F during debug.

![Figure 4-3. IDCODE Register Format](image)

4.5.2.2 BYPASS Data Register

The format for the 1-bit BYPASS Data Register defined by the *IEEE Standard 1149.1* is shown in Figure 4-4. The standard requires that every JTAG-compliant microcontroller implement either the BYPASS instruction or the IDCODE instruction as the default instruction. The LSB of the BYPASS Data Register is defined to be a 0 to distinguish it from the IDCODE instruction, which has an LSB of 1. This definition allows auto-configuration test tools to determine which instruction is the default instruction.

![Figure 4-4. BYPASS Register Format](image)

4.5.2.3 Boundary Scan Data Register

The format of the Boundary Scan Data Register is shown in Figure 4-5. Each GPIO pin, starting with a GPIO pin next to the JTAG port pins, is included in the Boundary Scan Data Register. Each GPIO pin has three associated digital signals that are included in the chain. These signals are input, output, and output enable, and are arranged in that order as shown in the figure.

When the Boundary Scan Data Register is accessed with the SAMPLE/PRELOAD instruction, the input, output, and output enable from each digital pad are sampled and then shifted out of the chain to be verified. The sampling of these values occurs on the rising edge of TCK in the Capture DR state of the TAP controller. While the sampled data is being shifted out of the Boundary Scan chain in the Shift DR state of the TAP controller, new data can be preloaded into the chain for use with the EXTEST instruction. The EXTEST instruction forces data out of the controller.
4.5.2.4 APACC Data Register

The format for the 35-bit APACC Data Register defined by ARM is described in the ARM® Debug Interface V5 Architecture Specification.

4.5.2.5 DPACC Data Register

The format for the 35-bit DPACC Data Register defined by ARM is described in the ARM® Debug Interface V5 Architecture Specification.

4.5.2.6 ABORT Data Register

The format for the 35-bit ABORT Data Register defined by ARM is described in the ARM® Debug Interface V5 Architecture Specification.
5 System Control

System control configures the overall operation of the device and provides information about the device. Configurable features include reset control, NMI operation, power control, clock control, and low-power modes.

5.1 Signal Description

The following table lists the external signals of the System Control module and describes the function of each. The NMI signal is the alternate function for two GPIO signals and functions as a GPIO after reset. The NMI pins are under commit protection and require a special process to be configured as any alternate function or to subsequently return to the GPIO function, see “Commit Control” on page 667. The column in the table below titled “Pin Mux/Pin Assignment” lists the GPIO pin placement for the NMI signal. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the NMI function. The number in parentheses is the encoding that must be programmed into the PMcn field in the GPIO Port Control (GPIOPCTL) register (page 702) to assign the NMI signal to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659. The remaining signals (with the word “fixed” in the Pin Mux/Pin Assignment column) have a fixed pin assignment and function.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMI</td>
<td>40 100</td>
<td>PF0 (8) PD7 (8)</td>
<td>I</td>
<td>TTL</td>
<td>Non-maskable interrupt.</td>
</tr>
<tr>
<td>OSC0</td>
<td>65</td>
<td>fixed</td>
<td>I</td>
<td>Analog</td>
<td>Main oscillator crystal input or an external clock reference input.</td>
</tr>
<tr>
<td>OSC1</td>
<td>66</td>
<td>fixed</td>
<td>O</td>
<td>Analog</td>
<td>Main oscillator crystal output. Leave unconnected when using a single-ended clock source.</td>
</tr>
<tr>
<td>RST</td>
<td>63</td>
<td>fixed</td>
<td>I</td>
<td>TTL</td>
<td>System reset input.</td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

5.2 Functional Description

The System Control module provides the following capabilities:

- Device identification, see “Device Identification” on page 212
- Local control, such as reset (see “Reset Control” on page 213), power (see “Power Control” on page 218) and clock control (see “Clock Control” on page 219)
- System control (Run, Sleep, and Deep-Sleep modes), see “System Control” on page 227

5.2.1 Device Identification

Several read-only registers provide software with information on the microcontroller, such as version, part number, memory sizes, and peripherals present on the device. The Device Identification 0 (DID0) (page 238) and Device Identification 1 (DID1) (page 240) registers provide details about the device’s version, package, temperature range, and so on. The Peripheral Present registers starting at System Control offset 0x300, such as the Watchdog Timer Peripheral Present (PPWD) register, provide information on how many of each type of module are included on the device. Finally,
information about the capabilities of the on-chip peripherals are provided at offset 0xFC0 in each peripheral’s register space in the Peripheral Properties registers, such as the GPTM Peripheral Properties (GPTMP) register. Previous devices used the Device Capabilities (DC0-DC9) registers for information about the peripherals and their capabilities. These registers are present on this device for backward software capability, but provide no information about peripherals that were not available on older devices.

5.2.2 Reset Control
This section discusses aspects of hardware functions during reset as well as system software requirements following the reset sequence.

5.2.2.1 Reset Sources
The TM4C123GH6PZ microcontroller has six sources of reset:

1. Power-on reset (POR) (see page 214).
2. External reset input pin (RST) assertion (see page 215).
3. A brown-out detection that can be caused by any of the following events: (see page 216).
   - \( V_{DD} \) under BOR0. The trigger value is the highest \( V_{DD} \) voltage level for BOR0.
   - \( V_{DD} \) under BOR1. The trigger value is the highest \( V_{DD} \) voltage level for BOR1.
4. Software-initiated reset (with the software reset registers) (see page 217).
5. A watchdog timer reset condition violation (see page 217).
6. MOSC failure (see page 218).

Table 5-2 provides a summary of results of the various reset operations.

<table>
<thead>
<tr>
<th>Reset Source</th>
<th>Core Reset?</th>
<th>JTAG Reset?</th>
<th>On-Chip Peripherals Reset?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-On Reset</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>RST</td>
<td>Yes</td>
<td>Pin Config Only</td>
<td>Yes</td>
</tr>
<tr>
<td>Brown-Out Reset</td>
<td>Yes</td>
<td>Pin Config Only</td>
<td>Yes</td>
</tr>
<tr>
<td>Software System Request Reset</td>
<td>Yes</td>
<td>Pin Config Only</td>
<td>Yes</td>
</tr>
<tr>
<td>Software System Request Reset</td>
<td>Yes</td>
<td>Pin Config Only</td>
<td>Yes</td>
</tr>
<tr>
<td>MOSC Failure Reset</td>
<td>No</td>
<td>Pin Config Only</td>
<td>Yes(^a)</td>
</tr>
</tbody>
</table>

\(^a\) Programmable on a module-by-module basis using the Software Reset Control Registers.

After a reset, the Reset Cause (RESC) register is set with the reset cause. The bits in this register are sticky and maintain their state across multiple reset sequences, except when an internal POR
is the cause, in which case, all the bits in the RESC register are cleared except for the POR indicator. A bit in the RESC register can be cleared by writing a 0.

At any reset that resets the core, the user has the opportunity to direct the core to execute the ROM Boot Loader or the application in Flash memory by using any GPIO signal as configured in the Boot Configuration (BOOTCFG) register.

At reset, the following sequence is performed:

1. The BOOTCFG register is read. If the EN bit is clear, the ROM Boot Loader is executed.

2. In the ROM Boot Loader, the status of the specified GPIO pin is compared with the specified polarity. If the status matches the specified polarity, the ROM is mapped to address 0x0000.0000 and execution continues out of the ROM Boot Loader.

3. If then EN bit is set or the status doesn’t match the specified polarity, the data at address 0x0000.0004 is read, and if the data at this address is 0xFFFF.FFFF, the ROM is mapped to address 0x0000.0000 and execution continues out of the ROM Boot Loader.

4. If there is data at address 0x0000.0004 that is not 0xFFFF.FFFF, the stack pointer (SP) is loaded from Flash memory at address 0x0000.0000 and the program counter (PC) is loaded from address 0x0000.0004. The user application begins executing.

Note: If the device fails the initialization phase, it toggles the TDO output pin as an indication the device is not executing. This feature is provided for debug purposes.

For example, if the BOOTCFG register is written and committed with the value of 0x0000.3C01, then PB7 is examined at reset to determine if the ROM Boot Loader should be executed. If PB7 is Low, the core unconditionally begins executing the ROM boot loader. If PB7 is High, then the application in Flash memory is executed if the reset vector at location 0x0000.0004 is not 0xFFFF.FFFF. Otherwise, the ROM boot loader is executed.

5.2.2.2 Power-On Reset (POR)

Note: The JTAG controller can only be reset by the power-on reset.

The internal Power-On Reset (POR) circuit monitors the power supply voltage (VDD) and generates a reset signal to all of the internal logic including JTAG when the power supply ramp reaches a threshold value (VDD_POK). The microcontroller must be operating within the specified operating parameters when the on-chip power-on reset pulse is complete (see “Power and Brown-Out” on page 1402). For applications that require the use of an external reset signal to hold the microcontroller in reset longer than the internal POR, the RST input may be used as discussed in "External RST Pin" on page 215.

The Power-On Reset sequence is as follows:

1. The microcontroller waits for internal POR to go inactive.

2. The internal reset is released and the core loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

The internal POR is only active on the initial power-up of the microcontroller and when the microcontroller wakes from hibernation. The Power-On Reset timing is shown in “Power and Brown-Out” on page 1402.
5.2.2.3 External RST Pin

**Note:** It is recommended that the trace for the RST signal must be kept as short as possible. Be sure to place any components connected to the RST signal as close to the microcontroller as possible.

If the application only uses the internal POR circuit, the RST input must be connected to the power supply (V_{DD}) through an optional pull-up resistor (0 to 100K Ω) as shown in Figure 5-1 on page 215. The RST input has filtering which requires a minimum pulse width in order for the reset pulse to be recognized, see Table 24-11 on page 1407.

**Figure 5-1. Basic RST Configuration**

![Figure 5-1. Basic RST Configuration](image)

R_{PU} = 0 to 100 kΩ

The external reset pin (RST) resets the microcontroller including the core and all the on-chip peripherals. The external reset sequence is as follows:

1. The external reset pin (RST) is asserted for the duration specified by T_{MIN} and then deasserted (see “Reset” on page 1407).
2. The internal reset is released and the core loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

To improve noise immunity and/or to delay reset at power up, the RST input may be connected to an RC network as shown in Figure 5-2 on page 215.

**Figure 5-2. External Circuitry to Extend Power-On Reset**

![Figure 5-2. External Circuitry to Extend Power-On Reset](image)

R_{PU} = 1 kΩ to 100 kΩ

C_{1} = 1 nF to 10 µF
If the application requires the use of an external reset switch, Figure 5-3 on page 216 shows the proper circuitry to use.

**Figure 5-3. Reset Circuit Controlled by Switch**

![Diagram of Reset Circuit Controlled by Switch]

Typical $R_{PU} = 10 \text{kΩ}$
Typical $R_S = 470 \text{Ω}$
$C_1 = 10 \text{nF}$

The $R_{PU}$ and $C_1$ components define the power-on delay.
The external reset timing is shown in Figure 24-11 on page 1408.

### 5.2.2.4 Brown-Out Reset (BOR)

The microcontroller provides a brown-out detection circuit that triggers if any of the following occur:

- $V_{DD}$ under BOR0. The external $V_{DD}$ supply voltage is below the specified $V_{DD}$ BOR0 value. The trigger value is the highest $V_{DD}$ voltage level for BOR0.

- $V_{DD}$ under BOR1. The external $V_{DD}$ supply voltage is below the specified $V_{DD}$ BOR1 value. The trigger value is the highest $V_{DD}$ voltage level for BOR1.

The application can identify that a BOR event caused a reset by reading the **Reset Cause (RESC)** register. When a brown-out condition is detected, the default condition is to generate a reset. The BOR events can also be programmed to generate an interrupt by clearing the **BOR0** bit or **BOR1** bit in the **Power-On and Brown-Out Reset Control (PBORCTL)** register.

The brown-out reset sequence is as follows:

1. When $V_{DD}$ drops below $V_{BORnTH}$, an internal BOR condition is set. Please refer to “Power and Brown-Out” on page 1402 for $V_{BORnTH}$ value.

2. If the BOR condition exists, an internal reset is asserted.

3. The internal reset is released and the microcontroller fetches and loads the initial stack pointer, the initial program counter, the first instruction designated by the program counter, and begins execution.

The result of a brown-out reset is equivalent to that of an assertion of the external $RST$ input, and the reset is held active until the proper $V_{DD}$ level is restored. The **RESC** register can be examined in the reset interrupt handler to determine if a Brown-Out condition was the cause of the reset, thus allowing software to determine what actions are required to recover.
The internal Brown-Out Reset timing is shown in “Power and Brown-Out” on page 1402.

5.2.2.5 Software Reset

Software can reset a specific peripheral or generate a reset to the entire microcontroller.

Peripherals can be individually reset by software via peripheral-specific reset registers available beginning at System Control offset 0x500 (for example the Watchdog Timer Software Reset (SRWD) register). If the bit position corresponding to a peripheral is set and subsequently cleared, the peripheral is reset.

The entire microcontroller, including the core, can be reset by software by setting the SYSRESREQ bit in the Application Interrupt and Reset Control (APINT) register. The software-initiated system reset sequence is as follows:

1. A software microcontroller reset is initiated by setting the SYSRESREQ bit.
2. An internal reset is asserted.
3. The internal reset is deasserted and the microcontroller loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

The core only can be reset by software by setting the VECTRESET bit in the APINT register. The software-initiated core reset sequence is as follows:

1. A core reset is initiated by setting the VECTRESET bit.
2. An internal reset is asserted.
3. The internal reset is deasserted and the microcontroller loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

The software-initiated system reset timing is shown in Figure 24-12 on page 1408.

5.2.2.6 Watchdog Timer Reset

The Watchdog Timer module's function is to prevent system hangs. The TM4C123GH6PZ microcontroller has two Watchdog Timer modules in case one watchdog clock source fails. One watchdog is run off the system clock and the other is run off the Precision Internal Oscillator (PIOSC). Each module operates in the same manner except that because the PIOSC watchdog timer module is in a different clock domain, register accesses must have a time delay between them. The watchdog timer can be configured to generate an interrupt or a non-maskable interrupt to the microcontroller on its first time-out and to generate a reset on its second time-out.

After the watchdog's first time-out event, the 32-bit watchdog counter is reloaded with the value of the Watchdog Timer Load (WDTLOAD) register and resumes counting down from that value. If the timer counts down to zero again before the first time-out interrupt is cleared, and the reset signal has been enabled, the watchdog timer asserts its reset signal to the microcontroller. The watchdog timer reset sequence is as follows:

1. The watchdog timer times out for the second time without being serviced.
2. An internal reset is asserted.
3. The internal reset is released and the microcontroller loads from memory the initial stack pointer, the initial program counter, and the first instruction designated by the program counter, and then begins execution.

For more information on the Watchdog Timer module, see "Watchdog Timers" on page 788. The watchdog reset timing is shown in Figure 24-13 on page 1408.

5.2.3 Non-Maskable Interrupt

The microcontroller has four sources of non-maskable interrupt (NMI):

- The assertion of the NMI signal
- A main oscillator verification error
- The NMISET bit in the Interrupt Control and State (INTCTRL) register in the Cortex™-M4F (see page 160).
- The Watchdog module time-out interrupt when the INTTYPE bit in the Watchdog Control (WDTCTL) register is set (see page 794).

Software must check the cause of the interrupt in order to distinguish among the sources.

5.2.3.1 NMI Pin

The NMI signal is an alternate function for either GPIO port pin PD7 or PF0. The alternate function must be enabled in the GPIO for the signal to be used as an interrupt, as described in “General-Purpose Input/Outputs (GPIOs)” on page 659. Note that enabling the NMI alternate function requires the use of the GPIO lock and commit function just like the GPIO port pins associated with JTAG/SWD functionality, see page 698. The active sense of the NMI signal is High; asserting the enabled NMI signal above VIH initiates the NMI interrupt sequence.

5.2.3.2 Main Oscillator Verification Failure

The TM4C123GH6PZ microcontroller provides a main oscillator verification circuit that generates an error condition if the oscillator is running too fast or too slow. If the main oscillator verification circuit is enabled and a failure occurs, either a power-on reset is generated and control is transferred to the NMI handler, or an interrupt is generated. The MOSCIN bit in the MOSCCTL register determines which action occurs. In either case, the system clock source is automatically switched to the PIOSC. If a MOSC failure reset occurs, the NMI handler is used to address the main oscillator verification failure because the necessary code can be removed from the general reset handler, speeding up reset processing. The detection circuit is enabled by setting the CVAL bit in the Main Oscillator Control (MOSCCTL) register. The main oscillator verification error is indicated in the main oscillator fail status (MOSCFAIL) bit in the Reset Cause (RESC) register. The main oscillator verification circuit action is described in more detail in “Main Oscillator Verification Circuit” on page 226.

5.2.4 Power Control

The TM4C123GH6PZ microcontroller provides an integrated LDO regulator that is used to provide power to the majority of the microcontroller's internal logic. Figure 5-4 shows the power architecture. An external LDO may not be used.

Note: VDDA must be supplied with a voltage that meets the specification in Table 24-5 on page 1397, or the microcontroller does not function properly. VDDA is the supply for all of the analog circuitry on the device, including the clock circuitry.
5.2.5 Clock Control

System control determines the control of clocks in this part.

5.2.5.1 Fundamental Clock Sources

There are multiple clock sources for use in the microcontroller:

- **Precision Internal Oscillator (PIOSC).** The precision internal oscillator is an on-chip clock source that is the clock source the microcontroller uses during and following POR. It does not require the use of any external components and provides a 16-MHz clock with ±1% accuracy with calibration and ±3% accuracy across temperature (see “PIOSC Specifications” on page 1412). The PIOSC allows for a reduced system cost in applications that require an accurate clock source. If the main oscillator is required, software must enable the main oscillator following reset and allow the main oscillator to stabilize before changing the clock reference. If the Hibernation Module clock source is a 32.768-kHz oscillator, the precision internal oscillator can be trimmed by software based on a reference clock for increased accuracy. Regardless of whether or not the PIOSC is the source for the system clock, the PIOSC can be configured to be the source for the ADC clock as well as the baud clock for the UART and SSI, see “System Control” on page 227.

- **Main Oscillator (MOSC).** The main oscillator provides a frequency-accurate clock source by one of two means: an external single-ended clock source is connected to the OSC0 input pin, or an external crystal is connected across the OSC0 input and OSC1 output pins. If the PLL is being
used, the crystal value must be one of the supported frequencies between 5 MHz to 25 MHz (inclusive). If the PLL is not being used, the crystal may be any one of the supported frequencies between 4 MHz to 25 MHz. The single-ended clock source range is as specified in Table 24-13 on page 1411. The supported crystals are listed in the XTAL bit field in the RCC register (see page 254). Note that the MOSC provides the clock source for the USB PLL and must be connected to a crystal or an oscillator.

- **Low-Frequency Internal Oscillator (LFIOSC).** The low-frequency internal oscillator is intended for use during Deep-Sleep power-saving modes. The frequency can have wide variations; refer to “Low-Frequency Internal Oscillator (LFIOSC) Specifications” on page 1412 for more details. This power-savings mode benefits from reduced internal switching and also allows the MOSC to be powered down. In addition, the PIOSC can be powered down while in Deep-Sleep mode.

- **Hibernation Module Clock Source.** The Hibernation module is clocked by a 32.768-kHz oscillator connected to the XOSCO pin. The 32.768-kHz oscillator can be used for the system clock, thus eliminating the need for an additional crystal or oscillator. The Hibernation module clock source is intended to provide the system with a real-time clock source and may also provide an accurate source of Deep-Sleep or Hibernate mode power savings.

The internal system clock (SysClk), is derived from any of the above sources plus two others: the output of the main internal PLL and the precision internal oscillator divided by four (4 MHz ± 1%). The frequency of the PLL clock reference must be in the range of 5 MHz to 25 MHz (inclusive). Table 5-3 on page 220 shows how the various clock sources can be used in a system.

<table>
<thead>
<tr>
<th>Clock Source</th>
<th>Drive PLL?</th>
<th>Used as SysClk?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Precision Internal Oscillator</td>
<td>Yes</td>
<td>BYPASS = 1, OSCSRC = 0x1</td>
</tr>
<tr>
<td>Precision Internal Oscillator divide by 4 (4 MHz ± 1%)</td>
<td>No</td>
<td>Yeas BYPASS = 1, OSCSRC = 0x2</td>
</tr>
<tr>
<td>Main Oscillator</td>
<td>Yes</td>
<td>BYPASS = 1, OSCSRC = 0x0</td>
</tr>
<tr>
<td>Low-Frequency Internal Oscillator (LFIOSC)</td>
<td>No</td>
<td>Yes BYPASS = 1, OSCSRC = 0x3</td>
</tr>
<tr>
<td>Hibernation Module 32.768-kHz Oscillator</td>
<td>No</td>
<td>Yeas BYPASS = 1, OSCSRC2 = 0x7</td>
</tr>
</tbody>
</table>

### 5.2.5.2 Clock Configuration

The **Run-Mode Clock Configuration (RCC)** and **Run-Mode Clock Configuration 2 (RCC2)** registers provide control for the system clock. The RCC2 register is provided to extend fields that offer additional encodings over the RCC register. When used, the RCC2 register field values are used by the logic over the corresponding field in the RCC register. In particular, RCC2 provides for a larger assortment of clock configuration options. These registers control the following clock functionality:

- Source of clocks in sleep and deep-sleep modes
- System clock derived from PLL or other clock source
- Enabling/disabling of oscillators and PLL
- Clock divisors
Crystal input selection

**Important:** Write the RCC register prior to writing the RCC2 register.

When transitioning the system clock configuration to use the MOSC as the fundamental clock source, the MOSCDIS bit must be set prior to reselecting the MOSC or an undefined system clock configuration can sporadically occur.

The configuration of the system clock must not be changed while an EEPROM operation is in process. Software must wait until the WORKING bit in the EEPROM Done Status (EEDONE) register is clear before making any changes to the system clock.

Figure 5-5 shows the logic for the main clock tree. The peripheral blocks are driven by the system clock signal and can be individually enabled/disabled. The ADC clock signal can be selected from the PIOSC, the system clock if the PLL is disabled, or the PLL output divided down to 16 MHz if the PLL is enabled. The PWM clock signal is a synchronous divide of the system clock to provide the PWM circuit with more range (set with PWMDIV in RCC).

**Note:** If the ADC module is not using the PIOSC as the clock source, the system clock must be at least 16 MHz. When the USB module is in operation, MOSC must be the clock source, either with or without using the PLL, and the system clock must be at least 20 MHz.
Figure 5-5. Main Clock Tree

Note:  
a. Control provided by RCC register bit/field.  
b. Control provided by RCC register bit/field or RCC2 register bit/field, if overridden with RCC2 register bit USERCC2.  
c. Control provided by RCC2 register bit/field.  
d. Also may be controlled by DSLPCCLKCFG when in deep sleep mode.  
e. Control provided by RCC register SYSDIV field, RCC2 register SYSDIV2 field if overridden with USERCC2 bit, or [SYSDIV2,SYSDIV2LSB] if both USERCC2 and DIV400 bits are set.  
f. Control provided by UARTCC, SSICC, and ADCCC register field.

Communication Clock Sources

In addition to the main clock tree described above, the UART, and SSI modules all have a Clock Control register in the peripheral's register map at offset 0xFC8 that can be used to select the clock source for the module's baud clock. Users can choose between the system clock, which is the default source for the baud clock, and the PIOSC. Note that there may be special considerations when using the PIOSC as the baud clock. For more information, see the Clock Control register description in the chapter describing the operation of the module.
Using the SYSDIV and SYSDIV2 Fields

In the RCC register, the SYSDIV field specifies which divisor is used to generate the system clock from either the PLL output or the oscillator source (depending on how the BYPASS bit in this register is configured). When using the PLL, the VCO frequency of 400 MHz is predivided by 2 before the divisor is applied. Table 5-4 shows how the SYSDIV encoding affects the system clock frequency, depending on whether the PLL is used (BYPASS=0) or another clock source is used (BYPASS=1). The divisor is equivalent to the SYSDIV2 encoding plus 1. For a list of possible clock sources, see Table 5-3 on page 220.

<table>
<thead>
<tr>
<th>SYSDIV</th>
<th>Divisor</th>
<th>Frequency (BYPASS=0)</th>
<th>Frequency (BYPASS=1)</th>
<th>TivaWare™ Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>/1</td>
<td>reserved</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_1</td>
</tr>
<tr>
<td>0x1</td>
<td>/2</td>
<td>reserved</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_2</td>
</tr>
<tr>
<td>0x2</td>
<td>/3</td>
<td>66.67 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_3</td>
</tr>
<tr>
<td>0x3</td>
<td>/4</td>
<td>50 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_4</td>
</tr>
<tr>
<td>0x4</td>
<td>/5</td>
<td>40 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_5</td>
</tr>
<tr>
<td>0x5</td>
<td>/6</td>
<td>33.33 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_6</td>
</tr>
<tr>
<td>0x6</td>
<td>/7</td>
<td>28.57 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_7</td>
</tr>
<tr>
<td>0x7</td>
<td>/8</td>
<td>25 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_8</td>
</tr>
<tr>
<td>0x8</td>
<td>/9</td>
<td>22.22 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_9</td>
</tr>
<tr>
<td>0x9</td>
<td>/10</td>
<td>20 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_10</td>
</tr>
<tr>
<td>0xA</td>
<td>/11</td>
<td>18.18 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_11</td>
</tr>
<tr>
<td>0xB</td>
<td>/12</td>
<td>16.67 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_12</td>
</tr>
<tr>
<td>0xC</td>
<td>/13</td>
<td>15.38 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_13</td>
</tr>
<tr>
<td>0xD</td>
<td>/14</td>
<td>14.29 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_14</td>
</tr>
<tr>
<td>0xE</td>
<td>/15</td>
<td>13.33 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_15</td>
</tr>
<tr>
<td>0xF</td>
<td>/16</td>
<td>12.5 MHz (default)</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_16</td>
</tr>
</tbody>
</table>

a. This parameter is used in functions such as SysCtlClockSet() in the TivaWare Peripheral Driver Library.

The SYSDIV2 field in the RCC2 register is 2 bits wider than the SYSDIV field in the RCC register so that additional larger divisors up to /64 are possible, allowing a lower system clock frequency for improved Deep Sleep power consumption. When using the PLL, the VCO frequency of 400 MHz is predivided by 2 before the divisor is applied. The divisor is equivalent to the SYSDIV2 encoding plus 1. Table 5-5 shows how the SYSDIV2 encoding affects the system clock frequency, depending on whether the PLL is used (BYPASS2=0) or another clock source is used (BYPASS2=1). For a list of possible clock sources, see Table 5-3 on page 220.

<table>
<thead>
<tr>
<th>SYSDIV2</th>
<th>Divisor</th>
<th>Frequency (BYPASS2=0)</th>
<th>Frequency (BYPASS2=1)</th>
<th>TivaWare Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>/1</td>
<td>reserved</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_1</td>
</tr>
<tr>
<td>0x01</td>
<td>/2</td>
<td>reserved</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_2</td>
</tr>
<tr>
<td>0x02</td>
<td>/3</td>
<td>66.67 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_3</td>
</tr>
<tr>
<td>0x03</td>
<td>/4</td>
<td>50 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_4</td>
</tr>
<tr>
<td>0x04</td>
<td>/5</td>
<td>40 MHz</td>
<td>Clock source frequency</td>
<td>SYSCTL_SYSDIV_5</td>
</tr>
</tbody>
</table>

...
Table 5-5. Examples of Possible System Clock Frequencies Using the SYSDIV2 Field
(continued)

<table>
<thead>
<tr>
<th>SYSDIV2</th>
<th>Divisor</th>
<th>Frequency (BYPASS2=0)</th>
<th>Frequency (BYPASS2=1)</th>
<th>TivaWare Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x09</td>
<td>/10</td>
<td>20 MHz</td>
<td>Clock source frequency/10</td>
<td>SYSCTL_SYSDIV_10</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0x3F</td>
<td>/64</td>
<td>3.125 MHz</td>
<td>Clock source frequency/64</td>
<td>SYSCTL_SYSDIV_64</td>
</tr>
</tbody>
</table>

a. This parameter is used in functions such as SysCtlClockSet() in the TivaWare Peripheral Driver Library.

To allow for additional frequency choices when using the PLL, the DIV400 bit is provided along with the SYSDIV2LSB bit. When the DIV400 bit is set, bit 22 becomes the LSB for SYSDIV2. In this situation, the divisor is equivalent to the (SYSDIV2 encoding with SYSDIV2LSB appended) plus one. Table 5-6 shows the frequency choices when DIV400 is set. When the DIV400 bit is clear, SYSDIV2LSB is ignored, and the system clock frequency is determined as shown in Table 5-5 on page 223.

Table 5-6. Examples of Possible System Clock Frequencies with DIV400=1

<table>
<thead>
<tr>
<th>SYSDIV2</th>
<th>SYSDIV2LSB</th>
<th>Divisor</th>
<th>Frequency (BYPASS2=0)</th>
<th>TivaWare Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>reserved</td>
<td>/2</td>
<td>reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x01</td>
<td>0</td>
<td>/3</td>
<td>reserved</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>/4</td>
<td>reserved</td>
<td>-</td>
</tr>
<tr>
<td>0x02</td>
<td>0</td>
<td>/5</td>
<td>80 MHz</td>
<td>SYSCTL_SYSDIV_2_5</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>/6</td>
<td>66.67 MHz</td>
<td>SYSCTL_SYSDIV_3</td>
</tr>
<tr>
<td>0x03</td>
<td>0</td>
<td>/7</td>
<td>reserved</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>/8</td>
<td>50 MHz</td>
<td>SYSCTL_SYSDIV_4</td>
</tr>
<tr>
<td>0x04</td>
<td>0</td>
<td>/9</td>
<td>44.44 MHz</td>
<td>SYSCTL_SYSDIV_4_5</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>/10</td>
<td>40 MHz</td>
<td>SYSCTL_SYSDIV_5</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0x3F</td>
<td>0</td>
<td>/127</td>
<td>3.15 MHz</td>
<td>SYSCTL_SYSDIV_63_5</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>/128</td>
<td>3.125 MHz</td>
<td>SYSCTL_SYSDIV_64</td>
</tr>
</tbody>
</table>

a. Note that DIV400 and SYSDIV2LSB are only valid when BYPASS2=0.
b. This parameter is used in functions such as SysCtlClockSet() in the TivaWare Peripheral Driver Library.

5.2.5.3 Precision Internal Oscillator Operation (PIOSC)

The microcontroller powers up with the PIOSC running. If another clock source is desired, the PIOSC must remain enabled as it is used for internal functions. The PIOSC can only be disabled during Deep-Sleep mode. It can be powered down by setting the PIOSCPD bit in the DSLPCLKCFG register.

The PIOSC generates a 16-MHz clock with ±1% accuracy with calibration and ±3% accuracy across temperature (see “PIOSC Specifications” on page 1412). At the factory, the PIOSC is set to 16 MHz, however, the frequency can be trimmed for other voltage or temperature conditions using software in one of three ways:

- Default calibration: clear the UTEN bit and set the UPDATE bit in the Precision Internal Oscillator Calibration (PIOSCCAL) register.

- User-defined calibration: The user can program the UT value to adjust the PIOSC frequency. As the UT value increases, the generated period increases. To commit a new UT value, first set the...
UTEN bit, then program the UT field, and then set the UPDATE bit. The adjustment finishes within a few clock periods and is glitch free.

- Automatic calibration using the Hibernation module with a functioning 32.768-kHz clock source: Set the CAL bit in the PIOSC2A register; the results of the calibration are shown in the RESULT field in the Precision Internal Oscillator Statistic (PIOSCSTAT) register. After calibration is complete, the PIOSC is trimmed using the trimmed value returned in the CT field.

### 5.2.5.4 Crystal Configuration for the Main Oscillator (MOSC)

The main oscillator supports the use of a select number of crystals from 4 to 25 MHz.

- The XTAL bit in the RCC register (see page 254) describes the available crystal choices and default programming values.
- Software configures the RCC register XTAL field with the crystal number. If the PLL is used in the design, the XTAL field value is internally translated to the PLL settings.

### 5.2.5.5 Main PLL Frequency Configuration

The main PLL is disabled by default during power-on reset and is enabled later by software if required. Software specifies the output divisor to set the system clock frequency and enables the main PLL to drive the output. The PLL operates at 400 MHz, but is divided by two prior to the application of the output divisor, unless the DIV400 bit in the RCC2 register is set.

To configure the PIOSC to be the clock source for the main PLL, program the OSCRC2 field in the Run-Mode Clock Configuration 2 (RCC2) register to be 0x1.

If the main oscillator provides the clock reference to the main PLL, the translation provided by hardware and used to program the PLL is available for software in the PLL Frequency n (PLLFFREQn) registers (see page 272). The internal translation provides a translation within ± 1% of the targeted PLL VCO frequency. Table 24-14 on page 1411 shows the actual PLL frequency and error for a given crystal choice.

- The Crystal Value field (XTAL) in the Run-Mode Clock Configuration (RCC) register (see page 254) describes the available crystal choices and default programming of the PLLFFREQn registers. Any time the XTAL field changes, the new settings are translated and the internal PLL settings are updated.

### 5.2.5.6 USB PLL Frequency Configuration

The USB PLL is disabled by default during power-on reset and is enabled later by software. The USB PLL must be enabled and running for proper USB function. The main oscillator is the only clock reference for the USB PLL. The USB PLL is enabled by clearing the USBPWRDN bit of the RCC2 register. The XTAL bit field (Crystal Value) of the RCC register describes the available crystal choices.

The main oscillator must be connected to one of the following crystal values in order to correctly generate the USB clock: 5, 6, 8, 10, 12, 16, 18, 20, 24, or 25 MHz. Only these crystals provide the necessary USB PLL VCO frequency to conform with the USB timing specifications.

### 5.2.5.7 PLL Modes

- Both PLLs have two modes of operation: Normal and Power-Down
  - Normal: The PLL multiplies the input clock reference and drives the output.
  - Power-Down: Most of the PLL internal circuitry is disabled and the PLL does not drive the output.

The modes are programmed using the RCC/RCC2 register fields (see page 254 and page 261).
5.2.5.8 PLL Operation

If a PLL configuration is changed, the PLL output frequency is unstable until it reconverges (relocks) to the new setting. The time between the configuration change and relock is $T_{\text{READY}}$ (see Table 24-13 on page 1411). During the relock time, the affected PLL is not usable as a clock reference. Software can poll the \texttt{LOCK} bit in the PLL Status (PLLSTAT) register to determine when the PLL has locked.

Either PLL is changed by one of the following:

- Change to the \texttt{XTAL} value in the RCC register—writes of the same value do not cause a relock.
- Change in the PLL from Power-Down to Normal mode.

A counter clocked by the system clock is used to measure the $T_{\text{READY}}$ requirement. The down counter is set to 0x200 if the PLL is powering up. If the M or N values in the PLLFREQn registers are changed, the counter is set to 0xC0. Hardware is provided to keep the PLL from being used as a system clock until the $T_{\text{READY}}$ condition is met after one of the two changes above. It is the user’s responsibility to have a stable clock source (like the main oscillator) before the RCC/RCC2 register is switched to use the PLL.

If the main PLL is enabled and the system clock is switched to use the PLL in one step, the system control hardware continues to clock the microcontroller from the oscillator selected by the RCC/RCC2 register until the main PLL is stable ($T_{\text{READY}}$ time met), after which it changes to the PLL. Software can use many methods to ensure that the system is clocked from the main PLL, including periodically polling the PLLRIS bit in the Raw Interrupt Status (RIS) register, and enabling the PLL Lock interrupt.

The USB PLL is not protected during the lock time ($T_{\text{READY}}$), and software should ensure that the USB PLL has locked before using the interface. Software can use many methods to ensure the $T_{\text{READY}}$ period has passed, including periodically polling the USBPLLRLIS bit in the Raw Interrupt Status (RIS) register, and enabling the USB PLL Lock interrupt.

5.2.5.9 Main Oscillator Verification Circuit

The clock control includes circuitry to ensure that the main oscillator is running at the appropriate frequency. The circuit monitors the main oscillator frequency and signals if the frequency is outside of the allowable band of attached crystals.

The detection circuit is enabled using the \texttt{CVAL} bit in the Main Oscillator Control (MOSCCTL) register. If this circuit is enabled and detects an error, and if the MOSCIM bit in the MOSCCTL register is clear, then the following sequence is performed by the hardware:

1. The MOSCFAIL bit in the Reset Cause (RESC) register is set.
2. The system clock is switched from the main oscillator to the PIOSC.
3. An internal power-on reset is initiated.
4. Reset is deasserted and the processor is directed to the NMI handler during the reset sequence.

if the MOSCIM bit in the MOSCCTL register is set, then the following sequence is performed by the hardware:

1. The system clock is switched from the main oscillator to the PIOSC.
2. The MOFRIS bit in the RIS register is set to indicate a MOSC failure.

5.2.6 System Control

For power-savings purposes, the peripheral-specific RCGCx, SCGCx, and DCGCx registers (for example, RCGCWD) control the clock gating logic for that peripheral or block in the system while the microcontroller is in Run, Sleep, and Deep-Sleep mode, respectively. These registers are located in the System Control register map starting at offsets 0x600, 0x700, and 0x800, respectively. There must be a delay of 3 system clocks after a peripheral module clock is enabled in the RCGC register before any module registers are accessed.

Important: To support legacy software, the RCGCn, SCGCn, and DCGCn registers are available at offsets 0x100 - 0x128. A write to any of these legacy registers also writes the corresponding bit in the peripheral-specific RCGCx, SCGCx, and DCGCx registers. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. It is recommended that new software use the new registers and not rely on legacy operation.

If software uses a peripheral-specific register to write a legacy peripheral (such as TIMER0), the write causes proper operation, but the value of that bit is not reflected in the legacy register. Any bits that are changed by writing to a legacy register can be read back correctly with a read of the legacy register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

There are four levels of operation for the microcontroller defined as:

- Run mode
- Sleep mode
- Deep-Sleep mode
- Hibernate mode

The following sections describe the different modes in detail.

Caution – If the Cortex-M4F Debug Access Port (DAP) has been enabled, and the device wakes from a low power sleep or deep-sleep mode, the core may start executing code before all clocks to peripherals have been restored to their Run mode configuration. The DAP is usually enabled by software tools accessing the JTAG or SWD interface when debugging or flash programming. If this condition occurs, a Hard Fault is triggered when software accesses a peripheral with an invalid clock.

A software delay loop can be used at the beginning of the interrupt routine that is used to wake up a system from a WFI (Wait For Interrupt) instruction. This stalls the execution of any code that accesses a peripheral register that might cause a fault. This loop can be removed for production software as the DAP is most likely not enabled during normal execution.

Because the DAP is disabled by default (power on reset), the user can also power cycle the device. The DAP is not enabled unless it is enabled through the JTAG or SWD interface.
5.2.6.1 Run Mode

In Run mode, the microcontroller actively executes code. Run mode provides normal operation of the processor and all of the peripherals that are currently enabled by the peripheral-specific RCGC registers. The system clock can be any of the available clock sources including the PLL.

5.2.6.2 Sleep Mode

In Sleep mode, the clock frequency of the active peripherals is unchanged, but the processor and the memory subsystem are not clocked and therefore no longer execute code. Sleep mode is entered by the Cortex-M4F core executing a WFI (Wait for Interrupt) instruction. Any properly configured interrupt event in the system brings the processor back into Run mode. See "Power Management" on page 114 for more details.

Peripherals are clocked that are enabled in the peripheral-specific SCGC registers when auto-clock gating is enabled (see the RCC register) or the peripheral-specific RCGC registers when the auto-clock gating is disabled. The system clock has the same source and frequency as that during Run mode.

Additional sleep modes are available that lower the power consumption of the SRAM and Flash memory. However, the lower power consumption modes have slower sleep and wake-up times, see "Dynamic Power Management" on page 229 for more information.

Important: Before executing the WFI instruction, software must confirm that the EEPROM is not busy by checking to see that the WORKING bit in the EEPROM Done Status (EEDONE) register is clear.

5.2.6.3 Deep-Sleep Mode

In Deep-Sleep mode, the clock frequency of the active peripherals may change (depending on the Deep-Sleep mode clock configuration) in addition to the processor clock being stopped. An interrupt returns the microcontroller to Run mode from one of the sleep modes; the sleep modes are entered on request from the code. Deep-Sleep mode is entered by first setting the SLEEPDEEP bit in the System Control (SYSCTRL) register (see page 166) and then executing a WFI instruction. Any properly configured interrupt event in the system brings the processor back into Run mode. See "Power Management" on page 114 for more details.

The Cortex-M4F processor core and the memory subsystem are not clocked in Deep-Sleep mode. Peripherals are clocked that are enabled in the peripheral-specific DCGC registers when auto-clock gating is enabled (see the RCC register) or the peripheral-specific RCGC registers when auto-clock gating is disabled. The system clock source is specified in the DSLPCLKCFG register. When the DSLPCLKCFG register is used, the internal oscillator source is powered up, if necessary, and other clocks are powered down. If the PLL is running at the time of the WFI instruction, hardware powers the PLL down and overrides the SYSDIV field of the active RCC/RCC2 register, to be determined by the DDSIVORIDE setting in the DSLPCLKCFG register, up to /16 or /64 respectively. USB PLL is not powered down by execution of WFI instruction. When the Deep-Sleep exit event occurs, hardware brings the system clock back to the source and frequency it had at the onset of Deep-Sleep mode before enabling the clocks that had been stopped during the Deep-Sleep duration. If the PIOSC is used as the PLL reference clock source, it may continue to provide the clock during Deep-Sleep. See page 265.

Important: Before executing the WFI instruction, software must confirm that the EEPROM is not busy by checking to see that the WORKING bit in the EEPROM Done Status (EEDONE) register is clear.
To provide the lowest possible Deep-Sleep power consumption as well as the ability to wake the processor from a peripheral without reconfiguring the peripheral for a change in clock, some of the communications modules have a Clock Control register at offset 0xFC8 in the module register space. The CS field in the Clock Control register allows the user to select the PIOSC as the clock source for the module’s baud clock. When the microcontroller enters Deep-Sleep mode, the PIOSC becomes the source for the module clock as well, which allows the transmit and receive FIFOs to continue operation while the part is in Deep-Sleep. Figure 5-6 on page 229 shows how the clocks are selected.

![Figure 5-6. Module Clock Selection](image)

Additional deep-sleep modes are available that lower the power consumption of the SRAM and Flash memory. However, the lower power consumption modes have slower deep-sleep and wake-up times, see “Dynamic Power Management” on page 229 for more information.

5.2.6.4 Dynamic Power Management

In addition to the Sleep and Deep-Sleep modes and the clock gating for the on-chip modules, there are several additional power mode options that allow the LDO, Flash memory, and SRAM into different levels of power savings while in Sleep or Deep-Sleep modes. Note that these features may not be available on all devices; the System Properties (SYSPROP) register provides information on whether a mode is supported on a given MCU. The following registers provide these capabilities:

- **LDO Sleep Power Control (LDOSPCTL)**: controls the LDO value in Sleep mode
- **LDO Deep-Sleep Power Control (LDODPCTL)**: controls the LDO value in Deep-Sleep mode
- **LDO Sleep Power Calibration (LDOSPCAL)**: provides factory recommendations for the LDO value in Sleep mode
- **LDO Deep-Sleep Power Calibration (LDODPCAL)**: provides factory recommendations for the LDO value in Deep-Sleep mode
- **Sleep Power Configuration (SLPPWRCFG)**: controls the power saving modes for Flash memory and SRAM in Sleep mode
- **Deep-Sleep Power Configuration (DSLPPWRCFG)**: controls the power saving modes for Flash memory and SRAM in Deep-Sleep mode
Deep-Sleep Clock Configuration (DSLPCFG): controls the clocking in Deep-Sleep mode

Sleep / Deep-Sleep Power Mode Status (SDPMST): provides status information on the various power saving events

**LDO Sleep/Deep-Sleep Power Control**

*Note:* While the device is connected through JTAG, the LDO control settings for Sleep or Deep-Sleep are not available and will not be applied.

The user can dynamically request to raise or lower the LDO voltage level to trade-off power/performance using either the LDOSPCTL register (see page 279) or the LDODPCTL register (see page 282). When lowering the LDO level, software must configure the system clock for the lower LDO value in RCC/RCC2 for Sleep mode and in DSLPCFG for Deep-Sleep mode before requesting the LDO to lower.

The LDO Power Calibration registers, LDOSPCAL and LDODPCAL, provide suggested values for the LDO in the various modes. If software requests an LDO value that is too low or too high, the value is not accepted and an error is reported in the SDPMST register.

The table below shows the maximum system clock frequency and PIOSC frequency with respect to the configured LDO voltage.

<table>
<thead>
<tr>
<th>Operating Voltage (LDO)</th>
<th>Maximum System Clock Frequency</th>
<th>PIOSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>80 MHz</td>
<td>16 MHz</td>
</tr>
<tr>
<td>0.9</td>
<td>20 MHz</td>
<td>16 MHz</td>
</tr>
</tbody>
</table>

**Flash Memory and SRAM Power Control**

During Sleep or Deep-Sleep mode, Flash memory can be in either the default active mode or the low power mode; SRAM can be in the default active mode, standby mode, or low power mode. The active mode in each case provides the fastest times to sleep and wake up, but consumes more power. Low power mode provides the lowest power consumption, but takes longer to sleep and wake up.

The SRAM can be programmed to prohibit any power management by configuring the SRAMSM bit in the System Properties (SYSPROP) register. This configuration operates in the same way that legacy Stellaris® devices operate and provides the fastest sleep and wake-up times, but consumes the most power while in Sleep and Deep-Sleep mode. Other power options are retention mode, and retention mode with lower SRAM voltage. The SRAM retention mode with lower SRAM voltage provides the lowest power consumption, but has the longest sleep and wake-up times. These modes can be independently configured for Flash memory and SRAM using the SLPPWRCFG and DSLPPWRCFG registers.

The following power saving options are available in Sleep and Deep-Sleep modes:

- The clocks can be gated according to the settings in the the peripheral-specific SCGC or DCGC registers.

- In Deep-Sleep mode, the clock source can be changed and the PIOSC can be powered off (if no active peripheral requires it) using the DSLPCFG register. These options are not available for Sleep mode.

- The LDO voltage can be changed using the LDOSPCTL or LDODPCTL register.
The Flash memory can be put into low power mode. Refer to Table 24-24 on page 1418 for wake times from Sleep and Deep-Sleep.

The SRAM can be put into standby or low power mode. Refer to Table 24-24 on page 1418 for wake times from Sleep and Deep-Sleep.

The SDPMST register provides results on the Dynamic Power Management command issued. It also has some real time status that can be viewed by a debugger or the core if it is running. These events do not trigger an interrupt and are meant to provide information to help tune software for power management. The status register gets written at the beginning of every Dynamic Power Management event request that provides error checking. There is no mechanism to clear the bits; they are overwritten on the next event. The real time data is real time and there is no event to register that information.

5.2.6.5 Hibernate Mode

In this mode, the power supplies are turned off to the main part of the microcontroller and only the Hibernation module's circuitry is active. An external wake event or RTC event is required to bring the microcontroller back to Run mode. The Cortex-M4F processor and peripherals outside of the Hibernation module see a normal "power on" sequence and the processor starts running code. Software can determine if the microcontroller has been restarted from Hibernate mode by inspecting the Hibernation module registers. For more information on the operation of Hibernate mode, see “Hibernation Module” on page 503.

5.3 Initialization and Configuration

The PLL is configured using direct register writes to the RCC/RCC2 register. If the RCC2 register is being used, the USERCC2 bit must be set and the appropriate RCC2 bit/field is used. The steps required to successfully change the PLL-based system clock are:

1. Bypass the PLL and system clock divider by setting the BYPASS bit and clearing the USESYS bit in the RCC register, thereby configuring the microcontroller to run off a "raw" clock source and allowing for the new PLL configuration to be validated before switching the system clock to the PLL.

2. Select the crystal value (XTAL) and oscillator source (OSCSRC), and clear the PWRDN bit in RCC/RCC2. Setting the XTAL field automatically pulls valid PLL configuration data for the appropriate crystal, and clearing the PWRDN bit powers and enables the PLL and its output.

3. Select the desired system divider (SYSDIV) in RCC/RCC2 and set the USESYS bit in RCC. The SYSDIV field determines the system frequency for the microcontroller.

4. Wait for the PLL to lock by polling the PLLLRIS bit in the Raw Interrupt Status (RIS) register.

5. Enable use of the PLL by clearing the BYPASS bit in RCC/RCC2.

5.4 Register Map

Table 5-7 on page 232 lists the System Control registers, grouped by function. The offset listed is a hexadecimal increment to the register's address, relative to the System Control base address of 0x400F.E000.

Note: Spaces in the System Control register space that are not used are reserved for future or internal use. Software should not modify any reserved memory address.
Additional Flash and ROM registers defined in the System Control register space are described in the “Internal Memory” on page 534.

### System Control Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>DID0</td>
<td>RO</td>
<td></td>
<td>Device Identification 0</td>
<td>238</td>
</tr>
<tr>
<td>0x004</td>
<td>DID1</td>
<td>RO</td>
<td>0x10C1.446E</td>
<td>Device Identification 1</td>
<td>240</td>
</tr>
<tr>
<td>0x030</td>
<td>PBORCTL</td>
<td>RW</td>
<td>0x0000.7FFF</td>
<td>Brown-Out Reset Control</td>
<td>243</td>
</tr>
<tr>
<td>0x050</td>
<td>RIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Raw Interrupt Status</td>
<td>244</td>
</tr>
<tr>
<td>0x054</td>
<td>IMC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Interrupt Mask Control</td>
<td>247</td>
</tr>
<tr>
<td>0x058</td>
<td>MISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>Masked Interrupt Status and Clear</td>
<td>249</td>
</tr>
<tr>
<td>0x05C</td>
<td>RESC</td>
<td>RW</td>
<td></td>
<td>Reset Cause</td>
<td>252</td>
</tr>
<tr>
<td>0x060</td>
<td>RCC</td>
<td>RW</td>
<td>0x078E.3AD1</td>
<td>Run-Mode Clock Configuration</td>
<td>254</td>
</tr>
<tr>
<td>0x06C</td>
<td>GPIOHBCTL</td>
<td>RW</td>
<td>0x0000.7E00</td>
<td>GPIO High-Performance Bus Control</td>
<td>258</td>
</tr>
<tr>
<td>0x070</td>
<td>RCC2</td>
<td>RW</td>
<td>0x07C0.6810</td>
<td>Run-Mode Clock Configuration 2</td>
<td>261</td>
</tr>
<tr>
<td>0x07C</td>
<td>MOSCCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Main Oscillator Control</td>
<td>264</td>
</tr>
<tr>
<td>0x144</td>
<td>DSLPCLKCFG</td>
<td>RW</td>
<td>0x0780.0000</td>
<td>Deep Sleep Clock Configuration</td>
<td>265</td>
</tr>
<tr>
<td>0x14C</td>
<td>SYSPROP</td>
<td>RO</td>
<td>0x0000.1D31</td>
<td>System Properties</td>
<td>267</td>
</tr>
<tr>
<td>0x150</td>
<td>PIOSSCAL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Precision Internal Oscillator Calibration</td>
<td>269</td>
</tr>
<tr>
<td>0x154</td>
<td>PIOSCSTAT</td>
<td>RO</td>
<td>0x0000.0040</td>
<td>Precision Internal Oscillator Statistics</td>
<td>271</td>
</tr>
<tr>
<td>0x160</td>
<td>PLLFREQ0</td>
<td>RO</td>
<td>0x0000.0032</td>
<td>PLL Frequency 0</td>
<td>272</td>
</tr>
<tr>
<td>0x164</td>
<td>PLLFREQ1</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>PLL Frequency 1</td>
<td>273</td>
</tr>
<tr>
<td>0x168</td>
<td>PLLSTAT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PLL Status</td>
<td>274</td>
</tr>
<tr>
<td>0x188</td>
<td>SLPPWRCFG</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Sleep Power Configuration</td>
<td>275</td>
</tr>
<tr>
<td>0x18C</td>
<td>DSLPPWRCFG</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Deep-Sleep Power Configuration</td>
<td>277</td>
</tr>
<tr>
<td>0x1B4</td>
<td>LDOSPCTL</td>
<td>RW</td>
<td>0x0000.0018</td>
<td>LDO Sleep Power Control</td>
<td>279</td>
</tr>
<tr>
<td>0x1B8</td>
<td>LDOSPCAL</td>
<td>RO</td>
<td>0x0000.1818</td>
<td>LDO Sleep Power Calibration</td>
<td>281</td>
</tr>
<tr>
<td>0x1BC</td>
<td>LDODPCTL</td>
<td>RW</td>
<td>0x0000.0012</td>
<td>LDO Deep-Sleep Power Control</td>
<td>282</td>
</tr>
<tr>
<td>0x1C0</td>
<td>LDODPCAL</td>
<td>RO</td>
<td>0x0000.1212</td>
<td>LDO Deep-Sleep Power Calibration</td>
<td>284</td>
</tr>
<tr>
<td>0x1CC</td>
<td>SDPMST</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Sleep / Deep-Sleep Power Mode Status</td>
<td>285</td>
</tr>
<tr>
<td>0x300</td>
<td>PPWD</td>
<td>RO</td>
<td>0x0000.0003</td>
<td>Watchdog Timer Peripheral Present</td>
<td>288</td>
</tr>
<tr>
<td>0x304</td>
<td>PPTIMER</td>
<td>RO</td>
<td>0x0000.003F</td>
<td>16/32-Bit General-Purpose Timer Peripheral Present</td>
<td>289</td>
</tr>
<tr>
<td>0x308</td>
<td>PPGPIO</td>
<td>RO</td>
<td>0x0000.03FF</td>
<td>General-Purpose Input/Output Peripheral Present</td>
<td>291</td>
</tr>
<tr>
<td>0x30C</td>
<td>PDMA</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>Micro Direct Memory Access Peripheral Present</td>
<td>294</td>
</tr>
</tbody>
</table>
### Table 5-7. System Control Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x314</td>
<td>PPHIB</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>Hibernation Peripheral Present</td>
<td>295</td>
</tr>
<tr>
<td>0x318</td>
<td>PPUART</td>
<td>RO</td>
<td>0x0000.00FF</td>
<td>Universal Asynchronous Receiver/Transmitter Peripheral Present</td>
<td>296</td>
</tr>
<tr>
<td>0x31C</td>
<td>PPSSI</td>
<td>RO</td>
<td>0x0000.000F</td>
<td>Synchronous Serial Interface Peripheral Present</td>
<td>298</td>
</tr>
<tr>
<td>0x320</td>
<td>PPI2C</td>
<td>RO</td>
<td>0x0000.003F</td>
<td>Inter-Integrated Circuit Peripheral Present</td>
<td>300</td>
</tr>
<tr>
<td>0x328</td>
<td>PPUSB</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>Universal Serial Bus Peripheral Present</td>
<td>302</td>
</tr>
<tr>
<td>0x334</td>
<td>PPCAN</td>
<td>RO</td>
<td>0x0000.0003</td>
<td>Controller Area Network Peripheral Present</td>
<td>303</td>
</tr>
<tr>
<td>0x338</td>
<td>PPADC</td>
<td>RO</td>
<td>0x0000.0003</td>
<td>Analog-to-Digital Converter Peripheral Present</td>
<td>304</td>
</tr>
<tr>
<td>0x33C</td>
<td>PPACMP</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>Analog Comparator Peripheral Present</td>
<td>305</td>
</tr>
<tr>
<td>0x340</td>
<td>PPPWM</td>
<td>RO</td>
<td>0x0000.0003</td>
<td>Pulse Width Modulator Peripheral Present</td>
<td>306</td>
</tr>
<tr>
<td>0x344</td>
<td>PPQEI</td>
<td>RO</td>
<td>0x0000.0003</td>
<td>Quadrature Encoder Interface Peripheral Present</td>
<td>307</td>
</tr>
<tr>
<td>0x358</td>
<td>PPEEPROM</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>EEPROM Peripheral Present</td>
<td>308</td>
</tr>
<tr>
<td>0x35C</td>
<td>PPWTIMER</td>
<td>RO</td>
<td>0x0000.003F</td>
<td>32/64-Bit Wide General-Purpose Timer Peripheral Present</td>
<td>309</td>
</tr>
<tr>
<td>0x500</td>
<td>SRWD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Watchdog Timer Software Reset</td>
<td>311</td>
</tr>
<tr>
<td>0x504</td>
<td>SRTIMER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>16/32-Bit General-Purpose Timer Software Reset</td>
<td>313</td>
</tr>
<tr>
<td>0x508</td>
<td>SRGPIO</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>General-Purpose Input/Output Software Reset</td>
<td>315</td>
</tr>
<tr>
<td>0x50C</td>
<td>SRDMA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Micro Direct Memory Access Software Reset</td>
<td>318</td>
</tr>
<tr>
<td>0x514</td>
<td>SRHIB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Hibernation Software Reset</td>
<td>319</td>
</tr>
<tr>
<td>0x518</td>
<td>SRUART</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Universal Asynchronous Receiver/Transmitter Software Reset</td>
<td>320</td>
</tr>
<tr>
<td>0x51C</td>
<td>SRSSI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Synchronous Serial Interface Software Reset</td>
<td>322</td>
</tr>
<tr>
<td>0x520</td>
<td>SRI2C</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Inter-Integrated Circuit Software Reset</td>
<td>324</td>
</tr>
<tr>
<td>0x528</td>
<td>SRUSB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Universal Serial Bus Software Reset</td>
<td>326</td>
</tr>
<tr>
<td>0x534</td>
<td>SRCAN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Controller Area Network Software Reset</td>
<td>327</td>
</tr>
<tr>
<td>0x538</td>
<td>SRADC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog-to-Digital Converter Software Reset</td>
<td>329</td>
</tr>
<tr>
<td>0x53C</td>
<td>SRACMP</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Software Reset</td>
<td>331</td>
</tr>
<tr>
<td>0x540</td>
<td>SRPWM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Pulse Width Modulator Software Reset</td>
<td>332</td>
</tr>
<tr>
<td>0x544</td>
<td>SRQEI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Quadrature Encoder Interface Software Reset</td>
<td>334</td>
</tr>
<tr>
<td>0x558</td>
<td>Sjeeeprom</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Software Reset</td>
<td>336</td>
</tr>
<tr>
<td>0x55C</td>
<td>SRWTIMER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>32/64-Bit Wide General-Purpose Timer Software Reset</td>
<td>337</td>
</tr>
<tr>
<td>0x600</td>
<td>RCGCWD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Watchdog Timer Run Mode Clock Gating Control</td>
<td>339</td>
</tr>
<tr>
<td>0x604</td>
<td>RCGCTIMER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>16/32-Bit General-Purpose Timer Run Mode Clock Gating Control</td>
<td>340</td>
</tr>
</tbody>
</table>
Table 5-7. System Control Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x608</td>
<td>RCGCGPIO</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>General-Purpose Input/Output Run Mode Clock Gating Control</td>
<td>342</td>
</tr>
<tr>
<td>0x60C</td>
<td>RCGCDMA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Micro Direct Memory Access Run Mode Clock Gating Control</td>
<td>345</td>
</tr>
<tr>
<td>0x614</td>
<td>RCGCHIB</td>
<td>RW</td>
<td>0x0000.00001</td>
<td>Hibernation Run Mode Clock Gating Control</td>
<td>346</td>
</tr>
<tr>
<td>0x618</td>
<td>RCGCUART</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Universal Asynchronous Receiver/Transmitter Run Mode Clock Gating Control</td>
<td>347</td>
</tr>
<tr>
<td>0x61C</td>
<td>RCGCSSI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Synchronous Serial Interface Run Mode Clock Gating Control</td>
<td>349</td>
</tr>
<tr>
<td>0x620</td>
<td>RCGCI2C</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Inter-Integrated Circuit Run Mode Clock Gating Control</td>
<td>351</td>
</tr>
<tr>
<td>0x628</td>
<td>RCGCUSB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Universal Serial Bus Run Mode Clock Gating Control</td>
<td>353</td>
</tr>
<tr>
<td>0x634</td>
<td>RCGCCAN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Controller Area Network Run Mode Clock Gating Control</td>
<td>354</td>
</tr>
<tr>
<td>0x638</td>
<td>RCGCADC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog-to-Digital Converter Run Mode Clock Gating Control</td>
<td>355</td>
</tr>
<tr>
<td>0x63C</td>
<td>RCGCACMP</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Run Mode Clock Gating Control</td>
<td>356</td>
</tr>
<tr>
<td>0x640</td>
<td>RCGCPWM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Pulse Width Modulator Run Mode Clock Gating Control</td>
<td>357</td>
</tr>
<tr>
<td>0x644</td>
<td>RCGCQEI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Quadrature Encoder Interface Run Mode Clock Gating Control</td>
<td>358</td>
</tr>
<tr>
<td>0x658</td>
<td>RCGCEEPROM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Run Mode Clock Gating Control</td>
<td>359</td>
</tr>
<tr>
<td>0x65C</td>
<td>RCGCWTIMER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>32/64-Bit Wide General-Purpose Timer Run Mode Clock Gating Control</td>
<td>360</td>
</tr>
<tr>
<td>0x700</td>
<td>SCGCWD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Watchdog Timer Sleep Mode Clock Gating Control</td>
<td>362</td>
</tr>
<tr>
<td>0x704</td>
<td>SCGCTIMER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>16/32-Bit General-Purpose Timer Sleep Mode Clock Gating Control</td>
<td>363</td>
</tr>
<tr>
<td>0x708</td>
<td>SCGCGPIO</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>General-Purpose Input/Output Sleep Mode Clock Gating Control</td>
<td>365</td>
</tr>
<tr>
<td>0x70C</td>
<td>SCGCDMA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Micro Direct Memory Access Sleep Mode Clock Gating Control</td>
<td>368</td>
</tr>
<tr>
<td>0x714</td>
<td>SCGCHIB</td>
<td>RW</td>
<td>0x0000.000001</td>
<td>Hibernation Sleep Mode Clock Gating Control</td>
<td>369</td>
</tr>
<tr>
<td>0x718</td>
<td>SCGCUART</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Universal Asynchronous Receiver/Transmitter Sleep Mode Clock Gating Control</td>
<td>370</td>
</tr>
<tr>
<td>0x71C</td>
<td>SCGCSSI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Synchronous Serial Interface Sleep Mode Clock Gating Control</td>
<td>372</td>
</tr>
<tr>
<td>0x720</td>
<td>SCGCI2C</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Inter-Integrated Circuit Sleep Mode Clock Gating Control</td>
<td>374</td>
</tr>
<tr>
<td>0x728</td>
<td>SCGCUSB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Universal Serial Bus Sleep Mode Clock Gating Control</td>
<td>376</td>
</tr>
<tr>
<td>0x734</td>
<td>SCGCCAN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Controller Area Network Sleep Mode Clock Gating Control</td>
<td>377</td>
</tr>
</tbody>
</table>
### Table 5-7. System Control Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x738</td>
<td>SCGCADC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog-to-Digital Converter Sleep Mode Clock Gating Control</td>
<td>378</td>
</tr>
<tr>
<td>0x73C</td>
<td>SCGCACMP</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Sleep Mode Clock Gating Control</td>
<td>379</td>
</tr>
<tr>
<td>0x740</td>
<td>SCGCPWM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Pulse Width Modulator Sleep Mode Clock Gating Control</td>
<td>380</td>
</tr>
<tr>
<td>0x744</td>
<td>SCGCQEI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Quadrature Encoder Interface Sleep Mode Clock Gating Control</td>
<td>381</td>
</tr>
<tr>
<td>0x758</td>
<td>SCGCEEPROM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Sleep Mode Clock Gating Control</td>
<td>382</td>
</tr>
<tr>
<td>0x75C</td>
<td>SCGCWTIMER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>32/64-Bit Wide General-Purpose Timer Sleep Mode Clock Gating Control</td>
<td>383</td>
</tr>
<tr>
<td>0x800</td>
<td>DCGCWDD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Watchdog Timer Deep-Sleep Mode Clock Gating Control</td>
<td>385</td>
</tr>
<tr>
<td>0x804</td>
<td>DCGCTIMER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>16/32-Bit General-Purpose Timer Deep-Sleep Mode Clock Gating Control</td>
<td>386</td>
</tr>
<tr>
<td>0x808</td>
<td>DCGCGPIO</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>General-Purpose Input/Output Deep-Sleep Mode Clock Gating Control</td>
<td>388</td>
</tr>
<tr>
<td>0x80C</td>
<td>DCGCDMA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Micro Direct Memory Access Deep-Sleep Mode Clock Gating Control</td>
<td>391</td>
</tr>
<tr>
<td>0x814</td>
<td>DCGCHIB</td>
<td>RW</td>
<td>0x0000.0001</td>
<td>Hibernation Deep-Sleep Mode Clock Gating Control</td>
<td>392</td>
</tr>
<tr>
<td>0x818</td>
<td>DCGCUART</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Universal Asynchronous Receiver/Transmitter Deep-Sleep Mode Clock Gating Control</td>
<td>393</td>
</tr>
<tr>
<td>0x81C</td>
<td>DCGCSSI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Synchronous Serial Interface Deep-Sleep Mode Clock Gating Control</td>
<td>395</td>
</tr>
<tr>
<td>0x820</td>
<td>DCGC12C</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Inter-Integrated Circuit Deep-Sleep Mode Clock Gating Control</td>
<td>397</td>
</tr>
<tr>
<td>0x828</td>
<td>DGCUSB</td>
<td>RW</td>
<td>0x0001.0000</td>
<td>Universal Serial Bus Deep-Sleep Mode Clock Gating Control</td>
<td>399</td>
</tr>
<tr>
<td>0x834</td>
<td>DGCACCAN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Controller Area Network Deep-Sleep Mode Clock Gating Control</td>
<td>400</td>
</tr>
<tr>
<td>0x838</td>
<td>DCGCADC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog-to-Digital Converter Deep-Sleep Mode Clock Gating Control</td>
<td>401</td>
</tr>
<tr>
<td>0x83C</td>
<td>DCGCACP</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Deep-Sleep Mode Clock Gating Control</td>
<td>402</td>
</tr>
<tr>
<td>0x840</td>
<td>DCGCPWM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Pulse Width Modulator Deep-Sleep Mode Clock Gating Control</td>
<td>403</td>
</tr>
<tr>
<td>0x844</td>
<td>DCGCQEI</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Quadrature Encoder Interface Deep-Sleep Mode Clock Gating Control</td>
<td>404</td>
</tr>
<tr>
<td>0x858</td>
<td>DCGEeprom</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Deep-Sleep Mode Clock Gating Control</td>
<td>405</td>
</tr>
<tr>
<td>0x85C</td>
<td>DGCWTIMER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>32/64-Bit Wide General-Purpose Timer Deep-Sleep Mode Clock Gating Control</td>
<td>406</td>
</tr>
<tr>
<td>0x880</td>
<td>PRWD</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Watchdog Timer Peripheral Ready</td>
<td>408</td>
</tr>
</tbody>
</table>
### Table 5-7. System Control Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA04</td>
<td>PRTIMER</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>16/32-Bit General-Purpose Timer Peripheral Ready</td>
<td>409</td>
</tr>
<tr>
<td>0xA08</td>
<td>PRGPIO</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>General-Purpose Input/Output Peripheral Ready</td>
<td>411</td>
</tr>
<tr>
<td>0xA0C</td>
<td>PRDMA</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Micro Direct Memory Access Peripheral Ready</td>
<td>413</td>
</tr>
<tr>
<td>0xA14</td>
<td>PRHIB</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>Hibernation Peripheral Ready</td>
<td>414</td>
</tr>
<tr>
<td>0xA18</td>
<td>PRUART</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Universal Asynchronous Receiver/Transmitter Peripheral Ready</td>
<td>415</td>
</tr>
<tr>
<td>0xA1C</td>
<td>PRSSI</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Synchronous Serial Interface Peripheral Ready</td>
<td>417</td>
</tr>
<tr>
<td>0xA20</td>
<td>PRI2C</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Inter-Integrated Circuit Peripheral Ready</td>
<td>419</td>
</tr>
<tr>
<td>0xA28</td>
<td>PRUSB</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Universal Serial Bus Peripheral Ready</td>
<td>421</td>
</tr>
<tr>
<td>0xA34</td>
<td>PRCAN</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Controller Area Network Peripheral Ready</td>
<td>422</td>
</tr>
<tr>
<td>0xA38</td>
<td>PRADC</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Analog-to-Digital Converter Peripheral Ready</td>
<td>423</td>
</tr>
<tr>
<td>0xA3C</td>
<td>PRACMP</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Analog Comparator Peripheral Ready</td>
<td>424</td>
</tr>
<tr>
<td>0xA40</td>
<td>PRPWM</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Pulse Width Modulator Peripheral Ready</td>
<td>425</td>
</tr>
<tr>
<td>0xA44</td>
<td>PRQEI</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Quadrature Encoder Interface Peripheral Ready</td>
<td>426</td>
</tr>
<tr>
<td>0xA58</td>
<td>PREEPROM</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>EEPROM Peripheral Ready</td>
<td>427</td>
</tr>
<tr>
<td>0xA5C</td>
<td>PRWTIMER</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>32/64-Bit Wide General-Purpose Timer Peripheral Ready</td>
<td>428</td>
</tr>
</tbody>
</table>

#### System Control Legacy Registers

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x008</td>
<td>DC0</td>
<td>RO</td>
<td>0x007F.007F</td>
<td>Device Capabilities 0</td>
<td>430</td>
</tr>
<tr>
<td>0x010</td>
<td>DC1</td>
<td>RO</td>
<td>0x1333.2FFF</td>
<td>Device Capabilities 1</td>
<td>432</td>
</tr>
<tr>
<td>0x014</td>
<td>DC2</td>
<td>RO</td>
<td>0x070F.F337</td>
<td>Device Capabilities 2</td>
<td>435</td>
</tr>
<tr>
<td>0x018</td>
<td>DC3</td>
<td>RO</td>
<td>0xBFFF.FFFF</td>
<td>Device Capabilities 3</td>
<td>438</td>
</tr>
<tr>
<td>0x01C</td>
<td>DC4</td>
<td>RO</td>
<td>0x0004.F1FF</td>
<td>Device Capabilities 4</td>
<td>442</td>
</tr>
<tr>
<td>0x020</td>
<td>DC5</td>
<td>RO</td>
<td>0x0F30.00FF</td>
<td>Device Capabilities 5</td>
<td>445</td>
</tr>
<tr>
<td>0x024</td>
<td>DC6</td>
<td>RO</td>
<td>0x0000.0013</td>
<td>Device Capabilities 6</td>
<td>447</td>
</tr>
<tr>
<td>0x028</td>
<td>DC7</td>
<td>RO</td>
<td>0xFFF.FFFF</td>
<td>Device Capabilities 7</td>
<td>448</td>
</tr>
<tr>
<td>0x02C</td>
<td>DC8</td>
<td>RO</td>
<td>0xFFFF.FFFF</td>
<td>Device Capabilities 8</td>
<td>451</td>
</tr>
<tr>
<td>0x040</td>
<td>SRCR0</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software Reset Control 0</td>
<td>454</td>
</tr>
<tr>
<td>0x044</td>
<td>SRCR1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software Reset Control 1</td>
<td>456</td>
</tr>
<tr>
<td>0x048</td>
<td>SRCR2</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software Reset Control 2</td>
<td>459</td>
</tr>
<tr>
<td>0x100</td>
<td>RCGC0</td>
<td>RO</td>
<td>0x0000.0040</td>
<td>Run Mode Clock Gating Control Register 0</td>
<td>461</td>
</tr>
<tr>
<td>0x104</td>
<td>RCGC1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Run Mode Clock Gating Control Register 1</td>
<td>465</td>
</tr>
<tr>
<td>0x108</td>
<td>RCGC2</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Run Mode Clock Gating Control Register 2</td>
<td>469</td>
</tr>
</tbody>
</table>
5.5 **System Control Register Descriptions**

All addresses given are relative to the System Control base address of 0x400F.E000. Registers provided for legacy software support only are listed in “System Control Legacy Register Descriptions” on page 429.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x110</td>
<td>SCGC0</td>
<td>RO</td>
<td>0x0000.0040</td>
<td>Sleep Mode Clock Gating Control Register 0</td>
<td>472</td>
</tr>
<tr>
<td>0x114</td>
<td>SCGC1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Sleep Mode Clock Gating Control Register 1</td>
<td>475</td>
</tr>
<tr>
<td>0x118</td>
<td>SCGC2</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Sleep Mode Clock Gating Control Register 2</td>
<td>479</td>
</tr>
<tr>
<td>0x120</td>
<td>DCGC0</td>
<td>RO</td>
<td>0x0000.0040</td>
<td>Deep Sleep Mode Clock Gating Control Register 0</td>
<td>482</td>
</tr>
<tr>
<td>0x124</td>
<td>DCGC1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Deep-Sleep Mode Clock Gating Control Register 1</td>
<td>485</td>
</tr>
<tr>
<td>0x128</td>
<td>DCGC2</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Deep Sleep Mode Clock Gating Control Register 2</td>
<td>489</td>
</tr>
<tr>
<td>0x190</td>
<td>DC9</td>
<td>RO</td>
<td>0x00FF.00FF</td>
<td>Device Capabilities 9</td>
<td>492</td>
</tr>
<tr>
<td>0x1A0</td>
<td>NVMSTAT</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>Non-Volatile Memory Information</td>
<td>494</td>
</tr>
</tbody>
</table>
Register 1: Device Identification 0 (DID0), offset 0x000

This register identifies the version of the microcontroller. Each microcontroller is uniquely identified by the combined values of the CLASS field in the DID0 register and the PARTNO field in the DID1 register. The MAJOR and MINOR bit fields indicate the die revision number. Combined, the MAJOR and MINOR bit fields indicate the part revision number.

<table>
<thead>
<tr>
<th>MAJOR Bitfield Value</th>
<th>MINOR Bitfield Value</th>
<th>Die Revision</th>
<th>Part Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0x0</td>
<td>A0</td>
<td>1</td>
</tr>
<tr>
<td>0x0</td>
<td>0x1</td>
<td>A1</td>
<td>2</td>
</tr>
<tr>
<td>0x0</td>
<td>0x2</td>
<td>A2</td>
<td>3</td>
</tr>
<tr>
<td>0x0</td>
<td>0x3</td>
<td>A3</td>
<td>4</td>
</tr>
<tr>
<td>0x1</td>
<td>0x0</td>
<td>B0</td>
<td>5</td>
</tr>
<tr>
<td>0x1</td>
<td>0x1</td>
<td>B1</td>
<td>6</td>
</tr>
<tr>
<td>0x1</td>
<td>0x2</td>
<td>B2</td>
<td>7</td>
</tr>
</tbody>
</table>

Device Identification 0 (DID0)

Base 0x400F.E000
Offset 0x000
Type RO, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>30:28</td>
<td>VER</td>
<td>RO</td>
<td>0x01</td>
<td>DID0 Version</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field defines the DID0 register format version. The version number is numeric. The value of the VER field is encoded as follows (all other encodings are reserved):</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>0x1</td>
<td>Second version of the DID0 register format.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>27:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x08</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
The **CLASS** field value identifies the internal design from which all mask sets are generated for all microcontrollers in a particular product line. The **CLASS** field value is changed for new product lines, for changes in fab process (for example, a remap or shrink), or any case where the **MAJOR** or **MINOR** fields require differentiation from prior microcontrollers. The value of the **CLASS** field is encoded as follows (all other encodings are reserved):

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x05</td>
<td>Tiva™ TM4C123x microcontrollers</td>
</tr>
</tbody>
</table>

The **MAJOR** field specifies the major revision number of the microcontroller. The major revision reflects changes to base layers of the design. This field is encoded as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Revision A (initial device)</td>
</tr>
<tr>
<td>0x1</td>
<td>Revision B (first base layer revision)</td>
</tr>
<tr>
<td>0x2</td>
<td>Revision C (second base layer revision)</td>
</tr>
</tbody>
</table>

and so on.

The **MINOR** field specifies the minor revision number of the microcontroller. The minor revision reflects changes to the metal layers of the design. The **MINOR** field value is reset when the **MAJOR** field is changed. This field is numeric and is encoded as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Initial device, or a major revision update.</td>
</tr>
<tr>
<td>0x1</td>
<td>First metal layer change.</td>
</tr>
<tr>
<td>0x2</td>
<td>Second metal layer change.</td>
</tr>
</tbody>
</table>

and so on.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:16</td>
<td>CLASS</td>
<td>RO</td>
<td>0x05</td>
<td>Device Class</td>
</tr>
<tr>
<td>15:8</td>
<td>MAJOR</td>
<td>RO</td>
<td>-</td>
<td>Major Die Revision</td>
</tr>
<tr>
<td>7:0</td>
<td>MINOR</td>
<td>RO</td>
<td>-</td>
<td>Minor Die Revision</td>
</tr>
</tbody>
</table>
Register 2: Device Identification 1 (DID1), offset 0x004

This register identifies the device family, part number, temperature range, pin count, and package type. Each microcontroller is uniquely identified by the combined values of the CLASS field in the DID0 register and the PARTNO field in the DID1 register.

Device Identification 1 (DID1)
Base 0x400F.E000
Offset 0x004
Type RO, reset 0x10C1.446E

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>VER</td>
<td>RO</td>
<td>0x1</td>
<td>DID1 Version</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Initial DID1 register format definition, indicating a Stellaris LM3Snnn device.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 Second version of the DID1 register format.</td>
</tr>
<tr>
<td>27:24</td>
<td>FAM</td>
<td>RO</td>
<td>0x0</td>
<td>Family</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Tiva™ C Series microcontrollers and legacy Stellaris microcontrollers, that is, all devices with external part numbers starting with TM4C, LM4F or LM3S.</td>
</tr>
<tr>
<td>23:16</td>
<td>PARTNO</td>
<td>RO</td>
<td>0xC1</td>
<td>Part Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0xC1 Part Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field provides the part number of the device within the family. The reset value shown indicates the TM4C123GH6PZ microcontroller.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>15:13</td>
<td>PINCOUNT</td>
<td>RO</td>
<td>0x2</td>
<td>Package Pin Count&lt;br&gt;This field specifies the number of pins on the device package. The value is encoded as follows (all other encodings are reserved):&lt;br&gt;&lt;br&gt;</td>
</tr>
<tr>
<td>0x0</td>
<td>reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2</td>
<td>100-pin package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x3</td>
<td>64-pin package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x4</td>
<td>144-pin package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x5</td>
<td>157-pin package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x6</td>
<td>168-pin package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:5</td>
<td>TEMP</td>
<td>RO</td>
<td>0x3</td>
<td>Temperature Range&lt;br&gt;This field specifies the temperature rating of the device. The value is encoded as follows (all other encodings are reserved):&lt;br&gt;&lt;br&gt;</td>
</tr>
<tr>
<td>0x0</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>Industrial temperature range (-40°C to 85°C)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2</td>
<td>Extended temperature range (-40°C to 105°C)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x3</td>
<td>Available in both industrial temperature range (-40°C to 85°C) and extended temperature range (-40°C to 105°C) devices. See “Package Information” on page 1440 for specific order numbers.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4:3</td>
<td>PKG</td>
<td>RO</td>
<td>0x1</td>
<td>Package Type&lt;br&gt;This field specifies the package type. The value is encoded as follows (all other encodings are reserved):&lt;br&gt;&lt;br&gt;</td>
</tr>
<tr>
<td>0x0</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>LQFP package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2</td>
<td>BGA package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>ROHS</td>
<td>RO</td>
<td>0x1</td>
<td>RoHS-Compliance&lt;br&gt;This bit specifies whether the device is RoHS-compliant. A 1 indicates the part is RoHS-compliant.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>1:0</td>
<td>QUAL</td>
<td>RO</td>
<td>0x2</td>
<td>Qualification Status</td>
</tr>
</tbody>
</table>

This field specifies the qualification status of the device. The value is encoded as follows (all other encodings are reserved):

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Engineering Sample (unqualified)</td>
</tr>
<tr>
<td>0x1</td>
<td>Pilot Production (unqualified)</td>
</tr>
<tr>
<td>0x2</td>
<td>Fully Qualified</td>
</tr>
</tbody>
</table>
Register 3: Brown-Out Reset Control (PBORCTL), offset 0x030

This register is responsible for controlling reset conditions after initial power-on reset.

**Note:** The BOR voltage values and center points are based on simulation only. These values are yet to be characterized and are subject to change.

### Brown-Out Reset Control (PBORCTL)

Base 0x400F.E000
Offset 0x030
Type RW, reset 0x0000.7FFF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 2         | BOR0  | RW   | 1     | VDD under BOR0 Event Action  
The VDD BOR0 trip value is 3.02V +/- 90mv.  
Value Description  
0 A BOR0 event causes an interrupt to be generated in the interrupt controller.  
1 A BOR0 event causes a reset of the microcontroller. |
| 1         | BOR1  | RW   | 1     | VDD under BOR1 Event Action  
The VDD BOR1 trip value is 2.88V +/- 90mv.  
Value Description  
0 A BOR1 event causes an interrupt to be generated to the interrupt controller.  
1 A BOR1 event causes a reset of the microcontroller. |
| 0         | reserved | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
Register 4: Raw Interrupt Status (RIS), offset 0x050

This register indicates the status for system control raw interrupts. An interrupt is sent to the interrupt controller if the corresponding bit in the Interrupt Mask Control (IMC) register is set. Writing a 1 to the corresponding bit in the Masked Interrupt Status and Clear (MISC) register clears an interrupt status bit.

Raw Interrupt Status (RIS)
Base 0x400F.E000
Offset 0x050
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>BOR0RIS</td>
<td>RO</td>
<td>0</td>
<td>VDD under BOR0 Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note the BOR0 bit in the PBORCTL register must be cleared to cause an interrupt due to a BOR0 Event. This bit is cleared by writing a 1 to the BORMIS bit in the MISC register.</td>
</tr>
<tr>
<td>10</td>
<td>VDDARIS</td>
<td>RO</td>
<td>0</td>
<td>VDDA Power OK Event Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the VDDAMIS bit in the MISC register.</td>
</tr>
<tr>
<td>9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------------------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>8</td>
<td>MOSCPUPRIS</td>
<td>RO</td>
<td>0</td>
<td>MOSC Power Up Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>Sufficient time has not passed for the MOSC to reach the expected frequency.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Sufficient time has passed for the MOSC to reach the expected frequency. The value for this power-up time is indicated by ( T_{MOSC_START} ).</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to the MOSCPUPMIS bit in the MISC register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>USBPLLLRIS</td>
<td>RO</td>
<td>0</td>
<td>USB PLL Lock Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>The USB PLL timer has not reached ( T_{READY} ).</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>The USB PLL timer has reached ( T_{READY} ) indicating that sufficient time has passed for the USB PLL to lock.</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to the USBPLLLMIS bit in the MISC register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PLLLRIS</td>
<td>RO</td>
<td>0</td>
<td>PLL Lock Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>The PLL timer has not reached ( T_{READY} ).</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>The PLL timer has reached ( T_{READY} ) indicating that sufficient time has passed for the PLL to lock.</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to the PLLLMIS bit in the MISC register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>MOFRIS</td>
<td>RO</td>
<td>0</td>
<td>Main Oscillator Failure Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>The main oscillator has not failed.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>The MOSCIM bit in the MOSCCTL register is set and the main oscillator has failed.</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to the MOFMIS bit in the MISC register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>BOR1IS</td>
<td>RO</td>
<td>0</td>
<td>VDD under BOR1 Raw Interrupt Status</td>
</tr>
</tbody>
</table>

Value Description

0 A VDDS BOR1 condition is not currently active.
1 A VDDS BOR1 condition is currently active.

Note the BOR1 bit in the PBORCTL register must be cleared to cause an interrupt due to a BOR1 Event. This bit is cleared by writing a 1 to the BOR1MIS bit in the MISC register.

0 reserved RO 0 Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
Register 5: Interrupt Mask Control (IMC), offset 0x054

This register contains the mask bits for system control raw interrupts. A raw interrupt, indicated by a bit being set in the Raw Interrupt Status (RIS) register, is sent to the interrupt controller if the corresponding bit in this register is set.

### Interrupt Mask Control (IMC)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x400F.E000</td>
<td>0x054</td>
<td>RW,</td>
<td>0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

#### Bit/Field | Name       | Type | Reset | Description                                                                 |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>BOR0IM</td>
<td>RW</td>
<td>0</td>
<td>VDD under BOR0 Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>VDDAIM</td>
<td>RW</td>
<td>0</td>
<td>VDDA Power OK Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>MOSCPUPIM</td>
<td>RW</td>
<td>0</td>
<td>MOSC Power Up Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>7</td>
<td>USBPLLIM</td>
<td>RW</td>
<td>0</td>
<td>USB PLL Lock Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The <strong>USBPLLIRIS</strong> interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the <strong>USBPLLIRIS</strong> bit in the <strong>RIS</strong> register is set.</td>
</tr>
<tr>
<td>6</td>
<td>PLLIM</td>
<td>RW</td>
<td>0</td>
<td>PLL Lock Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The <strong>PLLIRIS</strong> interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the <strong>PLLIRIS</strong> bit in the <strong>RIS</strong> register is set.</td>
</tr>
<tr>
<td>5:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>MOFIM</td>
<td>RW</td>
<td>0</td>
<td>Main Oscillator Failure Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The <strong>MOFRIS</strong> interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the <strong>MOFRIS</strong> bit in the <strong>RIS</strong> register is set.</td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>BOR1IM</td>
<td>RW</td>
<td>0</td>
<td>VDD under BOR1 Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The <strong>BOR1RIS</strong> interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the <strong>BOR1RIS</strong> bit in the <strong>RIS</strong> register is set.</td>
</tr>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
## Register 6: Masked Interrupt Status and Clear (MISC), offset 0x058

On a read, this register gives the current masked status value of the corresponding interrupt in the **Raw Interrupt Status (RIS)** register. All of the bits are RW1C, thus writing a 1 to a bit clears the corresponding raw interrupt bit in the RIS register (see page 244).

**Masked Interrupt Status and Clear (MISC)**
Base 0x400F.E000
Offset 0x058
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>BOR0MIS</td>
<td>RW1C</td>
<td>0</td>
<td>VDD under BOR0 Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>When read, a 0 indicates that a BOR0 condition has not occurred.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>When read, a 1 indicates that an unmasked interrupt was signaled because of a BOR0 condition. Writing a 1 to this bit clears it and also the BOR0RIS bit in the RIS register.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>VDDAMIS</td>
<td>RW1C</td>
<td>0</td>
<td>VDDA Power OK Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>When read, a 0 indicates that VDDA power is good. A write of 0 has no effect on the state of this bit.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>When read, a 1 indicates that an unmasked interrupt was signaled because VDDA was below the proper functioning voltage. Writing a 1 to this bit clears it and also the VDDARIS bit in the RIS register.</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------------------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>8</td>
<td>MOSCPUPMIS</td>
<td>RW1C</td>
<td>0</td>
<td>MOSC Power Up Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>When read, a 0 indicates that sufficient time has not passed for the MOSC PLL to lock.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A write of 0 has no effect on the state of this bit.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>When read, a 1 indicates that an unmasked interrupt was signaled because sufficient time has passed for the MOSC PLL to lock.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears it and also the MOSCPUPRIS bit in the RIS register.</td>
</tr>
</tbody>
</table>

| 7         | USBPLLMIS          | RW1C | 0     | USB PLL Lock Masked Interrupt Status                                        |
|           | Value Description |      |       |                                                                             |
|           | 0                  |      |       | When read, a 0 indicates that sufficient time has not passed for the USB PLL to lock. |
|           |                     |      |       | A write of 0 has no effect on the state of this bit.                       |
|           | 1                  |      |       | When read, a 1 indicates that an unmasked interrupt was signaled because sufficient time has passed for the USB PLL to lock. |
|           |                     |      |       | Writing a 1 to this bit clears it and also the USBPLLLRIS bit in the RIS register. |

| 6         | PLLLLMIS           | RW1C | 0     | PLL Lock Masked Interrupt Status                                           |
|           | Value Description |      |       |                                                                             |
|           | 0                  |      |       | When read, a 0 indicates that sufficient time has not passed for the PLL to lock. |
|           |                     |      |       | A write of 0 has no effect on the state of this bit.                       |
|           | 1                  |      |       | When read, a 1 indicates that an unmasked interrupt was signaled because sufficient time has passed for the PLL to lock. |
|           |                     |      |       | Writing a 1 to this bit clears it and also the PLLRIS bit in the RIS register. |

| 5:4       | reserved           | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |

<p>| 3         | MOFMIS             | RO   | 0     | Main Oscillator Failure Masked Interrupt Status                            |
|           | Value Description |      |       |                                                                             |
|           | 0                  |      |       | When read, a 0 indicates that the main oscillator has not failed.          |
|           |                     |      |       | A write of 0 has no effect on the state of this bit.                      |
|           | 1                  |      |       | When read, a 1 indicates that an unmasked interrupt was signaled because the main oscillator failed. |
|           |                     |      |       | Writing a 1 to this bit clears it and also the MOFRIS bit in the RIS register. |</p>
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>BOR1MIS</td>
<td>RW1C</td>
<td>0</td>
<td>VDD under BOR1 Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 7: Reset Cause (RESC), offset 0x05C

This register is set with the reset cause after reset. The bits in this register are sticky and maintain their state across multiple reset sequences, except when an power-on reset is the cause, in which case, all bits other than POR in the RESC register are cleared.

**Reset Cause (RESC)**
Base 0x400F.E000
Offset 0x05C
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>MOSCFAIL</td>
<td>RW</td>
<td>-</td>
<td>MOSC Failure Reset</td>
</tr>
<tr>
<td>15:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>WDT1</td>
<td>RW</td>
<td>-</td>
<td>Watchdog Timer 1 Reset</td>
</tr>
</tbody>
</table>

Value Description

- When read, this bit indicates that Watchdog Timer 1 has not generated a reset since the previous power-on reset.
- Writing a 0 to this bit clears it.
- When read, this bit indicates that Watchdog Timer 1 timed out and generated a reset.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>SW</td>
<td>RW</td>
<td>-</td>
<td>Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>When read, this bit indicates that a software reset has not generated a reset since the previous power-on reset. Writing a 0 to this bit clears it.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>When read, this bit indicates that a software reset has caused a reset event.</td>
</tr>
<tr>
<td>3</td>
<td>WDT0</td>
<td>RW</td>
<td>-</td>
<td>Watchdog Timer 0 Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>When read, this bit indicates that Watchdog Timer 0 has not generated a reset since the previous power-on reset. Writing a 0 to this bit clears it.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>When read, this bit indicates that Watchdog Timer 0 timed out and generated a reset.</td>
</tr>
<tr>
<td>2</td>
<td>BOR</td>
<td>RW</td>
<td>-</td>
<td>Brown-Out Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>When read, this bit indicates that a brown-out (BOR0 or BOR1) reset has not generated a reset since the previous power-on reset. Writing a 0 to this bit clears it.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>When read, this bit indicates that a brown-out (BOR0 or BOR1) reset has caused a reset event.</td>
</tr>
<tr>
<td>1</td>
<td>POR</td>
<td>RW</td>
<td>-</td>
<td>Power-On Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>When read, this bit indicates that a power-on reset has not generated a reset. Writing a 0 to this bit clears it.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>When read, this bit indicates that a power-on reset has caused a reset event.</td>
</tr>
<tr>
<td>0</td>
<td>EXT</td>
<td>RW</td>
<td>-</td>
<td>External Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>When read, this bit indicates that an external reset (RST assertion) has not caused a reset event since the previous power-on reset. Writing a 0 to this bit clears it.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>When read, this bit indicates that an external reset (RST assertion) has caused a reset event.</td>
</tr>
</tbody>
</table>
Register 8: Run-Mode Clock Configuration (RCC), offset 0x060

The bits in this register configure the system clock and oscillators.

**Important:** Write the RCC register prior to writing the RCC2 register.

Run-Mode Clock Configuration (RCC)

Base 0x400F.E000
Offset 0x060
Type RW, reset 0x078E.3AD1

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RWACG</td>
<td>27</td>
<td>Auto Clock Gating</td>
</tr>
<tr>
<td>SYSDIV</td>
<td>26:23</td>
<td>System Clock Divisor</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

This bit specifies whether the system uses the Sleep-Mode Clock Gating Control (SCGCn) registers and Deep-Sleep-Mode Clock Gating Control (DCGCn) registers if the microcontroller enters a Sleep or Deep-Sleep mode (respectively).

Value Description

0  The Run-Mode Clock Gating Control (RCGCn) registers are used when the microcontroller enters a sleep mode.
1  The SCGCn or DCGCn registers are used to control the clocks distributed to the peripherals when the microcontroller is in a sleep mode. The SCGCn and DCGCn registers allow unused peripherals to consume less power when the microcontroller is in a sleep mode.

The RCGCn registers are always used to control the clocks in Run mode.

Specifies which divisor is used to generate the system clock from either the PLL output or the oscillator source (depending on how the BYPASS bit in this register is configured). See Table 5-4 on page 223 for bit encodings.

If the SYSDIV value is less than MINSYSDIV (see page 432), and the PLL is being used, then the MINSYSDIV value is used as the divisor.

If the PLL is not being used, the SYSDIV value can be less than MINSYSDIV.
### Enable System Clock Divider

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>USESYSDIV</td>
<td>RW</td>
<td>0</td>
<td>Enable System Clock Divider</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: The system clock is used undivided.
- **1**: The system clock divider is the source for the system clock. The system clock divider is forced to be used when the PLL is selected as the source.

If the `USERCC2` bit in the `RCC2` register is set, then the `SYSDIV2` field in the `RCC2` register is used as the system clock divider rather than the `SYSDIV` field in this register.

### Enable PWM Clock Divisor

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>USEPWMDIV</td>
<td>RW</td>
<td>0</td>
<td>Enable PWM Clock Divisor</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: The system clock is the source for the PWM clock.
- **1**: The PWM clock divider is the source for the PWM clock.

Note that when the PWM divisor is used, it is applied to the clock for both PWM modules.

### PWM Unit Clock Divisor

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:17</td>
<td>PWMDIV</td>
<td>RW</td>
<td>0x7</td>
<td>PWM Unit Clock Divisor</td>
</tr>
</tbody>
</table>

This field specifies the binary divisor used to predivide the system clock down for use as the timing reference for the PWM module. The rising edge of this clock is synchronous with the system clock.

**Value Divisor**

- **0x0**: /2
- **0x1**: /4
- **0x2**: /8
- **0x3**: /16
- **0x4**: /32
- **0x5**: /64
- **0x6**: /64
- **0x7**: /64 (default)

### PLL Power Down

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>PWRDN</td>
<td>RW</td>
<td>1</td>
<td>PLL Power Down</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: The PLL is operating normally.
- **1**: The PLL is powered down. Care must be taken to ensure that another clock source is functioning and that the `BYPASS` bit is set before setting this bit.
Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

PLL Bypass

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The system clock is the PLL output clock divided by the divisor specified by SYSDIV.</td>
</tr>
<tr>
<td>1</td>
<td>The system clock is derived from the OSC source and divided by the divisor specified by SYSDIV.</td>
</tr>
</tbody>
</table>

See Table 5-4 on page 223 for programming guidelines.

**Note:** The ADC must be clocked from the PLL or directly from a 16-MHz clock source to operate properly.

Crystal Value

This field specifies the crystal value attached to the main oscillator. The encoding for this field is provided below.

Frequencies that may be used with the USB interface are indicated in the table. To function within the clocking requirements of the USB specification, a crystal of 5, 6, 8, 10, 12, or 16 MHz must be used.

<table>
<thead>
<tr>
<th>Value</th>
<th>Crystal Frequency (MHz) Not Using the PLL</th>
<th>Crystal Frequency (MHz) Using the PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00-0x5</td>
<td>reserved</td>
<td>reserved</td>
</tr>
<tr>
<td>0x06</td>
<td>4 MHz</td>
<td>reserved</td>
</tr>
<tr>
<td>0x07</td>
<td>4.096 MHz</td>
<td>reserved</td>
</tr>
<tr>
<td>0x08</td>
<td>4.9152 MHz</td>
<td>reserved</td>
</tr>
<tr>
<td>0x09</td>
<td>5 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x0A</td>
<td>5.12 MHz</td>
<td></td>
</tr>
<tr>
<td>0x0B</td>
<td>6 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x0C</td>
<td>6.144 MHz</td>
<td></td>
</tr>
<tr>
<td>0x0D</td>
<td>7.3728 MHz</td>
<td></td>
</tr>
<tr>
<td>0x0E</td>
<td>8 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x0F</td>
<td>8.192 MHz</td>
<td></td>
</tr>
<tr>
<td>0x10</td>
<td>10.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x11</td>
<td>12.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x12</td>
<td>12.288 MHz</td>
<td></td>
</tr>
<tr>
<td>0x13</td>
<td>13.56 MHz</td>
<td></td>
</tr>
<tr>
<td>0x14</td>
<td>14.31818 MHz</td>
<td></td>
</tr>
<tr>
<td>0x15</td>
<td>16.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x16</td>
<td>16.384 MHz</td>
<td></td>
</tr>
<tr>
<td>0x17</td>
<td>18.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x18</td>
<td>20.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x19</td>
<td>24.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x1A</td>
<td>25.0 MHz (USB)</td>
<td></td>
</tr>
</tbody>
</table>
**Oscillator Source**

Selects the input source for the OSC. The values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Input Source</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>MOSC</td>
<td>Main oscillator</td>
</tr>
<tr>
<td>0x1</td>
<td>PIOSC</td>
<td>Precision internal oscillator (default)</td>
</tr>
<tr>
<td>0x2</td>
<td>PIOSC/4</td>
<td>Precision internal oscillator / 4</td>
</tr>
<tr>
<td>0x3</td>
<td>LFIOSC</td>
<td>Low-frequency internal oscillator</td>
</tr>
</tbody>
</table>

For additional oscillator sources, see the **RCC2** register.

**Main Oscillator Disable**

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The main oscillator is enabled.</td>
</tr>
<tr>
<td>1</td>
<td>The main oscillator is disabled (default).</td>
</tr>
</tbody>
</table>
Register 9: GPIO High-Performance Bus Control (GPIOHBCTL), offset 0x06C

This register controls which internal bus is used to access each GPIO port. When a bit is clear, the corresponding GPIO port is accessed across the legacy Advanced Peripheral Bus (APB) bus and through the APB memory aperture. When a bit is set, the corresponding port is accessed across the Advanced High-Performance Bus (AHB) bus and through the AHB memory aperture. Each GPIO port can be individually configured to use AHB or APB, but may be accessed only through one aperture. The AHB bus provides better back-to-back access performance than the APB bus. The address aperture in the memory map changes for the ports that are enabled for AHB access (see Table 10-6 on page 671).

**Important:** Ports K-N and P-Q are only available on the AHB bus, and therefore the corresponding bits reset to 1. If one of these bits is cleared, the corresponding port is disabled. If any of these ports is in use, read-modify-write operations should be used to change the value of this register so that these ports remain enabled.

### GPIO High-Performance Bus Control (GPIOHBCTL)

**Base 0x400F.E000**
**Offset 0x06C**
**Type RW, reset 0x0000.7E00**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>PORTK</td>
<td>RW</td>
<td>1</td>
<td>Port K Advanced High-Performance Bus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port K.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Port K is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Advanced High-Performance Bus (AHB)</td>
</tr>
<tr>
<td>8</td>
<td>PORTJ</td>
<td>RW</td>
<td>0</td>
<td>Port J Advanced High-Performance Bus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port J.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Advanced Peripheral Bus (APB). This bus is the legacy bus.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Advanced High-Performance Bus (AHB)</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>7</td>
<td>PORTH</td>
<td>RW</td>
<td>0</td>
<td>Port H Advanced High-Performance Bus&lt;br&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port H.</td>
</tr>
<tr>
<td>6</td>
<td>PORTG</td>
<td>RW</td>
<td>0</td>
<td>Port G Advanced High-Performance Bus&lt;br&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port G.</td>
</tr>
<tr>
<td>5</td>
<td>PORTF</td>
<td>RW</td>
<td>0</td>
<td>Port F Advanced High-Performance Bus&lt;br&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port F.</td>
</tr>
<tr>
<td>4</td>
<td>PORTE</td>
<td>RW</td>
<td>0</td>
<td>Port E Advanced High-Performance Bus&lt;br&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port E.</td>
</tr>
<tr>
<td>3</td>
<td>PORTD</td>
<td>RW</td>
<td>0</td>
<td>Port D Advanced High-Performance Bus&lt;br&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port D.</td>
</tr>
<tr>
<td>2</td>
<td>PORTC</td>
<td>RW</td>
<td>0</td>
<td>Port C Advanced High-Performance Bus&lt;br&gt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port C.</td>
</tr>
</tbody>
</table>

## Value Description

- **0**: Advanced Peripheral Bus (APB). This bus is the legacy bus.
- **1**: Advanced High-Performance Bus (AHB)
### System Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PORTB</td>
<td>RW</td>
<td>0</td>
<td>Port B Advanced High-Performance Bus</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit defines the memory aperture for Port B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

| 0         | PORTA | RW   | 0     | Port A Advanced High-Performance Bus   |
|           |       |      |       | This bit defines the memory aperture for Port A. |
|           |       |      |       | **Value** | **Description**                      |
|           |       |      |       | 0       | Advanced Peripheral Bus (APB). This bus is the legacy bus. |
|           |       |      |       | 1       | Advanced High-Performance Bus (AHB)   |
Register 10: Run-Mode Clock Configuration 2 (RCC2), offset 0x070

This register overrides the RCC equivalent register fields, as shown in Table 5-8, when the USERCC2 bit is set, allowing the extended capabilities of the RCC2 register to be used while also providing a means to be backward-compatible to previous parts. Each RCC2 field that supersedes an RCC field is located at the same LSB bit position; however, some RCC2 fields are larger than the corresponding RCC field.

Table 5-8. RCC2 Fields that Override RCC Fields

<table>
<thead>
<tr>
<th>RCC2 Field...</th>
<th>Overrides RCC Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYSDIV2, bits[28:23]</td>
<td>SYSDIV, bits[26:23]</td>
</tr>
</tbody>
</table>

Important: Write the RCC register prior to writing the RCC2 register.

Run-Mode Clock Configuration 2 (RCC2)
Base 0x400F.E000
Offset 0x070
Type RW, reset 0x07C0.6810

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>Use RCC2</td>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>31</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The RCC register fields are used, and the fields in RCC2 are ignored.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The RCC2 register fields override the RCC register fields.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Divide PLL as 400 MHz versus 200 MHz</td>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>30</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Use SYSDIV2 as is and apply to 200 MHz predivided PLL output. See Table 5-5 on page 223 for programming guidelines.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Append the SYSDIV2LSB bit to the SYSDIV2 field to create a 7 bit divisor using the 400 MHz PLL output, see Table 5-6 on page 224.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------------------</td>
<td>------</td>
<td>-------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>29</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 28:23    | SYSDIV2            | RW   | 0x0F  | System Clock Divisor 2  
Specifies which divisor is used to generate the system clock from either the PLL output or the oscillator source (depending on how the BYPASS2 bit is configured). SYSDIV2 is used for the divisor when both the USESYSDIV bit in the RCC register and the USERCC2 bit in this register are set. See Table 5-5 on page 223 for programming guidelines. |
| 22       | SYSDIV2LSB         | RW   | 1     | Additional LSB for SYSDIV2  
When DIV400 is set, this bit becomes the LSB of SYSDIV2. If DIV400 is clear, this bit is not used. See Table 5-5 on page 223 for programming guidelines.  
This bit can only be set or cleared when DIV400 is set.                                                                                                                                                                                                                   |
| 21:15    | reserved           | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.                                                                                                                                                           |
| 14       | USBPWRDN           | RW   | 1     | Power-Down USB PLL  
Value Description  
0 The USB PLL operates normally.  
1 The USB PLL is powered down.                                                                                                                                                                                                                                                  |
| 13       | PWRDN2             | RW   | 1     | Power-Down PLL 2  
Value Description  
0 The PLL operates normally.  
1 The PLL is powered down.                                                                                                                                                                                                                                                  |
| 12       | reserved           | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.                                                                                                                                                           |
| 11       | BYPASS2            | RW   | 1     | PLL Bypass 2  
Value Description  
0 The system clock is the PLL output clock divided by the divisor specified by SYSDIV2.  
1 The system clock is derived from the OSC source and divided by the divisor specified by SYSDIV2. See Table 5-5 on page 223 for programming guidelines.                                                                                                                                 |
| 10:7     | reserved           | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.                                                                                                                                                           |

**Note:** The ADC must be clocked from the PLL or directly from a 16-MHz clock source to operate properly.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6:4</td>
<td>OSCSRC2</td>
<td>RW</td>
<td>0x1</td>
<td>Oscillator Source 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Selects the input source for the OSC. The values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>MOSC Main oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>PIOSC Precision internal oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>PIOSC/4 Precision internal oscillator / 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>LFIOSC Low-frequency internal oscillator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x4-0x6</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x7</td>
<td>32.768 kHz 32.768-kHz external oscillator</td>
</tr>
</tbody>
</table>

3:0 reserved RO 0x0 Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
Register 11: Main Oscillator Control (MOSCCTL), offset 0x07C

This register provides control over the features of the main oscillator, including the ability to enable the MOSC clock verification circuit, what action to take when the MOSC fails, and whether or not a crystal is connected. When enabled, this circuit monitors the frequency of the MOSC to verify that the oscillator is operating within specified limits. If the clock goes invalid after being enabled, the microcontroller issues a power-on reset and reboots to the NMI handler or generates an interrupt.

Main Oscillator Control (MOSCCTL)
Base 0x400F.E000
Offset 0x07C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>NOXTAL</td>
<td>RW</td>
<td>0</td>
<td>No Crystal Connected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 This bit should be cleared when a crystal or oscillator is connected to the OSC0 and OSC1 inputs, regardless of whether or not the MOSC is used or powered down.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 This bit should be set when a crystal or external oscillator is not connected to the OSC0 and OSC1 inputs to reduce power consumption.</td>
</tr>
<tr>
<td>1</td>
<td>MOSCIM</td>
<td>RW</td>
<td>0</td>
<td>MOSC Failure Action</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 If the MOSC fails, a MOSC failure reset is generated and reboots to the NMI handler.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 If the MOSC fails, an interrupt is generated as indicated by the MOFRIS bit in the RIS register..</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Regardless of the action taken, if the MOSC fails, the oscillator source is switched to the PIOSC automatically.</td>
</tr>
<tr>
<td>0</td>
<td>CVAL</td>
<td>RW</td>
<td>0</td>
<td>Clock Validation for MOSC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The MOSC monitor circuit is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MOSC monitor circuit is enabled.</td>
</tr>
</tbody>
</table>
## Register 12: Deep Sleep Clock Configuration (DSLPCLKCFG), offset 0x144

This register provides configuration information for the hardware control of Deep Sleep Mode.

**Deep Sleep Clock Configuration (DSLPCLKCFG)**

Base 0x400F.0E00  
Offset 0x144  
Type RW, reset 0x0780.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 28:23     | DSDIVORIDE      | RW   | 0x0F  | Divider Field Override  
|           |                 |      |       | If Deep-Sleep mode is enabled when the PLL is running, the PLL is disabled. This 6-bit field contains a system divider field that overrides the SYSDIV field in the RCC register or the SYSDIV2 field in the RCC2 register during Deep Sleep. This divider is applied to the source selected by the DSOSCSRC field. |
|           |                 |      |       | Description                                                                 |
|           |                 |      |       | Value | Description |
|           | 0x0  | /1       |
|           | 0x1  | /2       |
|           | 0x2  | /3       |
|           | 0x3  | /4       |
|           | ...  | ...      |
|           | 0x3F | /64      |
| 22:7      | reserved        | RO   | 0x000 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
### Clock Source

Specifies the clock source during Deep-Sleep mode.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>MOSC</td>
</tr>
</tbody>
</table>

Use the main oscillator as the source. To use the MOSC as the Deep-Sleep mode clock source, the MOSC must also be configured as the Run mode clock source in the *Run-Mode Clock Configuration (RCC)* register.

**Note:** If the PIOSC is being used as the clock reference for the PLL, the PIOSC is the clock source instead of MOSC in Deep-Sleep mode.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1</td>
<td>PIOSC</td>
</tr>
</tbody>
</table>

Use the precision internal 16-MHz oscillator as the source.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x2</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>LFIOSC</td>
</tr>
</tbody>
</table>

Use the low-frequency internal oscillator as the source.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4-0x6</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x7</td>
<td>32.768 kHz</td>
</tr>
</tbody>
</table>

Use the Hibernation module 32.768-kHz external oscillator as the source.

#### Bit/Field

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6:4</td>
<td>DSOSCSC</td>
<td>RW</td>
<td>0x0</td>
<td>Clock Source</td>
</tr>
</tbody>
</table>

Specifies the clock source during Deep-Sleep mode.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>MOSC</td>
</tr>
</tbody>
</table>

Use the main oscillator as the source. To use the MOSC as the Deep-Sleep mode clock source, the MOSC must also be configured as the Run mode clock source in the *Run-Mode Clock Configuration (RCC)* register.

**Note:** If the PIOSC is being used as the clock reference for the PLL, the PIOSC is the clock source instead of MOSC in Deep-Sleep mode.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1</td>
<td>PIOSC</td>
</tr>
</tbody>
</table>

Use the precision internal 16-MHz oscillator as the source.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x2</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>LFIOSC</td>
</tr>
</tbody>
</table>

Use the low-frequency internal oscillator as the source.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4-0x6</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x7</td>
<td>32.768 kHz</td>
</tr>
</tbody>
</table>

Use the Hibernation module 32.768-kHz external oscillator as the source.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PIOSCP D</td>
<td>RW</td>
<td>0</td>
<td>PIOSC Power Down Request</td>
</tr>
</tbody>
</table>

Allows software to request the PIOSC to be powered-down in Deep-Sleep mode. If the PIOSC is needed by an enabled peripheral during Deep-Sleep, the PIOSC is powered down, but a warning is generated using the PPDW bit in the SDPMST register. If it is not possible to power down the PIOSC, an error is reported using the PPDERR bit in the SDPMST register.

This bit can only be used to power down the PIOSC when the PIOSCPDE bit in the SYSPROP register is set.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No action.</td>
</tr>
<tr>
<td>1</td>
<td>Software requests that the PIOSC is powered down during Deep-Sleep mode.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 13: System Properties (SYSPROP), offset 0x14C

This register provides information on whether certain System Control properties are present on the microcontroller.

System Properties (SYSPROP)
Base 0x400F.E000
Offset 0x14C
Type RO, reset 0x0000.1D31

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12</td>
<td>PIOSCPDE</td>
<td>RO</td>
<td>0x1</td>
<td>PIOSC Power Down Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The status of the PIOSCPD bit is ignored.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The PIOSCPD bit can be set to power down the PIOSC in Deep-Sleep mode.</td>
</tr>
<tr>
<td>11</td>
<td>SRAMSM</td>
<td>RO</td>
<td>0x1</td>
<td>SRAM Sleep/Deep-Sleep Standby Mode Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 A value of 0x1 in the SRAMSM fields is ignored.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The SRAMSM fields can be configured to put the SRAM into Standby mode while in Sleep or Deep-Sleep mode.</td>
</tr>
<tr>
<td>10</td>
<td>SRAMLPM</td>
<td>RO</td>
<td>0x1</td>
<td>SRAM Sleep/Deep-Sleep Low Power Mode Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 A value of 0x3 in the SRAMLPM fields is ignored.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The SRAMLPM fields can be configured to put the SRAM into Low Power mode while in Sleep or Deep-Sleep mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>FLASHLPM</td>
<td>RO</td>
<td>0x1</td>
<td>Flash Memory Sleep/Deep-Sleep Low Power Mode Present This bit determines whether the FLASHP field in the SLPPWRCFG and DSLPPWRCFG registers can be configured to put the Flash memory into Low Power mode while in Sleep or Deep-Sleep mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x3</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>FPU</td>
<td>RO</td>
<td>0x1</td>
<td>FPU Present This bit indicates if the FPU is present in the Cortex-M4 core.</td>
</tr>
</tbody>
</table>

**Value**

- **0**: FPU is not present.
- **1**: FPU is present.
Register 14: Precision Internal Oscillator Calibration (PIOSCCAL), offset 0x150

This register provides the ability to update or recalibrate the precision internal oscillator. Note that a 32.768-kHz oscillator must be used as the Hibernation module clock source for the user to be able to calibrate the PIOSC.

### Precision Internal Oscillator Calibration (PIOSCCAL)
Base 0x400F.E000
Offset 0x150
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>UTEN</td>
<td>RW</td>
<td>0</td>
<td>Use User Trim Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>30:10</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>CAL</td>
<td>RW</td>
<td>0</td>
<td>Start Calibration</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>UPDATE</td>
<td>RW</td>
<td>0</td>
<td>Update Trim</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
### Bit/Field

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6:0</td>
<td>UT</td>
<td>RW</td>
<td>0x0</td>
<td>User Trim Value&lt;br&gt; User trim value that can be loaded into the PIOSC.&lt;br&gt; Refer to “Precision Internal Oscillator Operation (PIOSC)” on page 224 for more information on calibrating the PIOSC.</td>
</tr>
</tbody>
</table>
Register 15: Precision Internal Oscillator Statistics (PIOSCSTAT), offset 0x154

This register provides the user information on the PIOSC calibration. Note that a 32.768-kHz oscillator must be used as the Hibernation module clock source for the user to be able to calibrate the PIOSC.

Precision Internal Oscillator Statistics (PIOSCSTAT)
Base 0x400F.E000
Offset 0x154
Type RO, reset 0x0000.0040

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:23</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 22:16     | DT         | RO   | -     | Default Trim Value
This field contains the default trim value. This value is loaded into the PIOSC after every full power-up. |
| 15:10     | reserved   | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 9:8       | RESULT     | RO   | 0     | Calibration Result
Value Description
0x0 Calibration has not been attempted.
0x1 The last calibration operation completed to meet 1% accuracy.
0x2 The last calibration operation failed to meet 1% accuracy.
0x3 Reserved |
| 7         | reserved   | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 6:0       | CT         | RO   | 0x40  | Calibration Trim Value
This field contains the trim value from the last calibration operation. After factory calibration CT and DT are the same. |
Register 16: PLL Frequency 0 (PLLFREQ0), offset 0x160

This register always contains the current M value presented to the system PLL.

The PLL frequency can be calculated using the following equation:

\[
\text{PLL frequency} = \frac{\text{XTAL frequency} \times \text{MDIV}}{((Q + 1) \times (N + 1))}
\]

where

\[
\text{MDIV} = \text{MINT} + \left(\frac{\text{MFRAC}}{1024}\right)
\]

The Q and N values are shown in the PLLFREQ1 register. Table 24-14 on page 1411 shows the M, Q, and N values as well as the resulting PLL frequency for the various XTAL configurations.
Register 17: PLL Frequency 1 (PLLFREQ1), offset 0x164

This register always contains the current Q and N values presented to the system PLL.

The M value is shown in the PLLFREQ0 register. Table 24-14 on page 1411 shows the M, Q, and N values as well as the resulting PLL frequency for the various X\(\text{TAL}\) configurations.

PLL Frequency 1 (PLLFREQ1)
Base 0x400F.E000
Offset 0x164
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12:8</td>
<td>Q</td>
<td>RO</td>
<td>0x0</td>
<td>PLL Q Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field contains the PLL Q value.</td>
</tr>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4:0</td>
<td>N</td>
<td>RO</td>
<td>0x1</td>
<td>PLL N Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field contains the PLL N value.</td>
</tr>
</tbody>
</table>
Register 18: PLL Status (PLLSTAT), offset 0x168

This register shows the direct status of the PLL lock.

PLL Status (PLLSTAT)
Base 0x400F.E000
Offset 0x168
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>LOCK</td>
<td>RO</td>
<td>0x0</td>
<td>PLL Lock</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   The PLL is unpowered or is not yet locked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   The PLL is powered and locked.</td>
</tr>
</tbody>
</table>
Register 19: Sleep Power Configuration (SLPPWRCFG), offset 0x188

This register provides configuration information for the power control of the SRAM and Flash memory while in Sleep mode.

Sleep Power Configuration (SLPPWRCFG)
Base 0x400F.E000
Offset 0x188
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5:4</td>
<td>FLASHPM</td>
<td>RW</td>
<td>0x0</td>
<td>Flash Power Modes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Active Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Flash memory is not placed in a lower power mode. This mode provides the fastest time to sleep and wakeup but the highest power consumption while the microcontroller is in Sleep mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Low Power Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Flash memory is placed in low power mode. This mode provides the lowers power consumption but requires more time to come out of Sleep mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 Reserved</td>
</tr>
<tr>
<td>3:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>1:0</td>
<td>SRAMP</td>
<td>RW</td>
<td>0x0</td>
<td>SRAM Power Modes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field controls the low power modes of the on-chip SRAM, including the USB SRAM while the microcontroller is in Deep-Sleep mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SRAM is not placed in a lower power mode. This mode provides the fastest time to sleep and wakeup but the highest power consumption while the microcontroller is in Sleep mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SRAM is placed in standby mode while in Sleep mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SRAM is placed in low power mode. This mode provides the slowest time to sleep and wakeup but the lowest power consumption while in Sleep mode.</td>
</tr>
</tbody>
</table>
Register 20: Deep-Sleep Power Configuration (DSLPPWRCFG), offset 0x18C

This register provides configuration information for the power control of the SRAM and Flash memory while in Deep-Sleep mode.

### Deep-Sleep Power Configuration (DSLPPWRCFG)

Base 0x400F.E000  
Offset 0x18C  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RW</td>
<td>0x0</td>
<td>Flash Power Modes</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
</tr>
<tr>
<td>5:4</td>
<td>FLASHPM</td>
<td>RW</td>
<td>0x0</td>
</tr>
</tbody>
</table>

### Flash Power Modes

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0x0   | Active Mode  
Flash memory is not placed in a lower power mode. This mode provides the fastest time to sleep and wakeup but the highest power consumption while the microcontroller is in Deep-Sleep mode. |
| 0x1   | Reserved |
| 0x2   | Low Power Mode  
Flash memory is placed in low power mode. This mode provides the lowers power consumption but requires more time to come out of Deep-Sleep mode. |
| 0x3   | Reserved |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
### SRAM Power Modes

This field controls the low power modes of the on-chip SRAM, including the USB SRAM while the microcontroller is in Deep-Sleep mode.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Active Mode&lt;br&gt;SRAM is not placed in a lower power mode. This mode provides the fastest time to sleep and wakeup but the highest power consumption while the microcontroller is in Deep-Sleep mode.</td>
</tr>
<tr>
<td>0x1</td>
<td>Standby Mode&lt;br&gt;SRAM is placed in standby mode while in Deep-Sleep mode.</td>
</tr>
<tr>
<td>0x2</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>Low Power Mode&lt;br&gt;SRAM is placed in low power mode. This mode provides the slowest time to sleep and wakeup but the lowest power consumption while in Deep-Sleep mode.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>SRAMPM</td>
<td>RW</td>
<td>0x0</td>
<td>SRAM Power Modes&lt;br&gt;This field controls the low power modes of the on-chip SRAM, including the USB SRAM while the microcontroller is in Deep-Sleep mode.</td>
</tr>
</tbody>
</table>

**Texas Instruments-Production Data**

*June 12, 2014*
Register 21: LDO Sleep Power Control (LDOSPCTL), offset 0x1B4

This register specifies the LDO output voltage while in Sleep mode. Writes to the \texttt{VLDO} bit field have no effect on the LDO output voltage, regardless of what is specified for the \texttt{VADJEN} bit. The LDO output voltage is fixed at the recommended factory reset value.

The table below shows the maximum system clock frequency and PIOSC frequency with respect to the configured LDO voltage.

<table>
<thead>
<tr>
<th>Operating Voltage (LDO)</th>
<th>Maximum System Clock Frequency</th>
<th>PIOSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>80 MHz</td>
<td>16 MHz</td>
</tr>
<tr>
<td>0.9</td>
<td>20 MHz</td>
<td>16 MHz</td>
</tr>
</tbody>
</table>

\textbf{Note:}  
- The LDO will not automatically adjust in Sleep/Deepsleep mode if a debugger has been connected since the last power-on reset.  
- If the LDO voltage is adjusted, it will take an extra 4 us to wake up from Sleep or Deep-Sleep mode.

LDO Sleep Power Control (LDOSPCTL)

Base 0x400F.E000  
Offset 0x1B4  
Type RW, reset 0x0000.0018  

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31        | VADJEN | RW   | 0     | Voltage Adjust Enable  
This bit enables the value of the \texttt{VLDO} field to be used to specify the output voltage of the LDO in Sleep mode.  

Value Description  
0  
The LDO output voltage is set to the factory default value in Sleep mode. The value of the \texttt{VLDO} field does not affect the LDO operation.  
1  
The LDO output value in Sleep mode is configured by the value in the \texttt{VLDO} field.  

30:8  
reserved  
RO  
0x000.00  
Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>VLDO</td>
<td>RW</td>
<td>0x18</td>
<td>LDO Output Voltage</td>
</tr>
</tbody>
</table>

This field provides program control of the LDO output voltage in Run mode. The value of the field is only used for the LDO voltage when the VADJEN bit is set.

For lowest power in Sleep mode, it is recommended to configure an LDO output voltage that is equal to or lower than the default value of 1.2 V.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x12</td>
<td>0.90 V</td>
</tr>
<tr>
<td>0x13</td>
<td>0.95 V</td>
</tr>
<tr>
<td>0x14</td>
<td>1.00 V</td>
</tr>
<tr>
<td>0x15</td>
<td>1.05 V</td>
</tr>
<tr>
<td>0x16</td>
<td>1.10 V</td>
</tr>
<tr>
<td>0x17</td>
<td>1.15 V</td>
</tr>
<tr>
<td>0x18</td>
<td>1.20 V</td>
</tr>
<tr>
<td>0x19 - 0xFF</td>
<td>reserved</td>
</tr>
</tbody>
</table>
Register 22: LDO Sleep Power Calibration (LDOSPCAL), offset 0x1B8

This register provides factory determined values that are recommended for the VLDO field in the LDOSPCTL register while in Sleep mode.

LDO Sleep Power Calibration (LDOSPCAL)
Base 0x400F.E000
Offset 0x1B8
Type RO, reset 0x0000.1818

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:8</td>
<td>WITHPLL</td>
<td>RO</td>
<td>0x18</td>
<td>Sleep with PLL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value in this field is the suggested value for the VLDO field in the LDOSPCTL register when using the PLL. This value provides the lowest recommended LDO output voltage for use with the PLL at the maximum specified value.</td>
</tr>
<tr>
<td>7:0</td>
<td>NOPLL</td>
<td>RO</td>
<td>0x18</td>
<td>Sleep without PLL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value in this field is the suggested value for the VLDO field in the LDOSPCTL register when not using the PLL. This value provides the lowest recommended LDO output voltage for use without the PLL.</td>
</tr>
</tbody>
</table>
Register 23: LDO Deep-Sleep Power Control (LDODPCTL), offset 0x1BC

This register specifies the LDO output voltage while in Deep-Sleep mode. This register must be configured in Run mode before entering Deep-Sleep. Writes to the VLDO bit field have no effect on the LDO output voltage, regardless of what is specified for the VADJEN bit. The LDO output voltage is fixed at the recommended factory reset value.

The table below shows the maximum system clock frequency and PIOSC frequency with respect to the configured LDO voltage.

<table>
<thead>
<tr>
<th>Operating Voltage (LDO)</th>
<th>Maximum System Clock Frequency</th>
<th>PIOSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>80 MHz</td>
<td>16 MHz</td>
</tr>
<tr>
<td>0.9</td>
<td>20 MHz</td>
<td>16 MHz</td>
</tr>
</tbody>
</table>

**Note:**
- The LDO will not automatically adjust in Sleep/Deepsleep mode if a debugger has been connected since the last power-on reset.
- If the LDO voltage is adjusted, it will take an extra 4 us to wake up from Sleep or Deep-Sleep mode.

LDO Deep-Sleep Power Control (LDODPCTL)
Base 0x400F.E000
Offset 0x1BC
Type RW, reset 0x0000.0012

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>VADJEN</td>
<td>RW</td>
<td>0</td>
<td>Voltage Adjust Enable&lt;br&gt;This bit enables the value of the VLDO field to be used to specify the output voltage of the LDO in Deep-Sleep mode.</td>
</tr>
<tr>
<td>30:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>7:0</td>
<td>VLDO</td>
<td>RW</td>
<td>0x12</td>
<td>LDO Output Voltage</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field provides program control of the LDO output voltage in Run mode. The value of the field is only used for the LDO voltage when the VADJEN bit is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For lowest power in Deep-Sleep mode, it is recommended to configure the LDO output voltage to the default value of 0.90 V.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x12</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x13</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x14</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x15</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x17</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x18</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x19 - 0xFF reserved</td>
</tr>
</tbody>
</table>
Register 24: LDO Deep-Sleep Power Calibration (LDODPCAL), offset 0x1C0

This register provides factory determined values that are recommended for the VLDO field in the LDODPCTL register while in Deep-Sleep mode.

LDO Deep-Sleep Power Calibration (LDODPCAL)
Base 0x400F.E000
Offset 0x1C0
Type RO, reset 0x0000.1212

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:8</td>
<td>NOPLL</td>
<td>RO</td>
<td>0x12</td>
<td>Deep-Sleep without PLL The value in this field is the suggested value for the VLDO field in the LDODPCTL register when not using the PLL. This value provides the lowest recommended LDO output voltage for use with the system clock.</td>
</tr>
<tr>
<td>7:0</td>
<td>30KHZ</td>
<td>RO</td>
<td>0x12</td>
<td>Deep-Sleep with IOSC The value in this field is the suggested value for the VLDO field in the LDODPCTL register when not using the PLL. This value provides the lowest recommended LDO output voltage for use with the low-frequency internal oscillator.</td>
</tr>
</tbody>
</table>
Register 25: Sleep / Deep-Sleep Power Mode Status (SDPMST), offset 0x1CC

This register provides status information on the Sleep and Deep-Sleep power modes as well as some real time status that can be viewed by a debugger or the core if it is running. These events do not trigger an interrupt and are meant to provide information that can help tune software for power management. The status register gets written at the beginning of every Dynamic Power Management event request with the results of any error checking. There is no mechanism to clear the bits; they are overwritten on the next event. The LDOUA, FLASHLP, LOWPWR, PRACT bits provide real time data and there are no events to register that information.

Sleep / Deep-Sleep Power Mode Status (SDPMST)
Base 0x400F.E000
Offset 0x1CC
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19</td>
<td>LDOUA</td>
<td>RO</td>
<td>0</td>
<td>LDO Update Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The LDO voltage level is not changing.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The LDO voltage level is changing.</td>
</tr>
<tr>
<td>18</td>
<td>FLASHLP</td>
<td>RO</td>
<td>0</td>
<td>Flash Memory in Low Power State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The Flash memory is currently in the active state.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The Flash memory is currently in the low power state as programmed in the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SLPPWRCFG or DSLPPWRCFG register.</td>
</tr>
<tr>
<td>17</td>
<td>LOWPWR</td>
<td>RO</td>
<td>0</td>
<td>Sleep or Deep-Sleep Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The microcontroller is currently in Run mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The microcontroller is currently in Sleep or Deep-Sleep mode and is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>waiting for an interrupt or is in the process of powering up. The status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>of this bit is not affected by the power state of the Flash memory or</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SRAM.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------</td>
</tr>
<tr>
<td>16</td>
<td>PRACT</td>
<td>RO</td>
<td>0</td>
<td>Sleep or Deep-Sleep Power Request Active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       A power request is not active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The microcontroller is currently in Deep-Sleep mode or is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>in Sleep mode and a request to put the SRAM and/or Flash</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>memory into a lower power mode is currently active as</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>configured by the SLPPWRCFG register.</td>
</tr>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>provide compatibility with future products, the value of a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>reserved bit should be preserved across a read-modify-write</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>operation.</td>
</tr>
<tr>
<td>7</td>
<td>PPDW</td>
<td>RO</td>
<td>0</td>
<td>PIOSC Power Down Request Warning</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       No error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       A warning has occurred because software has requested</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>that the PIOSC be powered down during Deep-Sleep using the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PIOSCPD bit in the DSLPCLKCFG register and a peripheral</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>requires that it be active in Deep-Sleep. The PIOSC is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>powered down regardless of the warning.</td>
</tr>
<tr>
<td>6</td>
<td>LMAXERR</td>
<td>RO</td>
<td>0</td>
<td>VLDO Value Above Maximum Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       No error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       An error has occurred because software has requested</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>that the LDO voltage be above the maximum value allowed using</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the VLDO bit in the LDOSPCTL or LDODPCTL register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>In this situation, the LDO is set to the factory default value.</td>
</tr>
<tr>
<td>5</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>provide compatibility with future products, the value of a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>reserved bit should be preserved across a read-modify-write</td>
</tr>
<tr>
<td>4</td>
<td>LSMINERR</td>
<td>RO</td>
<td>0</td>
<td>VLDO Value Below Minimum Error in Sleep Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       No error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       An error has occurred because software has requested</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>that the LDO voltage be below the minimum value allowed using</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the VLDO bit in the LDOSPCTL register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>In this situation, the LDO voltage is not changed when entering</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Sleep mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>3</td>
<td>LDMINERR</td>
<td>RO</td>
<td>0</td>
<td><strong>VLDO Value Below Minimum Error in Deep-Sleep Mode</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An error has occurred because software has requested that the LDO voltage be below the minimum value allowed using the VLDO bit in the LDODPCTL register. In this situation, the LDO voltage is not changed when entering Deep-Sleep mode.</td>
</tr>
<tr>
<td>2</td>
<td>PPDERR</td>
<td>RO</td>
<td>0</td>
<td><strong>PIOSC Power Down Request Error</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An error has occurred because software has requested that the PIOSC be powered down during Deep-Sleep and it is not possible to power down the PIOSC. In this situation, the PIOSC is not powered down when entering Deep-Sleep mode.</td>
</tr>
<tr>
<td>1</td>
<td>FPDERR</td>
<td>RO</td>
<td>0</td>
<td><strong>Flash Memory Power Down Request Error</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An error has occurred because software has requested a Flash memory power down mode that is not available using the FLASHPM field in the SLPPWRCFG or the DSLPPWRCFG register.</td>
</tr>
<tr>
<td>0</td>
<td>SPDERR</td>
<td>RO</td>
<td>0</td>
<td><strong>SRAM Power Down Request Error</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An error has occurred because software has requested an SRAM power down mode that is not available using the SRAMPM field in the SLPPWRCFG or the DSLPPWRCFG register.</td>
</tr>
</tbody>
</table>
Register 26: Watchdog Timer Peripheral Present (PPWD), offset 0x300

The PPWD register provides software information regarding the watchdog modules.

**Important:** This register should be used to determine which watchdog timers are implemented on this microcontroller. However, to support legacy software, the DC1 register is available. A read of the DC1 register correctly identifies if a legacy module is present.

**Watchdog Timer Peripheral Present (PPWD)**

Base 0x400F.E000
Offset 0x300
Type RO, reset 0x0000.0003

---

**Bit/Field** | **Name** | **Type** | **Reset** | **Description**
---|---|---|---|---
31:2 | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

1 | P1 | RO | 0x1 | Watchdog Timer 1 Present

Value | Description
---|---
0 | Watchdog module 1 is not present.
1 | Watchdog module 1 is present.

0 | P0 | RO | 0x1 | Watchdog Timer 0 Present

Value | Description
---|---
0 | Watchdog module 0 is not present.
1 | Watchdog module 0 is present.
Register 27: 16/32-Bit General-Purpose Timer Peripheral Present (PPTIMER), offset 0x304

The PPTIMER register provides software information regarding the 16/32-bit general-purpose timer modules.

**Important:** This register should be used to determine which timers are implemented on this microcontroller. However, to support legacy software, the DC2 register is available. A read of the DC2 register correctly identifies if a legacy module is present. Software must use this register to determine if a module that is not supported by the DC2 register is present.

16/32-Bit General-Purpose Timer Peripheral Present (PPTIMER)
Base 0x400F.E000
Offset 0x304
Type RO, reset 0x0000.003F

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>P5</td>
<td>RO</td>
<td>0x1</td>
<td>16/32-Bit General-Purpose Timer 5 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 6 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  16/32-bit general-purpose timer module 5 is present.</td>
</tr>
<tr>
<td>4</td>
<td>P4</td>
<td>RO</td>
<td>0x1</td>
<td>16/32-Bit General-Purpose Timer 4 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 4 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  16/32-bit general-purpose timer module 4 is present.</td>
</tr>
<tr>
<td>3</td>
<td>P3</td>
<td>RO</td>
<td>0x1</td>
<td>16/32-Bit General-Purpose Timer 3 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 3 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  16/32-bit general-purpose timer module 3 is present.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>2</td>
<td>P2</td>
<td>RO</td>
<td>0x1</td>
<td>16/32-Bit General-Purpose Timer 2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>RO</td>
<td>0x1</td>
<td>16/32-Bit General-Purpose Timer 1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>16/32-Bit General-Purpose Timer 0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 28: General-Purpose Input/Output Peripheral Present (PPGPIO), offset 0x308

The PPGPIO register provides software information regarding the general-purpose input/output modules.

**Important:** This register should be used to determine which GPIO ports are implemented on this microcontroller. However, to support legacy software, the DC4 register is available. A read of the DC4 register correctly identifies if a legacy module is present. Software must use this register to determine if a module that is not supported by the DC4 register is present.

General-Purpose Input/Output Peripheral Present (PPGPIO)
Base 0x400F.E000
Offset 0x308
Type RO, reset 0x0000.03FF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:15</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>14</td>
<td>P14</td>
<td>RO</td>
<td>0x0</td>
<td>GPIO Port Q Present</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>GPIO Port Q is not present.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>GPIO Port Q is present.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>P13</td>
<td>RO</td>
<td>0x0</td>
<td>GPIO Port P Present</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>GPIO Port P is not present.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>GPIO Port P is present.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>P12</td>
<td>RO</td>
<td>0x0</td>
<td>GPIO Port N Present</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>GPIO Port N is not present.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>GPIO Port N is present.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>11</td>
<td>P11</td>
<td>RO</td>
<td>0x0</td>
<td>GPIO Port M Present</td>
</tr>
<tr>
<td>10</td>
<td>P10</td>
<td>RO</td>
<td>0x0</td>
<td>GPIO Port L Present</td>
</tr>
<tr>
<td>9</td>
<td>P9</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port K Present</td>
</tr>
<tr>
<td>8</td>
<td>P8</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port J Present</td>
</tr>
<tr>
<td>7</td>
<td>P7</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port H Present</td>
</tr>
<tr>
<td>6</td>
<td>P6</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port G Present</td>
</tr>
<tr>
<td>5</td>
<td>P5</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port F Present</td>
</tr>
</tbody>
</table>

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port M is not present.</td>
</tr>
<tr>
<td>1</td>
<td>GPIO Port M is present.</td>
</tr>
</tbody>
</table>

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port L is not present.</td>
</tr>
<tr>
<td>1</td>
<td>GPIO Port L is present.</td>
</tr>
</tbody>
</table>

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port K is not present.</td>
</tr>
<tr>
<td>1</td>
<td>GPIO Port K is present.</td>
</tr>
</tbody>
</table>

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port J is not present.</td>
</tr>
<tr>
<td>1</td>
<td>GPIO Port J is present.</td>
</tr>
</tbody>
</table>

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port H is not present.</td>
</tr>
<tr>
<td>1</td>
<td>GPIO Port H is present.</td>
</tr>
</tbody>
</table>

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port G is not present.</td>
</tr>
<tr>
<td>1</td>
<td>GPIO Port G is present.</td>
</tr>
</tbody>
</table>

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port F is not present.</td>
</tr>
<tr>
<td>1</td>
<td>GPIO Port F is present.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
</tr>
<tr>
<td>4</td>
<td>P4</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>P3</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>P2</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 29: Micro Direct Memory Access Peripheral Present (PPDMA), offset 0x30C

The **PPDMA** register provides software information regarding the μDMA module.

**Important:** This register should be used to determine if the μDMA module is implemented on this microcontroller. However, to support legacy software, the **DC7** register is available. A read of the **DC7** register correctly identifies if the μDMA module is present.

Micro Direct Memory Access Peripheral Present (PPDMA)

Base 0x400F.E000
Offset 0x30C
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>μDMA Module Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

System Control
Register 30: Hibernation Peripheral Present (PPHIB), offset 0x314

The **PPHIB** register provides software information regarding the Hibernation module.

**Important:** This register should be used to determine if the Hibernation module is implemented on this microcontroller. However, to support legacy software, the **DC1** register is available. A read of the **DC1** register correctly identifies if the Hibernation module is present.

---

**Hibernation Peripheral Present (PPHIB)**

Base 0x400F.E000
Offset 0x314
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>Hibernation Module Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 31: Universal Asynchronous Receiver/Transmitter Peripheral Present (PPUART), offset 0x318

The **PPUART** register provides software information regarding the UART modules.

**Important:** This register should be used to determine which UART modules are implemented on this microcontroller. However, to support legacy software, the **DC2** register is available. A read of the **DC2** register correctly identifies if a legacy UART module is present. Software must use this register to determine if a module that is not supported by the **DC2** register is present.

### Universal Asynchronous Receiver/Transmitter Peripheral Present (PPUART)

- **Base:** 0x400F.E000
- **Offset:** 0x318
- **Type:** RO, reset 0x0000.00FF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>P7</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 7 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 7 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 7 is present.</td>
</tr>
<tr>
<td>6</td>
<td>P6</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 6 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 6 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 6 is present.</td>
</tr>
<tr>
<td>5</td>
<td>P5</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 5 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 5 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 5 is present.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>4</td>
<td>P4</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 4 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>P3</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 3 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>P2</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 32: Synchronous Serial Interface Peripheral Present (PPSSI), offset 0x31C

The PPSSI register provides software information regarding the SSI modules.

**Important:** This register should be used to determine which SSI modules are implemented on this microcontroller. However, to support legacy software, the DC2 register is available. A read of the DC2 register correctly identifies if a legacy SSI module is present. Software must use this register to determine if a module that is not supported by the DC2 register is present.

### Synchronous Serial Interface Peripheral Present (PPSSI)

Base 0x400F.E000  
Offset 0x31C  
Type RO, reset 0x0000.000F

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>P3</td>
<td>RO</td>
<td>0x1</td>
<td>SSI Module 3 Present</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 SSI module 3 is not present.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 SSI module 3 is present.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>P2</td>
<td>RO</td>
<td>0x1</td>
<td>SSI Module 2 Present</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 SSI module 2 is not present.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 SSI module 2 is present.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>RO</td>
<td>0x1</td>
<td>SSI Module 1 Present</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 SSI module 1 is not present.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 SSI module 1 is present.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>SSI Module 0 Present</td>
</tr>
</tbody>
</table>

Value Description
0  SSI module 0 is not present.
1  SSI module 0 is present.
Register 33: Inter-Integrated Circuit Peripheral Present (PPI2C), offset 0x320

The PPI2C register provides software information regarding the I²C modules.

**Important:** This register should be used to determine which I²C modules are implemented on this microcontroller. However, to support legacy software, the DC2 register is available. A read of the DC2 register correctly identifies if a legacy I²C module is present. Software must use this register to determine if a module that is not supported by the DC2 register is present.

Inter-Integrated Circuit Peripheral Present (PPI2C)
Base 0x400F.E000
Offset 0x320
Type RO, reset 0x0000.003F

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>P5</td>
<td>RO</td>
<td>0x1</td>
<td>I²C Module 5 Present</td>
</tr>
<tr>
<td>4</td>
<td>P4</td>
<td>RO</td>
<td>0x1</td>
<td>I²C Module 4 Present</td>
</tr>
<tr>
<td>3</td>
<td>P3</td>
<td>RO</td>
<td>0x1</td>
<td>I²C Module 3 Present</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>----------------------</td>
</tr>
<tr>
<td>2</td>
<td>P2</td>
<td>RO</td>
<td>0x1</td>
<td>I2C Module 2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>RO</td>
<td>0x1</td>
<td>I2C Module 1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>I2C Module 0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 34: Universal Serial Bus Peripheral Present (PPUSB), offset 0x328

The **PPUSB** register provides software information regarding the USB module.

**Important:** This register should be used to determine if the USB module is implemented on this microcontroller. However, to support legacy software, the **DC6** register is available. A read of the **DC6** register correctly identifies if the USB module is present.

### Universal Serial Bus Peripheral Present (PPUSB)

Base 0x400F.E000
Offset 0x328
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>USB Module Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 35: Controller Area Network Peripheral Present (PPCAN), offset 0x334

The **PPCAN** register provides software information regarding the CAN modules.

**Important:** This register should be used to determine which CAN modules are implemented on this microcontroller. However, to support legacy software, the **DC1** register is available. A read of the **DC1** register correctly identifies if a legacy CAN module is present.

### Controller Area Network Peripheral Present (PPCAN)

Base 0x400F.E000  
Offset 0x334  
Type RO, reset 0x0000.0003

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>RO</td>
<td>0x1</td>
<td>CAN Module 1 Present</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>CAN Module 0 Present</td>
</tr>
</tbody>
</table>
### Register 36: Analog-to-Digital Converter Peripheral Present (PPADC), offset 0x338

The **PPADC** register provides software information regarding the ADC modules.

**Important:** This register should be used to determine which ADC modules are implemented on this microcontroller. However, to support legacy software, the **DC1** register is available. A read of the **DC1** register correctly identifies if a legacy ADC module is present.

#### Analog-to-Digital Converter Peripheral Present (PPADC)

- **Base:** 0x400F.E000
- **Offset:** 0x338
- **Type:** RO, reset 0x0000.0003

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>ADC module 1 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>ADC module 1 is present.</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>ADC module 0 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>ADC module 0 is present.</td>
</tr>
</tbody>
</table>
Register 37: Analog Comparator Peripheral Present (PPACMP), offset 0x33C

The PPACMP register provides software information regarding the analog comparator module.

**Important:** This register should be used to determine if the analog comparator module is implemented on this microcontroller. However, to support legacy software, the DC2 register is available. A read of the DC2 register correctly identifies if the analog comparator module is present.

Note that the **Analog Comparator Peripheral Properties (ACMPPP)** register indicates how many analog comparator blocks are included in the module.

Analog Comparator Peripheral Present (PPACMP)

Base 0x400F.E000
Offset 0x33C
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>Analog Comparator Module Present</td>
</tr>
</tbody>
</table>

**Valid Description Values**

- 0: Analog comparator module is not present.
- 1: Analog comparator module is present.
Register 38: Pulse Width Modulator Peripheral Present (PPPWM), offset 0x340

The **PPPWM** register provides software information regarding the PWM modules.

**Important:** This register should be used to determine which PWM modules are implemented on this microcontroller. However, to support legacy software, the **DC1** register is available. A read of the **DC1** register correctly identifies if the legacy PWM module is present. Software must use this register to determine if a module that is not supported by the **DC1** register is present.

Pulse Width Modulator Peripheral Present (PPPWM)

Base 0x400F.E000
Offset 0x340
Type RO, reset 0x0000.0003

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM Module 1 Present</td>
<td>0x1</td>
<td>RO</td>
<td>0</td>
<td>31.2</td>
</tr>
<tr>
<td>PWM Module 0 Present</td>
<td>0x1</td>
<td>RO</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

Value Description

- **0** PWM module 1 is not present.
- **1** PWM module 1 is present.

Value Description

- **0** PWM module 0 is not present.
- **1** PWM module 0 is present.
### Register 39: Quadrature Encoder Interface Peripheral Present (PPQEI), offset 0x344

The **PPQEI** register provides software information regarding the QEI modules.

**Important:** This register should be used to determine which QEI modules are implemented on this microcontroller. However, to support legacy software, the **DC2** register is available. A read of the **DC2** register correctly identifies if a legacy QEI module is present.

**Quadrature Encoder Interface Peripheral Present (PPQEI)**

Base 0x400F.E000  
Offset 0x344  
Type RO, reset 0x0000.0003

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>RO</td>
<td>0x1</td>
<td>QEI Module 1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>QEI Module 0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
</tbody>
</table>
Register 40: EEPROM Peripheral Present (PPEEPROM), offset 0x358

The **PPEEPROM** register provides software information regarding the EEPROM module.

EEPROM Peripheral Present (PPEEPROM)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>P0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x00</td>
<td>1</td>
</tr>
</tbody>
</table>

**Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.**

EEPROM Module Present

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>EEPROM module is not present.</td>
</tr>
<tr>
<td>1</td>
<td>EEPROM module is present.</td>
</tr>
</tbody>
</table>
Register 41: 32/64-Bit Wide General-Purpose Timer Peripheral Present (PPWTIMER), offset 0x35C

The **PPWTIMER** register provides software information regarding the 32/64-bit wide general-purpose timer modules.

32/64-Bit Wide General-Purpose Timer Peripheral Present (PPWTIMER)
Base 0x400F.E000
Offset 0x35C
Type RO, reset 0x0000.003F

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>P5</td>
<td>RO</td>
<td>0x1</td>
<td>32/64-Bit Wide General-Purpose Timer 5 Present</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 5 is not present.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>32/64-bit wide general-purpose timer module 5 is present.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>P4</td>
<td>RO</td>
<td>0x1</td>
<td>32/64-Bit Wide General-Purpose Timer 4 Present</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 4 is not present.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>32/64-bit wide general-purpose timer module 4 is present.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>P3</td>
<td>RO</td>
<td>0x1</td>
<td>32/64-Bit Wide General-Purpose Timer 3 Present</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 3 is not present.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>32/64-bit wide general-purpose timer module 3 is present.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>P2</td>
<td>RO</td>
<td>0x1</td>
<td>32/64-Bit Wide General-Purpose Timer 2 Present</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 2 is not present.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>32/64-bit wide general-purpose timer module 2 is present.</td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
<td>RO</td>
<td>0x1</td>
<td>32/64-Bit General-Purpose Timer 1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit general-purpose timer module 1 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 32/64-bit general-purpose timer module 1 is present.</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
<td>RO</td>
<td>0x1</td>
<td>32/64-Bit General-Purpose Timer 0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit general-purpose timer module 0 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 32/64-bit general-purpose timer module 0 is present.</td>
</tr>
</tbody>
</table>
Register 42: Watchdog Timer Software Reset (SRWD), offset 0x500

The SRWD register provides software the capability to reset the available watchdog modules. This register provides the same capability as the legacy Software Reset Control n SRCRn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SRCRn bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRWD register. While the SRWD bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRWD bit.

There may be latency from the clearing of the SRWD bit to when the peripheral is ready for use. Software can check the corresponding PRWD bit to be sure.

**Important:** This register should be used to reset the watchdog modules. To support legacy software, the SRCR0 register is available. Setting a bit in the SRCR0 register also resets the corresponding module. Any bits that are changed by writing to the SRCR0 register can be read back correctly when reading the SRCR0 register. If software uses this register to reset a legacy peripheral (such as Watchdog 1), the write causes proper operation, but the value of that bit is not reflected in the SRCR0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Watchdog Timer Software Reset (SRWD)

Base 0x400F.E000
Offset 0x500
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Timer 1 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Watchdog module 1 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Watchdog module 1 is reset.</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Timer 0 Software Reset</td>
</tr>
</tbody>
</table>

- **Value** Description
  - 0  Watchdog module 0 is not reset.
  - 1  Watchdog module 0 is reset.
Register 43: 16/32-Bit General-Purpose Timer Software Reset (SRTIMER), offset 0x504

The SRTIMER register provides software the capability to reset the available 16/32-bit timer modules. This register provides the same capability as the legacy Software Reset Control n SRCRn registers specifically for the timer modules and has the same bit polarity as the corresponding SRCRn bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRTIMER register. While the SRTIMER bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRTIMER bit.

There may be latency from the clearing of the SRTIMER bit to when the peripheral is ready for use. Software can check the corresponding PRTIMER bit to be sure.

**Important:** This register should be used to reset the timer modules. To support legacy software, the SRCR1 register is available. Setting a bit in the SRCR1 register also resets the corresponding module. Any bits that are changed by writing to the SRCR1 register can be read back correctly when reading the SRCR1 register. Software must use this register to reset modules that are not present in the legacy registers. If software uses this register to reset a legacy peripheral (such as Timer 1), the write causes proper operation, but the value of that bit is not reflected in the SRCR1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 4 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 4 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  16/32-bit general-purpose timer module 4 is reset.</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 3 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 3 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  16/32-bit general-purpose timer module 3 is reset.</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 2 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 2 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  16/32-bit general-purpose timer module 2 is reset.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 1 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 1 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  16/32-bit general-purpose timer module 1 is reset.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 0 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 0 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  16/32-bit general-purpose timer module 0 is reset.</td>
</tr>
</tbody>
</table>
Register 44: General-Purpose Input/Output Software Reset (SRGPIO), offset 0x508

The SRGPIO register provides software the capability to reset the available GPIO modules. This register provides the same capability as the legacy Software Reset Control n SRCRn registers specifically for the GPIO modules and has the same bit polarity as the corresponding SRCRn bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRGPIO register. While the SRGPIO bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRGPIO bit.

There may be latency from the clearing of the SRGPIO bit to when the peripheral is ready for use. Software can check the corresponding PRGPIO bit to be sure.

Important: This register should be used to reset the GPIO modules. To support legacy software, the SRCR2 register is available. Setting a bit in the SRCR2 register also resets the corresponding module. Any bits that are changed by writing to the SRCR2 register can be read back correctly when reading the SRCR2 register. Software must use this register to reset modules that are not present in the legacy registers. If software uses this register to reset a legacy peripheral (such as GPIO A), the write causes proper operation, but the value of that bit is not reflected in the SRCR2 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

General-Purpose Input/Output Software Reset (SRGPIO)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>R9</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port K Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port K is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port K is reset.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>8</td>
<td>R8</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port J Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port J is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>GPIO Port J is reset.</td>
</tr>
<tr>
<td>7</td>
<td>R7</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port H Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port H is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>GPIO Port H is reset.</td>
</tr>
<tr>
<td>6</td>
<td>R6</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port G Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port G is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>GPIO Port G is reset.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port F Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port F is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>GPIO Port F is reset.</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port E Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port E is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>GPIO Port E is reset.</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port D Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port D is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>GPIO Port D is reset.</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port C Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port C is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>GPIO Port C is reset.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port B Software Reset</td>
</tr>
</tbody>
</table>

Value | Description
--- | ---
0 | GPIO Port B is not reset.
1 | GPIO Port B is reset.

| 0         | R0   | RW   | 0     | GPIO Port A Software Reset   |

Value | Description
--- | ---
0 | GPIO Port A is not reset.
1 | GPIO Port A is reset.
Register 45: Micro Direct Memory Access Software Reset (SRDMA), offset 0x50C

The **SRDMA** register provides software the capability to reset the available μDMA module. This register provides the same capability as the legacy **Software Reset Control n SRCRn** registers specifically for the μDMA module and has the same bit polarity as the corresponding **SRCRn** bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the **SRDMA** register. While the **SRDMA** bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the **SRDMA** bit.

There may be latency from the clearing of the **SRDMA** bit to when the peripheral is ready for use. Software can check the corresponding **PRDMA** bit to be sure.

**Important:** This register should be used to reset the μDMA module. To support legacy software, the **SRCR2** register is available. Setting the **UDMA** bit in the **SRCR2** register also resets the μDMA module. If the **UDMA** bit is set by writing to the **SRCR2** register, it can be read back correctly when reading the **SRCR2** register. If software uses this register to reset the μDMA module, the write causes proper operation, but the value of the **UDMA** bit is not reflected in the **SRCR2** register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.
Register 46: Hibernation Software Reset (SRHIB), offset 0x514

The SRHIB register provides software the capability to reset the available Hibernation module. This register provides the same capability as the legacy Software Reset Control n SRCRn registers specifically for the Hibernation module and has the same bit polarity as the corresponding SRCRn bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRHIB register. While the SRHIB bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRHIB bit.

There may be latency from the clearing of the SRHIB bit to when the peripheral is ready for use. Software can check the corresponding PRHIB bit to be sure.

**Important**: This register should be used to reset the Hibernation module. To support legacy software, the SRCR0 register is available. Setting the HIB bit in the SRCR0 register also resets the Hibernation module. If the HIB bit is set by writing to the SRCR0 register, it can be read back correctly when reading the SRCR0 register. If software uses this register to reset the Hibernation module, the write causes proper operation, but the value of the HIB bit is not reflected in the SRCR0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

### Hibernation Software Reset (SRHIB)

*Base 0x400F.E000 Offset 0x514 Type RW, reset 0x0000.0000*

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hibernation module is not reset.</td>
<td>0</td>
</tr>
<tr>
<td>Hibernation module is reset.</td>
<td>1</td>
</tr>
</tbody>
</table>

---

**Bit/Field** | **Name** | **Type** | **Reset** | **Description**
--- | --- | --- | --- | ---
31:1 | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

0 | R0 | RW | 0 | Hibernation Module Software Reset

---

**Value** | **Description**
--- | ---
0 | Hibernation module is not reset.
1 | Hibernation module is reset.
Register 47: Universal Asynchronous Receiver/Transmitter Software Reset (SRUART), offset 0x518

The **SRUART** register provides software the capability to reset the available UART modules. This register provides the same capability as the legacy **Software Reset Control** in **SRCRn** registers specifically for the UART modules and has the same bit polarity as the corresponding **SRCRn** bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the **SRUART** register. While the **SRUART** bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the **SRUART** bit.

There may be latency from the clearing of the **SRUART** bit to when the peripheral is ready for use. Software can check the corresponding **PRUART** bit to be sure.

**Important:** This register should be used to reset the UART modules. To support legacy software, the **SRCR1** register is available. Setting a bit in the **SRCR1** register also resets the corresponding module. Any bits that are changed by writing to the **SRCR1** register can be read back correctly when reading the **SRCR1** register. Software must use this register to reset modules that are not present in the legacy registers. If software uses this register to reset a legacy peripheral (such as UART0), the write causes proper operation, but the value of that bit is not reflected in the **SRCR1** register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Universal Asynchronous Receiver/Transmitter Software Reset (SRUART)

<table>
<thead>
<tr>
<th>Base 0x400F.E000</th>
<th>Offset 0x518</th>
<th>Type RW, reset 0x0000.0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>R7</td>
<td>RW</td>
<td>0</td>
<td>UART Module 7 Software Reset</td>
</tr>
</tbody>
</table>

**Value Description**

0: UART module 7 is not reset.

1: UART module 7 is reset.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>R6</td>
<td>RW</td>
<td>0</td>
<td>UART Module 6 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 6 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 6 is reset.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RW</td>
<td>0</td>
<td>UART Module 5 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 5 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 5 is reset.</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>UART Module 4 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 4 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 4 is reset.</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>UART Module 3 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 3 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 3 is reset.</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>UART Module 2 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 2 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 2 is reset.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>UART Module 1 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 1 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 1 is reset.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>UART Module 0 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 0 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UART module 0 is reset.</td>
</tr>
</tbody>
</table>
Register 48: Synchronous Serial Interface Software Reset (SRSSI), offset 0x51C

The SRSSI register provides software the capability to reset the available SSI modules. This register provides the same capability as the legacy Software Reset Control n SRCRn registers specifically for the SSI modules and has the same bit polarity as the corresponding SRCRn bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRSSI register. While the SRSSI bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRSSI bit.

There may be latency from the clearing of the SRSSI bit to when the peripheral is ready for use. Software can check the corresponding PRSSI bit to be sure.

Important: This register should be used to reset the SSI modules. To support legacy software, the SRCR1 register is available. Setting a bit in the SRCR1 register also resets the corresponding module. Any bits that are changed by writing to the SRCR1 register can be read back correctly when reading the SRCR1 register. Software must use this register to reset modules that are not present in the legacy registers. If software uses this register to reset a legacy peripheral (such as SSI0), the write causes proper operation, but the value of that bit is not reflected in the SRCR1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Synchronous Serial Interface Software Reset (SRSSI)
Base 0x400F.E000
Offset 0x51C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide consistency with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 3 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  SSI module 3 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  SSI module 3 is reset.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 2 Software Reset</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 1 Software Reset</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 0 Software Reset</td>
</tr>
</tbody>
</table>

**SSI Module 2 Software Reset**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SSI module 2 is not reset.</td>
</tr>
<tr>
<td>1</td>
<td>SSI module 2 is reset.</td>
</tr>
</tbody>
</table>

**SSI Module 1 Software Reset**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SSI module 1 is not reset.</td>
</tr>
<tr>
<td>1</td>
<td>SSI module 1 is reset.</td>
</tr>
</tbody>
</table>

**SSI Module 0 Software Reset**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SSI module 0 is not reset.</td>
</tr>
<tr>
<td>1</td>
<td>SSI module 0 is reset.</td>
</tr>
</tbody>
</table>
Register 49: Inter-Integrated Circuit Software Reset (SRI2C), offset 0x520

The SRI2C register provides software the capability to reset the available \( \text{I}^2\text{C} \) modules. This register provides the same capability as the legacy Software Reset Control n SRCRn registers specifically for the \( \text{I}^2\text{C} \) modules and has the same bit polarity as the corresponding SRCRn bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRI2C register. While the SRI2C bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRI2C bit.

There may be latency from the clearing of the SRI2C bit to when the peripheral is ready for use. Software can check the corresponding PRI2C bit to be sure.

**Important:** This register should be used to reset the \( \text{I}^2\text{C} \) modules. To support legacy software, the SRCR1 register is available. Setting a bit in the SRCR1 register also resets the corresponding module. Any bits that are changed by writing to the SRCR1 register can be read back correctly when reading the SRCR1 register. Software must use this register to reset modules that are not present in the legacy registers. If software uses this register to reset a legacy peripheral (such as I2C0), the write causes proper operation, but the value of that bit is not reflected in the SRCR1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Inter-Integrated Circuit Software Reset (SRI2C)

**Base** 0x400F.E000
**Offset** 0x520
**Type** RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RW</td>
<td>0</td>
<td>( \text{I}^2\text{C} ) Module 5 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 ( \text{I}^2\text{C} ) module 5 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 ( \text{I}^2\text{C} ) module 5 is reset.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>----------------------------</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 4 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 3 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 2 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 1 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 0 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 50: Universal Serial Bus Software Reset (SRUSB), offset 0x528

The **SRUSB** register provides software the capability to reset the available USB module. This register provides the same capability as the legacy **Software Reset Control n SRCRn** registers specifically for the USB module and has the same bit polarity as the corresponding **SRCRn** bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the **SRUSB** register. While the **SRUSB** bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the **SRUSB** bit.

There may be latency from the clearing of the **SRUSB** bit to when the peripheral is ready for use. Software can check the corresponding **PRUSB** bit to be sure.

**Important:** This register should be used to reset the USB module. To support legacy software, the **SRCR2** register is available. Setting the **USB0** bit in the **SRCR2** register also resets the USB module. If the **USB0** bit is set by writing to the **SRCR2** register, it can be read back correctly when reading the **SRCR2** register. If software uses this register to reset the USB module, the write causes proper operation, but the value of the **USB0** bit is not reflected in the **SRCR2** register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

Universal Serial Bus Software Reset (SRUSB)

Base 0x400F.E000
Offset 0x528
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>USB Module Software Reset</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>USB module is not reset.</td>
</tr>
<tr>
<td>1</td>
<td>USB module is reset.</td>
</tr>
</tbody>
</table>
Register 51: Controller Area Network Software Reset (SRCAN), offset 0x534

The **SRCAN** register provides software the capability to reset the available CAN modules. This register provides the same capability as the legacy **Software Reset Control n SRCRn** registers specifically for the CAN modules and has the same bit polarity as the corresponding **SRCRn** bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the **SRCAN** register. While the **SRCAN** bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the **SRCAN** bit.

There may be latency from the clearing of the **SRCAN** bit to when the peripheral is ready for use. Software can check the corresponding **PRCAN** bit to be sure.

**Important:** This register should be used to reset the CAN modules. To support legacy software, the **SRCR0** register is available. Setting a bit in the **SRCR0** register also resets the corresponding module. Any bits that are changed by writing to the **SRCR0** register can be read back correctly when reading the **SRCR0** register. If software uses this register to reset a legacy peripheral (such as CAN0), the write causes proper operation, but the value of that bit is not reflected in the **SRCR0** register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Controller Area Network Software Reset (SRCAN)

**Base 0x400F.E000**

**Offset 0x534**

**Type RW, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>CAN Module 1 Software Reset</td>
</tr>
</tbody>
</table>

**Value Description**

- 0  CAN module 1 is not reset.
- 1  CAN module 1 is reset.
### System Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>CAN Module 0 Software Reset</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>CAN module 0 is not reset.</td>
</tr>
<tr>
<td>1</td>
<td>CAN module 0 is reset.</td>
</tr>
</tbody>
</table>
Register 52: Analog-to-Digital Converter Software Reset (SRADC), offset 0x538

The SRADC register provides software the capability to reset the available ADC modules. This register provides the same capability as the legacy Software Reset Control in SRCRn registers specifically for the ADC modules and has the same bit polarity as the corresponding SRCRn bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRADC register. While the SRADC bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRADC bit.

There may be latency from the clearing of the SRADC bit to when the peripheral is ready for use. Software can check the corresponding PRADC bit to be sure.

**Important:** This register should be used to reset the ADC modules. To support legacy software, the SRCR0 register is available. Setting a bit in the SRCR0 register also resets the corresponding module. Any bits that are changed by writing to the SRCR0 register can be read back correctly when reading the SRCR0 register. If software uses this register to reset a legacy peripheral (such as ADC0), the write causes proper operation, but the value of that bit is not reflected in the SRCR0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

**Analog-to-Digital Converter Software Reset (SRADC)**
Base 0x400F.E000
Offset 0x538
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>ADC Module 1 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>ADC module 1 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>ADC module 1 is reset.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>ADC Module 0 Software Reset</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ADC module 0 is not reset.</td>
</tr>
<tr>
<td>1</td>
<td>ADC module 0 is reset.</td>
</tr>
</tbody>
</table>
Register 53: Analog Comparator Software Reset (SRACMP), offset 0x53C

The SRACMP register provides software the capability to reset the available analog comparator module. This register provides the same capability as the legacy Software Reset Control n SRCRn registers specifically for the analog comparator module and has the same bit polarity as the corresponding SRCRn bits.

A block is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRACMP register. While the SRACMP bit is 1, the module is held in reset.

2. Software completes the reset process by clearing the SRACMP bit.

There may be latency from the clearing of the SRACMP bit to when the module is ready for use. Software can check the corresponding PRACMP bit to be sure.

Important: This register should be used to reset the analog comparator module. To support legacy software, the SRCR1 register is available. Setting any of the COMPn bits in the SRCR0 register also resets the analog comparator module. If any of the COMPn bits are set by writing to the SRCR1 register, it can be read back correctly when reading the SRCR0 register. If software uses this register to reset the analog comparator module, the write causes proper operation, but the value of R0 is not reflected by the COMPn bits in the SRCR1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.
Register 54: Pulse Width Modulator Software Reset (SRPWM), offset 0x540

The SRPWM register provides software the capability to reset the available PWM modules. This register provides the same capability as the legacy Software Reset Control n SRCRn registers specifically for the PWM modules and has the same bit polarity as the corresponding SRCRn bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRPWM register. While the SRPWM bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRPWM bit.

There may be latency from the clearing of the SRPWM bit to when the peripheral is ready for use. Software can check the corresponding PRPWM bit to be sure.

**Important:** This register should be used to reset the PWM modules. To support legacy software, the SRCR0 register is available. Setting the PWM bit in the SRCR0 register also resets the PWM0 module. If the PWM bit is changed by writing to the SRCR0 register, it can be read back correctly when reading the SRCR0 register. Software must use this register to reset PWM1, which is not present in the legacy registers. If software uses this register to reset PWM0, the write causes proper operation, but the value of that bit is not reflected in the SRCR0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Pulse Width Modulator Software Reset (SRPWM)

Base 0x400F.E000
Offset 0x540
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>PWM Module 1 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0        PWM module 1 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1        PWM module 1 is reset.</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>PWM Module 0 Software Reset</td>
</tr>
</tbody>
</table>

Value  Description
0       PWM module 0 is not reset.
1       PWM module 0 is reset.
The **SRQEI** register provides software the capability to reset the available QEI modules. This register provides the same capability as the legacy **Software Reset Control n SRCRn** registers specifically for the QEI modules and has the same bit polarity as the corresponding **SRCRn** bits.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the **SRQEI** register. While the **SRQEI** bit is 1, the peripheral is held in reset.
2. Software completes the reset process by clearing the **SRQEI** bit.

There may be latency from the clearing of the **SRQEI** bit to when the peripheral is ready for use. Software can check the corresponding **PRQEI** bit to be sure.

**Important:** This register should be used to reset the QEI modules. To support legacy software, the **SRCR1** register is available. Setting a bit in the **SRCR1** register also resets the corresponding module. Any bits that are changed by writing to the **SRCR1** register can be read back correctly when reading the **SRCR1** register. If software uses this register to reset a legacy peripheral (such as QEI0), the write causes proper operation, but the value of that bit is not reflected in the **SRCR1** register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Quadrature Encoder Interface Software Reset (SRQEI)

| Base 0x400F.E000 | Offset 0x544 |
| Type RW, reset 0x0000.0000 |

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Type**

- **RO**: Read-Only
- **RW**: Read-Write

**Reset**

- **0**: Default value
- **1**: Set by software

**Bit/Field** | **Name** | **Type** | **Reset** | **Description** |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>QEI Module 1 Software Reset</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: QEI module 1 is not reset.
- **1**: QEI module 1 is reset.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>QEI Module 0 Software Reset</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>QEI module 0 is not reset.</td>
</tr>
<tr>
<td>1</td>
<td>QEI module 0 is reset.</td>
</tr>
</tbody>
</table>
Register 56: EEPROM Software Reset (SREEPROM), offset 0x558

The SREEPROM register provides software the capability to reset the available EEPROM module.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SREEPROM register. While the SREEPROM bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SREEPROM bit.

There may be latency from the clearing of the SREEPROM bit to when the peripheral is ready for use. Software can check the corresponding PREEPROM bit to be sure.

EEPROM Software Reset (SREEPROM)

<table>
<thead>
<tr>
<th>Base 0x400F.E000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset 0x558</td>
</tr>
<tr>
<td>Type RW, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>EEPROM Module Software Reset</td>
</tr>
</tbody>
</table>

Value Description

0  EEPROM module is not reset.
1  EEPROM module is reset.
Register 57: 32/64-Bit Wide General-Purpose Timer Software Reset (SRWTIMER), offset 0x55C

The SRWTIMER register provides software the capability to reset the available 32/64-bit wide timer modules.

A peripheral is reset by software using a simple two-step process:

1. Software sets a bit (or bits) in the SRWTIMER register. While the SRWTIMER bit is 1, the peripheral is held in reset.

2. Software completes the reset process by clearing the SRWTIMER bit.

There may be latency from the clearing of the SRWTIMER bit to when the peripheral is ready for use. Software can check the corresponding PRWTIMER bit to be sure.

32/64-Bit Wide General-Purpose Timer Software Reset (SRWTIMER)

Base 0x400F.E000
Offset 0x55C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 5 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 4 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 3 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 2 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 2 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>32/64-bit wide general-purpose timer module 2 is reset.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 1 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 1 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>32/64-bit wide general-purpose timer module 1 is reset.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 0 Software Reset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 0 is not reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>32/64-bit wide general-purpose timer module 0 is reset.</td>
</tr>
</tbody>
</table>
Register 58: Watchdog Timer Run Mode Clock Gating Control (RCGCWD), offset 0x600

The RCGCWD register provides software the capability to enable and disable watchdog modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

Important: This register should be used to control the clocking for the watchdog modules. To support legacy software, the RCGC0 register is available. A write to the RCGC0 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC0 register can be read back correctly with a read of the RCGC0 register. If software uses this register to write a legacy peripheral (such as Watchdog 0), the write causes proper operation, but the value of that bit is not reflected in the RCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Timer 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>Watchdog module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Enable and provide a clock to Watchdog module 1 in Run mode.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Timer 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>Watchdog module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Enable and provide a clock to Watchdog module 0 in Run mode.</td>
</tr>
</tbody>
</table>
**Register 59: 16/32-Bit General-Purpose Timer Run Mode Clock Gating Control (RCGCTIMER), offset 0x604**

The RCGCTIMER register provides software the capability to enable and disable 16/32-bit timer modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the timer modules and has the same bit polarity as the corresponding RCGCn bits.

**Important:** This register should be used to control the clocking for the timer modules. To support legacy software, the RCGC1 register is available. A write to the RCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC1 register can be read back correctly with a read of the RCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as Timer 0), the write causes proper operation, but the value of that bit is not reflected in the RCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 4 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 4 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 4 in Run mode.</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 3 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 3 in Run mode.</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 2 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 2 in Run mode.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 1 in Run mode.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 0 in Run mode.</td>
</tr>
</tbody>
</table>
Register 60: General-Purpose Input/Output Run Mode Clock Gating Control (RCGCGPIO), offset 0x608

The RCGCGPIO register provides software the capability to enable and disable GPIO modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

**Important:** This register should be used to control the clocking for the GPIO modules. To support legacy software, the RCGC2 register is available. A write to the RCGC2 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC2 register can be read back correctly with a read of the RCGC2 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as GPIO A), the write causes proper operation, but the value of that bit is not reflected in the RCGC2 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

General-Purpose Input/Output Run Mode Clock Gating Control (RCGCGPIO)

Base 0x400F.E000
Offset 0x608
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>R9</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port K Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port K is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to GPIO Port K in Run mode.</td>
</tr>
<tr>
<td>8</td>
<td>R8</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port J Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>GPIO Port J is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to GPIO Port J in Run mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------------------------</td>
</tr>
<tr>
<td>7</td>
<td>R7</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port H Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>R6</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port G Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port F Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port E Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port D Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port C Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port B Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
### System Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port A Run Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value | Description
--- | ---
0    | GPIO Port A is disabled.
1    | Enable and provide a clock to GPIO Port A in Run mode.
Register 61: Micro Direct Memory Access Run Mode Clock Gating Control (RCGCDMA), offset 0x60C

The **RCGCDMA** register provides software the capability to enable and disable the μDMA module in Run mode. When enabled, the module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

**Important:** This register should be used to control the clocking for the μDMA module. To support legacy software, the RCGC2 register is available. A write to the UDMA bit in the RCGC2 register also writes the R0 bit in this register. If the UDMA bit is changed by writing to the RCGC2 register, it can be read back correctly with a read of the RCGC2 register. If software uses this register to control the clock for the μDMA module, the write causes proper operation, but the UDMA bit in the RCGC2 register does not reflect the value of the R0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

### Micro Direct Memory Access Run Mode Clock Gating Control (RCGCDMA)

<table>
<thead>
<tr>
<th>Base 0x400F.E000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset 0x60C</td>
</tr>
<tr>
<td>Type RW, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>μDMA Module Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0  μDMA module is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to the μDMA module in Run mode.</td>
</tr>
</tbody>
</table>
Register 62: Hibernation Run Mode Clock Gating Control (RCGCHIB), offset 0x614

The RCGCHIB register provides software the capability to enable and disable the Hibernation module in Run mode. When enabled, the module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

Important: This register should be used to control the clocking for the Hibernation module. To support legacy software, the RCGC0 register is available. A write to the HIB bit in the RCGC0 register also writes the R0 bit in this register. If the HIB bit is changed by writing to the RCGC0 register, it can be read back correctly with a read of the RCGC0 register. If software uses this register to control the clock for the Hibernation module, the write causes proper operation, but the HIB bit in the RCGC0 register does not reflect the value of the R0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>1</td>
<td>Hibernation Module Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Hibernation module is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to the Hibernation module in Run mode.</td>
</tr>
</tbody>
</table>
Register 63: Universal Asynchronous Receiver/Transmitter Run Mode Clock Gating Control (RCGCUART), offset 0x618

The RCGCUART register provides software the capability to enable and disable the UART modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

**Important:** This register should be used to control the clocking for the UART modules. To support legacy software, the RCGC1 register is available. A write to the RCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC1 register can be read back correctly with a read of the RCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as UART0), the write causes proper operation, but the value of that bit is not reflected in the RCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Universal Asynchronous Receiver/Transmitter Run Mode Clock Gating Control (RCGCUART)

Base 0x400F.E000  
Offset 0x618  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>R7</td>
<td>RW</td>
<td>0</td>
<td>UART Module 7 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td>6</td>
<td>R6</td>
<td>RW</td>
<td>0</td>
<td>UART Module 6 Run Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

### UART Module 7 Run Mode Clock Gating Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>R7</td>
<td>RW</td>
<td>0</td>
<td>UART Module 7 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>UART module 7 is disabled.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to UART module 7 in Run mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### UART Module 6 Run Mode Clock Gating Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>R6</td>
<td>RW</td>
<td>0</td>
<td>UART Module 6 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>UART module 6 is disabled.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to UART module 6 in Run mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RW</td>
<td>0</td>
<td>UART Module 5 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   UART module 5 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Enable and provide a clock to UART module 5 in Run mode.</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>UART Module 4 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   UART module 4 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Enable and provide a clock to UART module 4 in Run mode.</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>UART Module 3 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   UART module 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Enable and provide a clock to UART module 3 in Run mode.</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>UART Module 2 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   UART module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Enable and provide a clock to UART module 2 in Run mode.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>UART Module 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   UART module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Enable and provide a clock to UART module 1 in Run mode.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>UART Module 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   UART module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Enable and provide a clock to UART module 0 in Run mode.</td>
</tr>
</tbody>
</table>
Register 64: Synchronous Serial Interface Run Mode Clock Gating Control (RCGCSSI), offset 0x61C

The RCGCSSI register provides software the capability to enable and disable the SSI modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

Important: This register should be used to control the clocking for the SSI modules. To support legacy software, the RCGC1 register is available. A write to the RCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC1 register can be read back correctly with a read of the RCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as SSI0), the write causes proper operation, but the value of that bit is not reflected in the RCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Synchronous Serial Interface Run Mode Clock Gating Control (RCGCSSI)
Base 0x400F.E000
Offset 0x61C
Type RW, reset 0x0000.0000
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  SSI module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to SSI module 1 in Run mode.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  SSI module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to SSI module 0 in Run mode.</td>
</tr>
</tbody>
</table>
Register 65: Inter-Integrated Circuit Run Mode Clock Gating Control (RCGCI2C), offset 0x620

The RCGCI2C register provides software the capability to enable and disable the I²C modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

**Important:** This register should be used to control the clocking for the I²C modules. To support legacy software, the RCGC1 register is available. A write to the RCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC1 register can be read back correctly with a read of the RCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as I2C0), the write causes proper operation, but the value of that bit is not reflected in the RCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

### Inter-Integrated Circuit Run Mode Clock Gating Control (RCGCI2C)

**Base 0x400F.E000**  
**Offset 0x620**  
**Type RW, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 5 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   I²C module 5 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Enable and provide a clock to I²C module 5 in Run mode.</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 4 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   I²C module 4 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   Enable and provide a clock to I²C module 4 in Run mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 3 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 2 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 66: Universal Serial Bus Run Mode Clock Gating Control (RCGCUSB), offset 0x628

The RCGCUSB register provides software the capability to enable and disable the USB module in Run mode. When enabled, the module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

Important: This register should be used to control the clocking for the USB module. To support legacy software, the RCGC2 register is available. A write to the USB0 bit in the RCGC2 register also writes the R0 bit in this register. If the USB0 bit is changed by writing to the RCGC2 register, it can be read back correctly with a read of the RCGC2 register. If software uses this register to control the clock for the USB module, the write causes proper operation, but the USB0 bit in the RCGC2 register does not reflect the value of the R0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Universal Serial Bus Run Mode Clock Gating Control (RCGCUSB)
Base 0x400F.E000
Offset 0x628
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>USB Module Run Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value Description
0  USB module is disabled.
1  Enable and provide a clock to the USB module in Run mode.
Register 67: Controller Area Network Run Mode Clock Gating Control (RCGCCAN), offset 0x634

The RCGCCAN register provides software the capability to enable and disable the CAN modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

**Important:** This register should be used to control the clocking for the CAN modules. To support legacy software, the RCGC0 register is available. A write to the RCGC0 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC0 register can be read back correctly with a read of the RCGC0 register. If software uses this register to write a legacy peripheral (such as CAN0), the write causes proper operation, but the value of that bit is not reflected in the RCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

### Controller Area Network Run Mode Clock Gating Control (RCGCCAN)

Base 0x400F.E000
Offset 0x634
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>CAN Module 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value: Description</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Enable and provide a clock to CAN module 1 in Run mode.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>CAN Module 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value: Description</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Enable and provide a clock to CAN module 0 in Run mode.</td>
</tr>
</tbody>
</table>
Register 68: Analog-to-Digital Converter Run Mode Clock Gating Control (RCGCADC), offset 0x638

The RCGCADC register provides software the capability to enable and disable the ADC modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

Important: This register should be used to control the clocking for the ADC modules. To support legacy software, the RCGC0 register is available. A write to the RCGC0 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC0 register can be read back correctly with a read of the RCGC0 register. If software uses this register to write a legacy peripheral (such as ADC0), the write causes proper operation, but the value of that bit is not reflected in the RCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Analog-to-Digital Converter Run Mode Clock Gating Control (RCGCADC)
Base 0x400F.E000
Offset 0x638
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>ADC Module 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>ADC Module 0 Run Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
Register 69: Analog Comparator Run Mode Clock Gating Control (RCGCACMP), offset 0x63C

The RCGCACMP register provides software the capability to enable and disable the analog comparator module in Run mode. When enabled, the module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

**Important:** This register should be used to control the clocking for the analog comparator module. To support legacy software, the RCGC1 register is available. Setting any of the COMPn bits in the RCGC1 register also sets the R0 bit in this register. If any of the COMPn bits are set by writing to the RCGC1 register, it can be read back correctly when reading the RCGC1 register. If software uses this register to change the clocking for the analog comparator module, the write causes proper operation, but the value R0 is not reflected by the COMPn bits in the RCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Analog Comparator Run Mode Clock Gating Control (RCGCACMP)
Base 0x400F.E000
Offset 0x63C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>Analog Comparator Module 0 Run Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value Description
0  Analog comparator module is disabled.
1  Enable and provide a clock to the analog comparator module in Run mode.
The **RCGCPWM** register provides software the capability to enable and disable the PWM modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register \( n \) \( \text{RCGCn} \) registers specifically for the watchdog modules and has the same bit polarity as the corresponding \( \text{RCGCn} \) bits.

**Important:** This register should be used to control the clocking for the PWM modules. To support legacy software, the \( \text{RCGC0} \) register is available. A write to the PWM bit in the \( \text{RCGC0} \) register also writes the \( R0 \) bit in this register. If the PWM bit is changed by writing to the \( \text{RCGC0} \) register, it can be read back correctly with a read of the \( \text{RCGC0} \) register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write to \( R0 \), the write causes proper operation, but the value of that bit is not reflected in the PWM bit in the \( \text{RCGC0} \) register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Pulse Width Modulator Run Mode Clock Gating Control (RCGCPWM)

**Base** 0x400F.E000  
**Offset** 0x640  
**Type RW, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>PWM Module 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>PWM module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to PWM module 1 in Run mode.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>PWM Module 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>PWM module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to PWM module 0 in Run mode.</td>
</tr>
</tbody>
</table>
Register 71: Quadrature Encoder Interface Run Mode Clock Gating Control (RCGCQEI), offset 0x644

The RCGCQEI register provides software the capability to enable and disable the QEI modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding RCGCn bits.

**Important:** This register should be used to control the clocking for the QEI modules. To support legacy software, the RCGC1 register is available. A write to the RCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the RCGC1 register can be read back correctly with a read of the RCGC1 register. If software uses this register to write a legacy peripheral (such as QEI0), the write causes proper operation, but the value of that bit is not reflected in the RCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Quadrature Encoder Interface Run Mode Clock Gating Control (RCGCQEI)

Base 0x400F.E000
Offset 0x644
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>QEI Module 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>QEI module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to QEI module 1 in Run mode.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>QEI Module 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>QEI module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to QEI module 0 in Run mode.</td>
</tr>
</tbody>
</table>
Register 72: EEPROM Run Mode Clock Gating Control (RCGCEEPROM), offset 0x658

The RCGCEEPROM register provides software the capability to enable and disable the EEPROM module in Run mode. When enabled, the module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault.

**EEPROM Run Mode Clock Gating Control (RCGCEEPROM)**

Base 0x400F.E000
Offset 0x658
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>EEPROM Module Run Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value Description

0    EEPROM module is disabled.
1    Enable and provide a clock to the EEPROM module in Run mode.
Register 73: 32/64-Bit Wide General-Purpose Timer Run Mode Clock Gating Control (RCGCWTIMER), offset 0x65C

The RCGCWTIMER register provides software the capability to enable and disable 3264-bit timer modules in Run mode. When enabled, a module is provided a clock and accesses to module registers are allowed. When disabled, the clock is disabled to save power and accesses to module registers generate a bus fault. This register provides the same capability as the legacy Run Mode Clock Gating Control Register n RCGCn registers specifically for the timer modules and has the same bit polarity as the corresponding RCGCn bits.

32/64-Bit Wide General-Purpose Timer Run Mode Clock Gating Control (RCGCWTIMER)
Base 0x400F.E000
Offset 0x65C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 5 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 4 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 3 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 2 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide general-purpose timer module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 32/64-bit wide general-purpose timer module 2 in Run mode.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 1 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide general-purpose timer module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 32/64-bit wide general-purpose timer module 1 in Run mode.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 0 Run Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide general-purpose timer module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 32/64-bit wide general-purpose timer module 0 in Run mode.</td>
</tr>
</tbody>
</table>
Register 74: Watchdog Timer Sleep Mode Clock Gating Control (SCGCWD), offset 0x700

The SCGCWD register provides software the capability to enable and disable watchdog modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

Important: This register should be used to control the clocking for the watchdog modules. To support legacy software, the SCGC0 register is available. A write to the SCGC0 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC0 register can be read back correctly with a read of the SCGC0 register. If software uses this register to write a legacy peripheral (such as Watchdog 0), the write causes proper operation, but the value of that bit is not reflected in the SCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Watchdog Timer Sleep Mode Clock Gating Control (SCGCWD)
Base 0x400F.E000
Offset 0x700
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Timer 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 Watchdog module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to Watchdog module 1 in sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Timer 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 Watchdog module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to Watchdog module 0 in sleep mode.</td>
</tr>
</tbody>
</table>
Register 75: 16/32-Bit General-Purpose Timer Sleep Mode Clock Gating Control (SCGCTIMER), offset 0x704

The SCGCTIMER register provides software the capability to enable and disable 16/32-bit timer modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Registers n SCGCn registers specifically for the timer modules and has the same bit polarity as the corresponding SCGCn bits.

**Important:** This register should be used to control the clocking for the timer modules. To support legacy software, the SCGC1 register is available. A write to the SCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC1 register can be read back correctly with a read of the SCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as Timer 0), the write causes proper operation, but the value of that bit is not reflected in the SCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### 16/32-Bit General-Purpose Timer Sleep Mode Clock Gating Control (SCGCTIMER)

<table>
<thead>
<tr>
<th>Base 0x400F.E000</th>
<th>Offset 0x704</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RW, reset 0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>S5</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 5 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td>4</td>
<td>S4</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 4 Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

**Value Description**

- 0: 16/32-bit general-purpose timer module 5 is disabled.
- 1: Enable and provide a clock to 16/32-bit general-purpose timer module 5 in sleep mode.

- 0: 16/32-bit general-purpose timer module 4 is disabled.
- 1: Enable and provide a clock to 16/32-bit general-purpose timer module 4 in sleep mode.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>S3</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 3 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>S2</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 2 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 76: General-Purpose Input/Output Sleep Mode Clock Gating Control (SCGCGPIO), offset 0x708

The SCGCGPIO register provides software the capability to enable and disable GPIO modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

**Important:** This register should be used to control the clocking for the GPIO modules. To support legacy software, the SCGC2 register is available. A write to the SCGC2 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC2 register can be read back correctly with a read of the SCGC2 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as GPIO A), the write causes proper operation, but the value of that bit is not reflected in the SCGC2 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>S9</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port K Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>GPIO Port K is disabled.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Enable and provide a clock to GPIO Port K in sleep mode.</td>
</tr>
<tr>
<td>8</td>
<td>S8</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port J Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>GPIO Port J is disabled.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>Enable and provide a clock to GPIO Port J in sleep mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>7</td>
<td>S7</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port H Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port H is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to GPIO Port H in sleep mode.</td>
</tr>
<tr>
<td>6</td>
<td>S6</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port G Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port G is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to GPIO Port G in sleep mode.</td>
</tr>
<tr>
<td>5</td>
<td>S5</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port F Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port F is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to GPIO Port F in sleep mode.</td>
</tr>
<tr>
<td>4</td>
<td>S4</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port E Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port E is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to GPIO Port E in sleep mode.</td>
</tr>
<tr>
<td>3</td>
<td>S3</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port D Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port D is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to GPIO Port D in sleep mode.</td>
</tr>
<tr>
<td>2</td>
<td>S2</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port C Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port C is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to GPIO Port C in sleep mode.</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port B Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port B is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to GPIO Port B in sleep mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port A Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port A is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to GPIO Port A in sleep mode.</td>
</tr>
</tbody>
</table>
Register 77: Micro Direct Memory Access Sleep Mode Clock Gating Control (SCGCDMA), offset 0x70C

The SCGCDMA register provides software the capability to enable and disable the μDMA module in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

**Important:** This register should be used to control the clocking for the μDMA module. To support legacy software, the SCGC2 register is available. A write to the UDMA bit in the SCGC2 register also writes the S0 bit in this register. If the UDMA bit is changed by writing to the SCGC2 register, it can be read back correctly with a read of the SCGC2 register. If software uses this register to control the clock for the μDMA module, the write causes proper operation, but the UDMA bit in the SCGC2 register does not reflect the value of the S0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

### Micro Direct Memory Access Sleep Mode Clock Gating Control (SCGCDMA)

| Base 0x400F.E000 | Offset 0x70C | Type RW, reset 0x0000.0000 |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>μDMA Module Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value Description

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>μDMA module is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to the μDMA module in sleep mode.</td>
</tr>
</tbody>
</table>
Register 78: Hibernation Sleep Mode Clock Gating Control (SCGCHIB), offset 0x714

The SCGCHIB register provides software the capability to enable and disable the Hibernation module in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

Important: This register should be used to control the clocking for the Hibernation module. To support legacy software, the SCGC0 register is available. A write to the HIB bit in the SCGC0 register also writes the S0 bit in this register. If the HIB bit is changed by writing to the SCGC0 register, it can be read back correctly with a read of the SCGC0 register. If software uses this register to control the clock for the Hibernation module, the write causes proper operation, but the HIB bit in the SCGC0 register does not reflect the value of the S0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Hibernation Sleep Mode Clock Gating Control (SCGCHIB)

```
Base 0x400F.E000
Offset 0x714
Type RW, reset 0x0000.0001
```

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>1</td>
<td>Hibernation Module Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 79: Universal Asynchronous Receiver/Transmitter Sleep Mode Clock Gating Control (SCGCUART), offset 0x718

The SCGCUART register provides software the capability to enable and disable the UART modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

Important: This register should be used to control the clocking for the UART modules. To support legacy software, the SCGC1 register is available. A write to the SCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC1 register can be read back correctly with a read of the SCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as UART0), the write causes proper operation, but the value of that bit is not reflected in the SCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Universal Asynchronous Receiver/Transmitter Sleep Mode Clock Gating Control (SCGCUART)

Base 0x400F.E000
Offset 0x718
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>S7</td>
<td>RW</td>
<td>0</td>
<td>UART Module 7 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 7 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to UART module 7 in sleep mode.</td>
</tr>
<tr>
<td>6</td>
<td>S6</td>
<td>RW</td>
<td>0</td>
<td>UART Module 6 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 6 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to UART module 6 in sleep mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>5</td>
<td>S5</td>
<td>RW</td>
<td>0</td>
<td>UART Module 5 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 5 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to UART module 5 in sleep mode.</td>
</tr>
<tr>
<td>4</td>
<td>S4</td>
<td>RW</td>
<td>0</td>
<td>UART Module 4 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 4 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to UART module 4 in sleep mode.</td>
</tr>
<tr>
<td>3</td>
<td>S3</td>
<td>RW</td>
<td>0</td>
<td>UART Module 3 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to UART module 3 in sleep mode.</td>
</tr>
<tr>
<td>2</td>
<td>S2</td>
<td>RW</td>
<td>0</td>
<td>UART Module 2 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to UART module 2 in sleep mode.</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>UART Module 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to UART module 1 in sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>UART Module 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>UART module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to UART module 0 in sleep mode.</td>
</tr>
</tbody>
</table>
Register 80: Synchronous Serial Interface Sleep Mode Clock Gating Control (SCGCSSI), offset 0x71C

The SCGCSSI register provides software the capability to enable and disable the SSI modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

**Important:** This register should be used to control the clocking for the SSI modules. To support legacy software, the SCGC1 register is available. A write to the SCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC1 register can be read back correctly with a read of the SCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as SSI0), the write causes proper operation, but the value of that bit is not reflected in the SCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Register Description

**Type:** RW, reset 0x0000.0000
**Base:** 0x400F.E000
**Offset:** 0x71C

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name Description</th>
<th>Value Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>S3</td>
<td>SSI Module 3 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 SSI module 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Enable and provide a clock to SSI module 3 in sleep mode.</td>
</tr>
<tr>
<td>2</td>
<td>S2</td>
<td>SSI Module 2 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 SSI module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Enable and provide a clock to SSI module 2 in sleep mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 81: Inter-Integrated Circuit Sleep Mode Clock Gating Control (SCGCI2C), offset 0x720

The SCGCI2C register provides software the capability to enable and disable the I²C modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

Important: This register should be used to control the clocking for the I²C modules. To support legacy software, the SCGC1 register is available. A write to the SCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC1 register can be read back correctly with a read of the SCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as I²C0), the write causes proper operation, but the value of that bit is not reflected in the SCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Inter-Integrated Circuit Sleep Mode Clock Gating Control (SCGCI2C)
Base 0x400F.E000
Offset 0x720
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>S5</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 5 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>I²C module 5 is disabled.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to I²C module 5 in sleep mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>S4</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 4 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>I²C module 4 is disabled.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to I²C module 4 in sleep mode.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>3</td>
<td>S3</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 3 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  I²C module 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to I²C module 3 in sleep mode.</td>
</tr>
<tr>
<td>2</td>
<td>S2</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 2 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  I²C module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to I²C module 2 in sleep mode.</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  I²C module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to I²C module 1 in sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  I²C module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to I²C module 0 in sleep mode.</td>
</tr>
</tbody>
</table>
Register 82: Universal Serial Bus Sleep Mode Clock Gating Control (SCGCUSB), offset 0x728

The SCGCUSB register provides software the capability to enable and disable the USB module in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

**Important:** This register should be used to control the clocking for the USB module. To support legacy software, the SCGC2 register is available. A write to the USB0 bit in the SCGC2 register also writes the S0 bit in this register. If the USB0 bit is changed by writing to the SCGC2 register, it can be read back correctly with a read of the SCGC2 register. If software uses this register to control the clock for the USB module, the write causes proper operation, but the USB0 bit in the SCGC2 register does not reflect the value of the S0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Universal Serial Bus Sleep Mode Clock Gating Control (SCGCUSB)

**Base 0x400F.E000**
**Offset 0x728**
**Type RW, reset 0x0000.0000**

#### Bit/Field

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>USB Module Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

**Value**

- 0  
  USB module is disabled.
- 1  
  Enable and provide a clock to the USB module in sleep mode.
Register 83: Controller Area Network Sleep Mode Clock Gating Control (SCGCCAN), offset 0x734

The SCGCCAN register provides software the capability to enable and disable the CAN modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

Important: This register should be used to control the clocking for the CAN modules. To support legacy software, the SCGC0 register is available. A write to the SCGC0 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC0 register can be read back correctly with a read of the SCGC0 register. If software uses this register to write a legacy peripheral (such as CAN0), the write causes proper operation, but the value of that bit is not reflected in the SCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Controller Area Network Sleep Mode Clock Gating Control (SCGCCAN)
Base 0x400F.E000
Offset 0x734
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>CAN Module 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 CAN module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to CAN module 1 in sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>CAN Module 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 CAN module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to CAN module 0 in sleep mode.</td>
</tr>
</tbody>
</table>
Register 84: Analog-to-Digital Converter Sleep Mode Clock Gating Control
(SCGCADC), offset 0x738

The SCGCADC register provides software the capability to enable and disable the ADC modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

**Important:** This register should be used to control the clocking for the ADC modules. To support legacy software, the SCGC0 register is available. A write to the SCGC0 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC0 register can be read back correctly with a read of the SCGC0 register. If software uses this register to write a legacy peripheral (such as ADC0), the write causes proper operation, but the value of that bit is not reflected in the SCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Analog-to-Digital Converter Sleep Mode Clock Gating Control (SCGCADC)

Base 0x400F.E000
Offset 0x738
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>ADC Module 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>ADC module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to ADC module 1 in sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>ADC Module 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>ADC module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to ADC module 0 in sleep mode.</td>
</tr>
</tbody>
</table>
Register 85: Analog Comparator Sleep Mode Clock Gating Control (SCGCACMP), offset 0x73C

The SCGCACMP register provides software the capability to enable and disable the analog comparator module in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

Important: This register should be used to control the clocking for the analog comparator module. To support legacy software, the SCGC1 register is available. Setting any of the COMPn bits in the SCGC1 register also sets the S0 bit in this register. If any of the COMPn bits are set by writing to the SCGC1 register, it can be read back correctly when reading the SCGC1 register. If software uses this register to change the clocking for the analog comparator module, the write causes proper operation, but the value S0 is not reflected by the COMPn bits in the SCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Analog Comparator Sleep Mode Clock Gating Control (SCGCACMP)
Base 0x400F.E000
Offset 0x73C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>31:1</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>Analog Comparator Module 0 Sleep Mode Clock Gating Control Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Analog comparator module is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Enable and provide a clock to the analog comparator module in sleep mode.</td>
</tr>
</tbody>
</table>
Register 86: Pulse Width Modulator Sleep Mode Clock Gating Control (SCGCPWM), offset 0x740

The SCGCPWM register provides software the capability to enable and disable the PWM modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register n SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

**Important:** This register should be used to control the clocking for the PWM modules. To support legacy software, the SCGC0 register is available. A write to the PWM bit in the SCGC0 register also writes the S0 bit in this register. If the PWM bit is changed by writing to the SCG0 register, it can be read back correctly with a read of the SCGC0 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write to S0, the write causes proper operation, but the value of that bit is not reflected in the PWM bit in the SCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>PWM Module 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>PWM module 1 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enable and provide a clock to PWM module 1 in sleep mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>PWM Module 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>PWM module 0 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enable and provide a clock to PWM module 0 in sleep mode.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 87: Quadrature Encoder Interface Sleep Mode Clock Gating Control (SCGCQEI), offset 0x744

The SCGCQEI register provides software the capability to enable and disable the QEI modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Register for SCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding SCGCn bits.

**Important:** This register should be used to control the clocking for the QEI modules. To support legacy software, the SCGC1 register is available. A write to the SCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the SCGC1 register can be read back correctly with a read of the SCGC1 register. If software uses this register to write a legacy peripheral (such as QEI0), the write causes proper operation, but the value of that bit is not reflected in the SCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Quadrature Encoder Interface Sleep Mode Clock Gating Control (SCGCQEI)
Base 0x400F.E000
Offset 0x744
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>QEI Module 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>QEI module 1 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enable and provide a clock to QEI module 1 in sleep mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>QEI Module 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>QEI module 0 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enable and provide a clock to QEI module 0 in sleep mode.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 88: EEPROM Sleep Mode Clock Gating Control (SCGCEEPROM), offset 0x758

The SCGCEEPROM register provides software the capability to enable and disable the EEPROM module in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power.

EEPROM Sleep Mode Clock Gating Control (SCGCEEPROM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>EEPROM Module Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 89: 32/64-Bit Wide General-Purpose Timer Sleep Mode Clock Gating Control (SCGCWTIMER), offset 0x75C

The SCGCWTIMER register provides software the capability to enable and disable 32/64-bit timer modules in sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Sleep Mode Clock Gating Control Registers SCGCn registers specifically for the timer modules and has the same bit polarity as the corresponding SCGCn bits.

32/64-Bit Wide General-Purpose Timer Sleep Mode Clock Gating Control (SCGCWTIMER)

Base 0x400F.E000
Offset 0x75C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>S5</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 5 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 5 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to 32/64-bit wide general-purpose timer module 5 in sleep mode.</td>
</tr>
<tr>
<td>4</td>
<td>S4</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 4 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 4 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to 32/64-bit wide general-purpose timer module 4 in sleep mode.</td>
</tr>
<tr>
<td>3</td>
<td>S3</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 3 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to 32/64-bit wide general-purpose timer module 3 in sleep mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>2</td>
<td>S2</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 2 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>S1</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 1 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>S0</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 0 Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 90: Watchdog Timer Deep-Sleep Mode Clock Gating Control (DCGCWD), offset 0x800

The DDCGCWD register provides software the capability to enable and disable watchdog modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

**Important:** This register should be used to control the clocking for the watchdog modules. To support legacy software, the DDCGC0 register is available. A write to the DDCGC0 register also writes the corresponding bit in this register. Any bits that are changed by writing to the DDCGC0 register can be read back correctly with a read of the DDCGC0 register. If software uses this register to write a legacy peripheral (such as Watchdog 0), the write causes proper operation, but the value of that bit is not reflected in the DDCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Watchdog Timer Deep-Sleep Mode Clock Gating Control (DCGCWD)

**Base** 0x400F.E000  
**Offset** 0x800  
**Type** RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Timer 1 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Watchdog module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to Watchdog module 1 in deep-sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Timer 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Watchdog module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to Watchdog module 0 in deep-sleep mode.</td>
</tr>
</tbody>
</table>
The **DCGCTIMER** register provides software the capability to enable and disable 16/32-bit timer modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy **Deep-Sleep Mode Clock Gating Control Register** and **DCGCn** registers specifically for the timer modules and has the same bit polarity as the corresponding **DCGCn** bits.

**Important:** This register should be used to control the clocking for the timer modules. To support legacy software, the **DCGC1** register is available. A write to the **DCGC1** register also writes the corresponding bit in this register. Any bits that are changed by writing to the **DCGC1** register can be read back correctly with a read of the **DCGC1** register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as Timer 0), the write causes proper operation, but the value of that bit is not reflected in the **DCGC1** register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

16/32-Bit General-Purpose Timer Deep-Sleep Mode Clock Gating Control (DCGCTIMER)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>D5</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 5 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  16/32-bit general-purpose timer module 5 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 5 in deep-sleep mode.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>4</td>
<td>D4</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 4 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 4 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 4 in deep-sleep mode.</td>
</tr>
<tr>
<td>3</td>
<td>D3</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 3 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 3 in deep-sleep mode.</td>
</tr>
<tr>
<td>2</td>
<td>D2</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 2 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 2 in deep-sleep mode.</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 1 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 1 in deep-sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit general-purpose timer module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 16/32-bit general-purpose timer module 0 in deep-sleep mode.</td>
</tr>
</tbody>
</table>
Register 92: General-Purpose Input/Output Deep-Sleep Mode Clock Gating Control (DCGCGPIO), offset 0x808

The DCGCGPIO register provides software the capability to enable and disable GPIO modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

Important: This register should be used to control the clocking for the GPIO modules. To support legacy software, the DCGC2 register is available. A write to the DCGC2 register also writes the corresponding bit in this register. Any bits that are changed by writing to the DCGC2 register can be read back correctly with a read of the DCGC2 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as GPIO A), the write causes proper operation, but the value of that bit is not reflected in the DCGC2 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

General-Purpose Input/Output Deep-Sleep Mode Clock Gating Control (DCGCGPIO)

Base 0x400F.E000
Offset 0x808
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>D9</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port K Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>D8</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port J Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>7</td>
<td>D7</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port H Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>D6</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port G Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>D5</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port F Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>D4</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port E Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>D3</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port D Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>D2</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port C Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port B Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
### GPIO Port A Deep-Sleep Mode Clock Gating Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>GPIO Port A Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>GPIO Port A is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to GPIO Port A in deep-sleep mode.</td>
</tr>
</tbody>
</table>
Register 93: Micro Direct Memory Access Deep-Sleep Mode Clock Gating Control (DCGCDMA), offset 0x80C

The DCGCDMA register provides software the capability to enable and disable the μDMA module in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register and DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

**Important:** This register should be used to control the clocking for the μDMA module. To support legacy software, the DCGC2 register is available. A write to the UDMA bit in the DCGC2 register also writes the D0 bit in this register. If the UDMA bit is changed by writing to the DCGC2 register, it can be read back correctly with a read of the DCGC2 register. If software uses this register to control the clock for the μDMA module, the write causes proper operation, but the UDMA bit in the DCGC2 register does not reflect the value of the D0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Micro Direct Memory Access Deep-Sleep Mode Clock Gating Control (DCGCDMA)

<table>
<thead>
<tr>
<th>Base 0x400F.E000</th>
<th>Offset 0x80C</th>
<th>Type RW, reset 0x0000.0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>μDMA Module Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 μDMA module is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to the μDMA module in deep-sleep mode.</td>
</tr>
</tbody>
</table>
Register 94: Hibernation Deep-Sleep Mode Clock Gating Control (DCGCHIB), offset 0x814

The DCGCHIB register provides software the capability to enable and disable the Hibernation module in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

**Important:** This register should be used to control the clocking for the Hibernation module. To support legacy software, the DCGC0 register is available. A write to the HIB bit in the DCGC0 register also writes the D0 bit in this register. If the HIB bit is changed by writing to the DCGC0 register, it can be read back correctly with a read of the DCGC0 register. If software uses this register to control the clock for the Hibernation module, the write causes proper operation, but the HIB bit in the DCGC0 register does not reflect the value of the D0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Hibernation Deep-Sleep Mode Clock Gating Control (DCGCHIB)

Base 0x400F.E000
Offset 0x814
Type RW, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>1</td>
<td>Hibernation Module Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value Description
0   Hibernation module is disabled.
1   Enable and provide a clock to the Hibernation module in deep-sleep mode.
The DCGCUART register provides software the capability to enable and disable the UART modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

**Important:** This register should be used to control the clocking for the UART modules. To support legacy software, the DCGC1 register is available. A write to the DCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the DCGC1 register can be read back correctly with a read of the DCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as UART0), the write causes proper operation, but the value of that bit is not reflected in the DCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

**Universal Asynchronous Receiver/Transmitter Deep-Sleep Mode Clock Gating Control (DCGCUART)**

Base 0x400F.E000
Offset 0x818
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>D7</td>
<td>RW</td>
<td>0</td>
<td>UART Module 7 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td>6</td>
<td>D6</td>
<td>RW</td>
<td>0</td>
<td>UART Module 6 Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

**June 12, 2014**

*Texas Instruments-Production Data*
## UART Module 0 Deep-Sleep Mode Clock Gating Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>UART module 0 is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>UART module 1 is disabled.</td>
</tr>
<tr>
<td>2</td>
<td>D2</td>
<td>RW</td>
<td>0</td>
<td>UART module 2 is disabled.</td>
</tr>
<tr>
<td>3</td>
<td>D3</td>
<td>RW</td>
<td>0</td>
<td>UART module 3 is disabled.</td>
</tr>
<tr>
<td>4</td>
<td>D4</td>
<td>RW</td>
<td>0</td>
<td>UART module 4 is disabled.</td>
</tr>
<tr>
<td>5</td>
<td>D5</td>
<td>RW</td>
<td>0</td>
<td>UART module 5 is disabled.</td>
</tr>
</tbody>
</table>

### Description

**Value**

- **0**: UART module 0 is disabled.
- **1**: Enable and provide a clock to UART module 0 in deep-sleep mode.

**Value**

- **0**: UART module 1 is disabled.
- **1**: Enable and provide a clock to UART module 1 in deep-sleep mode.

**Value**

- **0**: UART module 2 is disabled.
- **1**: Enable and provide a clock to UART module 2 in deep-sleep mode.

**Value**

- **0**: UART module 3 is disabled.
- **1**: Enable and provide a clock to UART module 3 in deep-sleep mode.

**Value**

- **0**: UART module 4 is disabled.
- **1**: Enable and provide a clock to UART module 4 in deep-sleep mode.

**Value**

- **0**: UART module 5 is disabled.
- **1**: Enable and provide a clock to UART module 5 in deep-sleep mode.
Register 96: Synchronous Serial Interface Deep-Sleep Mode Clock Gating Control (DCGCSSI), offset 0x81C

The DCGCSSI register provides software the capability to enable and disable the SSI modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

**Important:** This register should be used to control the clocking for the SSI modules. To support legacy software, the DCGC1 register is available. A write to the DCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the DCGC1 register can be read back correctly with a read of the DCGC1 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as SSI0), the write causes proper operation, but the value of that bit is not reflected in the DCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

**Synchronous Serial Interface Deep-Sleep Mode Clock Gating Control (DCGCSSI)**

Base 0x400F.E000
Offset 0x81C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>D3</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 3 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td>2</td>
<td>D2</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 2 Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

---

_Texas Instruments-Production Data_
### SSI Module 1 Deep-Sleep Mode Clock Gating Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 1 Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

**Value**  
0  
SSI module 1 is disabled.  
1  
Enable and provide a clock to SSI module 1 in deep-sleep mode.

### SSI Module 0 Deep-Sleep Mode Clock Gating Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>SSI Module 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

**Value**  
0  
SSI module 0 is disabled.  
1  
Enable and provide a clock to SSI module 0 in deep-sleep mode.
Register 97: Inter-Integrated Circuit Deep-Sleep Mode Clock Gating Control (DCGCI2C), offset 0x820

The DCGCI2C register provides software the capability to enable and disable the I\(^2\)C modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DGC\(\text{C}n\) registers specifically for the watchdog modules and has the same bit polarity as the corresponding DGC\(\text{C}n\) bits.

Important: This register should be used to control the clocking for the I\(^2\)C modules. To support legacy software, the DGC\(\text{C}1\) register is available. A write to the DGC\(\text{C}1\) register also writes the corresponding bit in this register. Any bits that are changed by writing to the DGC\(\text{C}1\) register can be read back correctly with a read of the DGC\(\text{C}1\) register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write a legacy peripheral (such as I\(^2\)C0), the write causes proper operation, but the value of that bit is not reflected in the DGC\(\text{C}1\) register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Inter-Integrated Circuit Deep-Sleep Mode Clock Gating Control (DCGCI2C)

Base 0x400F.E000
Offset 0x820
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>D5</td>
<td>RW</td>
<td>0</td>
<td>I(^2)C Module 5 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>I(^2)C module 5 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enable and provide a clock to I(^2)C module 5 in deep-sleep mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>D4</td>
<td>RW</td>
<td>0</td>
<td>I(^2)C Module 4 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>I(^2)C module 4 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enable and provide a clock to I(^2)C module 4 in deep-sleep mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>3</td>
<td>D3</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 3 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>I²C module 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to I²C module 3 in deep-sleep mode.</td>
</tr>
<tr>
<td>2</td>
<td>D2</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 2 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>I²C module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to I²C module 2 in deep-sleep mode.</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 1 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>I²C module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to I²C module 1 in deep-sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>I²C Module 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>I²C module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to I²C module 0 in deep-sleep mode.</td>
</tr>
</tbody>
</table>
Register 98: Universal Serial Bus Deep-Sleep Mode Clock Gating Control (DCGCUSB), offset 0x828

The DCGCUSB register provides software the capability to enable and disable the USB module in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

**Important:** This register should be used to control the clocking for the USB module. To support legacy software, the DCGC2 register is available. A write to the USB0 bit in the DCGC2 register also writes the D0 bit in this register. If the USB0 bit is changed by writing to the DCGC2 register, it can be read back correctly with a read of the DCGC2 register. If software uses this register to control the clock for the USB module, the write causes proper operation, but the USB0 bit in the DCGC2 register does not reflect the value of the D0 bit. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Universal Serial Bus Deep-Sleep Mode Clock Gating Control (DCGCUSB)

Base 0x400F.E000  
Offset 0x828  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>USB Module Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value Description

- 0  USB module is disabled.
- 1  Enable and provide a clock to the USB module in deep-sleep mode.
**Register 99: Controller Area Network Deep-Sleep Mode Clock Gating Control (DCGCCAN), offset 0x834**

The **DCGCCAN** register provides software the capability to enable and disable the CAN modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy **Deep-Sleep Mode Clock Gating Control Register n DCGCn** registers specifically for the watchdog modules and has the same bit polarity as the corresponding **DCGCn** bits.

**Important:** This register should be used to control the clocking for the CAN modules. To support legacy software, the **DCGC0** register is available. A write to the **DCGC0** register also writes the corresponding bit in this register. Any bits that are changed by writing to the **DCGC0** register can be read back correctly with a read of the **DCGC0** register. If software uses this register to write a legacy peripheral (such as CAN0), the write causes proper operation, but the value of that bit is not reflected in the **DCGC0** register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

**Controller Area Network Deep-Sleep Mode Clock Gating Control (DCGCCAN)**

*Base 0x400F.E000 Offset 0x834 Type RW, reset 0x0000.0000*

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RW</td>
<td>0</td>
<td>CAN Module 1 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>CAN Module 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

---

*June 12, 2014*  
*Texas Instruments-Production Data*
Register 100: Analog-to-Digital Converter Deep-Sleep Mode Clock Gating Control (DCGCADC), offset 0x838

The DCGCADC register provides software the capability to enable and disable the ADC modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

Important: This register should be used to control the clocking for the ADC modules. To support legacy software, the DCGC0 register is available. A write to the DCGC0 register also writes the corresponding bit in this register. Any bits that are changed by writing to the DCGC0 register can be read back correctly with a read of the DCGC0 register. If software uses this register to write a legacy peripheral (such as ADC0), the write causes proper operation, but the value of that bit is not reflected in the DCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Analog-to-Digital Converter Deep-Sleep Mode Clock Gating Control (DCGCADC)
Base 0x400E.FE00
Offset 0x838
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>ADC Module 1 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to ADC module 1 in deep-sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>ADC Module 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable and provide a clock to ADC module 0 in deep-sleep mode.</td>
</tr>
</tbody>
</table>
Register 101: Analog Comparator Deep-Sleep Mode Clock Gating Control (DCGCACMP), offset 0x83C

The DCGCACMP register provides software the capability to enable and disable the analog comparator module in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

**Important:** This register should be used to control the clocking for the analog comparator module. To support legacy software, the DCGC1 register is available. Setting any of the COMPn bits in the DCGC1 register also sets the D0 bit in this register. If any of the COMPn bits are set by writing to the DCGC1 register, it can be read back correctly when reading the DCGC1 register. If software uses this register to change the clocking for the analog comparator module, the write causes proper operation, but the value D0 is not reflected by the COMPn bits in the DCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

### Analog Comparator Deep-Sleep Mode Clock Gating Control (DCGCACMP)

<table>
<thead>
<tr>
<th>Base 0x400F.E000</th>
<th>Offset 0x83C</th>
<th>Type RW, reset 0x0000.0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>Analog Comparator Module 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value Description:
- 0 Analog comparator module is disabled.
- 1 Enable and provide a clock to the analog comparator module in deep-sleep mode.
Register 102: Pulse Width Modulator Deep-Sleep Mode Clock Gating Control (DCGCPWM), offset 0x840

The DCGCPWM register provides software the capability to enable and disable the PWM modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

Important: This register should be used to control the clocking for the PWM modules. To support legacy software, the DDCGC0 register is available. A write to the PWM bit in the DDCGC0 register also writes the D0 bit in this register. If the PWM bit is changed by writing to the DDCGC0 register, it can be read back correctly with a read of the DDCGC0 register. Software must use this register to support modules that are not present in the legacy registers. If software uses this register to write to D0, the write causes proper operation, but the value of that bit is not reflected in the PWM bit in the DDCGC0 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.
Register 103: Quadrature Encoder Interface Deep-Sleep Mode Clock Gating Control (DCGCQEI), offset 0x844

The DCGCQEI register provides software the capability to enable and disable the QEI modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the watchdog modules and has the same bit polarity as the corresponding DCGCn bits.

**Important:** This register should be used to control the clocking for the QEI modules. To support legacy software, the DCGC1 register is available. A write to the DCGC1 register also writes the corresponding bit in this register. Any bits that are changed by writing to the DCGC1 register can be read back correctly with a read of the DCGC1 register. If software uses this register to write a legacy peripheral (such as QEIO), the write causes proper operation, but the value of that bit is not reflected in the DCGC1 register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Quadrature Encoder Interface Deep-Sleep Mode Clock Gating Control (DCGCQEI)

Base 0x400F.E000
Offset 0x844
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>QEI Module 1 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 QEI module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to QEI module 1 in deep-sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>QEI Module 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 QEI module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to QEI module 0 in deep-sleep mode.</td>
</tr>
</tbody>
</table>
Register 104: EEPROM Deep-Sleep Mode Clock Gating Control (DCGCEEPROM), offset 0x858

The DCGCEEPROM register provides software the capability to enable and disable the EEPROM module in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power.

EEPROM Deep-Sleep Mode Clock Gating Control (DCGCEEPROM)

Base 0x400F.E000
Offset 0x858
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>EEPROM Module Deep-Sleep Mode Clock Gating Control</td>
</tr>
</tbody>
</table>

Value   Description
0       EEPROM module is disabled.
1       Enable and provide a clock to the EEPROM module in deep-sleep mode.
Register 105: 32/64-Bit Wide General-Purpose Timer Deep-Sleep Mode Clock Gating Control (DCGCWTIMER), offset 0x85C

The DCGCW TIMER register provides software the capability to enable and disable 32/64-bit wide timer modules in deep-sleep mode. When enabled, a module is provided a clock. When disabled, the clock is disabled to save power. This register provides the same capability as the legacy Deep-Sleep Mode Clock Gating Control Register n DCGCn registers specifically for the timer modules and has the same bit polarity as the corresponding DCGCn bits.

### 32/64-Bit Wide General-Purpose Timer Deep-Sleep Mode Clock Gating Control (DCGCWTIMER)

<table>
<thead>
<tr>
<th>Offset 0x85C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RW, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>32/64-Bit Wide General-Purpose Timer 5 Deep-Sleep Mode Clock Gating Control</td>
<td></td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 5 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to 32/64-bit wide general-purpose timer module 5 in deep-sleep mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32/64-Bit Wide General-Purpose Timer 4 Deep-Sleep Mode Clock Gating Control</td>
<td></td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 4 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to 32/64-bit wide general-purpose timer module 4 in deep-sleep mode.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32/64-Bit Wide General-Purpose Timer 3 Deep-Sleep Mode Clock Gating Control</td>
<td></td>
<td>RW</td>
<td>0</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>32/64-bit wide general-purpose timer module 3 is disabled.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enable and provide a clock to 32/64-bit wide general-purpose timer module 3 in deep-sleep mode.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>D5</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 5 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td>RO</td>
<td>D4</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 4 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td>RO</td>
<td>D3</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 3 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>2</td>
<td>D2</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 2 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide general-purpose timer module 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 32/64-bit wide general-purpose timer module 2 in deep-sleep mode.</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 1 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide general-purpose timer module 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 32/64-bit wide general-purpose timer module 1 in deep-sleep mode.</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 0 Deep-Sleep Mode Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide general-purpose timer module 0 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enable and provide a clock to 32/64-bit wide general-purpose timer module 0 in deep-sleep mode.</td>
</tr>
</tbody>
</table>
Register 106: Watchdog Timer Peripheral Ready (PRWD), offset 0xA00

The **PRWD** register indicates whether the watchdog modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding **RGCWD** bit is changed. A reset change is initiated if the corresponding **SRWD** bit is changed from 0 to 1.

The **PRWD** bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

### Watchdog Timer Peripheral Ready (PRWD)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog module 1 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
<td>0</td>
</tr>
<tr>
<td>Watchdog module 1 is ready for access.</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog module 0 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
<td>0</td>
</tr>
<tr>
<td>Watchdog module 0 is ready for access.</td>
<td>1</td>
</tr>
</tbody>
</table>
The **PRTIMER** register indicates whether the timer modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding **RCGCTIMER** bit is changed. A reset change is initiated if the corresponding **SRTIMER** bit is changed from 0 to 1.

The **PRTIMER** bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

### 16/32-Bit General-Purpose Timer Peripheral Ready (PRTIMER)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RO</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 5 Peripheral Ready</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RO</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 4 Peripheral Ready</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RO</td>
<td>0</td>
<td>16/32-Bit General-Purpose Timer 3 Peripheral Ready</td>
</tr>
</tbody>
</table>
## System Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>R2</td>
<td>RO</td>
<td>0</td>
<td><strong>16/32-Bit General-Purpose Timer 2 Peripheral Ready</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit timer module 2 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 16/32-bit timer module 2 is ready for access.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td><strong>16/32-Bit General-Purpose Timer 1 Peripheral Ready</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit timer module 1 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 16/32-bit timer module 1 is ready for access.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td><strong>16/32-Bit General-Purpose Timer 0 Peripheral Ready</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 16/32-bit timer module 0 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 16/32-bit timer module 0 is ready for access.</td>
</tr>
</tbody>
</table>
Register 108: General-Purpose Input/Output Peripheral Ready (PRGPIO), offset 0xA08

The PRGPIO register indicates whether the GPIO modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCGPIO bit is changed. A reset change is initiated if the corresponding SRGPIO bit is changed from 0 to 1.

The PRGPIO bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

General-Purpose Input/Output Peripheral Ready (PRGPIO)
Base 0x400F.E000
Offset 0xA08
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>R9</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port K Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port K is not ready for access. It is unclocked, unpowered,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port K is ready for access.</td>
</tr>
<tr>
<td>8</td>
<td>R8</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port J Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port J is not ready for access. It is unclocked, unpowered,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port J is ready for access.</td>
</tr>
<tr>
<td>7</td>
<td>R7</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port H Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port H is not ready for access. It is unclocked, unpowered,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port H is ready for access.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>6</td>
<td>R6</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port G Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port G is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port G is ready for access.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port F Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port F is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port F is ready for access.</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port E Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port E is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port E is ready for access.</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port D Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port D is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port D is ready for access.</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port C Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port C is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port C is ready for access.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port B Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port B is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port B is ready for access.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>GPIO Port A Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  GPIO Port A is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  GPIO Port A is ready for access.</td>
</tr>
</tbody>
</table>
Register 109: Micro Direct Memory Access Peripheral Ready (PRDMA), offset 0xA0C

The PRDMA register indicates whether the μDMA module is ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCDMA bit is changed. A reset change is initiated if the corresponding SRDMA bit is changed from 0 to 1.

The PRDMA bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

Micro Direct Memory Access Peripheral Ready (PRDMA)
Base 0x400F.E000
Offset 0xA0C
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>μDMA Module Peripheral Ready</td>
</tr>
</tbody>
</table>

Value Description

0 The μDMA module is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.
1 The μDMA module is ready for access.
Register 110: Hibernation Peripheral Ready (PRHIB), offset 0xA14

The PRHIB register indicates whether the Hibernation module is ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCHIB bit is changed. A reset change is initiated if the corresponding SRHIB bit is changed from 0 to 1.

The PRHIB bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

Hibernation Peripheral Ready (PRHIB)
Base 0x400F.E000
Offset 0xA14
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>1</td>
<td>Hibernation Module Peripheral Ready</td>
</tr>
</tbody>
</table>

Value Description
0 The Hibernation module is not ready for access. It is uncleaked, unpowered, or in the process of completing a reset sequence.
1 The Hibernation module is ready for access.
Register 111: Universal Asynchronous Receiver/Transmitter Peripheral Ready (PRUART), offset 0xA18

The PRUART register indicates whether the UART modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCUART bit is changed. A reset change is initiated if the corresponding SRUART bit is changed from 0 to 1.

The PRUART bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

Universal Asynchronous Receiver/Transmitter Peripheral Ready (PRUART)

Base 0x400F.E000
Offset 0xA18
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>R7</td>
<td>RO</td>
<td>0</td>
<td>UART Module 7 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Value Description</td>
<td>0</td>
<td>UART module 7 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>UART module 7 is ready for access.</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>R6</td>
<td>RO</td>
<td>0</td>
<td>UART Module 6 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Value Description</td>
<td>0</td>
<td>UART module 6 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>UART module 6 is ready for access.</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RO</td>
<td>0</td>
<td>UART Module 5 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Value Description</td>
<td>0</td>
<td>UART module 5 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>UART module 5 is ready for access.</td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RO</td>
<td>0</td>
<td>UART Module 4 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RO</td>
<td>0</td>
<td>UART Module 3 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RO</td>
<td>0</td>
<td>UART Module 2 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td>UART Module 1 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>UART Module 0 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 112: Synchronous Serial Interface Peripheral Ready (PRSSI), offset 0xA1C

The PRSSI register indicates whether the SSI modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCSSI bit is changed. A reset change is initiated if the corresponding SRSSI bit is changed from 0 to 1.

The PRSSI bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

### Synchronous Serial Interface Peripheral Ready (PRSSI)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x400F.E000</td>
<td>0xA1C</td>
<td>RO</td>
<td>0x0000.0000</td>
</tr>
</tbody>
</table>

**Bit/Field** | **Name** | **Type** | **Reset** | **Description**
--- | --- | --- | --- | ---
31:4 | **reserved** | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
3 | **R3** | RO | 0 | SSI Module 3 Peripheral Ready
Value Description
0 | SSI module 3 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.
1 | SSI module 3 is ready for access.
2 | **R2** | RO | 0 | SSI Module 2 Peripheral Ready
Value Description
0 | SSI module 2 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.
1 | SSI module 2 is ready for access.
1 | **R1** | RO | 0 | SSI Module 1 Peripheral Ready
Value Description
0 | SSI module 1 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.
1 | SSI module 1 is ready for access.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>SSI Module 0 Peripheral Ready</td>
</tr>
</tbody>
</table>

Value    Description
0  SSI module 0 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.
1  SSI module 0 is ready for access.
Register 113: Inter-Integrated Circuit Peripheral Ready (PRI2C), offset 0xA20

The PRI2C register indicates whether the I\(^2\)C modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGC\(_{I2C}\) bit is changed. A reset change is initiated if the corresponding SRI2C bit is changed from 0 to 1.

The PRI2C bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

### Inter-Integrated Circuit Peripheral Ready (PRI2C)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Field</th>
<th>Base</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA20</td>
<td></td>
<td>0x400F.E000</td>
<td>RO</td>
<td>0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RO</td>
<td>0</td>
<td>I(^2)C Module 5 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 I(^2)C module 5 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 I(^2)C module 5 is ready for access.</td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RO</td>
<td>0</td>
<td>I(^2)C Module 4 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 I(^2)C module 4 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 I(^2)C module 4 is ready for access.</td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RO</td>
<td>0</td>
<td>I(^2)C Module 3 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 I(^2)C module 3 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 I(^2)C module 3 is ready for access.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RO</td>
<td>0</td>
<td>I²C Module 2 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td>I²C Module 1 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>I²C Module 0 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 114: Universal Serial Bus Peripheral Ready (PRUSB), offset 0xA28

The PRUSB register indicates whether the USB module is ready to be accessed by software following a change in Run mode clocking or reset. A Run mode clocking change is initiated if the corresponding RCGCUSB bit is changed. A reset change is initiated if the corresponding SRUSB bit is changed from 0 to 1.

The PRUSB bit is cleared on either of the above events and is not set again until the module is completely powered, enabled, and internally reset.

### Universal Serial Bus Peripheral Ready (PRUSB)

**Base** 0x400F.E000  
**Offset** 0xA28  
**Type** RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>USB Module Peripheral Ready</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>USB Module Peripheral Ready</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The USB module is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td>1</td>
<td>The USB module is ready for access.</td>
</tr>
</tbody>
</table>
Register 115: Controller Area Network Peripheral Ready (PRCAN), offset 0xA34

The PRCAN register indicates whether the CAN modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCCAN bit is changed. A reset change is initiated if the corresponding SRCAN bit is changed from 0 to 1.

The PRCAN bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

Controller Area Network Peripheral Ready (PRCAN)
Base 0x400F.E000
Offset 0xA34
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td>CAN Module 1 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>CAN Module 0 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 116: Analog-to-Digital Converter Peripheral Ready (PRADC), offset 0xA38

The PRADC register indicates whether the ADC modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCADC bit is changed. A reset change is initiated if the corresponding SRADC bit is changed from 0 to 1.

The PRADC bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

### Analog-to-Digital Converter Peripheral Ready (PRADC)
Base 0x400F.E000
Offset 0x0A38
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td>ADC Module 1 Peripheral Ready</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>ADC Module 0 Peripheral Ready</td>
</tr>
</tbody>
</table>
Register 117: Analog Comparator Peripheral Ready (PRACMP), offset 0xA3C

The PRACMP register indicates whether the analog comparator module is ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RGCACMP bit is changed. A reset change is initiated if the corresponding SRACMP bit is changed from 0 to 1.

The PRACMP bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

Analog Comparator Peripheral Ready (PRACMP)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>Analog Comparator Module 0 Peripheral Ready</td>
</tr>
</tbody>
</table>

Value Description

0 The analog comparator module is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.

1 The analog comparator module is ready for access.
Register 118: Pulse Width Modulator Peripheral Ready (PRPWM), offset 0xA40

The PRPWM register indicates whether the PWM modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCPWM bit is changed. A reset change is initiated if the corresponding SRPWM bit is changed from 0 to 1.

The PRPWM bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

Pulse Width Modulator Peripheral Ready (PRPWM)
Base 0x400F.E000
Offset 0xA40
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td>PWM Module 1 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>PWM module 1 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>PWM module 1 is ready for access.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>PWM Module 0 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>PWM module 0 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>PWM module 0 is ready for access.</td>
</tr>
</tbody>
</table>
Register 119: Quadrature Encoder Interface Peripheral Ready (PRQEI), offset 0xA44

The PRQEI register indicates whether the QEI modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCQEI bit is changed. A reset change is initiated if the corresponding SRQEI bit is changed from 0 to 1.

The PRQEI bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

Quadrature Encoder Interface Peripheral Ready (PRQEI)
Base 0x400F.E000
Offset 0xA44
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td>QEI Module 1 Peripheral Ready</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>QEI Module 0 Peripheral Ready</td>
</tr>
</tbody>
</table>
Register 120: EEPROM Peripheral Ready (PREEPROM), offset 0xA58

The PREEPROM register indicates whether the EEPROM module is ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCEEPROM bit is changed. A reset change is initiated if the corresponding SREEPROM bit is changed from 0 to 1.

The PREEPROM bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

EEPROM Peripheral Ready (PREEPROM)

Base 0x400F.E000
Offset 0xA58
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>EEPROM Module Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The EEPROM module is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The EEPROM module is ready for access.</td>
</tr>
</tbody>
</table>
Register 121: 32/64-Bit Wide General-Purpose Timer Peripheral Ready (PRWTIMER), offset 0xA5C

The PRWTIMER register indicates whether the timer modules are ready to be accessed by software following a change in status of power, Run mode clocking, or reset. A Run mode clocking change is initiated if the corresponding RCGCWVTIMER bit is changed. A reset change is initiated if the corresponding SRWTIMER bit is changed from 0 to 1.

The PRWTIMER bit is cleared on any of the above events and is not set again until the module is completely powered, enabled, and internally reset.

32/64-Bit Wide General-Purpose Timer Peripheral Ready (PRWTIMER)
Base 0x400F.E000
Offset 0xA5C
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>R5</td>
<td>RO</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 5 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Value</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>0</td>
<td>32/64-bit wide timer module 5 is not ready for access. It is unclecked, unpowered, or in the process of completing a reset sequence.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>1</td>
<td>32/64-bit wide timer module 5 is ready for access.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>R4</td>
<td>RO</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 4 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Value</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>0</td>
<td>32/64-bit wide timer module 4 is not ready for access. It is unclecked, unpowered, or in the process of completing a reset sequence.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>1</td>
<td>32/64-bit wide timer module 4 is ready for access.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>R3</td>
<td>RO</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 3 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td>Value</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>0</td>
<td>32/64-bit wide timer module 3 is not ready for access. It is unclecked, unpowered, or in the process of completing a reset sequence.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>1</td>
<td>32/64-bit wide timer module 3 is ready for access.</td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>2</td>
<td>R2</td>
<td>RO</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 2 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide timer module 2 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 32/64-bit wide timer module 2 is ready for access.</td>
</tr>
<tr>
<td>1</td>
<td>R1</td>
<td>RO</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 1 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide timer module 1 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 32/64-bit wide timer module 1 is ready for access.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>RO</td>
<td>0</td>
<td>32/64-Bit Wide General-Purpose Timer 0 Peripheral Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 32/64-bit wide timer module 0 is not ready for access. It is unclocked, unpowered, or in the process of completing a reset sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 32/64-bit wide timer module 0 is ready for access.</td>
</tr>
</tbody>
</table>

### 5.6 System Control Legacy Register Descriptions

All addresses given are relative to the System Control base address of 0x400F.E000.

**Important:** Register in this section are provided for legacy software support only; registers in “System Control Register Descriptions” on page 237 should be used instead.
Register 122: Device Capabilities 0 (DC0), offset 0x008

This legacy register is predefined by the part and can be used to verify features.

**Important:** This register is provided for legacy software support only.

The **Flash Size (FSIZE)** and **SRAM Size (SSIZE)** registers should be used to determine this microcontroller's memory sizes. A read of **DC0** correctly identifies legacy memory sizes but software must use **FSIZE** and **SSIZE** for memory sizes that are not listed below.

---

**Device Capabilities 0 (DC0)**

Base 0x400F.E000
Offset 0x008
Type RO, reset 0x007F.007F

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:16     | SRAMSZ  | RO   | 0x7F  | SRAM Size
|           |         |      |       | Indicates the size of the on-chip SRAM. |

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x7</td>
<td>2 KB of SRAM</td>
</tr>
<tr>
<td>0xF</td>
<td>4 KB of SRAM</td>
</tr>
<tr>
<td>0x17</td>
<td>6 KB of SRAM</td>
</tr>
<tr>
<td>0x1F</td>
<td>8 KB of SRAM</td>
</tr>
<tr>
<td>0x2F</td>
<td>12 KB of SRAM</td>
</tr>
<tr>
<td>0x3F</td>
<td>16 KB of SRAM</td>
</tr>
<tr>
<td>0x4F</td>
<td>20 KB of SRAM</td>
</tr>
<tr>
<td>0x5F</td>
<td>24 KB of SRAM</td>
</tr>
<tr>
<td>0x7F</td>
<td>32 KB of SRAM</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
</tr>
<tr>
<td>15:0</td>
<td>FLASHSZ</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3</td>
<td>8 KB of Flash</td>
</tr>
<tr>
<td>0x7</td>
<td>16 KB of Flash</td>
</tr>
<tr>
<td>0xF</td>
<td>32 KB of Flash</td>
</tr>
<tr>
<td>0x1F</td>
<td>64 KB of Flash</td>
</tr>
<tr>
<td>0x2F</td>
<td>96 KB of Flash</td>
</tr>
<tr>
<td>0x3F</td>
<td>128 KB of Flash</td>
</tr>
<tr>
<td>0x5F</td>
<td>192 KB of Flash</td>
</tr>
<tr>
<td>0x7F</td>
<td>256 KB of Flash</td>
</tr>
</tbody>
</table>
Register 123: Device Capabilities 1 (DC1), offset 0x010

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC0, SCGC0, DCGC0, and the peripheral-specific RCGC, SCGC, and DCGC registers cannot be set.

**Important:** This register is provided for legacy software support only.

The Peripheral Present registers should be used to determine which modules are implemented on this microcontroller. A read of DC1 correctly identifies if a legacy module is present but software must use the Peripheral Present registers to determine if a module is present that is not supported by the DCn registers.

Likewise, the ADC Peripheral Properties (ADCPP) register should be used to determine the maximum ADC sample rate and whether the temperature sensor is present. However, to support legacy software, the MAXADChSPD fields and the TEMPSNS bit are available. A read of DC1 correctly identifies the maximum ADC sample rate for legacy rates and whether the temperature sensor is present.

### Device Capabilities 1 (DC1)

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>28</td>
<td>WDT1</td>
<td>RO</td>
<td>0x1</td>
<td>Watchdog Timer1 Present When set, indicates that watchdog timer 1 is present.</td>
</tr>
<tr>
<td>27:26</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>25</td>
<td>CAN1</td>
<td>RO</td>
<td>0x1</td>
<td>CAN Module 1 Present When set, indicates that CAN unit 1 is present.</td>
</tr>
<tr>
<td>24</td>
<td>CAN0</td>
<td>RO</td>
<td>0x1</td>
<td>CAN Module 0 Present When set, indicates that CAN unit 0 is present.</td>
</tr>
<tr>
<td>23:22</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>21</td>
<td>PWM1</td>
<td>RO</td>
<td>0x1</td>
<td>PWM Module 1 Present When set, indicates that the PWM module is present.</td>
</tr>
</tbody>
</table>
### Bit/Field | Name | Type | Reset | Description
--- | --- | --- | --- | ---
20 | PWM0 | RO | 0x1 | PWM Module 0 Present
When set, indicates that the PWM module is present.
19:18 | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
17 | ADC1 | RO | 0x1 | ADC Module 1 Present
When set, indicates that ADC module 1 is present.
16 | ADC0 | RO | 0x1 | ADC Module 0 Present
When set, indicates that ADC module 0 is present.
15:12 | MINSYSDIV | RO | 0x2 | System Clock Divider
Minimum 4-bit divider value for system clock. The reset value is hardware-dependent. See the RCC register for how to change the system clock divisor using the SYSDIV bit.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x2</td>
<td>Specifies an 80-MHz CPU clock with a PLL divider of 2.5.</td>
</tr>
<tr>
<td>0x3</td>
<td>Specifies a 50-MHz CPU clock with a PLL divider of 4.</td>
</tr>
<tr>
<td>0x4</td>
<td>Specifies a 40-MHz CPU clock with a PLL divider of 5.</td>
</tr>
<tr>
<td>0x7</td>
<td>Specifies a 25-MHz clock with a PLL divider of 8.</td>
</tr>
<tr>
<td>0x9</td>
<td>Specifies a 20-MHz clock with a PLL divider of 10.</td>
</tr>
</tbody>
</table>

11:10 | MAXADC1SPD | RO | 0x3 | Max ADC1 Speed
This field indicates the maximum rate at which the ADC samples data.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3</td>
<td>1M samples/second</td>
</tr>
<tr>
<td>0x2</td>
<td>500K samples/second</td>
</tr>
<tr>
<td>0x1</td>
<td>250K samples/second</td>
</tr>
<tr>
<td>0x0</td>
<td>125K samples/second</td>
</tr>
</tbody>
</table>

9:8 | MAXADC0SPD | RO | 0x3 | Max ADC0 Speed
This field indicates the maximum rate at which the ADC samples data.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3</td>
<td>1M samples/second</td>
</tr>
<tr>
<td>0x2</td>
<td>500K samples/second</td>
</tr>
<tr>
<td>0x1</td>
<td>250K samples/second</td>
</tr>
<tr>
<td>0x0</td>
<td>125K samples/second</td>
</tr>
</tbody>
</table>

7 | MPU | RO | 0x1 | MPU Present
When set, indicates that the Cortex-M4F Memory Protection Unit (MPU) module is present. See the "Cortex-M4F Peripherals" chapter for details on the MPU.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>HIB</td>
<td>RO</td>
<td>0x1</td>
<td>Hibernation Module Present When set, indicates that the Hibernation module is present.</td>
</tr>
<tr>
<td>5</td>
<td>TEMPSNS</td>
<td>RO</td>
<td>0x1</td>
<td>Temp Sensor Present When set, indicates that the on-chip temperature sensor is present.</td>
</tr>
<tr>
<td>4</td>
<td>PLL</td>
<td>RO</td>
<td>0x1</td>
<td>PLL Present When set, indicates that the on-chip Phase Locked Loop (PLL) is present.</td>
</tr>
<tr>
<td>3</td>
<td>WDT0</td>
<td>RO</td>
<td>0x1</td>
<td>Watchdog Timer 0 Present When set, indicates that watchdog timer 0 is present.</td>
</tr>
<tr>
<td>2</td>
<td>SWO</td>
<td>RO</td>
<td>0x1</td>
<td>SWO Trace Port Present When set, indicates that the Serial Wire Output (SWO) trace port is present.</td>
</tr>
<tr>
<td>1</td>
<td>SWD</td>
<td>RO</td>
<td>0x1</td>
<td>SWD Present When set, indicates that the Serial Wire Debugger (SWD) is present.</td>
</tr>
<tr>
<td>0</td>
<td>JTAG</td>
<td>RO</td>
<td>0x1</td>
<td>JTAG Present When set, indicates that the JTAG debugger interface is present.</td>
</tr>
</tbody>
</table>
Register 124: Device Capabilities 2 (DC2), offset 0x014

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC1, SCGC1, DCGC1, and the peripheral-specific RCGC, SCGC, and DCGC registers cannot be set.

**Important:** This register is provided for legacy software support only.

The Peripheral Present registers should be used to determine which modules are implemented on this microcontroller. A read of DC2 correctly identifies if a legacy module is present but software must use the Peripheral Present registers to determine if a module is present that is not supported by the DCn registers.

Note that the Analog Comparator Peripheral Present (PPACMP) register identifies whether the analog comparator module is present. The Analog Comparator Peripheral Properties (ACMPPP) register indicates how many analog comparator blocks are present in the module.

### Device Capabilities 2 (DC2)

Base 0x400F.E000
Offset 0x014
Type RO, reset 0x070F.F337

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>30</td>
<td>EPI0</td>
<td>RO</td>
<td>0x0</td>
<td>EPI Module 0 Present When set, indicates that EPI module 0 is present.</td>
</tr>
<tr>
<td>29</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>28</td>
<td>I2S0</td>
<td>RO</td>
<td>0x0</td>
<td>I2S Module 0 Present When set, indicates that I2S module 0 is present.</td>
</tr>
<tr>
<td>27</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>26</td>
<td>COMP2</td>
<td>RO</td>
<td>0x1</td>
<td>Analog Comparator 2 Present When set, indicates that analog comparator 2 is present.</td>
</tr>
<tr>
<td>25</td>
<td>COMP1</td>
<td>RO</td>
<td>0x1</td>
<td>Analog Comparator 1 Present When set, indicates that analog comparator 1 is present.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>24</td>
<td>COMP0</td>
<td>RO</td>
<td>0x1</td>
<td>Analog Comparator 0 Present When set, indicates that analog comparator 0 is present.</td>
</tr>
<tr>
<td>23:20</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19</td>
<td>TIMER3</td>
<td>RO</td>
<td>0x1</td>
<td>Timer Module 3 Present When set, indicates that General-Purpose Timer module 3 is present.</td>
</tr>
<tr>
<td>18</td>
<td>TIMER2</td>
<td>RO</td>
<td>0x1</td>
<td>Timer Module 2 Present When set, indicates that General-Purpose Timer module 2 is present.</td>
</tr>
<tr>
<td>17</td>
<td>TIMER1</td>
<td>RO</td>
<td>0x1</td>
<td>Timer Module 1 Present When set, indicates that General-Purpose Timer module 1 is present.</td>
</tr>
<tr>
<td>16</td>
<td>TIMER0</td>
<td>RO</td>
<td>0x1</td>
<td>Timer Module 0 Present When set, indicates that General-Purpose Timer module 0 is present.</td>
</tr>
<tr>
<td>15</td>
<td>I2C1HS</td>
<td>RO</td>
<td>0x1</td>
<td>I2C Module 1 Speed When set, indicates that I2C module 1 can operate in high-speed mode.</td>
</tr>
<tr>
<td>14</td>
<td>I2C1</td>
<td>RO</td>
<td>0x1</td>
<td>I2C Module 1 Present When set, indicates that I2C module 1 is present.</td>
</tr>
<tr>
<td>13</td>
<td>I2C0HS</td>
<td>RO</td>
<td>0x1</td>
<td>I2C Module 0 Speed When set, indicates that I2C module 0 can operate in high-speed mode.</td>
</tr>
<tr>
<td>12</td>
<td>I2C0</td>
<td>RO</td>
<td>0x1</td>
<td>I2C Module 0 Present When set, indicates that I2C module 0 is present.</td>
</tr>
<tr>
<td>11:10</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>QE11</td>
<td>RO</td>
<td>0x1</td>
<td>QEI Module 1 Present When set, indicates that QEI module 1 is present.</td>
</tr>
<tr>
<td>8</td>
<td>QE10</td>
<td>RO</td>
<td>0x1</td>
<td>QEI Module 0 Present When set, indicates that QEI module 0 is present.</td>
</tr>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>SSI1</td>
<td>RO</td>
<td>0x1</td>
<td>SSI Module 1 Present When set, indicates that SSI module 1 is present.</td>
</tr>
<tr>
<td>4</td>
<td>SSI0</td>
<td>RO</td>
<td>0x1</td>
<td>SSI Module 0 Present When set, indicates that SSI module 0 is present.</td>
</tr>
<tr>
<td>3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>UART2</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 2 Present&lt;br&gt;When set, indicates that UART module 2 is present.</td>
</tr>
<tr>
<td>1</td>
<td>UART1</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 1 Present&lt;br&gt;When set, indicates that UART module 1 is present.</td>
</tr>
<tr>
<td>0</td>
<td>UART0</td>
<td>RO</td>
<td>0x1</td>
<td>UART Module 0 Present&lt;br&gt;When set, indicates that UART module 0 is present.</td>
</tr>
</tbody>
</table>
Register 125: Device Capabilities 3 (DC3), offset 0x018

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the feature is not present.

**Important:** This register is provided for legacy software support only.

For some modules, the peripheral-resident Peripheral Properties registers should be used to determine which pins are available on this microcontroller. A read of DC3 correctly identifies if a legacy pin is present but software must use the Peripheral Properties registers to determine if a pin is present that is not supported by the DCn registers.

---

### Device Capabilities 3 (DC3)

Base 0x400F.E000  
Offset 0x018  
Type RO, reset 0xBFFF.FFFF

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31  | 32KHZ      | RO    | 0x1   | 32KHz Input Clock Available  
When set, indicates an even CCP pin is present and can be used as a 32-KHz input clock.  
**Note:** The GPTMPP register does not provide this information. |
| 30  | reserved   | RO    | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 29  | CCP5       | RO    | 0x1   | T2CCP1 Pin Present  
When set, indicates that Capture/Compare/PWM pin T2CCP1 is present.  
**Note:** The GPTMPP register does not provide this information. |
| 28  | CCP4       | RO    | 0x1   | T2CCP0 Pin Present  
When set, indicates that Capture/Compare/PWM pin T2CCP0 is present.  
**Note:** The GPTMPP register does not provide this information. |
| 27  | CCP3       | RO    | 0x1   | T1CCP1 Pin Present  
When set, indicates that Capture/Compare/PWM pin T1CCP1 is present.  
**Note:** The GPTMPP register does not provide this information. |
| 26  | CCP2       | RO    | 0x1   | T1CCP0 Pin Present  
When set, indicates that Capture/Compare/PWM pin T1CCP0 is present.  
**Note:** The GPTMPP register does not provide this information. |
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>CCP1</td>
<td>RO</td>
<td>0x1</td>
<td>T0CCP1 Pin Present&lt;br&gt;When set, indicates that Capture/Compare/PWM pin T0CCP1 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The GPTMPP register does not provide this information.</td>
</tr>
<tr>
<td>24</td>
<td>CCP0</td>
<td>RO</td>
<td>0x1</td>
<td>T0CCP0 Pin Present&lt;br&gt;When set, indicates that Capture/Compare/PWM pin T0CCP0 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The GPTMPP register does not provide this information.</td>
</tr>
<tr>
<td>23</td>
<td>ADC0AIN7</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN7 Pin Present&lt;br&gt;When set, indicates that ADC module 0 input pin 7 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The CH field in the ADCCP register provides this information.</td>
</tr>
<tr>
<td>22</td>
<td>ADC0AIN6</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN6 Pin Present&lt;br&gt;When set, indicates that ADC module 0 input pin 6 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The CH field in the ADCCP register provides this information.</td>
</tr>
<tr>
<td>21</td>
<td>ADC0AIN5</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN5 Pin Present&lt;br&gt;When set, indicates that ADC module 0 input pin 5 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The CH field in the ADCCP register provides this information.</td>
</tr>
<tr>
<td>20</td>
<td>ADC0AIN4</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN4 Pin Present&lt;br&gt;When set, indicates that ADC module 0 input pin 4 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The CH field in the ADCCP register provides this information.</td>
</tr>
<tr>
<td>19</td>
<td>ADC0AIN3</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN3 Pin Present&lt;br&gt;When set, indicates that ADC module 0 input pin 3 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The CH field in the ADCCP register provides this information.</td>
</tr>
<tr>
<td>18</td>
<td>ADC0AIN2</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN2 Pin Present&lt;br&gt;When set, indicates that ADC module 0 input pin 2 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The CH field in the ADCCP register provides this information.</td>
</tr>
<tr>
<td>17</td>
<td>ADC0AIN1</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN1 Pin Present&lt;br&gt;When set, indicates that ADC module 0 input pin 1 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The CH field in the ADCCP register provides this information.</td>
</tr>
<tr>
<td>16</td>
<td>ADC0AIN0</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN0 Pin Present&lt;br&gt;When set, indicates that ADC module 0 input pin 0 is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The CH field in the ADCCP register provides this information.</td>
</tr>
<tr>
<td>15</td>
<td>PWMFAULT</td>
<td>RO</td>
<td>0x1</td>
<td>PWM Fault Pin Present&lt;br&gt;When set, indicates that a PWM Fault pin is present. See DC5 for specific Fault pins on this device.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The FCNT field in the PWMPP register provides this information.</td>
</tr>
<tr>
<td>14</td>
<td>C2O</td>
<td>RO</td>
<td>0x1</td>
<td>C2O Pin Present&lt;br&gt;When set, indicates that the analog comparator 2 output pin is present.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The C2O bit in the ACMPPP register provides this information.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>13</td>
<td>C2PLUS</td>
<td>RO</td>
<td>0x1</td>
<td>C2+ Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the analog comparator 2 (+) input pin is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This pin is present when analog comparator 2 is present.</td>
</tr>
<tr>
<td>12</td>
<td>C2MINUS</td>
<td>RO</td>
<td>0x1</td>
<td>C2- Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the analog comparator 2 (-) input pin is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This pin is present when analog comparator 2 is present.</td>
</tr>
<tr>
<td>11</td>
<td>C1O</td>
<td>RO</td>
<td>0x1</td>
<td>C1o Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the analog comparator 1 output pin is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The <strong>C1O</strong> bit in the <strong>ACMPPP</strong> register provides this information.</td>
</tr>
<tr>
<td>10</td>
<td>C1PLUS</td>
<td>RO</td>
<td>0x1</td>
<td>C1+ Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the analog comparator 1 (+) input pin is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This pin is present when analog comparator 1 is present.</td>
</tr>
<tr>
<td>9</td>
<td>C1MINUS</td>
<td>RO</td>
<td>0x1</td>
<td>C1- Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the analog comparator 1 (-) input pin is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This pin is present when analog comparator 1 is present.</td>
</tr>
<tr>
<td>8</td>
<td>C0O</td>
<td>RO</td>
<td>0x1</td>
<td>C0o Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the analog comparator 0 output pin is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The <strong>C0O</strong> bit in the <strong>ACMPPP</strong> register provides this information.</td>
</tr>
<tr>
<td>7</td>
<td>C0PLUS</td>
<td>RO</td>
<td>0x1</td>
<td>C0+ Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the analog comparator 0 (+) input pin is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This pin is present when analog comparator 0 is present.</td>
</tr>
<tr>
<td>6</td>
<td>C0MINUS</td>
<td>RO</td>
<td>0x1</td>
<td>C0- Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the analog comparator 0 (-) input pin is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This pin is present when analog comparator 0 is present.</td>
</tr>
<tr>
<td>5</td>
<td>PWM5</td>
<td>RO</td>
<td>0x1</td>
<td>PWM5 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the PWM pin 5 is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The <strong>GCNT</strong> field in the <strong>PWMPP</strong> register provides this information.</td>
</tr>
<tr>
<td>4</td>
<td>PWM4</td>
<td>RO</td>
<td>0x1</td>
<td>PWM4 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the PWM pin 4 is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The <strong>GCNT</strong> field in the <strong>PWMPP</strong> register provides this information.</td>
</tr>
<tr>
<td>3</td>
<td>PWM3</td>
<td>RO</td>
<td>0x1</td>
<td>PWM3 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the PWM pin 3 is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The <strong>GCNT</strong> field in the <strong>PWMPP</strong> register provides this information.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| 2         | PWM2 | RO   | 0x1   | PWM2 Pin Present  
When set, indicates that the PWM pin 2 is present.  
**Note:** The **GCNT** field in the **PWMPP** register provides this information. |
| 1         | PWM1 | RO   | 0x1   | PWM1 Pin Present  
When set, indicates that the PWM pin 1 is present.  
**Note:** The **GCNT** field in the **PWMPP** register provides this information. |
| 0         | PWM0 | RO   | 0x1   | PWM0 Pin Present  
When set, indicates that the PWM pin 0 is present.  
**Note:** The **GCNT** field in the **PWMPP** register provides this information. |
Register 126: Device Capabilities 4 (DC4), offset 0x01C

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC2, SCGC2, DCGC2, and the peripheral-specific RCRC, SCRC, and DRCG registers cannot be set.

**Important:** This register is provided for legacy software support only.

The Peripheral Present registers should be used to determine which modules are implemented on this microcontroller. A read of DC4 correctly identifies if a legacy module is present but software must use the Peripheral Present registers to determine if a module is present that is not supported by the DCn registers.

The peripheral-resident Peripheral Properties registers should be used to determine which pins and features are available on this microcontroller. A read of DC4 correctly identifies if a legacy pin or feature is present. Software must use the Peripheral Properties registers to determine if a pin or feature is present that is not supported by the DCn registers.

### Device Capabilities 4 (DC4)

Base 0x400F.E000
Offset 0x01C
Type RO, reset 0x0004.F1FF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>30</td>
<td>EPHY0</td>
<td>RO</td>
<td>0x0</td>
<td>Ethernet PHY Layer 0 Present When set, indicates that Ethernet PHY layer 0 is present.</td>
</tr>
<tr>
<td>29</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>28</td>
<td>EMAC0</td>
<td>RO</td>
<td>0x0</td>
<td>Ethernet MAC Layer 0 Present When set, indicates that Ethernet MAC layer 0 is present.</td>
</tr>
<tr>
<td>27:25</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>24</td>
<td>E1588</td>
<td>RO</td>
<td>0x0</td>
<td>1588 Capable When set, indicates that Ethernet MAC layer 0 is 1588 capable.</td>
</tr>
</tbody>
</table>
### Description
Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

### PIOSC Calibrate
When set, indicates that the PIOSC can be calibrated by software.

### T3CCP1 Pin Present
When set, indicates that Capture/Compare/PWM pin T3CCP1 is present.

**Note:** The GPTMPP register does not provide this information.

### T3CCP0 Pin Present
When set, indicates that Capture/Compare/PWM pin T3CCP0 is present.

**Note:** The GPTMPP register does not provide this information.

### Micro-DMA Module Present
When set, indicates that the micro-DMA module present.

### Internal Code ROM Present
When set, indicates that internal code ROM is present.

### GPIO Port Present
When set, indicates that GPIO Port is present.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:19</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>with future products, the value of a reserved bit should be preserved across a read-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>modify-write operation.</td>
</tr>
<tr>
<td>18</td>
<td>PICAL</td>
<td>RO</td>
<td>0x1</td>
<td>PIOSC Calibrate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the PIOSC can be calibrated by software.</td>
</tr>
<tr>
<td>17:16</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>with future products, the value of a reserved bit should be preserved across a read-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>modify-write operation.</td>
</tr>
<tr>
<td>15</td>
<td>CCP7</td>
<td>RO</td>
<td>0x1</td>
<td>T3CCP1 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that Capture/Compare/PWM pin T3CCP1 is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The GPTMPP register does not provide this information.</td>
</tr>
<tr>
<td>14</td>
<td>CCP6</td>
<td>RO</td>
<td>0x1</td>
<td>T3CCP0 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that Capture/Compare/PWM pin T3CCP0 is present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The GPTMPP register does not provide this information.</td>
</tr>
<tr>
<td>13</td>
<td>UDMA</td>
<td>RO</td>
<td>0x1</td>
<td>Micro-DMA Module Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the micro-DMA module present.</td>
</tr>
<tr>
<td>12</td>
<td>ROM</td>
<td>RO</td>
<td>0x1</td>
<td>Internal Code ROM Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that internal code ROM is present.</td>
</tr>
<tr>
<td>11:9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>with future products, the value of a reserved bit should be preserved across a read-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>GPIOJ</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port J Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port J is present.</td>
</tr>
<tr>
<td>7</td>
<td>GPIOH</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port H Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port H is present.</td>
</tr>
<tr>
<td>6</td>
<td>GPIOG</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port G Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port G is present.</td>
</tr>
<tr>
<td>5</td>
<td>GPIOF</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port F Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port F is present.</td>
</tr>
<tr>
<td>4</td>
<td>GPIOE</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port E Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port E is present.</td>
</tr>
<tr>
<td>3</td>
<td>GPIOD</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port D Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port D is present.</td>
</tr>
<tr>
<td>2</td>
<td>GPIOC</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port C Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port C is present.</td>
</tr>
<tr>
<td>1</td>
<td>GPIOB</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port B Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port B is present.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>GPIOA</td>
<td>RO</td>
<td>0x1</td>
<td>GPIO Port A Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that GPIO Port A is present.</td>
</tr>
</tbody>
</table>

**System Control**
Register 127: Device Capabilities 5 (DC5), offset 0x020

This register is predefined by the part and can be used to verify PWM features. If any bit is clear in this register, the module is not present.

**Important:** This register is provided for legacy software support only.

The **PWM Peripheral Properties (PWMPP)** register should be used to determine what pins and features are available on PWM modules. A read of this register correctly identifies if a legacy pin or feature is present. Software must use the **PWMPP** register to determine if a pin or feature that is not supported by the **DCn** registers is present.

### Device Capabilities 5 (DC5)

Base 0x400F.E000
Offset 0x020
Type RO, reset 0x0F30.00FF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>27</td>
<td>PWMFAULT3</td>
<td>RO</td>
<td>0x1</td>
<td>PWM Fault 3 Pin Present when set, indicates that the PWM Fault 3 pin is present.</td>
</tr>
<tr>
<td>26</td>
<td>PWMFAULT2</td>
<td>RO</td>
<td>0x1</td>
<td>PWM Fault 2 Pin Present when set, indicates that the PWM Fault 2 pin is present.</td>
</tr>
<tr>
<td>25</td>
<td>PWMFAULT1</td>
<td>RO</td>
<td>0x1</td>
<td>PWM Fault 1 Pin Present when set, indicates that the PWM Fault 1 pin is present.</td>
</tr>
<tr>
<td>24</td>
<td>PWMFAULT0</td>
<td>RO</td>
<td>0x1</td>
<td>PWM Fault 0 Pin Present when set, indicates that the PWM Fault 0 pin is present.</td>
</tr>
<tr>
<td>23:22</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>21</td>
<td>PWMEFLT</td>
<td>RO</td>
<td>0x1</td>
<td>PWM Extended Fault Active when set, indicates that the PWM Extended Fault feature is active.</td>
</tr>
<tr>
<td>20</td>
<td>PWMESSYNC</td>
<td>RO</td>
<td>0x1</td>
<td>PWM Extended SYNC Active when set, indicates that the PWM Extended SYNC feature is active.</td>
</tr>
<tr>
<td>19:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| 7         | PWM7 | RO   | 0x1   | PWM7 Pin Present  
When set, indicates that the PWM pin 7 is present. |
| 6         | PWM6 | RO   | 0x1   | PWM6 Pin Present  
When set, indicates that the PWM pin 6 is present. |
| 5         | PWM5 | RO   | 0x1   | PWM5 Pin Present  
When set, indicates that the PWM pin 5 is present. |
| 4         | PWM4 | RO   | 0x1   | PWM4 Pin Present  
When set, indicates that the PWM pin 4 is present. |
| 3         | PWM3 | RO   | 0x1   | PWM3 Pin Present  
When set, indicates that the PWM pin 3 is present. |
| 2         | PWM2 | RO   | 0x1   | PWM2 Pin Present  
When set, indicates that the PWM pin 2 is present. |
| 1         | PWM1 | RO   | 0x1   | PWM1 Pin Present  
When set, indicates that the PWM pin 1 is present. |
| 0         | PWM0 | RO   | 0x1   | PWM0 Pin Present  
When set, indicates that the PWM pin 0 is present. |
Register 128: Device Capabilities 6 (DC6), offset 0x024

This register is predefined by the part and can be used to verify features. If any bit is clear in this register, the module is not present. The corresponding bit in the RCGC0, SCGC0, and DCGC0 registers cannot be set.

**Important:** This register is provided for legacy software support only.

The **USB Peripheral Properties (USBPP)** register should be used to determine what features are available on the USB module. A read of this register correctly identifies if a legacy feature is present. Software must use the **USBPP** register to determine if a pin or feature that is not supported by the DCn registers is present.

Device Capabilities 6 (DC6)
Base 0x400F.E000
Offset 0x024
Type RO, reset 0x0000.0013

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>USB0PHY</td>
<td>RO</td>
<td>0x1</td>
<td>USB Module 0 PHY Present When set, indicates that the USB module 0 PHY is present.</td>
</tr>
<tr>
<td>3:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1:0</td>
<td>USB0</td>
<td>RO</td>
<td>0x3</td>
<td>USB Module 0 Present This field indicates that USB module 0 is present and specifies its capability.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>sysValue</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>NA</td>
</tr>
<tr>
<td>0x1</td>
<td>DEVICE</td>
</tr>
<tr>
<td>0x2</td>
<td>HOST</td>
</tr>
<tr>
<td>0x3</td>
<td>OTG</td>
</tr>
</tbody>
</table>

USB0 is not present.
USB0 is Device Only.
USB0 is Device or Host.
USB0 is OTG.
**Register 129: Device Capabilities 7 (DC7), offset 0x028**

This register is predefined by the part and can be used to verify μDMA channel features. A 1 indicates the channel is available on this device; a 0 that the channel is only available on other devices in the family. Channels can have multiple assignments, see "Channel Assignments" on page 597 for more information.

**Important:** This register is provided for legacy software support only. The DMACHANS bit field in the DMA Status (DMASTAT) register indicates the number of DMA channels.

---

**Device Capabilities 7 (DC7)**

Base 0x400F.E000  
Offset 0x028  
Type RO, reset 0xFFFF.FFFF

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>reserved</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 31</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 31 is available.</td>
</tr>
<tr>
<td>30</td>
<td>DMACH30</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 30</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 30 is available.</td>
</tr>
<tr>
<td>29</td>
<td>DMACH29</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 29</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 29 is available.</td>
</tr>
<tr>
<td>28</td>
<td>DMACH28</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 28</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 28 is available.</td>
</tr>
<tr>
<td>27</td>
<td>DMACH27</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 27</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 27 is available.</td>
</tr>
<tr>
<td>26</td>
<td>DMACH26</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 26</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 26 is available.</td>
</tr>
<tr>
<td>25</td>
<td>DMACH25</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 25</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 25 is available.</td>
</tr>
<tr>
<td>24</td>
<td>DMACH24</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 24</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 24 is available.</td>
</tr>
<tr>
<td>23</td>
<td>DMACH23</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 23</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 23 is available.</td>
</tr>
<tr>
<td>22</td>
<td>DMACH22</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 22</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 22 is available.</td>
</tr>
</tbody>
</table>

---

Texas Instruments-Production Data

June 12, 2014
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>DMACH21</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 21 When set, indicates μDMA channel 21 is available.</td>
</tr>
<tr>
<td>20</td>
<td>DMACH20</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 20 When set, indicates μDMA channel 20 is available.</td>
</tr>
<tr>
<td>19</td>
<td>DMACH19</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 19 When set, indicates μDMA channel 19 is available.</td>
</tr>
<tr>
<td>18</td>
<td>DMACH18</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 18 When set, indicates μDMA channel 18 is available.</td>
</tr>
<tr>
<td>17</td>
<td>DMACH17</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 17 When set, indicates μDMA channel 17 is available.</td>
</tr>
<tr>
<td>16</td>
<td>DMACH16</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 16 When set, indicates μDMA channel 16 is available.</td>
</tr>
<tr>
<td>15</td>
<td>DMACH15</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 15 When set, indicates μDMA channel 15 is available.</td>
</tr>
<tr>
<td>14</td>
<td>DMACH14</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 14 When set, indicates μDMA channel 14 is available.</td>
</tr>
<tr>
<td>13</td>
<td>DMACH13</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 13 When set, indicates μDMA channel 13 is available.</td>
</tr>
<tr>
<td>12</td>
<td>DMACH12</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 12 When set, indicates μDMA channel 12 is available.</td>
</tr>
<tr>
<td>11</td>
<td>DMACH11</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 11 When set, indicates μDMA channel 11 is available.</td>
</tr>
<tr>
<td>10</td>
<td>DMACH10</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 10 When set, indicates μDMA channel 10 is available.</td>
</tr>
<tr>
<td>9</td>
<td>DMACH9</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 9 When set, indicates μDMA channel 9 is available.</td>
</tr>
<tr>
<td>8</td>
<td>DMACH8</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 8 When set, indicates μDMA channel 8 is available.</td>
</tr>
<tr>
<td>7</td>
<td>DMACH7</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 7 When set, indicates μDMA channel 7 is available.</td>
</tr>
<tr>
<td>6</td>
<td>DMACH6</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 6 When set, indicates μDMA channel 6 is available.</td>
</tr>
<tr>
<td>5</td>
<td>DMACH5</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 5 When set, indicates μDMA channel 5 is available.</td>
</tr>
<tr>
<td>4</td>
<td>DMACH4</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 4 When set, indicates μDMA channel 4 is available.</td>
</tr>
</tbody>
</table>
### DMA Channel Availability

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>DMACH3</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 3 is available.</td>
</tr>
<tr>
<td>2</td>
<td>DMACH2</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 2 is available.</td>
</tr>
<tr>
<td>1</td>
<td>DMACH1</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 1 is available.</td>
</tr>
<tr>
<td>0</td>
<td>DMACH0</td>
<td>RO</td>
<td>0x1</td>
<td>DMA Channel 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates μDMA channel 0 is available.</td>
</tr>
</tbody>
</table>
Register 130: Device Capabilities 8 (DC8), offset 0x02C

This register is predefined by the part and can be used to verify features.

**Important:** This register is provided for legacy software support only.

The ADC Peripheral Properties (ADCPP) register should be used to determine how many input channels are available on the ADC module. A read of this register correctly identifies if legacy channels are present but software must use the ADCPP register to determine if a channel is present that is not supported by the DCn registers.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>ADC1AIN5</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 1 AIN5 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 1 input pin 5 is present.</td>
</tr>
<tr>
<td>20</td>
<td>ADC1AIN4</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 1 AIN4 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 1 input pin 4 is present.</td>
</tr>
<tr>
<td>19</td>
<td>ADC1AIN3</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 1 AIN3 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 1 input pin 3 is present.</td>
</tr>
<tr>
<td>18</td>
<td>ADC1AIN2</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 1 AIN2 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 1 input pin 2 is present.</td>
</tr>
<tr>
<td>17</td>
<td>ADC1AIN1</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 1 AIN1 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 1 input pin 1 is present.</td>
</tr>
<tr>
<td>16</td>
<td>ADC1AIN0</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 1 AIN0 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 1 input pin 0 is present.</td>
</tr>
<tr>
<td>15</td>
<td>ADC0AIN15</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN15 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 15 is present.</td>
</tr>
<tr>
<td>14</td>
<td>ADC0AIN14</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN14 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 14 is present.</td>
</tr>
<tr>
<td>13</td>
<td>ADC0AIN13</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN13 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 13 is present.</td>
</tr>
<tr>
<td>12</td>
<td>ADC0AIN12</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN12 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 12 is present.</td>
</tr>
<tr>
<td>11</td>
<td>ADC0AIN11</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN11 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 11 is present.</td>
</tr>
<tr>
<td>10</td>
<td>ADC0AIN10</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN10 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 10 is present.</td>
</tr>
<tr>
<td>9</td>
<td>ADC0AIN9</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN9 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 9 is present.</td>
</tr>
<tr>
<td>8</td>
<td>ADC0AIN8</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN8 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 8 is present.</td>
</tr>
<tr>
<td>7</td>
<td>ADC0AIN7</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN7 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 7 is present.</td>
</tr>
<tr>
<td>6</td>
<td>ADC0AIN6</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN6 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 6 is present.</td>
</tr>
<tr>
<td>5</td>
<td>ADC0AIN5</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN5 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 5 is present.</td>
</tr>
<tr>
<td>4</td>
<td>ADC0AIN4</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN4 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 4 is present.</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>ADC0AIN3</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN3 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 3 is present.</td>
</tr>
<tr>
<td>2</td>
<td>ADC0AIN2</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN2 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 2 is present.</td>
</tr>
<tr>
<td>1</td>
<td>ADC0AIN1</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN1 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 1 is present.</td>
</tr>
<tr>
<td>0</td>
<td>ADC0AIN0</td>
<td>RO</td>
<td>0x1</td>
<td>ADC Module 0 AIN0 Pin Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 input pin 0 is present.</td>
</tr>
</tbody>
</table>
Register 131: Software Reset Control 0 (SRCR0), offset 0x040

This register allows individual modules to be reset. Writes to this register are masked by the bits in the Device Capabilities 1 (DC1) register.

**Important:** This register is provided for legacy software support only.

The peripheral-specific Software Reset registers (such as SRWD) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this legacy register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as Watchdog 1), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Software Reset Control 0 (SRCR0)
Base 0x400F.E000
Offset 0x040
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 28        | WDT1       | RO   | 0x0   | WDT1 Reset Control  
When this bit is set, Watchdog Timer module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set. |
| 27:26     | reserved   | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 25        | CAN1       | RO   | 0x0   | CAN1 Reset Control  
When this bit is set, CAN module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set. |
| 24        | CAN0       | RO   | 0x0   | CAN0 Reset Control  
When this bit is set, CAN module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set. |
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23:21</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>20</td>
<td>PWM0</td>
<td>RO</td>
<td>0x0</td>
<td>PWM Reset Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, PWM module 0 is reset. All internal data is lost and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the registers are returned to their reset states. This bit must be manually</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>cleared after being set.</td>
</tr>
<tr>
<td>19:18</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>17</td>
<td>ADC1</td>
<td>RO</td>
<td>0x0</td>
<td>ADC1 Reset Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, ADC module 1 is reset. All internal data is lost and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the registers are returned to their reset states. This bit must be manually</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>cleared after being set.</td>
</tr>
<tr>
<td>16</td>
<td>ADC0</td>
<td>RO</td>
<td>0x0</td>
<td>ADC0 Reset Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, ADC module 0 is reset. All internal data is lost and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the registers are returned to their reset states. This bit must be manually</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>cleared after being set.</td>
</tr>
<tr>
<td>15:7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6</td>
<td>HIB</td>
<td>RO</td>
<td>0x0</td>
<td>HIB Reset Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, the Hibernation module is reset. All internal data is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>lost and the registers are returned to their reset states. This bit must be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>manually cleared after being set.</td>
</tr>
<tr>
<td>5:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>WDT0</td>
<td>RO</td>
<td>0x0</td>
<td>WDT0 Reset Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, Watchdog Timer module 0 is reset. All internal data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>is lost and the registers are returned to their reset states. This bit must</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>be manually cleared after being set.</td>
</tr>
<tr>
<td>2:0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 132: Software Reset Control 1 (SRCR1), offset 0x044

This register allows individual modules to be reset. Writes to this register are masked by the bits in the Device Capabilities 2 (DC2) register.

Important: This register is provided for legacy software support only.

The peripheral-specific Software Reset registers (such as SRTIMER) should be used to reset specific peripherals. A write to this register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as TIMER0), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Note that the Software Reset Analog Comparator (SRACMP) register has only one bit to set the analog comparator module. Resetting the module resets all the blocks. If any of the COMPn bits are set, the entire analog comparator module is reset. It is not possible to reset the blocks individually.

Software Reset Control 1 (SRCR1)
Base 0x400F.E000
Offset 0x044
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>31:27</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>26</td>
<td>COMP2</td>
<td>RO</td>
<td>0x0</td>
<td>Analog Comp 2 Reset Control When this bit is set, Analog Comparator module 2 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>25</td>
<td>COMP1</td>
<td>RO</td>
<td>0x0</td>
<td>Analog Comp 1 Reset Control When this bit is set, Analog Comparator module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>------</td>
<td>--------</td>
<td>-------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>COMP0</td>
<td>RO</td>
<td>0x0</td>
<td>Analog Comp 0 Reset Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, Analog Comparator module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:20</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>TIMER3</td>
<td>RO</td>
<td>0x0</td>
<td>Timer 3 Reset Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, General-Purpose Timer module 3 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>TIMER2</td>
<td>RO</td>
<td>0x0</td>
<td>Timer 2 Reset Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, General-Purpose Timer module 2 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>TIMER1</td>
<td>RO</td>
<td>0x0</td>
<td>Timer 1 Reset Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, General-Purpose Timer module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>TIMER0</td>
<td>RO</td>
<td>0x0</td>
<td>Timer 0 Reset Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, General-Purpose Timer module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>I2C1</td>
<td>RO</td>
<td>0x0</td>
<td>I2C1 Reset Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, I2C module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>I2C0</td>
<td>RO</td>
<td>0x0</td>
<td>I2C0 Reset Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, I2C module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:10</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>QEI1</td>
<td>RO</td>
<td>0x0</td>
<td>QEI1 Reset Control</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, QEI module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### System Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>QEIO</td>
<td>RO</td>
<td>0x0</td>
<td>QEIO Reset Control&lt;br&gt;When this bit is set, QEIO module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>SSI1</td>
<td>RO</td>
<td>0x0</td>
<td>SSI1 Reset Control&lt;br&gt;When this bit is set, SSI module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>4</td>
<td>SSI0</td>
<td>RO</td>
<td>0x0</td>
<td>SSI0 Reset Control&lt;br&gt;When this bit is set, SSI module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>UART2</td>
<td>RO</td>
<td>0x0</td>
<td>UART2 Reset Control&lt;br&gt;When this bit is set, UART module 2 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>1</td>
<td>UART1</td>
<td>RO</td>
<td>0x0</td>
<td>UART1 Reset Control&lt;br&gt;When this bit is set, UART module 1 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>0</td>
<td>UART0</td>
<td>RO</td>
<td>0x0</td>
<td>UART0 Reset Control&lt;br&gt;When this bit is set, UART module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
</tbody>
</table>
Register 133: Software Reset Control 2 (SRCR2), offset 0x048

This register allows individual modules to be reset. Writes to this register are masked by the bits in the Device Capabilities 4 (DC4) register.

**Important:** This register is provided for legacy software support only.

The peripheral-specific Software Reset registers (such as SRDMA) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as the μDMA), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

Software Reset Control 2 (SRCR2)

<table>
<thead>
<tr>
<th>Base 0x400F.E000</th>
<th>Offset 0x048</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RO, reset 0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>USB0</td>
<td>RO</td>
<td>0x0</td>
<td>USB0 Reset Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, USB module 0 is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>15:14</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>UDMA</td>
<td>RO</td>
<td>0x0</td>
<td>Micro-DMA Reset Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this bit is set, uDMA module is reset. All internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>12:9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>8</td>
<td>GPIOJ</td>
<td>RO</td>
<td>0x0</td>
<td>Port J Reset Control&lt;br&gt;When this bit is set, Port J module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>7</td>
<td>GPIOH</td>
<td>RO</td>
<td>0x0</td>
<td>Port H Reset Control&lt;br&gt;When this bit is set, Port H module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>6</td>
<td>GPIOG</td>
<td>RO</td>
<td>0x0</td>
<td>Port G Reset Control&lt;br&gt;When this bit is set, Port G module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>5</td>
<td>GPIOF</td>
<td>RO</td>
<td>0x0</td>
<td>Port F Reset Control&lt;br&gt;When this bit is set, Port F module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>4</td>
<td>GPIOE</td>
<td>RO</td>
<td>0x0</td>
<td>Port E Reset Control&lt;br&gt;When this bit is set, Port E module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>3</td>
<td>GPIOD</td>
<td>RO</td>
<td>0x0</td>
<td>Port D Reset Control&lt;br&gt;When this bit is set, Port D module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>2</td>
<td>GPIOC</td>
<td>RO</td>
<td>0x0</td>
<td>Port C Reset Control&lt;br&gt;When this bit is set, Port C module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>1</td>
<td>GPIOB</td>
<td>RO</td>
<td>0x0</td>
<td>Port B Reset Control&lt;br&gt;When this bit is set, Port B module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
<tr>
<td>0</td>
<td>GPIOA</td>
<td>RO</td>
<td>0x0</td>
<td>Port A Reset Control&lt;br&gt;When this bit is set, Port A module is reset. All</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internal data is lost and the registers are returned to their reset states. This bit must be manually cleared after being set.</td>
</tr>
</tbody>
</table>
Register 134: Run Mode Clock Gating Control Register 0 (RCGC0), offset 0x100

This register controls the clock gating logic in normal Run mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. RCGC0 is the clock configuration register for running operation, SCGC0 for Sleep operation, and DCGC0 for Deep-Sleep operation. Setting the ACG bit in the Run-Mode Clock Configuration (RCC) register specifies that the system uses sleep modes. Note that there must be a delay of 3 system clocks after a module clock is enabled before any registers in that module are accessed.

Important: This register is provided for legacy software support only.

The peripheral-specific Run Mode Clock Gating Control registers (such as RCGCWD) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as Watchdog 1), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Likewise, the ADC Peripheral Configuration (ADCPH) register should be used to configure the ADC sample rate. However, to support legacy software, the MAXADCnSPD fields are available. A write to these legacy fields also writes the corresponding field in the peripheral-specific register. If a field is changed by writing to this register, it can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support rates that are not available in this register. If software uses a peripheral-specific register to set the ADC rate, the write causes proper operation, but the value of that field is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.
Run Mode Clock Gating Control Register 0 (RCGC0)

Base 0x400F.E000
Offset 0x100
Type RO, reset 0x0000.0040

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>28</td>
<td>WDT1</td>
<td>RO</td>
<td>0x0</td>
<td>WDT1 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for the Watchdog Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>27:26</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>25</td>
<td>CAN1</td>
<td>RO</td>
<td>0x0</td>
<td>CAN1 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for CAN module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>24</td>
<td>CAN0</td>
<td>RO</td>
<td>0x0</td>
<td>CAN0 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for CAN module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>23:21</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>20</td>
<td>PWM0</td>
<td>RO</td>
<td>0x0</td>
<td>PWM Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for the PWM module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
</tbody>
</table>
| 19:18     | reserved      | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 17        | ADC1        | RO   | 0x0   | ADC1 Clock Gating Control
This bit controls the clock gating for SAR ADC module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 16        | ADC0        | RO   | 0x0   | ADC0 Clock Gating Control
This bit controls the clock gating for ADC module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 15:12     | reserved    | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 11:10     | MAXADC1SPD  | RO   | 0x0   | ADC1 Sample Speed
This field sets the rate at which ADC module 1 samples data. You cannot set the rate higher than the maximum rate. You can set the sample rate by setting the MAXADC1SPD bit as follows (all other encodings are reserved): |
|           |             |      |       | **Value** | **Description** |
|           |             |      |       | 0x0  | 125K samples/second |
|           |             |      |       | 0x1  | 250K samples/second |
|           |             |      |       | 0x2  | 500K samples/second |
|           |             |      |       | 0x3  | 1M samples/second |
| 9:8       | MAXADC0SPD  | RO   | 0x0   | ADC0 Sample Speed
This field sets the rate at which ADC0 samples data. You cannot set the rate higher than the maximum rate. You can set the sample rate by setting the MAXADC0SPD bit as follows (all other encodings are reserved): |
|           |             |      |       | **Value** | **Description** |
|           |             |      |       | 0x0  | 125K samples/second |
|           |             |      |       | 0x1  | 250K samples/second |
|           |             |      |       | 0x2  | 500K samples/second |
|           |             |      |       | 0x3  | 1M samples/second |
| 7         | reserved    | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 6         | HIB         | RO   | 0x1   | HIB Clock Gating Control
This bit controls the clock gating for the Hibernation module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
<p>| 5:4       | reserved    | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |</p>
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 3        | WDT0    | RO   | 0x0   | WDT0 Clock Gating Control  
This bit controls the clock gating for the Watchdog Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 2:0      | reserved| RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
Register 135: Run Mode Clock Gating Control Register 1 (RCGC1), offset 0x104

This register controls the clock gating logic in normal Run mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. RCGC1 is the clock configuration register for running operation, SCGC1 for Sleep operation, and DCGC1 for Deep-Sleep operation. Setting the ACG bit in the Run-Mode Clock Configuration (RCC) register specifies that the system uses sleep modes. Note that there must be a delay of 3 system clocks after a module clock is enabled before any registers in that module are accessed.

Important: This register is provided for legacy software support only.

The peripheral-specific Run Mode Clock Gating Control registers (such as RCGCTIMER) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as Timer 0), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Run Mode Clock Gating Control Register 1 (RCGC1)

Base 0x400F.E000
Offset 0x104
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
</tr>
<tr>
<td>----------</td>
<td>---------</td>
<td>------</td>
</tr>
<tr>
<td>26</td>
<td>COMP2</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>COMP1</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>COMP0</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:20</td>
<td>reserved</td>
<td>RO</td>
</tr>
<tr>
<td>19</td>
<td>TIMER3</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>TIMER2</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>TIMER1</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>TIMER0</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>reserved</td>
<td>RO</td>
</tr>
<tr>
<td>14</td>
<td>I2C1</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
</tr>
<tr>
<td>----------</td>
<td>-------------</td>
<td>------</td>
</tr>
<tr>
<td>13</td>
<td>reserved</td>
<td>RO</td>
</tr>
<tr>
<td>12</td>
<td>I2C0</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:10</td>
<td>reserved</td>
<td>RO</td>
</tr>
<tr>
<td>9</td>
<td>QEI1</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>QEI0</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
</tr>
<tr>
<td>5</td>
<td>SSI1</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SSI0</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>reserved</td>
<td>RO</td>
</tr>
<tr>
<td>2</td>
<td>UART2</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>UART1</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
</tr>
</tbody>
</table>
| 0         | UART0 | RO   | 0x0   | UART0 Clock Gating Control |}

This bit controls the clock gating for UART module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
Register 136: Run Mode Clock Gating Control Register 2 (RCGC2), offset 0x108

This register controls the clock gating logic in normal Run mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC2** is the clock configuration register for running operation, **SCGC2** for Sleep operation, and **DCGC2** for Deep-Sleep operation. Setting the **ACG** bit in the **Run-Mode Clock Configuration (RCC)** register specifies that the system uses sleep modes. Note that there must be a delay of 3 system clocks after a module clock is enabled before any registers in that module are accessed.

**Important:** This register is provided for legacy software support only.

The peripheral-specific Run Mode Clock Gating Control registers (such as **RCGCDMA**) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as the μDMA), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

**Run Mode Clock Gating Control Register 2 (RCGC2)**

Base 0x400F.E000
Offset 0x108
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td></td>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
## System Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>USB0</td>
<td>RO</td>
<td>0x0</td>
<td>USB0 Clock Gating Control&lt;br&gt;This bit controls the clock gating for USB module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>15:14</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>UDMA</td>
<td>RO</td>
<td>0x0</td>
<td>Micro-DMA Clock Gating Control&lt;br&gt;This bit controls the clock gating for micro-DMA. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>12:9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>GPIOJ</td>
<td>RO</td>
<td>0x0</td>
<td>Port J Clock Gating Control&lt;br&gt;This bit controls the clock gating for Port J. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>7</td>
<td>GPIOH</td>
<td>RO</td>
<td>0x0</td>
<td>Port H Clock Gating Control&lt;br&gt;This bit controls the clock gating for Port H. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>6</td>
<td>GPIOG</td>
<td>RO</td>
<td>0x0</td>
<td>Port G Clock Gating Control&lt;br&gt;This bit controls the clock gating for Port G. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>5</td>
<td>GPIOF</td>
<td>RO</td>
<td>0x0</td>
<td>Port F Clock Gating Control&lt;br&gt;This bit controls the clock gating for Port F. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>4</td>
<td>GPIOE</td>
<td>RO</td>
<td>0x0</td>
<td>Port E Clock Gating Control&lt;br&gt;Port E Clock Gating Control. This bit controls the clock gating for Port E. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>3</td>
<td>GPIOD</td>
<td>RO</td>
<td>0x0</td>
<td>Port D Clock Gating Control&lt;br&gt;Port D Clock Gating Control. This bit controls the clock gating for Port D. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>2</td>
<td>GPIOC</td>
<td>RO</td>
<td>0x0</td>
<td>Port C Clock Gating Control&lt;br&gt;This bit controls the clock gating for Port C. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>1</td>
<td>GPIOB</td>
<td>RO</td>
<td>0x0</td>
<td>Port B Clock Gating Control&lt;br&gt;This bit controls the clock gating for Port B. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>0</td>
<td>GPIOA</td>
<td>RO</td>
<td>0x0</td>
<td>Port A Clock Gating Control&lt;br&gt;This bit controls the clock gating for Port A. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
</tbody>
</table>
Register 137: Sleep Mode Clock Gating Control Register 0 (SCGC0), offset 0x110

This register controls the clock gating logic in Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC0** is the clock configuration register for running operation, **SCGC0** for Sleep operation, and **DCGC0** for Deep-Sleep operation. Setting the **ACG** bit in the Run-Mode Clock Configuration (RCC) register specifies that the system uses sleep modes.

**Important:** This register is provided for legacy software support only.

The peripheral-specific Sleep Mode Clock Gating Control registers (such as **SCGCWD**) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as Watchdog 1), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

Sleep Mode Clock Gating Control Register 0 (SCGC0)
Base 0x400F.E000
Offset 0x110
Type RO, reset 0x0000.0040

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 28        | WDT1         | RO   | 0x0   | WDT1 Clock Gating Control
This bit controls the clock gating for Watchdog Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unlocked, a read or write to the module generates a bus fault. |
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>27:26</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>25</td>
<td>CAN1</td>
<td>RO</td>
<td>0x0</td>
<td>CAN1 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for CAN module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>24</td>
<td>CAN0</td>
<td>RO</td>
<td>0x0</td>
<td>CAN0 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for CAN module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>23:21</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>20</td>
<td>PWM0</td>
<td>RO</td>
<td>0x0</td>
<td>PWM Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for the PWM module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>19:18</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>17</td>
<td>ADC1</td>
<td>RO</td>
<td>0x0</td>
<td>ADC1 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for ADC module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>16</td>
<td>ADC0</td>
<td>RO</td>
<td>0x0</td>
<td>ADC0 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for ADC module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>15:7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6</td>
<td>HIB</td>
<td>RO</td>
<td>0x1</td>
<td>HIB Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for the Hibernation module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>5:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>3</td>
<td>WDT0</td>
<td>RO</td>
<td>0x0</td>
<td>WDT0 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for the Watchdog Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>2:0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 138: Sleep Mode Clock Gating Control Register 1 (SCGC1), offset 0x114

This register controls the clock gating logic in Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. RCuGC1 is the clock configuration register for running operation, SCGC1 for Sleep operation, and DCGC1 for Deep-Sleep operation. Setting the ACG bit in the Run-Mode Clock Configuration (RCC) register specifies that the system uses sleep modes.

Important: This register is provided for legacy software support only.

The peripheral-specific Sleep Mode Clock Gating Control registers (such as SCGCTIMER) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as Timer 0), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Sleep Mode Clock Gating Control Register 1 (SCGC1)

**Base:** 0x400F.E000  
**Offset:** 0x114  
**Type:** RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
</tbody>
</table>

**Bit/Field**  | **Name**  | **Type**  | **Reset**  | **Description**  
--- | --- | --- | --- | ---  
31:27 | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.  
26 | COMP2 | RO | 0x0 | Analog Comparator 2 Clock Gating  
This bit controls the clock gating for analog comparator 2. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>COMP1</td>
<td>RO</td>
<td>0x0</td>
<td>Analog Comparator 1 Clock Gating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for analog comparator 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>24</td>
<td>COMP0</td>
<td>RO</td>
<td>0x0</td>
<td>Analog Comparator 0 Clock Gating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for analog comparator 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>23:20</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19</td>
<td>TIMER3</td>
<td>RO</td>
<td>0x0</td>
<td>Timer 3 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for General-Purpose Timer module 3. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>18</td>
<td>TIMER2</td>
<td>RO</td>
<td>0x0</td>
<td>Timer 2 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for General-Purpose Timer module 2. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>17</td>
<td>TIMER1</td>
<td>RO</td>
<td>0x0</td>
<td>Timer 1 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for General-Purpose Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>16</td>
<td>TIMER0</td>
<td>RO</td>
<td>0x0</td>
<td>Timer 0 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for General-Purpose Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>15</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>14</td>
<td>I2C1</td>
<td>RO</td>
<td>0x0</td>
<td>I2C1 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for I2C module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>13</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| 12        | I2C0   | RO   | 0x0   | I2C0 Clock Gating Control  
This bit controls the clock gating for I2C module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 11:10     | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 9         | QEI1   | RO   | 0x0   | QEI1 Clock Gating Control  
This bit controls the clock gating for QEI module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 8         | QEI0   | RO   | 0x0   | QEI0 Clock Gating Control  
This bit controls the clock gating for QEI module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 7:6       | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 5         | SSI1   | RO   | 0x0   | SSI1 Clock Gating Control  
This bit controls the clock gating for SSI module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 4         | SSI0   | RO   | 0x0   | SSI0 Clock Gating Control  
This bit controls the clock gating for SSI module 0. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 3         | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 2         | UART2  | RO   | 0x0   | UART2 Clock Gating Control  
This bit controls the clock gating for UART module 2. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 1         | UART1  | RO   | 0x0   | UART1 Clock Gating Control  
This bit controls the clock gating for UART module 1. If set, the module receives a clock and functions. Otherwise, the module is unlocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>UART0</td>
<td>RO</td>
<td>0x0</td>
<td>UART0 Clock Gating Control</td>
</tr>
</tbody>
</table>

This bit controls the clock gating for UART module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
Register 139: Sleep Mode Clock Gating Control Register 2 (SCGC2), offset 0x118

This register controls the clock gating logic in Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. RCGC2 is the clock configuration register for running operation, SCGC2 for Sleep operation, and DCGC2 for Deep-Sleep operation. Setting the ACG bit in the Run-Mode Clock Configuration (RCC) register specifies that the system uses sleep modes.

**Important:** This register is provided for legacy software support only.

The peripheral-specific Sleep Mode Clock Gating Control registers (such as SCGCDMA) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as the μDMA), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

### Sleep Mode Clock Gating Control Register 2 (SCGC2)

Base 0x400F.E000  
Offset 0x118  
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>USB0</td>
<td>RO</td>
<td>0x0</td>
<td>USB0 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for USB module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>---------------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>15:14</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>UDMA</td>
<td>RO</td>
<td>0x0</td>
<td>Micro-DMA Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for micro-DMA. If set, the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>receives a clock and functions. Otherwise, the module is unclocked and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>disabled. If the module is unclocked, a read or write to the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>generates a bus fault.</td>
</tr>
<tr>
<td>12:9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>GPIOJ</td>
<td>RO</td>
<td>0x0</td>
<td>Port J Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for Port J. If set, the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>receives a clock and functions. Otherwise, the module is unclocked and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>disabled. If the module is unclocked, a read or write to the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>generates a bus fault.</td>
</tr>
<tr>
<td>7</td>
<td>GPIOH</td>
<td>RO</td>
<td>0x0</td>
<td>Port H Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for Port H. If set, the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>receives a clock and functions. Otherwise, the module is unclocked and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>disabled. If the module is unclocked, a read or write to the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>generates a bus fault.</td>
</tr>
<tr>
<td>6</td>
<td>GPIOG</td>
<td>RO</td>
<td>0x0</td>
<td>Port G Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for Port G. If set, the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>receives a clock and functions. Otherwise, the module is unclocked and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>disabled. If the module is unclocked, a read or write to the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>generates a bus fault.</td>
</tr>
<tr>
<td>5</td>
<td>GPIOF</td>
<td>RO</td>
<td>0x0</td>
<td>Port F Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for Port F. If set, the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>receives a clock and functions. Otherwise, the module is unclocked and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>disabled. If the module is unclocked, a read or write to the module</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>generates a bus fault.</td>
</tr>
<tr>
<td>4</td>
<td>GPIOE</td>
<td>RO</td>
<td>0x0</td>
<td>Port E Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Port E Clock Gating Control. This bit controls the clock gating for Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>E. If set, the module receives a clock and functions. Otherwise, the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>module is unclocked and disabled. If the module is unclocked, a read or</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>write to the module generates a bus fault.</td>
</tr>
<tr>
<td>3</td>
<td>GPIOD</td>
<td>RO</td>
<td>0x0</td>
<td>Port D Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Port D Clock Gating Control. This bit controls the clock gating for Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D. If set, the module receives a clock and functions. Otherwise, the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>module is unclocked and disabled. If the module is unclocked, a read or</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>write to the module generates a bus fault.</td>
</tr>
<tr>
<td>2</td>
<td>GPIOC</td>
<td>RO</td>
<td>0x0</td>
<td>Port C Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Port C Clock Gating Control. This bit controls the clock gating for Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C. If set, the module receives a clock and functions. Otherwise, the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>module is unclocked and disabled. If the module is unclocked, a read or</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>write to the module generates a bus fault.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>GPIOB</td>
<td>RO</td>
<td>0x0</td>
<td>Port B Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for Port B. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>0</td>
<td>GPIOA</td>
<td>RO</td>
<td>0x0</td>
<td>Port A Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for Port A. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
</tbody>
</table>
**Register 140: Deep Sleep Mode Clock Gating Control Register 0 (DCGC0), offset 0x120**

This register controls the clock gating logic in Deep-Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. **RCGC0** is the clock configuration register for running operation, **SCGC0** for Sleep operation, and **DCGC0** for Deep-Sleep operation. Setting the ACG bit in the Run-Mode Clock Configuration (RCC) register specifies that the system uses sleep modes.

**Important:** This register is provided for legacy software support only.

The peripheral-specific Deep Sleep Mode Clock Gating Control registers (such as **DCGCWD**) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as Watchdog 1), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

---

**Deep Sleep Mode Clock Gating Control Register 0 (DCGC0)**

<table>
<thead>
<tr>
<th>Base 0x400F.E000 Offset 0x120 Type RO, reset 0x0000.0040</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:29</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>28</td>
<td>WDT1</td>
<td>RO</td>
<td>0x0</td>
<td>WDT1 Clock Gating Control</td>
</tr>
</tbody>
</table>

This bit controls the clock gating for the Watchdog Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>27:26</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>25</td>
<td>CAN1</td>
<td>RO</td>
<td>0x0</td>
<td>CAN1 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for CAN module 1. If set, the module receives a clock and functions. Otherwise, the module is uncleked and disabled. If the module is uncleked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>24</td>
<td>CAN0</td>
<td>RO</td>
<td>0x0</td>
<td>CAN0 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for CAN module 0. If set, the module receives a clock and functions. Otherwise, the module is uncleked and disabled. If the module is uncleked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>23:21</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>20</td>
<td>PWM0</td>
<td>RO</td>
<td>0x0</td>
<td>PWM Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for the PWM module. If set, the module receives a clock and functions. Otherwise, the module is uncleked and disabled. If the module is uncleked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>19:18</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>17</td>
<td>ADC1</td>
<td>RO</td>
<td>0x0</td>
<td>ADC1 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for ADC module 1. If set, the module receives a clock and functions. Otherwise, the module is uncleked and disabled. If the module is uncleked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>16</td>
<td>ADC0</td>
<td>RO</td>
<td>0x0</td>
<td>ADC0 Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for ADC module 0. If set, the module receives a clock and functions. Otherwise, the module is uncleked and disabled. If the module is uncleked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>15:7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6</td>
<td>HIB</td>
<td>RO</td>
<td>0x1</td>
<td>HIB Clock Gating Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for the Hibernation module. If set, the module receives a clock and functions. Otherwise, the module is uncleked and disabled. If the module is uncleked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>5:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>3</td>
<td>WDT0</td>
<td>RO</td>
<td>0x0</td>
<td>WDT0 Clock Gating Control This bit controls the clock gating for the Watchdog Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>2:0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 141: Deep-Sleep Mode Clock Gating Control Register 1 (DCGC1), offset 0x124

This register controls the clock gating logic in Deep-Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. 

RCGC1 is the clock configuration register for running operation, SCGC1 for Sleep operation, and DCGC1 for Deep-Sleep operation. Setting the ACG bit in the Run-Mode Clock Configuration (RCC) register specifies that the system uses sleep modes.

Important: This register is provided for legacy software support only.

The peripheral-specific Deep Sleep Mode Clock Gating Control registers (such as DCGCTIMER) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as Timer 0), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Deep-Sleep Mode Clock Gating Control Register 1 (DCGC1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Type</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>26</td>
<td>COMP2</td>
<td>RO</td>
<td>0x0</td>
<td>Analog Comparator 2 Clock Gating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the clock gating for analog comparator 2. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.</td>
</tr>
</tbody>
</table>
## System Control

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 25        | COMP1   | RO   | 0x0   | Analog Comparator 1 Clock Gating  
This bit controls the clock gating for analog comparator 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 24        | COMP0   | RO   | 0x0   | Analog Comparator 0 Clock Gating  
This bit controls the clock gating for analog comparator 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 23:20     | reserved| RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 19        | TIMER3  | RO   | 0x0   | Timer 3 Clock Gating Control  
This bit controls the clock gating for General-Purpose Timer module 3. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 18        | TIMER2  | RO   | 0x0   | Timer 2 Clock Gating Control  
This bit controls the clock gating for General-Purpose Timer module 2. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 17        | TIMER1  | RO   | 0x0   | Timer 1 Clock Gating Control  
This bit controls the clock gating for General-Purpose Timer module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 16        | TIMER0  | RO   | 0x0   | Timer 0 Clock Gating Control  
This bit controls the clock gating for General-Purpose Timer module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 15        | reserved| RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 14        | I2C1    | RO   | 0x0   | I2C1 Clock Gating Control  
This bit controls the clock gating for I2C module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
<p>| 13        | reserved| RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |</p>
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 12        | I2C0   | RO   | 0x0   | I2C0 Clock Gating Control  
This bit controls the clock gating for I2C module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 11:10     | reserved | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 9         | QEI1   | RO   | 0x0   | QEI1 Clock Gating Control  
This bit controls the clock gating for QEI module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 8         | QEI0   | RO   | 0x0   | QEI0 Clock Gating Control  
This bit controls the clock gating for QEI module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 7:6       | reserved | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 5         | SSI1   | RO   | 0x0   | SSI1 Clock Gating Control  
This bit controls the clock gating for SSI module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 4         | SSI0   | RO   | 0x0   | SSI0 Clock Gating Control  
This bit controls the clock gating for SSI module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 3         | reserved | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 2         | UART2  | RO   | 0x0   | UART2 Clock Gating Control  
This bit controls the clock gating for UART module 2. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 1         | UART1  | RO   | 0x0   | UART1 Clock Gating Control  
This bit controls the clock gating for UART module 1. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
## UART0 Clock Gating Control

This bit controls the clock gating for UART module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>UART0</td>
<td>RO</td>
<td>0x0</td>
<td>UART0 Clock Gating Control</td>
</tr>
</tbody>
</table>
Register 142: Deep Sleep Mode Clock Gating Control Register 2 (DCGC2), offset 0x128

This register controls the clock gating logic in Deep-Sleep mode. Each bit controls a clock enable for a given interface, function, or module. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled (saving power). If the module is unclocked, reads or writes to the module generate a bus fault. The reset state of these bits is 0 (unclocked) unless otherwise noted, so that all functional modules are disabled. It is the responsibility of software to enable the ports necessary for the application. Note that these registers may contain more bits than there are interfaces, functions, or modules to control. This configuration is implemented to assure reasonable code compatibility with other family and future parts. RCGC2 is the clock configuration register for running operation, SCGC2 for Sleep operation, and DCGC2 for Deep-Sleep operation. Setting the ACG bit in the Run-Mode Clock Configuration (RCC) register specifies that the system uses sleep modes.

Important: This register is provided for legacy software support only.

The peripheral-specific Deep Sleep Mode Clock Gating Control registers (such as DCGCDMA) should be used to reset specific peripherals. A write to this legacy register also writes the corresponding bit in the peripheral-specific register. Any bits that are changed by writing to this register can be read back correctly with a read of this register. Software must use the peripheral-specific registers to support modules that are not present in the legacy registers. If software uses a peripheral-specific register to write a legacy peripheral (such as the μDMA), the write causes proper operation, but the value of that bit is not reflected in this register. If software uses both legacy and peripheral-specific register accesses, the peripheral-specific registers must be accessed by read-modify-write operations that affect only peripherals that are not present in the legacy registers. In this manner, both the peripheral-specific and legacy registers have coherent information.

Deep Sleep Mode Clock Gating Control Register 2 (DCGC2)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-17</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 16   | USB0          | RO   | 0x0   | USB0 Clock Gating Control
This bit controls the clock gating for USB module 0. If set, the module receives a clock and functions. Otherwise, the module is unclocked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:14</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>UDMA</td>
<td>RO</td>
<td>0x0</td>
<td>Micro-DMA Clock Gating Control This bit controls the clock gating for micro-DMA. If set, the module receives a clock and functions. Otherwise, the module is uncleared and disabled. If the module is uncleared, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>12:9</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>GPIOJ</td>
<td>RO</td>
<td>0x0</td>
<td>Port J Clock Gating Control This bit controls the clock gating for Port J. If set, the module receives a clock and functions. Otherwise, the module is uncleared and disabled. If the module is uncleared, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>7</td>
<td>GPIOH</td>
<td>RO</td>
<td>0x0</td>
<td>Port H Clock Gating Control This bit controls the clock gating for Port H. If set, the module receives a clock and functions. Otherwise, the module is uncleared and disabled. If the module is uncleared, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>6</td>
<td>GPIOG</td>
<td>RO</td>
<td>0x0</td>
<td>Port G Clock Gating Control This bit controls the clock gating for Port G. If set, the module receives a clock and functions. Otherwise, the module is uncleared and disabled. If the module is uncleared, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>5</td>
<td>GPIOF</td>
<td>RO</td>
<td>0x0</td>
<td>Port F Clock Gating Control This bit controls the clock gating for Port F. If set, the module receives a clock and functions. Otherwise, the module is uncleared and disabled. If the module is uncleared, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>4</td>
<td>GPIOE</td>
<td>RO</td>
<td>0x0</td>
<td>Port E Clock Gating Control Port E Clock Gating Control. This bit controls the clock gating for Port E. If set, the module receives a clock and functions. Otherwise, the module is uncleared and disabled. If the module is uncleared, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>3</td>
<td>GPIOD</td>
<td>RO</td>
<td>0x0</td>
<td>Port D Clock Gating Control Port D Clock Gating Control. This bit controls the clock gating for Port D. If set, the module receives a clock and functions. Otherwise, the module is uncleared and disabled. If the module is uncleared, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>2</td>
<td>GPIOC</td>
<td>RO</td>
<td>0x0</td>
<td>Port C Clock Gating Control This bit controls the clock gating for Port C. If set, the module receives a clock and functions. Otherwise, the module is uncleared and disabled. If the module is uncleared, a read or write to the module generates a bus fault.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>----------------------------------------------------------------------------</td>
</tr>
</tbody>
</table>
| 1        | GPIOB | RO   | 0x0   | Port B Clock Gating Control  
This bit controls the clock gating for Port B. If set, the module receives a clock and functions. Otherwise, the module is unclecked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
| 0        | GPIOA | RO   | 0x0   | Port A Clock Gating Control  
This bit controls the clock gating for Port A. If set, the module receives a clock and functions. Otherwise, the module is unclecked and disabled. If the module is unclocked, a read or write to the module generates a bus fault. |
Register 143: Device Capabilities 9 (DC9), offset 0x190

This register is predefined by the part and can be used to verify ADC digital comparator features.

**Important:** This register is provided for legacy software support only. The ADC Peripheral Properties (ADCPP) register should be used to determine how many digital comparators are available on the ADC module. A read of this register correctly identifies if legacy comparators are present. Software must use the ADCPP register to determine if a comparator that is not supported by the DCn registers is present.

### Device Capabilities 9 (DC9)

Base 0x400F.E000
Offset 0x190
Type RO, reset 0x00FF.00FF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23</td>
<td>ADC1DC7</td>
<td>RO</td>
<td>0x1</td>
<td>ADC1 DC7 Present When set, indicates that ADC module 1 Digital Comparator 7 is present.</td>
</tr>
<tr>
<td>22</td>
<td>ADC1DC6</td>
<td>RO</td>
<td>0x1</td>
<td>ADC1 DC6 Present When set, indicates that ADC module 1 Digital Comparator 6 is present.</td>
</tr>
<tr>
<td>21</td>
<td>ADC1DC5</td>
<td>RO</td>
<td>0x1</td>
<td>ADC1 DC5 Present When set, indicates that ADC module 1 Digital Comparator 5 is present.</td>
</tr>
<tr>
<td>20</td>
<td>ADC1DC4</td>
<td>RO</td>
<td>0x1</td>
<td>ADC1 DC4 Present When set, indicates that ADC module 1 Digital Comparator 4 is present.</td>
</tr>
<tr>
<td>19</td>
<td>ADC1DC3</td>
<td>RO</td>
<td>0x1</td>
<td>ADC1 DC3 Present When set, indicates that ADC module 1 Digital Comparator 3 is present.</td>
</tr>
<tr>
<td>18</td>
<td>ADC1DC2</td>
<td>RO</td>
<td>0x1</td>
<td>ADC1 DC2 Present When set, indicates that ADC module 1 Digital Comparator 2 is present.</td>
</tr>
<tr>
<td>17</td>
<td>ADC1DC1</td>
<td>RO</td>
<td>0x1</td>
<td>ADC1 DC1 Present When set, indicates that ADC module 1 Digital Comparator 1 is present.</td>
</tr>
<tr>
<td>16</td>
<td>ADC1DC0</td>
<td>RO</td>
<td>0x1</td>
<td>ADC1 DC0 Present When set, indicates that ADC module 1 Digital Comparator 0 is present.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>ADC0DC7</td>
<td>RO</td>
<td>0x1</td>
<td>ADC0 DC7 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 Digital Comparator 7 is present.</td>
</tr>
<tr>
<td>6</td>
<td>ADC0DC6</td>
<td>RO</td>
<td>0x1</td>
<td>ADC0 DC6 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 Digital Comparator 6 is present.</td>
</tr>
<tr>
<td>5</td>
<td>ADC0DC5</td>
<td>RO</td>
<td>0x1</td>
<td>ADC0 DC5 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 Digital Comparator 5 is present.</td>
</tr>
<tr>
<td>4</td>
<td>ADC0DC4</td>
<td>RO</td>
<td>0x1</td>
<td>ADC0 DC4 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 Digital Comparator 4 is present.</td>
</tr>
<tr>
<td>3</td>
<td>ADC0DC3</td>
<td>RO</td>
<td>0x1</td>
<td>ADC0 DC3 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 Digital Comparator 3 is present.</td>
</tr>
<tr>
<td>2</td>
<td>ADC0DC2</td>
<td>RO</td>
<td>0x1</td>
<td>ADC0 DC2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 Digital Comparator 2 is present.</td>
</tr>
<tr>
<td>1</td>
<td>ADC0DC1</td>
<td>RO</td>
<td>0x1</td>
<td>ADC0 DC1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 Digital Comparator 1 is present.</td>
</tr>
<tr>
<td>0</td>
<td>ADC0DC0</td>
<td>RO</td>
<td>0x1</td>
<td>ADC0 DC0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that ADC module 0 Digital Comparator 0 is present.</td>
</tr>
</tbody>
</table>
Register 144: Non-Volatile Memory Information (NVMSTAT), offset 0x1A0

This register is predefined by the part and can be used to verify features.

**Important:** This register is provided for legacy software support only.

The **ROM Third-Party Software (ROMSWMAP)** register should be used to determine the presence of third-party software in the on-chip ROM on this microcontroller. A read of the **TPSW** bit in this register correctly identifies the presence of legacy third-party software. Software should use the **ROMSWMAP** register for software that is not on legacy devices.

---

### Non-Volatile Memory Information (NVMSTAT)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x400F.E000</td>
<td>0x1A0</td>
<td>RO</td>
<td>0x0000.0001</td>
<td></td>
</tr>
</tbody>
</table>

#### Bit/Field  Name      Type  Reset  Description

- 31:1  reserved  RO  0  Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
- 0  FWB  RO  0x1  32 Word Flash Write Buffer Available
  When set, indicates that the 32 word Flash memory write buffer feature is available.
6 System Exception Module

This module is an AHB peripheral that handles system-level Cortex-M4 FPU exceptions. For functions with registers mapped into this aperture, if the function is not available on a device, then all writes to the associated registers are ignored and reads return zeros.

6.1 Functional Description

The System Exception module provides control and status of the system-level interrupts. All the interrupt events are ORed together before being sent to the interrupt controller, so the System Exception module can only generate a single interrupt request to the controller at any given time. Software can service multiple interrupt events in a single interrupt service routine by reading the System Exception Masked Interrupt Status (SYSEXCMIS) register. The interrupt events that can trigger a controller-level interrupt are defined in the System Exception Interrupt Mask (SYSEXCIM) register by setting the corresponding interrupt mask bits. If interrupts are not used, the raw interrupt status is always visible via the System Exception Raw Interrupt Status (SYSEXCRIS) register. Interrupts are always cleared (for both the SYSEXCMIS and SYSEXCRIS registers) by writing a 1 to the corresponding bit in the System Exception Interrupt Clear (SYSEXCIC) register.

6.2 Register Map

Table 6-1 on page 495 lists the System Exception module registers. The offset listed is a hexadecimal increment to the register's address, relative to the System Exception base address of 0x400F.9000.

Note: Spaces in the System Exception register space that are not used are reserved for future or internal use. Software should not modify any reserved memory address.

Table 6-1. System Exception Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>SYSEXCRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>System Exception Raw Interrupt Status</td>
<td>496</td>
</tr>
<tr>
<td>0x004</td>
<td>SYSEXCIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>System Exception Interrupt Mask</td>
<td>498</td>
</tr>
<tr>
<td>0x008</td>
<td>SYSEXCMIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>System Exception Masked Interrupt Status</td>
<td>500</td>
</tr>
<tr>
<td>0x00C</td>
<td>SYSEXCIC</td>
<td>W1C</td>
<td>0x0000.0000</td>
<td>System Exception Interrupt Clear</td>
<td>502</td>
</tr>
</tbody>
</table>

6.3 Register Descriptions

All addresses given are relative to the System Exception base address of 0x400F.9000.
Register 1: System Exception Raw Interrupt Status (SYSEXCRIS), offset 0x000

The **SYSEXCRIS** register is the raw interrupt status register. On a read, this register gives the current raw status value of the corresponding interrupt. A write has no effect.

### System Exception Raw Interrupt Status (SYSEXCRIS)

<table>
<thead>
<tr>
<th>Base</th>
<th>0x400F.9000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset</td>
<td>0x0000</td>
</tr>
<tr>
<td>Type RO</td>
<td>reset 0x0000.0000</td>
</tr>
</tbody>
</table>

#### Bit/Field | Name             | Type | Reset   | Description                                                                 |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>FPIXCRIS</td>
<td>RO</td>
<td>0</td>
<td>Floating-Point Inexact Exception Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A floating-point inexact exception has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the IXCIC bit in the SYSEXCIC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>4</td>
<td>FPOFSCRIS</td>
<td>RO</td>
<td>0</td>
<td>Floating-Point Overflow Exception Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A floating-point overflow exception has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the OFCIC bit in the SYSEXCIC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>3</td>
<td>FPUFSCRIS</td>
<td>RO</td>
<td>0</td>
<td>Floating-Point Underflow Exception Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A floating-point underflow exception has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the UFCIC bit in the SYSEXCIC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-----------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>FPIOCRIS</td>
<td>RO</td>
<td>0</td>
<td>Floating-Point Invalid Operation Raw Interrupt Status</td>
</tr>
</tbody>
</table>

Value | Description
--- | ---
0     | No interrupt
1     | A floating-point invalid operation exception has occurred.

This bit is cleared by writing a 1 to the IIOCIC bit in the SYSEXCIC register.

| 1        | FPDZCRIS  | RO   | 0     | Floating-Point Divide By 0 Exception Raw Interrupt Status |

Value | Description
--- | ---
0     | No interrupt
1     | A floating-point divide by 0 exception has occurred.

This bit is cleared by writing a 1 to the DZCIC bit in the SYSEXCIC register.

| 0        | FPIDCRIS  | RO   | 0     | Floating-Point Input Denormal Exception Raw Interrupt Status |

Value | Description
--- | ---
0     | No interrupt
1     | A floating-point input denormal exception has occurred.

This bit is cleared by writing a 1 to the IDCIC bit in the SYSEXCIC register.
Register 2: System Exception Interrupt Mask (SYSEXCIM), offset 0x004

The SYSEXCIM register is the interrupt mask set/clear register.

On a read, this register gives the current value of the mask on the relevant interrupt. Setting a bit allows the corresponding raw interrupt signal to be routed to the interrupt controller. Clearing a bit prevents the raw interrupt signal from being sent to the interrupt controller.

**System Exception Interrupt Mask (SYSEXCIM)**

Base 0x400F.9000
Offset 0x004
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RW</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>FPIXCIM</td>
<td>RW</td>
<td>0</td>
<td>Floating-Point Inexact Exception Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The FPIXCRIS interrupt is suppressed and not sent to the interrupt controller.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the FPISCRIS bit in the SYSEXCRIS register is set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>FPOFCIM</td>
<td>RW</td>
<td>0</td>
<td>Floating-Point Overflow Exception Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The FPOFCRIS interrupt is suppressed and not sent to the interrupt controller.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the FPOFCRIS bit in the SYSEXCRIS register is set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>FPUFCIM</td>
<td>RW</td>
<td>0</td>
<td>Floating-Point Underflow Exception Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The FPUFCCRIS interrupt is suppressed and not sent to the interrupt controller.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the FPUFCCRIS bit in the SYSEXCRIS register is set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>FPIOCIM</td>
<td>RW</td>
<td>0</td>
<td>Floating-Point Invalid Operation Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>FPDZCIM</td>
<td>RW</td>
<td>0</td>
<td>Floating-Point Divide By 0 Exception Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>FPIDCIM</td>
<td>RW</td>
<td>0</td>
<td>Floating-Point Input Denormal Exception Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 3: System Exception Masked Interrupt Status (SYSEXCMIS), offset 0x008

The SYSEXCMIS register is the masked interrupt status register. On a read, this register gives the current masked status value of the corresponding interrupt. A write has no effect.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>FPIOCMIS</td>
<td>RO</td>
<td>0</td>
<td>Floating-Point Invalid Operation Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value    Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0        An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1        An unmasked interrupt was signaled due to an invalid operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the FPIOCMIS bit in the SYSEXCIC register.</td>
</tr>
<tr>
<td>1</td>
<td>FPDZCMIS</td>
<td>RO</td>
<td>0</td>
<td>Floating-Point Divide By 0 Exception Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value    Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0        An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1        An unmasked interrupt was signaled due to a divide by 0 exception.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the FPDZCMIS bit in the SYSEXCIC register.</td>
</tr>
<tr>
<td>0</td>
<td>FPIDCMIS</td>
<td>RO</td>
<td>0</td>
<td>Floating-Point Input Denormal Exception Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value    Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0        An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1        An unmasked interrupt was signaled due to an input denormal exception.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the FPIDCMIS bit in the SYSEXCIC register.</td>
</tr>
</tbody>
</table>
Register 4: System Exception Interrupt Clear (SYSEXCIC), offset 0x00C

The SYSEXCIC register is the interrupt clear register. On a write of 1, the corresponding interrupt (both raw interrupt and masked interrupt, if enabled) is cleared. A write of 0 has no effect.

System Exception Interrupt Clear (SYSEXCIC)
Base 0x400F.9000
Offset 0x00C
Type W1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>W1C</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>FPIXCIC</td>
<td>W1C</td>
<td>0</td>
<td>Floating-Point Inexact Exception Interrupt Clear Writing a 1 to this bit clears the FPIXCRIS bit in the SYSEXCRIS register and the FPIXCMIS bit in the SYSEXCMIS register.</td>
</tr>
<tr>
<td>4</td>
<td>FPOFCIC</td>
<td>W1C</td>
<td>0</td>
<td>Floating-Point Overflow Exception Interrupt Clear Writing a 1 to this bit clears the FPOFCRIS bit in the SYSEXCRIS register and the FPOFCMIS bit in the SYSEXCMIS register.</td>
</tr>
<tr>
<td>3</td>
<td>FPUFCIC</td>
<td>W1C</td>
<td>0</td>
<td>Floating-Point Underflow Exception Interrupt Clear Writing a 1 to this bit clears the FPUFCRIS bit in the SYSEXCRIS register and the FPUFCMIS bit in the SYSEXCMIS register.</td>
</tr>
<tr>
<td>2</td>
<td>FPIOCIC</td>
<td>W1C</td>
<td>0</td>
<td>Floating-Point Invalid Operation Interrupt Clear Writing a 1 to this bit clears the FPIOCRIS bit in the SYSEXCRIS register and the FPIOCMIS bit in the SYSEXCMIS register.</td>
</tr>
<tr>
<td>1</td>
<td>FPDZCIC</td>
<td>W1C</td>
<td>0</td>
<td>Floating-Point Divide By 0 Exception Interrupt Clear Writing a 1 to this bit clears the FPDZCRIS bit in the SYSEXCRIS register and the FPDZCMIS bit in the SYSEXCMIS register.</td>
</tr>
<tr>
<td>0</td>
<td>FPIDCIC</td>
<td>W1C</td>
<td>0</td>
<td>Floating-Point Input Denormal Exception Interrupt Clear Writing a 1 to this bit clears the FPIDCRIS bit in the SYSEXCRIS register and the FPIDCMIS bit in the SYSEXCMIS register.</td>
</tr>
</tbody>
</table>
7 Hibernation Module

The Hibernation Module manages removal and restoration of power to provide a means for reducing system power consumption. When the processor and peripherals are idle, power can be completely removed with only the Hibernation module remaining powered. Power can be restored based on an external signal or at a certain time using the built-in Real-Time Clock (RTC). The Hibernation module can be independently supplied from an external battery or an auxiliary power supply.

The Hibernation module has the following features:

- 32-bit real-time seconds counter (RTC) with 1/32,768 second resolution and a 15-bit sub-seconds counter
  - 32-bit RTC seconds match register and a 15-bit sub seconds match for timed wake-up and interrupt generation with 1/32,768 second resolution
  - RTC predivider trim for making fine adjustments to the clock rate
- Two mechanisms for power control
  - System power control using discrete external regulator
  - On-chip power control using internal switches under register control
- Dedicated pin for waking using an external signal
- RTC operational and hibernation memory valid as long as $V_{DD}$ or $V_{BAT}$ is valid
- Low-battery detection, signaling, and interrupt generation, with optional wake on low battery
- GPIO pin state can be retained during hibernation
- Clock source from a 32.768-kHz external crystal or oscillator
- Sixteen 32-bit words of battery-backed memory to save state during hibernation
- Programmable interrupts for:
  - RTC match
  - External wake
  - Low battery
7.1 Block Diagram

Figure 7-1. Hibernation Module Block Diagram

7.2 Signal Description

The following table lists the external signals of the Hibernation module and describes the function of each.

Table 7-1. Hibernate Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GNDX</td>
<td>53</td>
<td>fixed</td>
<td>-</td>
<td>Power</td>
<td>GND for the Hibernation oscillator. When using a crystal clock source, this pin should be connected to digital ground along with the crystal load capacitors. When using an external oscillator, this pin should be connected to digital ground.</td>
</tr>
<tr>
<td>HIB</td>
<td>51</td>
<td>fixed</td>
<td>O</td>
<td>TTL</td>
<td>An output that indicates the processor is in Hibernate mode.</td>
</tr>
<tr>
<td>VBAT</td>
<td>55</td>
<td>fixed</td>
<td>-</td>
<td>Power</td>
<td>Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.</td>
</tr>
<tr>
<td>WAKE</td>
<td>50</td>
<td>fixed</td>
<td>I</td>
<td>TTL</td>
<td>An external input that brings the processor out of Hibernate mode when asserted.</td>
</tr>
</tbody>
</table>
Table 7-1. Hibernate Signals (100LQFP) (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOSC0</td>
<td>52</td>
<td>fixed</td>
<td>I</td>
<td>Analog</td>
<td>Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 32.768-kHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC.</td>
</tr>
<tr>
<td>XOSC1</td>
<td>54</td>
<td>fixed</td>
<td>O</td>
<td>Analog</td>
<td>Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.</td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

7.3 Functional Description

The Hibernation module provides two mechanisms for power control:

- The first mechanism uses internal switches to control power to the Cortex-M4F as well as to most analog and digital functions while retaining I/O pin power (VDD3ON mode).
- The second mechanism controls the power to the microcontroller with a control signal (\texttt{HIB}) that signals an external voltage regulator to turn on or off.

The Hibernation module power source is determined dynamically. The supply voltage of the Hibernation module is the larger of the main voltage source (V\textsubscript{DD}) or the battery/auxilliary voltage source (V\textsubscript{BAT}). The Hibernation module also has an independent clock source to maintain a real-time clock (RTC) when the system clock is powered down. Hibernate mode can be entered through one of two ways:

- The user initiates hibernation by setting the \texttt{HIBREQ} bit in the Hibernation Control (HIBCTL) register
- Power is arbitrarily removed from V\textsubscript{DD} while a valid V\textsubscript{BAT} is applied

Once in hibernation, the module signals an external voltage regulator to turn the power back on when an external pin (\texttt{WAKE}) is asserted or when the internal RTC reaches a certain value. The Hibernation module can also detect when the battery voltage is low and optionally prevent hibernation or wake from hibernation when the battery voltage falls below a certain threshold.

When waking from hibernation, the \texttt{HIB} signal is deasserted. The return of V\textsubscript{DD} causes a POR to be executed. The time from when the \texttt{WAKE} signal is asserted to when code begins execution is equal to the wake-up time (\texttt{tWAKE_TO_HIB}) plus the power-on reset time (T\textsubscript{POR}).

7.3.1 Register Access Timing

Because the Hibernation module has an independent clocking domain, hibernation registers must be written only with a timing gap between accesses. The delay time is \texttt{tHIB_REG_ACCESS}, therefore software must guarantee that this delay is inserted between back-to-back writes to Hibernation registers or between a write followed by a read. The \texttt{WC} interrupt in the HIBMIS register can be used to notify the application when the Hibernation modules registers can be accessed. Alternatively, software may make use of the \texttt{WRC} bit in the Hibernation Control (HIBCTL) register to ensure that the required timing gap has elapsed. This bit is cleared on a write operation and set once the write completes, indicating to software that another write or read may be started safely. Software should poll HIBCTL for \texttt{WRC}=1 prior to accessing any hibernation register.
Back-to-back reads from Hibernation module registers have no timing restrictions. Reads are performed at the full peripheral clock rate.

7.3.2 Hibernation Clock Source

In systems where the Hibernation module is used, the module must be clocked by an external source that is independent from the main system clock, even if the RTC feature is not used. An external oscillator or crystal is used for this purpose. To use a crystal, a 32.768-kHz crystal is connected to the XOSC0 and XOSC1 pins. Alternatively, a 32.768-kHz oscillator can be connected to the XOSC0 pin, leaving XOSC1 unconnected. Care must be taken that the voltage amplitude of the 32.768-kHz oscillator is less than $V_{BAT}$, otherwise, the Hibernation module may draw power from the oscillator and not $V_{BAT}$ during hibernation. See Figure 7-2 on page 506 and Figure 7-3 on page 507.

The Hibernation clock source is enabled by setting the CLK32EN bit of the HIBCTL register. The CLK32EN bit must be set before accessing any other Hibernation module register. If a crystal is used for the clock source, the software must leave a delay of $t_{HIBOSC_START}$ after writing to the CLK32EN bit and before any other accesses to the Hibernation module registers. The delay allows the crystal to power up and stabilize. If an external oscillator is used for the clock source, no delay is needed. When using an external clock source, the OSCBYP bit in the HIBCTL register should be set. When using a crystal clock source, the GNDX pin should be connected to digital ground along with the crystal load capacitors, as shown in Figure 7-2 on page 506. When using an external clock source, the GNDX pin should be connected to digital ground.

**Note:** In the figures below the parameters $R_{BAT}$ and $C_{BAT}$ have recommended values of $51\Omega \pm 5\%$ and $0.1\mu F \pm 5\%$, respectively. See “Hibernation Module” on page 1420 for more information.

**Figure 7-2. Using a Crystal as the Hibernation Clock Source with a Single Battery Source**

- **Note:** Some devices may not supply the GNDX signal. If GNDX is absent, the crystal load capacitors can be tied to GND externally. See “Signal Tables” on page 1354 for pins specific to your device.

- $X_1$ = Crystal frequency is $f_{XOSC\_XTAL}$.

- $C_{1,2}$ = Capacitor value derived from crystal vendor load capacitance specifications.

- $R_{PU}$ = Pull-up resistor is 200 kΩ

- $R_{BAT}$ = $51\Omega \pm 5\%$

- $C_{BAT}$ = $0.1\mu F \pm 20\%$

See “Hibernation Clock Source Specifications” on page 1412 for specific parameter values.

---

*Texas Instruments-Production Data*
Figure 7-3. Using a Dedicated Oscillator as the Hibernation Clock Source with VDD3ON Mode

7.3.3 System Implementation

Several different system configurations are possible when using the Hibernation module:

- Using a single battery source, where the battery provides both V_{DD} and V_{BAT}, as shown in Figure 7-2 on page 506.

- Using the VDD3ON mode, where V_{DD} continues to be powered in hibernation, allowing the GPIO pins to retain their states, as shown in Figure 7-3 on page 507. In this mode, V_{DDC} is powered off internally. The GPIO retention will be released when power is reapplied and the GPIOs will be initialized to their default values.

- Using separate sources for V_{DD} and V_{BAT}. In this mode, additional circuitry is required for system start-up without a battery or with a depleted battery.

- Using a regulator to provide both V_{DD} and V_{BAT} with a switch enabled by HIB to remove V_{DD} during hibernation as shown in Figure 7-4 on page 508.

**Note:** Some devices may not supply the GNDX, WAKE, or HIB signals. See “Signal Tables” on page 1354 for pins specific to your device.

\[ R_{PU} = \text{Pull-up resistor is } 1 \, \text{M} \Omega \]
\[ R_{BAT} = 51 \Omega \pm 5\% \]
\[ C_{BAT} = 0.1\mu F \pm 20\% \]
Adding external capacitance to the \( V_{BAT} \) supply reduces the accuracy of the low-battery measurement and should be avoided if possible. The diagrams referenced in this section only show the connection to the Hibernation pins and not to the full system.

If the application does not require the use of the Hibernation module, refer to “Connections for Unused Signals” on page 1393. In this situation, the \texttt{HIB} bit in the \texttt{Run Mode Clock Gating Control Register 0 (RCGC0)} and the \texttt{Hibernation Run Mode Clock Gating Control (RCGCHIB)} registers must be cleared, disabling the system clock to the Hibernation module and Hibernation module registers are not accessible.

### 7.3.4 Battery Management

**Important:** System-level factors may affect the accuracy of the low-battery detect circuit. The designer should consider battery type, discharge characteristics, and a test load during battery voltage measurements.

The Hibernation module can be independently powered by a battery or an auxiliary power source using the \( V_{BAT} \) pin. The module can monitor the voltage level of the battery and detect when the voltage drops below \( V_{LOWBAT} \). The voltage threshold can be between 1.9 V and 2.5 V and is configured using the \texttt{VBATSEL} field in the \texttt{HIBCTL} register. The module can also be configured so that it does not go into Hibernate mode if the battery voltage drops below this threshold. In addition, battery voltage is monitored while in hibernation, and the microcontroller can be configured to wake from hibernation if the battery voltage goes below the threshold using the \texttt{BATWKEN} bit in the \texttt{HIBCTL} register.

The Hibernation module is designed to detect a low-battery condition and set the \texttt{LOWBAT} bit of the \texttt{Hibernation Raw Interrupt Status (HIBRIS)} register when this occurs. If the \texttt{VABORT} bit in the \texttt{HIBCTL} register is also set, then the module is prevented from entering Hibernate mode when a low-battery is detected. The module can also be configured to generate an interrupt for the low-battery condition (see “Interrupts and Status” on page 512).

Note that the Hibernation module draws power from whichever source (\( V_{BAT} \) or \( V_{DD} \)) has the higher voltage. Therefore, it is important to design the circuit to ensure that \( V_{DD} \) is higher than \( V_{BAT} \) under nominal conditions or else the Hibernation module draws power from the battery even when \( V_{DD} \) is available.
7.3.5 Real-Time Clock

The RTC module is designed to keep wall time. The RTC can operate in seconds counter mode. A 32.768 kHz clock source along with a 15-bit predivider reduces the clock to 1 Hz. The 1 Hz clock is used to increment the 32-bit counter and keep track of seconds. A match register can be configured to interrupt or wake the system from hibernate. In addition, a software trim register is implemented to allow the user to compensate for oscillator inaccuracies using software.

7.3.5.1 RTC Counter - Seconds/Subseconds Mode

The clock signal to the RTC is provided by either of the 32.768-kHz clock sources available to the Hibernation module. The Hibernation RTC Counter (HIBRTCC) register displays the seconds value. The Hibernation RTC Sub Seconds register (HIBRTCSS) is provided for additional time resolution of an application requiring less than one-second divisions.

The RTC is enabled by setting the RTCEN bit of the HIBCTL register. The RTC counter and sub-seconds counters begin counting immediately once RTCEN is set. Both counters count up. The RTC continues counting as long as the RTC is enabled and a valid V_BAT is present, regardless of whether V_DD is present or if the device is in hibernation.

The HIBRTCC register is set by writing the Hibernation RTC Load (HIBRTCLD) register. A write to the HIBRTCLD register clears the 15-bit sub-seconds counter field, RTCSSC, in the HIBRTCSS register. To ensure a valid read of the RTC value, the HIBRTC register should be read first, followed by a read of the RTCSSC field in the HIBRTCSS register and then a re-read of the HIBRTC register. If the two values for the HIBRTC are equal, the read is valid. By following this procedure, errors in the application caused by the HIBRTC register rolling over by a count of 1 during a read of the RTCSSC field are prevented. The RTC can be configured to generate an alarm by setting the RTCAL0 bit in the HIBIM register. When an RTC match occurs, an interrupt is generated and displayed in the HIBRIS register. Refer to “RTC Match - Seconds/Subseconds Mode” on page 509 for more information.

If the RTC is enabled, only a cold POR, where both V_BAT and V_DD are removed, resets the RTC registers. If any other reset occurs while the RTC is enabled, such as an external RST assertion or BOR reset, the RTC is not reset. The RTC registers can be reset under any type of system reset as long as the RTC and external wake pins are not enabled.

7.3.5.2 RTC Match - Seconds/Subseconds Mode

The Hibernation module includes a 32-bit match register, HIBRTCM0, which is compared to the value of the RTC 32-bit counter, HIBRTCC. The match functionality also extends to the sub-seconds counter. The 15-bit field (RTCSSM) in the HIBRTCSS register is compared to the value of the 15-bit sub-seconds counter. When a match occurs, the RTCAL0 bit is set in the HIBRIS register. For applications using Hibernate mode, the processor can be programmed to wake from Hibernate mode by setting the RTCWEN bit in the HIBCTL register. The processor can also be programmed to generate an interrupt to the interrupt controller by setting the RTCAL0 bit in the HIBIM register.

The match interrupt generation takes priority over an interrupt clear. Therefore, writes to the RTCAL0 bit in the Hibernation Interrupt Clear (HIBIC) register do not clear the RTCAL0 bit if the HIBRTCC value and the HIBRTCM0 value are equal. There are several methodologies to avoid this occurrence, such as writing a new value to the HIBRTCLD register prior to writing the HIBIC to clear the RTCAL0. Another example, would be to disable the RTC and re-enable the RTC by clearing and setting the RTCEN bit in the HIBCTL register.

Note: A Hibernate request made while a match event is valid causes the module to immediately wake up. This occurs when the RTCWEN bit is set and the RTCAL0 bit in the HIBRIS register is set at the same time the HIBREQ bit in the HIBCTL register is written to 1. This can be
avoided by clearing the RTCAL0 bit in the HIBRIS register by writing a 1 to the corresponding bit in the HIBIC register before setting the HIBREQ bit. Another example would be to disable the RTC and re-enable the RTC by clearing and setting the RTCEN bit in the HIBCTL register.

7.3.5.3 RTC Trim

The RTC counting rate can be adjusted to compensate for inaccuracies in the clock source by using the predivider trim register, HIBRTCT. This register has a nominal value of 0x7FFF, and is used for one second out of every 64 seconds in RTC counter mode, when bits [5:0] in the HIBRTCC register change from 0x00 to 0x01, to divide the input clock. This configuration allows the software to make fine corrections to the clock rate by adjusting the predivider trim register up or down from 0x7FFF. The predivider trim should be adjusted up from 0x7FFF in order to slow down the RTC rate and down from 0x7FFF in order to speed up the RTC rate.

Care must be taken when using trim values that are near to the sub seconds match value in the HIBRTCSS register. It is possible when using trim values above 0x7FFF to receive two match interrupts for the same counter value. In addition, it is possible when using trim values below 0x7FFF to miss a match interrupt.

In the case of a trim value above 0x7FFF, when the RTCSSC value in the HIBRTCSS register reaches 0x7FFF, the RTCC value increments from 0x0 to 0x1 while the RTCSSC value is decreased by the trim amount. The RTCSSC value is counted up again to 0x7FFF before rolling over to 0x0 to begin counting up again. If the match value is within this range, the match interrupt is triggered twice. For example, as shown in Figure 7-5 on page 510, if the match interrupt was configured with RTCM0=0x1 and RTCSSM=0x7FFD, two interrupts would be triggered.

Figure 7-5. Counter Behavior with a TRIM Value of 0x8002

In the case of a trim value below 0x7FFF, the RTCSSC value is advanced from 0x7FFF to the trim value while the RTCC value is incremented from 0x0 to 0x1. If the match value is within that range, the match interrupt is not triggered. For example, as shown in Figure 7-6 on page 510, if the match interrupt was configured with RTCM0=0x1 and RTCSSM=0x2, an interrupt would never be triggered.

Figure 7-6. Counter Behavior with a TRIM Value of 0x7FFC
7.3.6 Battery-Backed Memory

The Hibernation module contains 16 32-bit words of memory that are powered from the battery or an auxiliary power supply and therefore retained during hibernation. The processor software can save state information in this memory prior to hibernation and recover the state upon waking. The battery-backed memory can be accessed through the HIBDATA registers. If both V_DD and V_BAT are removed, the contents of the HIBDATA registers are not retained.

7.3.7 Power Control Using HIB

**Important:** The Hibernation Module requires special system implementation considerations when using HIB to control power, as it is intended to power-down all other sections of the microcontroller. All system signals and power supplies that connect to the chip must be driven to 0 V or powered down with the same regulator controlled by HIB.

The Hibernation module controls power to the microcontroller through the use of the HIB pin which is intended to be connected to the enable signal of the external regulator(s) providing 3.3 V to the microcontroller and other circuits. When the HIB signal is asserted by the Hibernation module, the external regulator is turned off and no longer powers the microcontroller and any parts of the system that are powered by the regulator. The Hibernation module remains powered from the V_BAT supply until a Wake event. Power to the microcontroller is restored by deasserting the HIB signal, which causes the external regulator to turn power back on to the chip.

7.3.8 Power Control Using VDD3ON Mode

The Hibernation module may also be configured to cut power to all internal modules during Hibernate mode. While in this state, if VDD3ON is set in the HIBCTL register, all pins are held in the state they were in prior to entering hibernation. For example, inputs remain inputs; outputs driven high remain driven high, and so on. There are important procedural and functional items to note when in VDD3ON mode:

- In the VDD3ON mode, the regulator should maintain 3.3 V power to the microcontroller during Hibernate. GPIO retention is disabled when the RETCLR bit is cleared in the HIBCTL register.

7.3.9 Initiating Hibernate

Hibernate mode is initiated when the HIBREQ bit of the HIBCTL register is set. If a wake-up condition has not been configured using the PINWEN or RTCWEN bits in the HIBCTL register, the hibernation request is ignored. If a Flash memory write operation is in progress when the HIBREQ bit is set, an interlock feature holds off the transition into Hibernate mode until the write has completed. In addition, if the battery voltage is below the threshold voltage defined by the VBATSEL field in the HIBCTL register, the hibernation request is ignored.

7.3.10 Waking from Hibernate

The Hibernation module is configured to wake from the external WAKE pin by setting the PINWEN bit of the HIBCTL register. It is configured to wake from RTC match by setting the RTCWEN bit. Note that the WAKE pin uses the Hibernation module’s internal power supply as the logic 1 reference.

The Hibernation module can also be configured to wake from hibernate when the following events occur:

- RTC match wake event
- Low Battery wake event
By setting the RTCWEN bit in the HIBCTL register a wake from hibernate can occur when the value of the HIBRTCC register matches the value of the HIBRTCM0 register and the value of the RTCSSC field matches the RTCSSM field in the HIBRTCSS register.

To allow a wake from Hibernate on a low battery event, the BATWKEN bit in the HIBCTL register must be set. In this configuration, the battery voltage is checked every 512 seconds while in hibernation. If the voltage is below the level specified by the VBATSEL field, the LOWBAT interrupt is set in the HIBRIS register.

Upon external wake-up, external reset, or RTC match, the Hibernation module delays coming out of hibernation until V\textsubscript{DD} is above the minimum specified voltage, see Table 24-5 on page 1397.

When the Hibernation module wakes, the microcontroller performs a normal power-on reset. The normal power-on reset does not reset the Hibernation module, but does reset the rest of the microcontroller. Software can detect that the power-on was due to a wake from hibernation by examining the raw interrupt status register (see “Interrupts and Status” on page 512) and by looking for state data in the battery-backed memory (see “Battery-Backed Memory” on page 511).

### 7.3.11 Arbitrary Power Removal

The microcontroller goes into hibernation if V\textsubscript{DD} is arbitrarily removed when the CLK32EN bit is set and any of the following bits are set:

- PINWEN bit in the HIBCTL register
- RTCEN bit in the HIBCTL register

The microcontroller wakes from hibernation when power is reapplied.

If the CLK32EN bit is set but the PINWEN, and RTCEN bits are all clear, the microcontroller still goes into hibernation if power is removed; however, when V\textsubscript{DD} is reapplied, the MCU executes a cold POR and the Hibernation module is reset. If the CLK32EN bit is not set and V\textsubscript{DD} is arbitrarily removed, the part is simply powered off and executes a cold POR when power is reapplied.

If V\textsubscript{DD} is arbitrarily removed while a Flash memory or HIBDATA register write operation is in progress, the write operation must be retried after V\textsubscript{DD} is reapplied.

### 7.3.12 Interrupts and Status

The Hibernation module can generate interrupts when the following conditions occur:

- Assertion of WAKE pin
- RTC match
- Low battery detected
- Write complete/capable
- Assertion of an external RESET pin

All of the interrupts are ORed together before being sent to the interrupt controller, so the Hibernation module can only generate a single interrupt request to the controller at any given time. The software interrupt handler can service multiple interrupt events by reading the Hibernation Masked Interrupt Status (HIBMIS) register. Software can also read the status of the Hibernation module at any time by reading the HIBRIS register which shows all of the pending events. This register can be used
after waking from hibernation to see if a wake condition was caused by one of the events above or by a power loss.

The \texttt{WAKE} pin can generate interrupts in Run, Sleep and Deep Sleep Mode. The events that can trigger an interrupt are configured by setting the appropriate bits in the \texttt{Hibernation Interrupt Mask (HIBIM)} register. Pending interrupts can be cleared by writing the corresponding bit in the \texttt{Hibernation Interrupt Clear (HIBIC)} register.

### 7.4 Initialization and Configuration

The Hibernation module has several different configurations. The following sections show the recommended programming sequence for various scenarios. Because the Hibernation module runs at a low frequency and is asynchronous to the rest of the microcontroller, which is run off the system clock, software must allow a delay of $t_{\text{HIB\_REG\_ACCESS}}$ after writes to registers (see “Register Access Timing” on page 505). The \texttt{WC} interrupt in the \texttt{HIBMIS} register can be used to notify the application when the Hibernation modules registers can be accessed.

#### 7.4.1 Initialization

The Hibernation module comes out of reset with the system clock enabled to the module, but if the system clock to the module has been disabled, then it must be re-enabled, even if the RTC feature is not used. See page 346.

If a 32.768-kHz crystal is used as the Hibernation module clock source, perform the following steps:

1. Write 0x0000.0010 to the \texttt{HIBIM} register to enable the \texttt{WC} interrupt.
2. Write 0x40 to the \texttt{HIBCTL} register at offset 0x10 to enable the oscillator input.
3. Wait until the \texttt{WC} interrupt in the \texttt{HIBMIS} register has been triggered before performing any other operations with the Hibernation module.

If a 32.768-kHz single-ended oscillator is used as the Hibernation module clock source, then perform the following steps:

1. Write 0x0000.0010 to the \texttt{HIBIM} register to enable the \texttt{WC} interrupt.
2. Write 0x0001.0040 to the \texttt{HIBCTL} register at offset 0x10 to enable the oscillator input and bypass the on-chip oscillator.
3. Wait until the \texttt{WC} interrupt in the \texttt{HIBMIS} register has been triggered before performing any other operations with the Hibernation module.

The above steps are only necessary when the entire system is initialized for the first time. If the microcontroller has been in hibernation, then the Hibernation module has already been powered up and the above steps are not necessary. The software can detect that the Hibernation module and clock are already powered by examining the \texttt{CLK32EN} bit of the \texttt{HIBCTL} register.

Table 7-2 on page 513 illustrates how the clocks function with various bit setting both in normal operation and in hibernation.

<table>
<thead>
<tr>
<th>\texttt{CLK32EN}</th>
<th>\texttt{PINWEN}</th>
<th>\texttt{RTCWEN}</th>
<th>\texttt{RTCEN}</th>
<th>\texttt{Result Normal Operation}</th>
<th>\texttt{Result Hibernation}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Hibernation module disabled</td>
<td>Hibernation module disabled</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>RTC match capability enabled</td>
<td>No hibernation</td>
</tr>
</tbody>
</table>

\textit{Texas Instruments-Production Data}
Table 7-2. Hibernation Module Clock Operation (continued)

<table>
<thead>
<tr>
<th>CLK32EN</th>
<th>PINWEN</th>
<th>RTCWEN</th>
<th>RTCEN</th>
<th>Result Normal Operation</th>
<th>Result Hibernation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Module clocked</td>
<td>RTC match for wake-up event</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Module clocked</td>
<td>Clock is powered down during hibernation and powered up again on external wake-up event.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Module clocked</td>
<td>Clock is powered up during hibernation for RTC. Wake up on external event.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Module clocked</td>
<td>RTC match or external wake-up event, whichever occurs first.</td>
</tr>
</tbody>
</table>

7.4.2 RTC Match Functionality (No Hibernation)

Use the following steps to implement the RTC match functionality of the Hibernation module:

1. Write 0x0000.0040 to the HIBCTL register at offset 0x010 to enable 32.768-kHz Hibernation oscillator.
2. Write the required RTC match value to the HIBRTCM0 register at offset 0x004 and the RTCSSM field in the HIBRTCSS register at offset 0x028.
3. Write the required RTC load value to the HIBRTCLD register at offset 0x00C.
4. Set the required RTC match interrupt mask in the RTCALT0 in the HIBIM register at offset 0x014.
5. Write 0x0000.0041 to the HIBCTL register at offset 0x010 to enable the RTC to begin counting.

7.4.3 RTC Match/Wake-Up from Hibernation

Use the following steps to implement the RTC match and wake-up functionality of the Hibernation module:

1. Write 0x0000.0040 to the HIBCTL register at offset 0x010 to enable 32.768-kHz Hibernation oscillator.
2. Write the required RTC match value to the HIBRTCM0 register at offset 0x004 and the RTCSSM field in the HIBRTCSS register at offset 0x028.
3. Write the required RTC load value to the HIBRTCLD register at offset 0x00C. This write causes the 15-bit sub seconds counter to be cleared.
4. Write any data to be retained during hibernation to the HIBDATA register at offsets 0x030-0x06F.
5. Set the RTC Match Wake-Up and start the hibernation sequence by writing 0x0000.004B to the HIBCTL register at offset 0x010.

7.4.4 External Wake-Up from Hibernation

Use the following steps to implement the Hibernation module with the external WAKE pin as the wake-up source for the microcontroller:

1. Write 0x0000.0040 to the HIBCTL register at offset 0x010 to enable 32.768-kHz Hibernation oscillator.
2. Write any data to be retained during hibernation to the HIBDATA register at offsets 0x030-0x06F.
3. Enable the external wake and start the hibernation sequence by writing 0x0000.0052 to the HIBCTL register at offset 0x010.

### 7.4.5 RTC or External Wake-Up from Hibernation

1. Write 0x0000.0040 to the HIBCTL register at offset 0x010 to enable 32.768-kHz Hibernation oscillator.

2. Write the required RTC match value to the HIBRTC0 register at offset 0x004 and the RTCSSM field in the HIBRTCSS register at offset 0x028.

3. Write the required RTC load value to the HIBRTCLD register at offset 0x00C. This write causes the 15-bit sub seconds counter to be cleared.

4. Write any data to be retained during hibernation to the HIBDATA register at offsets 0x030-0x06F.

5. Set the RTC Match/External Wake-Up and start the hibernation sequence by writing 0x0000.005B to the HIBCTL register at offset 0x010.

### 7.5 Register Map

Table 7-3 on page 515 lists the Hibernation registers. All addresses given are relative to the Hibernation Module base address at 0x400F.C000. Note that the system clock to the Hibernation module must be enabled before the registers can be programmed (see page 346). There must be a delay of 3 system clocks after the Hibernation module clock is enabled before any Hibernation module registers are accessed. In addition, the CLK32EN bit in the HIBCTL register must be set before accessing any other Hibernation module register.

**Note:** The Hibernation module registers are on the Hibernation module clock domain and have special timing requirements. Software should make use of the WRC bit in the HIBCTL register to ensure that the required timing gap has elapsed. If the WRC bit is clear, any attempted write access is ignored. See “Register Access Timing” on page 505.

**Important:** The Hibernation module registers are reset under two conditions:

1. Any type of system reset (if the RTCEN and the PINWEN bits in the HIBCTL register are clear).

2. A cold POR occurs when both the VDD and VBAT supplies are removed.

Any other reset condition is ignored by the Hibernation module.

#### Table 7-3. Hibernation Module Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>HIBRTCC</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Hibernation RTC Counter</td>
<td>517</td>
</tr>
<tr>
<td>0x004</td>
<td>HIBRTC0</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Hibernation RTC Match 0</td>
<td>518</td>
</tr>
<tr>
<td>0x00C</td>
<td>HIBRTC0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Hibernation RTC Load</td>
<td>519</td>
</tr>
<tr>
<td>0x010</td>
<td>HIBCTL</td>
<td>RW</td>
<td>0x8000.2000</td>
<td>Hibernation Control</td>
<td>520</td>
</tr>
<tr>
<td>0x014</td>
<td>HIBIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Hibernation Interrupt Mask</td>
<td>524</td>
</tr>
</tbody>
</table>
7.6 Register Descriptions

The remainder of this section lists and describes the Hibernation module registers, in numerical order by address offset.

Table 7-3. Hibernation Module Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x018</td>
<td>HIBRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Hibernation Raw Interrupt Status</td>
<td>526</td>
</tr>
<tr>
<td>0x01C</td>
<td>HIIBMIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Hibernation Masked Interrupt Status</td>
<td>528</td>
</tr>
<tr>
<td>0x020</td>
<td>HIBIC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>Hibernation Interrupt Clear</td>
<td>530</td>
</tr>
<tr>
<td>0x024</td>
<td>HIBRTCT</td>
<td>RW</td>
<td>0x0000.7FF</td>
<td>Hibernation RTC Trim</td>
<td>531</td>
</tr>
<tr>
<td>0x028</td>
<td>HIBRTCSS</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Hibernation RTC Sub Seconds</td>
<td>532</td>
</tr>
<tr>
<td>0x030-0x06F</td>
<td>HIBDATA</td>
<td>RW</td>
<td>-</td>
<td>Hibernation Data</td>
<td>533</td>
</tr>
</tbody>
</table>
Register 1: Hibernation RTC Counter (HIBRTCC), offset 0x000

This register is the current 32-bit value of the RTC counter.

The RTC counter consists of a 32-bit seconds counter and a 15-bit sub seconds counter. The RTC counters are reset by the Hibernation module reset. The RTC 32-bit seconds counter can be set by the user using the HIBRTCLD register. When the 32-bit seconds counter is set, the 15-bit sub second counter is cleared.

The RTC value can be read by first reading the HIBRTCC register, reading the RTCSSC field in the HIBRTCSS register, and then rereading the HIBRTCC register. If the two values for HIBRTCC are equal, the read is valid.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>RTCC</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>RTC Counter</td>
</tr>
</tbody>
</table>

A read returns the 32-bit counter value, which represents the seconds elapsed since the RTC was enabled. This register is read-only. To change the value, use the HIBRTCLD register.
Register 2: Hibernation RTC Match 0 (HIBRTCM0), offset 0x004

This register is the 32-bit seconds match register for the RTC counter. The 15-bit sub second match value is stored in the reading the RTCSSC field in the HIBRTCSS register and can be used in conjunction with this register for a more precise time match.

**Note:** The Hibernation module registers are on the Hibernation module clock domain and have special timing requirements. Software should make use of the WRC bit in the HIBCTL register to ensure that the required timing gap has elapsed. If the WRC bit is clear, any attempted write access is ignored. See “Register Access Timing” on page 505.

Hibernation RTC Match 0 (HIBRTCM0)
Base 0x400F.C000
Offset 0x004
Type RW, reset 0xFFFF.FFFF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>RTCM0</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>RTC Match 0&lt;br&gt;A write loads the value into the RTC match register.&lt;br&gt;A read returns the current match value.</td>
</tr>
</tbody>
</table>
Register 3: Hibernation RTC Load (HIBRTCLD), offset 0x00C

This register is used to load a 32-bit value loaded into the RTC counter. The load occurs immediately upon this register being written. When this register is written, the 15-bit sub seconds counter is also cleared.

Note: The Hibernation module registers are on the Hibernation module clock domain and have special timing requirements. Software should make use of the WRC bit in the HIBCTL register to ensure that the required timing gap has elapsed. If the WRC bit is clear, any attempted write access is ignored. See “Register Access Timing” on page 505.

Hibernation RTC Load (HIBRTCLD)
Base 0x400F.C000
Offset 0x00C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>RTCLD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>RTC Load</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A write loads the current value into the RTC counter (RTCC).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A read returns the 32-bit load value.</td>
</tr>
</tbody>
</table>
Register 4: Hibernation Control (HIBCTL), offset 0x010

This register is the control register for the Hibernation module. This register must be written last before a hibernate event is issued. Writes to other registers after the HIBREQ bit is set are not guaranteed to complete before hibernation is entered.

**Note:** Writes to this register have special timing requirements. Software should make use of the WRC bit in the HIBCTL register to ensure that the required synchronization has elapsed. While the WRC bit is clear, any attempts to write this register are ignored. Reads may occur at any time.

Hibernation Control (HIBCTL)

<table>
<thead>
<tr>
<th>Base 0x400F.C000</th>
<th>Offset 0x010</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RW, reset 0x8000.2000</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Bit/Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>WRC</td>
<td>RO</td>
<td>1</td>
<td>Write Complete/Capable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Software must poll this bit between write requests and defer writes until WRC=1 to ensure proper operation. An interrupt can be configured to indicate the WRC has completed.

The bit name WRC means "Write Complete," which is the normal use of the bit (between write accesses). However, because the bit is set out-of-reset, the name can also mean "Write Capable" which simply indicates that the interface may be written to by software. This difference may be exploited by software at reset time to detect which method of programming is appropriate: 0 = software delay loops required; 1 = WRC paced available.

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
### Oscillator Drive Capability

This bit is used to compensate for larger or smaller filtering capacitors.

**Note:** This bit is not meant to be changed once the Hibernation oscillator has started. Oscillator stability is not guaranteed if the user changes this value after the oscillator is running.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Low drive strength is enabled, 12 pF.</td>
</tr>
<tr>
<td>1</td>
<td>High drive strength is enabled, 24 pF.</td>
</tr>
</tbody>
</table>

### Oscillator Bypass

The internal 32.768-kHz Hibernation oscillator is enabled. This bit should be cleared when using an external 32.768-kHz crystal.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The internal 32.768-kHz Hibernation oscillator is disabled and powered down. This bit should be set when using a single-ended oscillator attached to XOSCO.</td>
</tr>
<tr>
<td>1</td>
<td>The internal 32.768-kHz Hibernation oscillator is enabled.</td>
</tr>
</tbody>
</table>

### Software should not rely on the value of a reserved bit.

To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

<table>
<thead>
<tr>
<th>Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>reserved</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit.</td>
</tr>
<tr>
<td>reserved</td>
<td>0x1</td>
<td>Software should not rely on the value of a reserved bit.</td>
</tr>
</tbody>
</table>

### Select for Low-Battery Comparator

This field selects the battery level that is used when checking the battery status. If the battery voltage is below the specified level, the LOWBAT interrupt bit in the HIBRIS register is set.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>1.9 Volts</td>
</tr>
<tr>
<td>0x1</td>
<td>2.1 Volts (default)</td>
</tr>
<tr>
<td>0x2</td>
<td>2.3 Volts</td>
</tr>
<tr>
<td>0x3</td>
<td>2.5 Volts</td>
</tr>
</tbody>
</table>

### Check Battery Status

When read, indicates that the low-battery comparator cycle is not active. Writing a 0 has no effect.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>When read, indicates that the low-battery comparator cycle is not active.</td>
</tr>
<tr>
<td>1</td>
<td>When read, indicates the low-battery comparator cycle has not completed. Setting this bit initiates a low-battery comparator cycle. If the battery voltage is below the level specified by VBATSEL field, the LOWBAT interrupt bit in the HIBRIS register is set. A hibernation request is held off if a battery check is in progress.</td>
</tr>
</tbody>
</table>
### Hibernation Module

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>BATWKEN</td>
<td>RW</td>
<td>0</td>
<td>Wake on Low Battery</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The battery voltage level is not automatically checked. Low battery voltage does not cause the microcontroller to wake from hibernation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: When this bit is set, the battery voltage level is checked every 512 seconds while in hibernation. If the voltage is below the level specified by VBATSEL field, the microcontroller wakes from hibernation and the LOWBAT interrupt bit in the HIBRIS register is set.</td>
</tr>
<tr>
<td>8</td>
<td>VDD3ON</td>
<td>RW</td>
<td>0</td>
<td>VDD Powered</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The internal switches are not used. The HIB signal should be used to control an external switch or regulator.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The internal switches control the power to the on-chip modules (VDD3ON mode).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Regardless of the status of the VDD3ON bit, the HIB signal is asserted during Hibernate mode. Thus, when VDD3ON is set, the HIB signal should not be connected to the 3.3V regulator, and the 3.3V power source should remain connected. When this bit is set while in hibernation, all pins are held in the state they were in prior to entering hibernation. For example, inputs remain inputs; outputs driven high remain driven high, and so on.</td>
</tr>
<tr>
<td>7</td>
<td>VABORT</td>
<td>RW</td>
<td>0</td>
<td>Power Cut Abort Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The microcontroller goes into hibernation regardless of the voltage level of the battery.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: When this bit is set, the battery voltage level is checked before entering hibernation. If VBAT is less than the voltage specified by VBATSEL, the microcontroller does not go into hibernation.</td>
</tr>
<tr>
<td>6</td>
<td>CLK32EN</td>
<td>RW</td>
<td>0</td>
<td>Clocking Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit must be enabled to use the Hibernation module.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The Hibernation module clock source is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The Hibernation module clock source is enabled.</td>
</tr>
<tr>
<td>5</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>4</td>
<td>PINWEN</td>
<td>RW</td>
<td>0</td>
<td>External Wake Pin Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The status of the WAKE pin has no effect on hibernation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An assertion of the WAKE pin takes the microcontroller out of hibernation.</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>The external I/O wake pad interrupt is set if the WAKE pin is asserted in Run, Sleep, or Deep Sleep mode regardless of whether the PINWEN bit is 0x0 or 0x1. The interrupt may be forwarded to the processor by setting the EXTW bit in the HIBIM register.</td>
</tr>
<tr>
<td>3</td>
<td>RTCWEN</td>
<td>RW</td>
<td>0</td>
<td>RTC Wake-up Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An RTC match event has no effect on hibernation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An RTC match event (the value the HIBRTC register matches the value of the HIBRTCM0 register and the value of the RTCSSC field matches the RTCSSM field in the HIBRTCSS register) takes the microcontroller out of hibernation.</td>
</tr>
<tr>
<td>2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>HIBREQ</td>
<td>RW</td>
<td>0</td>
<td>Hibernation Request</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No hibernation request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Set this bit to initiate hibernation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>After a wake-up event, this bit is automatically cleared by hardware.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A hibernation request is ignored if both the PINWEN and RTCWEN bits are clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A hibernation request is held off if the BATCHK bit is set.</td>
</tr>
<tr>
<td>0</td>
<td>RTCEN</td>
<td>RW</td>
<td>0</td>
<td>RTC Timer Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The Hibernation module RTC is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The Hibernation module RTC is enabled.</td>
</tr>
</tbody>
</table>
Register 5: Hibernation Interrupt Mask (HIBIM), offset 0x014

This register is the interrupt mask register for the Hibernation module interrupt sources. Each bit in this register masks the corresponding bit in the Hibernation Raw Interrupt Status (HIBRIS) register. If a bit is unmasked, the interrupt is sent to the interrupt controller. If the bit is masked, the interrupt is not sent to the interrupt controller. The WC bit of the HIBIM register may be set before the CLK32EN bit of the HIBCTL register is set. This allows software to use the WC interrupt trigger to detect when the RTCOSC clock is stable, which may be in excess of one second. If the WC bit is set before the CLK32EN has been set, the mask value is not preserved over a hibernate cycle unless the bit is written a second time.

**Note:** The WC bit of this register is in the system clock domain such that a write to this bit is immediate and may be done before the CLK32EN bit is set in the HIBCTL register.

### Hibernation Module

#### Hibernation Interrupt Mask (HIBIM)

Base 0x400F.C000  
Offset 0x014  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>WC</td>
<td>RW</td>
<td>0</td>
<td>External Write Complete/Capable Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>EXTW</td>
<td>RW</td>
<td>0</td>
<td>External Wake-Up Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------------</td>
<td>------</td>
<td>-------</td>
<td>---------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>LOWBAT</td>
<td>RW</td>
<td>0</td>
<td>Low Battery Voltage Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>RTCALT0</td>
<td>RW</td>
<td>0</td>
<td>RTC Alert 0 Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 6: Hibernation Raw Interrupt Status (HIBRIS), offset 0x018

This register is the raw interrupt status for the Hibernation module interrupt sources. Each bit can be masked by clearing the corresponding bit in the HIBIM register. When a bit is masked, the interrupt is not sent to the interrupt controller. Bits in this register are cleared by writing a 1 to the corresponding bit in the Hibernation Interrupt Clear (HIBIC) register or by entering hibernation.

**Note:** The bits in this register do not reflect hibernation due to an arbitrary power loss on V_{DD}. If the LOWBAT bit was set prior to the loss of power, it will still be set when power is reapplied. In addition, the EXTW bit is self-clearing when exiting from hibernation, so if it was set prior to the power loss, the event is lost after the power is reapplied.

### Hibernation Raw Interrupt Status (HIBRIS)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>WC</td>
<td>RO</td>
<td>0</td>
<td>Write Complete/ capable Raw Interrupt Status</td>
</tr>
<tr>
<td>3</td>
<td>EXTW</td>
<td>RO</td>
<td>0</td>
<td>External Wake-Up Raw Interrupt Status</td>
</tr>
</tbody>
</table>

**Value Description**

- **0** The **WRC** bit in the HIBCTL has not been set.
- **1** The **WRC** bit in the HIBCTL has been set.

This bit is cleared by writing a 1 to the **wc** bit in the HIBIC register.

**Note:** The **EXTW** bit is set if the **WAKE** pin is asserted in any mode of operation (Run, Sleep, Deep Sleep) regardless of whether the **PINWEN** bit is set in the HIBCTL register.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>LOWBAT</td>
<td>RO</td>
<td>0</td>
<td>Low Battery Voltage Raw Interrupt Status</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The battery voltage has not dropped below $V_{LOWBAT}$.</td>
</tr>
<tr>
<td>1</td>
<td>The battery voltage dropped below $V_{LOWBAT}$.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the LOWBAT bit in the HIBIC register.

| 1      | reserved    | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |

| 0      | RTCALT0     | RO   | 0     | RTC Alert 0 Raw Interrupt Status |

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No match</td>
</tr>
<tr>
<td>1</td>
<td>The value of the HIBRTCC register matches the value in the HIBRTCM0 register and the value of the RTCSSC field matches the RTCSSM field in the HIBRTCSS register.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the RTCALT0 bit in the HIBIC register.
Register 7: Hibernation Masked Interrupt Status (HIBMIS), offset 0x01C

This register is the masked interrupt status for the Hibernation module interrupt sources. Bits in this register are the AND of the corresponding bits in the HIBRIS and HIBIM registers. When both corresponding bits are set, the bit in this register is set, and the interrupt is sent to the interrupt controller.

Hibernation Masked Interrupt Status (HIBMIS)
Base 0x400F.C000
Offset 0x01C
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>WC</td>
<td>RO</td>
<td>0</td>
<td>Write Complete/Capable Masked Interrupt Status</td>
</tr>
<tr>
<td>3</td>
<td>EXTW</td>
<td>RO</td>
<td>0</td>
<td>External Wake-Up Masked Interrupt Status</td>
</tr>
<tr>
<td>2</td>
<td>LOWBAT</td>
<td>RO</td>
<td>0</td>
<td>Low Battery Voltage Masked Interrupt Status</td>
</tr>
<tr>
<td>1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>RTCALT0</td>
<td>RO</td>
<td>0</td>
<td>RTC Alert 0 Masked Interrupt Status</td>
</tr>
</tbody>
</table>

- **Value** Description
  - 0  An RTC match interrupt has not occurred or is masked.
  - 1  An unmasked interrupt was signaled due to an RTC match.

This bit is cleared by writing a 1 to the RTCALT0 bit in the HIBC register.
Register 8: Hibernation Interrupt Clear (HIBIC), offset 0x020

This register is the interrupt write-one-to-clear register for the Hibernation module interrupt sources. Writing a 1 to a bit clears the corresponding interrupt in the HIBRIS register.

Hibernation Interrupt Clear (HIBIC)
Base 0x400F.C000
Offset 0x020
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>WC</td>
<td>RW1C</td>
<td>0</td>
<td>Write Complete/Capable Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the WC bit in the HIBRIS and HIBMIS registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reads return the raw interrupt status.</td>
</tr>
<tr>
<td>3</td>
<td>EXTW</td>
<td>RW1C</td>
<td>0</td>
<td>External Wake-Up Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the EXTW bit in the HIBRIS and HIBMIS registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reads return the raw interrupt status.</td>
</tr>
<tr>
<td>2</td>
<td>LOWBAT</td>
<td>RW1C</td>
<td>0</td>
<td>Low Battery Voltage Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the LOWBAT bit in the HIBRIS and HIBMIS registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reads return the raw interrupt status.</td>
</tr>
<tr>
<td>1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>RTCALT0</td>
<td>RW1C</td>
<td>0</td>
<td>RTC Alert0 Masked Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the RTCALT0 bit in the HIBRIS and HIBMIS registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reads return the raw interrupt status.</td>
</tr>
</tbody>
</table>

Note: The timer interrupt source cannot be cleared if the RTC value and the HIBRTC0 register / RTCMS field values are equal. The match interrupt takes priority over the interrupt clear.
Register 9: Hibernation RTC Trim (HIBRTCT), offset 0x024

This register contains the value that is used to trim the RTC clock predivider. It represents the computed underflow value that is used during the trim cycle. It is represented as 0x7FFF ± N clock cycles, where N is the number of clock cycles to add or subtract every 64 seconds in RTC mode.

**Note:** The Hibernation module registers are on the Hibernation module clock domain and have special timing requirements. Software should make use of the WRC bit in the HIBCTL register to ensure that the required timing gap has elapsed. If the WRC bit is clear, any attempted write access is ignored. See “Register Access Timing” on page 505.

Hibernation RTC Trim (HIBRTCT)
Base 0x400F.C000
Offset 0x024
Type RW, reset 0x0000.7FFF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>TRIM</td>
<td>RW</td>
<td>0x7FFF</td>
<td>RTC Trim Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This value is loaded into the RTC predivider every 64 seconds in RTC counter mode. It is used to adjust the RTC rate to account for drift and inaccuracy in the clock source. Compensation can be adjusted by software by moving the default value of 0x7FFF up or down. Moving the value up slows down the RTC and moving the value down speeds up the RTC.</td>
</tr>
</tbody>
</table>
Register 10: Hibernation RTC Sub Seconds (HIBRTCSS), offset 0x028

This register contains the RTC sub seconds counter and match values. The RTC value can be read by first reading the HIBRTCC register, reading the RTCSSC field in the HIBRTCSS register, and then rereading the HIBRTCC register. If the two values for HIBRTCC are equal, the read is valid.

Note: The Hibernation module registers are on the Hibernation module clock domain and have special timing requirements. Software should make use of the WRC bit in the HIBCTL register to ensure that the required timing gap has elapsed. If the WRC bit is clear, any attempted write access is ignored. See “Register Access Timing” on page 505.

Hibernation RTC Sub Seconds (HIBRTCSS)
Base 0x400F.C000
Offset 0x028
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>30:16</td>
<td>RTCSSM</td>
<td>RW</td>
<td>0x0000</td>
<td>RTC Sub Seconds Match</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A write loads the value into the RTC sub seconds match register in</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1/32,768 of a second increments.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A read returns the current 1/32,768 seconds match value.</td>
</tr>
<tr>
<td>15</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>14:0</td>
<td>RTCSSC</td>
<td>RO</td>
<td>0x0000</td>
<td>RTC Sub Seconds Count</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A read returns the sub second RTC count in 1/32,768 seconds.</td>
</tr>
</tbody>
</table>
Register 11: Hibernation Data (HIBDATA), offset 0x030-0x06F

This address space is implemented as a 16x32-bit memory (64 bytes). It can be loaded by the system processor in order to store state information and retains its state during a power cut operation as long as a battery is present.

**Note:** The Hibernation module registers are on the Hibernation module clock domain and have special timing requirements. Software should make use of the WRC bit in the HIBCTL register to ensure that the required timing gap has elapsed. If the WRC bit is clear, any attempted write access is ignored. See “Register Access Timing” on page 505.

**Note:** If V<sub>DD</sub> is arbitrarily removed while a HIBDATA register write operation is in progress, the write operation must be retried after V<sub>DD</sub> is reapplied.

Hibernation Data (HIBDATA)

<table>
<thead>
<tr>
<th>Base 0x400F.C000</th>
<th>Offset 0x030-0x06F</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RW, reset -</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>RTD</td>
<td>RW</td>
<td>-</td>
<td>Hibernation Module NV Data</td>
</tr>
</tbody>
</table>


8 Internal Memory

The TM4C123GH6PZ microcontroller comes with 32 KB of bit-banded SRAM, internal ROM, 256 KB of Flash memory, and 2KB of EEPROM. The Flash memory controller provides a user-friendly interface, making Flash memory programming a simple task. Flash memory is organized in 1-KB independently erasable blocks and memory protection can be applied to the Flash memory on a 2-KB block basis. The EEPROM module provides a well-defined register interface to support accesses to the EEPROM with both a random access style of read and write as well as a rolling or sequential access scheme. A password model allows the application to lock one or more EEPROM blocks to control access on 16-word boundaries.

8.1 Block Diagram

Figure 8-1 on page 534 illustrates the internal SRAM, ROM, and Flash memory blocks and control logic. The dashed boxes in the figure indicate registers residing in the System Control module.

Figure 8-1. Internal Memory Block Diagram
Figure 8-2 on page 535 illustrates the internal EEPROM block and control logic. The EEPROM block is connected to the AHB bus.

**Figure 8-2. EEPROM Block Diagram**

8.2 Functional Description

This section describes the functionality of the SRAM, ROM, Flash, and EEPROM memories.

**Note:** The μDMA controller can transfer data to and from the on-chip SRAM. However, because the Flash memory and ROM are located on a separate internal bus, it is not possible to transfer data from the Flash memory or ROM with the μDMA controller.

8.2.1 SRAM

The internal SRAM of the TM4C123GH6PZ device is located at address 0x2000.0000 of the device memory map. To reduce the number of time consuming read-modify-write (RMW) operations, ARM provides bit-banding technology in the processor. With a bit-band-enabled processor, certain regions in the memory map (SRAM and peripheral space) can use address aliases to access individual bits in a single, atomic operation. The bit-band base is located at address 0x2200.0000.

The bit-band alias is calculated by using the formula:

\[
\text{bit-band alias} = \text{bit-band base} + (\text{byte offset} \times 32) + (\text{bit number} \times 4)
\]

For example, if bit 3 at address 0x2000.1000 is to be modified, the bit-band alias is calculated as:

\[
0x2200.0000 + (0x1000 \times 32) + (3 \times 4) = 0x2202.000C
\]

With the alias address calculated, an instruction performing a read/write to address 0x2202.000C allows direct access to only bit 3 of the byte at address 0x2000.1000.

For details about bit-banding, see “Bit-Banding” on page 97.
Note: The SRAM is implemented using two 32-bit wide SRAM banks (separate SRAM arrays). The banks are partitioned such that one bank contains all even words (the even bank) and the other contains all odd words (the odd bank). A write access that is followed immediately by a read access to the same bank incurs a stall of a single clock cycle. However, a write to one bank followed by a read of the other bank can occur in successive clock cycles without incurring any delay.

8.2.2 ROM

The internal ROM of the TM4C123GH6PZ device is located at address 0x0100.0000 of the device memory map. Detailed information on the ROM contents can be found in the Tiva™ C Series TM4C123x ROM User’s Guide (literature number SPMU367).

The ROM contains the following components:

- TivaWare™ Boot Loader and vector table
- TivaWare Peripheral Driver Library (DriverLib) release for product-specific peripherals and interfaces
- Advanced Encryption Standard (AES) cryptography tables
- Cyclic Redundancy Check (CRC) error detection functionality

The boot loader is used as an initial program loader (when the Flash memory is empty) as well as an application-initiated firmware upgrade mechanism (by calling back to the boot loader). The Peripheral Driver Library APIs in ROM can be called by applications, reducing Flash memory requirements and freeing the Flash memory to be used for other purposes (such as additional features in the application). Advanced Encryption Standard (AES) is a publicly defined encryption standard used by the U.S. Government and Cyclic Redundancy Check (CRC) is a technique to validate if a block of data has the same contents as when previously checked.

8.2.2.1 Boot Loader Overview

The TivaWare Boot Loader is used to download code to the Flash memory of a device without the use of a debug interface. When the core is reset, the user has the opportunity to direct the core to execute the ROM Boot Loader or the application in Flash memory by using any GPIO signal in Ports A-H as configured in the Boot Configuration (BOOTCFG) register (see page 591).

At reset, the following sequence is performed:

1. The BOOTCFG register is read. If the EN bit is clear, the ROM Boot Loader is executed.

2. In the ROM Boot Loader, the status of the specified GPIO pin is compared with the specified polarity. If the status matches the specified polarity, the ROM is mapped to address 0x0000.0000 and execution continues out of the ROM Boot Loader.

3. If the EN bit is set or the status doesn't match the specified polarity, the data at address 0x0000.0004 is read, and if the data at this address is 0xFFFF.FFFF, the ROM is mapped to address 0x0000.0000 and execution continues out of the ROM Boot Loader.

4. If there is data at address 0x0000.0004 that is not 0xFFFF.FFFF, the stack pointer (SP) is loaded from Flash memory at address 0x0000.0000 and the program counter (PC) is loaded from address 0x0000.0004. The user application begins executing.
The boot loader uses a simple packet interface to provide synchronous communication with the device. The speed of the boot loader is determined by the internal oscillator (PIOSC) frequency as it does not enable the PLL. The following serial interfaces can be used:

- UART0
- SSIO
- I²C0
- USB

The data format and communication protocol are identical for the UART0, SSIO, and I²C0 interfaces.

**Note:** The Flash-memory-resident version of the boot loader also supports CAN.

See the *TivaWare™ Boot Loader for C Series User's Guide (literature number SPMU301)* for information on the boot loader software. The USB boot loader uses the standard Device Firmware Upgrade USB device class.

**Considerations When Using the UART Boot Loader in ROM**

U0Tx is not driven by the ROM boot loader until the auto-bauding process has completed. If U0Tx is floating during this time, the receiver it is connected to may see transitions on the signal, which could be interpreted by its UART as valid characters. To handle this situation, put a pull-up or pull-down on U0Tx, providing a defined state for the signal until the ROM boot loader begins driving U0Tx. A pull-up is preferred as it indicates that the UART is idle, rather than a pull-down, which indicates a break condition.

### 8.2.2.2 TivaWare Peripheral Driver Library

The TivaWare Peripheral Driver Library contains a file called `driverlib/rom.h` that assists with calling the peripheral driver library functions in the ROM. The detailed description of each function is available in the *Tiva™ C Series TM4C123x ROM User's Guide (literature number SPMU367)*. See the "Using the ROM" chapter of the *TivaWare™ Peripheral Driver Library for C Series User's Guide (literature number SPMU298)* for more details on calling the ROM functions and using `driverlib/rom.h`. The `driverlib/rom_map.h` header file is also provided to aid portability when using different Tiva™ C Series devices which might have a different subset of DriverLib functions in ROM. The `driverlib/rom_map.h` header file uses build-time labels to route function calls to the ROM if those functions are available on a given device, otherwise, it routes to Flash-resident versions of the functions.

A table at the beginning of the ROM points to the entry points for the APIs that are provided in the ROM. Accessing the API through these tables provides scalability; while the API locations may change in future versions of the ROM, the API tables will not. The tables are split into two levels; the main table contains one pointer per peripheral which points to a secondary table that contains one pointer per API that is associated with that peripheral. The main table is located at 0x0100.0010, right after the Cortex-M4F vector table in the ROM.

DriverLib functions are described in detail in the *TivaWare™ Peripheral Driver Library for C Series User's Guide (literature number SPMU298)*.

Additional APIs are available for graphics and USB functions, but are not preloaded into ROM. The TivaWare Graphics Library provides a set of graphics primitives and a widget set for creating graphical user interfaces on Tiva™ C Series microcontroller-based boards that have a graphical display (for more information, see the *TivaWare™ Graphics Library for C Series User's Guide (literature number SPMU300)*). The TivaWare USB Library is a set of data types and functions for creating USB Device,
Host or On-The-Go (OTG) applications on Tiva™ C Series microcontroller-based boards (for more information, see the TivaWare™ USB Library for C Series User’s Guide (literature number SPMU297)).

8.2.2.3 Advanced Encryption Standard (AES) Cryptography Tables

AES is a strong encryption method with reasonable performance and size. AES is fast in both hardware and software, is fairly easy to implement, and requires little memory. AES is ideal for applications that can use prearranged keys, such as setup during manufacturing or configuration. Four data tables used by the XySSL AES implementation are provided in the ROM. The first is the forward S-box substitution table, the second is the reverse S-box substitution table, the third is the forward polynomial table, and the final is the reverse polynomial table. See the Tiva™ C Series TM4C123x ROM User’s Guide (literature number SPMU367) for more information on AES.

8.2.2.4 Cyclic Redundancy Check (CRC) Error Detection

The CRC technique can be used to validate correct receipt of messages (nothing lost or modified in transit), to validate data after decompression, to validate that Flash memory contents have not been changed, and for other cases where the data needs to be validated. A CRC is preferred over a simple checksum (for example, XOR all bits) because it catches changes more readily. See the Tiva™ C Series TM4C123x ROM User’s Guide (literature number SPMU367) for more information on CRC.

8.2.3 Flash Memory

At system clock speeds of 40 MHz and below, the Flash memory is read in a single cycle. The Flash memory is organized as a set of 1-KB blocks that can be individually erased. An individual 32-bit word can be programmed to change bits from 1 to 0. In addition, a write buffer provides the ability to program 32 continuous words in Flash memory in half the time of programming the words individually. Erasing a block causes the entire contents of the block to be reset to all 1s. The 1-KB blocks are paired into sets of 2-KB blocks that can be individually protected. The protection allows blocks to be marked as read-only or execute-only, providing different levels of code protection. Read-only blocks cannot be erased or programmed, protecting the contents of those blocks from being modified. Execute-only blocks cannot be erased or programmed and can only be read by the controller instruction fetch mechanism, protecting the contents of those blocks from being read by either the controller or a debugger.

8.2.3.1 Prefetch Buffer

The Flash memory controller has a prefetch buffer that is automatically used when the CPU frequency is greater than 40 MHz. In this mode, the Flash memory operates at half of the system clock. The prefetch buffer fetches two 32-bit words per clock allowing instructions to be fetched with no wait states while code is executing linearly. The fetch buffer includes a branch speculation mechanism that recognizes a branch and avoids extra wait states by not reading the next word pair. Also, short loop branches often stay in the buffer. As a result, some branches can be executed with no wait states. Other branches incur a single wait state.

8.2.3.2 Flash Memory Protection

The user is provided two forms of Flash memory protection per 2-KB Flash memory block in four pairs of 32-bit wide registers. The policy for each protection form is controlled by individual bits (per policy per block) in the FMPPEn and FMPREn registers.
Flash Memory Protection Program Enable (FMPPEn): If a bit is set, the corresponding block may be programmed (written) or erased. If a bit is cleared, the corresponding block may not be changed.

Flash Memory Protection Read Enable (FMPREn): If a bit is set, the corresponding block may be executed or read by software or debuggers. If a bit is cleared, the corresponding block may only be executed, and contents of the memory block are prohibited from being read as data.

The policies may be combined as shown in Table 8-1 on page 539.

<table>
<thead>
<tr>
<th>Protection</th>
<th>FMPPEn</th>
<th>FMPREn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Execute-only protection. The block may only be executed and may not be written or erased. This mode is used to protect code.</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>The block may be written, erased or executed, but not read. This combination is unlikely to be used.</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Read-only protection. The block may be read or executed but may not be written or erased. This mode is used to lock the block from further modification while allowing any read or execute access.</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>No protection. The block may be written, erased, executed or read.</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

A Flash memory access that attempts to read a read-protected block (FMPREn bit is set) is prohibited and generates a bus fault. A Flash memory access that attempts to program or erase a program-protected block (FMPPEn bit is set) is prohibited and can optionally generate an interrupt (by setting the AMASK bit in the Flash Controller Interrupt Mask (FCIM) register) to alert software developers of poorly behaving software during the development and debug phases.

The factory settings for the FMPREn and FMPPEn registers are a value of 1 for all implemented banks. These settings create a policy of open access and programmability. The register bits may be changed by clearing the specific register bit. The changes are effective immediately, but are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The changes are committed using the Flash Memory Control (FMC) register. Details on programming these bits are discussed in “Non-Volatile Register Programming” on page 542.

### 8.2.3.3 Execute-Only Protection

Execute-only protection prevents both modification and visibility to a protected flash block. This mode is intended to be used in situations where a device requires debug capability, yet portions of the application space must be protected from external access. An example of this is a company who wishes to sell Tiva™ C Series devices with their proprietary software preprogrammed, yet allow the end user to add custom code to an unprotected region of the flash (such as a motor control module with a customizable motor configuration section in flash).

Literal data introduces a complication to the protection mechanism. When C code is compiled and linked, literal data (constants, and so on) is typically placed in the text section, between functions, by the compiler. The literal data is accessed at run time through the use of the LDR instruction, which loads the data from memory using a PC-relative memory address. The execution of the LDR instruction generates a read transaction across the Cortex-M3’s DCode bus, which is subject to the execute-only protection mechanism. If the accessed block is marked as execute only, the transaction is blocked, and the processor is prevented from loading the constant data and, therefore, inhibiting correct execution. Therefore, using execute-only protection requires that literal data be handled differently. There are three ways to address this:
1. Use a compiler that allows literal data to be collected into a separate section that is put into one or more read-enabled flash blocks. Note that the LDR instruction may use a PC-relative address—in which case the literal pool cannot be located outside the span of the offset—or the software may reserve a register to point to the base address of the literal pool and the LDR offset is relative to the beginning of the pool.

2. Use a compiler that generates literal data from arithmetic instruction immediate data and subsequent computation.

3. Use method 1 or 2, but in assembly language, if the compiler does not support either method.

8.2.3.4 Read-Only Protection

Read-only protection prevents the contents of the flash block from being re-programmed, while still allowing the content to be read by processor or the debug interface. Note that if a FMPREn bit is cleared, all read accesses to the Flash memory block are disallowed, including any data accesses. Care must be taken not to store required data in a Flash memory block that has the associated FMPREn bit cleared.

The read-only mode does not prevent read access to the stored program, but it does provide protection against accidental (or malicious) erasure or programming. Read-only is especially useful for utilities like the boot loader when the debug interface is permanently disabled. In such combinations, the boot loader, which provides access control to the Flash memory, is protected from being erased or modified.

8.2.3.5 Permanently Disabling Debug

For extremely sensitive applications, the debug interface to the processor and peripherals can be permanently disabled, blocking all accesses to the device through the JTAG or SWD interfaces. With the debug interface disabled, it is still possible to perform standard IEEE instructions (such as boundary scan operations), but access to the processor and peripherals is blocked.

The DBG0 and DBG1 bits of the Boot Configuration (BOOTCFG) register control whether the debug interface is turned on or off.

The debug interface should not be permanently disabled without providing some mechanism—such as the boot loader—to provide customer-installable updates or bug fixes. Disabling the debug interface is permanent and cannot be reversed.

8.2.3.6 Interrupts

The Flash memory controller can generate interrupts when the following conditions are observed:

- Programming Interrupt - signals when a program or erase action is complete.
- Access Interrupt - signals when a program or erase action has been attempted on a 2-kB block of memory that is protected by its corresponding FMPPEn bit.

The interrupt events that can trigger a controller-level interrupt are defined in the Flash Controller Masked Interrupt Status (FCMIS) register (see page 559) by setting the corresponding MASK bits. If interrupts are not used, the raw interrupt status is always visible via the Flash Controller Raw Interrupt Status (FCRIS) register (see page 556).

Interrupts are always cleared (for both the FCMIS and FCRIS registers) by writing a 1 to the corresponding bit in the Flash Controller Masked Interrupt Status and Clear (FCMISC) register (see page 561).
8.2.3.7 Flash Memory Programming

The Tiva™ C Series devices provide a user-friendly interface for Flash memory programming. All erase/program operations are handled via three registers: Flash Memory Address (FMA), Flash Memory Data (FMD), and Flash Memory Control (FMC). Note that if the debug capabilities of the microcontroller have been deactivated, resulting in a "locked" state, a recovery sequence must be performed in order to reactivate the debug module. See "Recovering a "Locked" Microcontroller” on page 205.

During a Flash memory operation (write, page erase, or mass erase) access to the Flash memory is inhibited. As a result, instruction and literal fetches are held off until the Flash memory operation is complete. If instruction execution is required during a Flash memory operation, the code that is executing must be placed in SRAM and executed from there while the flash operation is in progress.

**Note:** When programming Flash memory, the following characteristics of the memory must be considered:

- Only an erase can change bits from 0 to 1.
- A write can only change bits from 1 to 0. If the write attempts to change a 0 to a 1, the write fails and no bits are changed.
- A flash operation can be started before entering the Sleep or Deep-Sleep mode (using the wait for interrupt instruction, WFI). It can also be completed while in Sleep or Deep-Sleep. If the Flash program/erase event comes in succession to EEPROM access, the Flash event gets completed after waking from Sleep/Deep-Sleep and is started after the wake-up.

8.2.3.8 Basic Program / Erase Operations

**To program a 32-bit word**

1. Write source data to the FMD register.
2. Write the target address to the FMA register.
3. Write the Flash memory write key and the WRITE bit to the FMC register. Depending on the value of the KEY bit in the BOOTCFG register, the value 0xA442 or 0x71D5 must be written into the WRKEY field for a Flash memory write to occur.
4. Poll the FMC register until the WRITE bit is cleared.

**To perform an erase of a 1-KB page**

1. Write the page address to the FMA register.
2. Write the Flash memory write key and the ERASE bit to the FMC register. Depending on the value of the KEY bit in the BOOTCFG register, the value 0xA442 or 0x71D5 must be written into the WRKEY field for a Flash memory write to occur.
3. Poll the FMC register until the ERASE bit is cleared or, alternatively, enable the programming interrupt using the PMASK bit in the FCIM register.
To perform a mass erase of the Flash memory

1. Write the Flash memory write key and the MEREASE bit to the FMC register. Depending on the value of the KEY bit in the BOOTCFG register, the value 0xA442 or 0x71D5 must be written into the WRKEY field for a Flash memory write to occur.

2. Poll the FMC register until the MEREASE bit is cleared or, alternatively, enable the programming interrupt using the PMASK bit in the FCIM register.

8.2.3.9 32-Word Flash Memory Write Buffer

A 32-word write buffer provides the capability to perform faster write accesses to the Flash memory by programming 2 32-bit words at a time, allowing 32 words to be programmed in the same time as 16 would take using the method described above. The data for the buffered write is written to the Flash Write Buffer (FWBn) registers.

The registers are 32-word aligned with Flash memory, and therefore the register FWB0 corresponds with the address in FMA where bits [6:0] of FMA are all 0. FWB1 corresponds with the address in FMA + 0x4 and so on. Only the FWBn registers that have been updated since the previous buffered Flash memory write operation are written. The Flash Write Buffer Valid (FWBVAL) register shows which registers have been written since the last buffered Flash memory write operation. This register contains a bit for each of the 32 FWBn registers, where bit[n] of FWBVAL corresponds to FWBn. The FWBn register has been updated if the corresponding bit in the FWBVAL register is set.

To program 32 words with a single buffered Flash memory write operation

1. Write the source data to the FWBn registers.

2. Write the target address to the FMA register. This must be a 32-word aligned address (that is, bits [6:0] in FMA must be 0s).

3. Write the Flash memory write key and the WRBUF bit to the FMC2 register. Depending on the value of the KEY bit in the BOOTCFG register, the value 0xA442 or 0x71D5 must be written into the WRKEY field for a Flash memory write to occur.

4. Poll the FMC2 register until the WRBUF bit is cleared or wait for the PMIS interrupt to be signaled.

8.2.3.10 Non-Volatile Register Programming

Note: The Boot Configuration (BOOTCFG) register requires a POR before the committed changes take effect.

This section discusses how to update the registers shown in Table 8-2 on page 543 that are resident within the Flash memory itself. These registers exist in a separate space from the main Flash memory array and are not affected by an ERASE or MASS ERASE operation. With the exception of the Boot Configuration (BOOTCFG) register, the settings in these registers can be written, their functions verified, and their values read back before they are committed, at which point they become non-volatile. If a value in one of these registers has not been committed, a power-on reset restores the last committed value or the default value if the register has never been committed. Other types of reset have no effect. Once the register contents are committed, the only way to restore the factory default values is to perform the sequence described in “Recovering a "Locked" Microcontroller” on page 205.

To write to a non-volatile register:

- Bits can only be changed from 1 to 0.
For all registers except the **BOOTCFG** register, write the data to the register address provided in the register description. For the **BOOTCFG** register, write the data to the **FMD** register.

The registers can be read to verify their contents. To verify what is to be stored in the **BOOTCFG** register, read the **FMD** register. Reading the **BOOTCFG** register returns the previously committed value or the default value if the register has never been committed.

The new values are effectively immediately for all registers except **BOOTCFG**, as the new value for the register is not stored in the register until it has been committed.

Prior to committing the register value, a power-on reset restores the last committed value or the default value if the register has never been committed.

To commit a new value to a non-volatile register:

- Write the data as described above.
- Write to the **FMA** register the value shown in Table 8-2 on page 543.
- Write the Flash memory write key and set the **COMT** bit in the **FMC** register. These values must be written to the **FMC** register at the same time.

Committing a non-volatile register has the same timing as a write to regular Flash memory, defined by $T_{PROG64}$, as shown in Table 24-27 on page 1421. Software can poll the **COMT** bit in the **FMC** register to determine when the operation is complete, or an interrupt can be enabled by setting the **PMASK** bit in the **FCIM** register.

When committing the **BOOTCFG** register, the **INVDRIS** bit in the **FCRIS** register is set if a bit that has already been committed as a 0 is attempted to be committed as a 1.

Once the value has been committed, a power-on reset has no effect on the register contents.

Changes to the **BOOTCFG** register are effective after the next power-on reset.

Once the **NW** bit has been changed to 0 and committed, further changes to the **BOOTCFG** register are not allowed.

**Important:** After being committed, these registers can only be restored to their factory default values by performing the sequence described in “Recovering a "Locked" Microcontroller” on page 205. The mass erase of the main Flash memory array caused by the sequence is performed prior to restoring these registers.

<table>
<thead>
<tr>
<th>Register to be Committed</th>
<th>FMA Value</th>
<th>Data Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>FMPRE0</td>
<td>0x0000.0000</td>
<td>FMPRE0</td>
</tr>
<tr>
<td>FMPRE1</td>
<td>0x0000.0002</td>
<td>FMPRE1</td>
</tr>
<tr>
<td>FMPRE2</td>
<td>0x0000.0004</td>
<td>FMPRE2</td>
</tr>
<tr>
<td>FMPRE3</td>
<td>0x0000.0006</td>
<td>FMPRE3</td>
</tr>
<tr>
<td>FMPPE0</td>
<td>0x0000.0001</td>
<td>FMPPE0</td>
</tr>
<tr>
<td>FMPPE1</td>
<td>0x0000.0003</td>
<td>FMPPE1</td>
</tr>
<tr>
<td>FMPPE2</td>
<td>0x0000.0005</td>
<td>FMPPE2</td>
</tr>
<tr>
<td>FMPPE3</td>
<td>0x0000.0007</td>
<td>FMPPE3</td>
</tr>
</tbody>
</table>

**June 12, 2014**

**Texas Instruments-Production Data**
The TM4C123GH6PZ microcontroller includes an EEPROM with the following features:

- 2Kbytes of memory accessible as 512 32-bit words
- 32 blocks of 16 words (64 bytes) each
- Built-in wear leveling
- Access protection per block
- Lock protection option for the whole peripheral as well as per block using 32-bit to 96-bit unlock codes (application selectable)
- Interrupt support for write completion to avoid polling
- Endurance of 500K writes (when writing at fixed offset in every alternate page in circular fashion) to 15M operations (when cycling through two pages per each 2-page block).

8.2.4.1 Functional Description

The EEPROM module provides a well-defined register interface to support accesses to the EEPROM with both a random access style of read and write as well as a rolling or sequential access scheme.

A protection mechanism allows locking EEPROM blocks to prevent writes under a set of circumstances as well as reads under the same or different circumstances. The password model allows the application to lock one or more EEPROM blocks to control access on 16-word boundaries.

**Important:** The configuration of the system clock must not be changed while an EEPROM operation is in process. Software must wait until the **WORKING** bit in the **EEPROM Done Status (EEDONE)** register is clear before making any changes to the system clock.

**Blocks**

There are 32 blocks of 16 words each in the EEPROM. Bytes and half-words can be read, and these accesses do not have to occur on a word boundary. The entire word is read and any unneeded data is simply ignored. They are writable only on a word basis. To write a byte, it is necessary to read the word value, modify the appropriate byte, and write the word back.

Each block is addressable as an offset within the EEPROM, using a block select register. Each word is offset addressable within the selected block.

The current block is selected by the **EEPROM Current Block (EEBLOCK)** register. The current offset is selected and checked for validity by the **EEPROM Current Offset (EEOFFSET)** register. The application may write the **EEOFFSET** register any time, and it is also automatically incremented.
when the **EEPROM Read-Write with Increment (EERDWRINC)** register is accessed. However, the **EERDWRINC** register does not increment the block number, but instead wraps within the block.

Blocks are individually protectable. Attempts to read from a block for which the application does not have permission return 0xFFFF.FFFF. Attempts to write into a block for which the application does not have permission results in an error in the **EEDONE** register.

**Timing Considerations**

After enabling or resetting the EEPROM module, software must wait until the **WORKING** bit in the **EEDONE** register is clear before accessing any EEPROM registers.

In the event that there are Flash memory writes or erases and EEPROM writes active, it is possible for the EEPROM process to be interrupted by the Flash memory write/erase and then continue after the Flash memory write is completed. This action may change the amount of time that the EEPROM operation takes.

EEPROM operations must be completed before entering Sleep or Deep-Sleep mode. Ensure the EEPROM operations have completed by checking the **EEPROM Done Status (EEDONE)** register before issuing a **WFI** instruction to enter Sleep or Deep-Sleep.

Reads of words within a block are at direct speed, which means that wait states are automatically generated if the system clock is faster than the speed of the EEPROM. The read access time is specified in Table 24-28 on page 1421.

Writing the **EEOFFSET** register also does not incur any penalties.

Writing the **EEBLOCK** register is not delayed, but any attempt to access data within that block is delayed by 4 clocks after writing **EEBLOCK**. This time is used to load block specific information.

Writes to words within a block are delayed by a variable amount of time. The application may use an interrupt to be notified when the write is done, or alternatively poll for the done status in the **EEDONE** register. The variability ranges from the write timing of the EEPROM to the erase timing of EEPROM, where the erase timing is less than the write timing of most external EEPROMs.

**Locking and Passwords**

The EEPROM can be locked at both the module level and the block level. The lock is controlled by a password that is stored in the **EEPROM Password (EEPASSn)** registers and can be any 32-bit to 96-bit value other than all 1s. Block 0 is the master block, the password for block 0 protects the control registers as well as all other blocks. Each block can be further protected with a password for that block.

If a password is registered for block 0, then the whole module is locked at reset. The locking behavior is such that blocks 1 to 31 are inaccessible until block 0 is unlocked, and block 0 follows the rules defined by its protection bits. As a result, the **EEBLOCK** register cannot be changed from 0 until block 0 is unlocked.

A password registered with any block, including block 0, allows for protection rules that control access of that block based on whether it is locked or unlocked. Generally, the lock can be used to prevent write accesses when locked or can prevent read and write accesses when locked.

All password-protected blocks are locked at reset. To unlock a block, the correct password value must be written to the **EEPROM Unlock (EEUNLOCK)** register by writing to it one to three times to form the 32-bit, 64-bit, or 96-bit password registered using the **EEPASSn** register. The value used to configure the **EEPASS0** register must always be written last. For example, for a 96-bit password, the value used to configure the **EEPASS2** register must be written first, followed by the **EEPASS1** and the **EEPASS0** register values. A block or the module may be re-locked by writing 0xFFFF.FFFF to the **EEUNLOCK** register because 0xFFFF.FFFF is not a valid password.
Protection and Access Control

The protection bits provide discrete control of read and write access for each block which allows various protection models per block, including:

- Without password: Readable and writable at any time. This mode is the default when there is no password.
- Without password: Readable but not writable.
- With password: Readable, but only writable when unlocked by the password. This mode is the default when there is a password.
- With password: Readable or writable only when unlocked.
- With password: Readable only when unlocked, not writable.

Additionally, access protection may be applied based on the processor mode. This configuration allows for supervisor-only access or supervisor and user access, which is the default. Supervisor-only access mode also prevents access by the µDMA and Debugger.

Additionally, the master block may be used to control access protection for the protection mechanism itself. If access control for block 0 is for supervisor only, then the whole module may only be accessed in supervisor mode. In addition, the protection level for block 0 sets the minimum protection level for the entire EEPROM. For example, if the PROT field in the EEPROT register is configured to 0x1 for block 0, then block 1 could be configured with the PROT field to be 0x1, 0x2, or 0x3, but not 0x0.

Note that for blocks 1 to 31, they are inaccessible for read or write if block 0 has a password and it is not unlocked. If block 0 has a master password, then the strictest protection defined for block 0 or an individual block is implemented on the remaining blocks.

Hidden Blocks

Hiding provides a temporary form of protection. Every block except block 0 can be hidden, which prevents all accesses until the next reset.

This mechanism can allow a boot or initialization routine to access some data which is then made inaccessible to all further accesses. Because boot and initialization routines control the capabilities of the application, hidden blocks provide a powerful isolation of the data when debug is disabled.

A typical use model would be to have the initialization code store passwords, keys, and/or hashes to use for verification of the rest of the application. Once performed, the block is then hidden and made inaccessible until the next reset which then re-enters the initialization code.

Power and Reset Safety

Once the EEONE register indicates that a location has been successfully written, the data is retained until that location is written again. There is no power or reset race after the EEONE register indicates a write has completed.

Interrupt Control

The EEPROM module allows for an interrupt when a write completes to eliminate the need for polling. The interrupt can be used to drive an application ISR which can then write more words or verify completion. The interrupt mechanism is used any time the EEONE register goes from working to done, whether because of an error or the successful completion of a program or erase operation. This interrupt mechanism works for data writes, writes to password and protection registers, forced erase by the EEPROM Support Control and Status (EESUPP) register, and mass erase using
the EEPROM Debug Mass Erase (EEDGBME) register. The EEPROM interrupt is signaled to the core using the Flash memory interrupt vector. Software can determine that the source of the interrupt was the EEPROM by examining bit 2 of the Flash Controller Masked Interrupt Status and Clear (FCMSC) register.

**Theory of Operation**

The EEPROM operates using a traditional Flash bank model which implements EEPROM-type cells, but uses sector erase. Additionally, words are replicated in the pages to allow 500K+ erase cycles when needed, which means that each word has a latest version. As a result, a write creates a new version of the word in a new location, making the previous value obsolete.

Each sector contains two blocks. Each block contains locations for the active copy plus six redundant copies. Passwords, protection bits, and control data are all stored in the pages.

When a page runs out of room to store the latest version of a word, a copy buffer is used. The copy buffer copies the latest words of each block. The original page is then erased. Finally, the copy buffer contents are copied back to the page. This mechanism ensures that data cannot be lost due to power down, even during an operation. The EEPROM mechanism properly tracks all state information to provide complete safety and protection. Although it should not normally be possible, errors during programming can occur in certain circumstances, for example, the voltage rail dropping during programming. In these cases, the EESUPP register can be used to finish an operation as described in the section called “Error During Programming” on page 547.

**Manual Copy Buffer Erase**

The copy buffer is only used when a main block is full because a word has been written seven times and there is no more room to store its latest version. In this situation, the latest versions of all the words in the block are copied to the copy buffer, allowing the main block to be erased safely, providing power down safety. If the copy buffer itself is full, then it must first be erased, which adds extra time. By performing a manual erase of the copy buffer, this overhead does not occur during a future write access. The ERQ bit in the EESUPP register is set if the copy buffer must be erased. If so, the START bit can be written by the application to force the erase at a more convenient time. The EEDONE and EEINT registers can be used to detect completion.

**Debug Mass Erase**

The EEPROM debug mass erase allows the developer to mass erase the EEPROM. For the mass erase to occur correctly, there can be no active EEPROM operations. After the last EEPROM operation, the application must ensure that no EEPROM registers are updated, including modifying the EEBLOCK and the EEOFFSET registers without doing an actual read or write operation. To hold off these operations, the application should reset the EEPROM module by setting the R0 bit in the EEPROM Software Reset (SREEPROM) register, wait until WORKING bit in the EEPROM Done Status (EEDONE) register is clear, and then enable the debug mass erase by setting the ME bit in the EEPROM Debug Mass Erase (EEDBGME) register.

**Error During Programming**

Operations such as data-write, password set, protection set, and copy buffer erase may perform multiple operations. For example, a normal write performs two underlying writes: the control word write and the data write. If the control word writes but the data fails (for example, due to a voltage drop), the overall write fails with indication provided in the EEDONE register. Failure and the corrective action is broken down by the type of operation:

- If a normal write fails such that the control word is written but the data fails to write, the safe course of action is to retry the operation once the system is otherwise stable, for example, when
the voltage is stabilized. After the retry, the control word and write data are advanced to the next location.

- If a password or protection write fails, the safe course of action is to retry the operation once the system is otherwise stable. In the event that multi-word passwords may be written outside of a manufacturing or bring-up mode, care must be taken to ensure all words are written in immediate succession. If not, then partial password unlock would need to be supported to recover.

- If the word write requires the block to be written to the copy buffer, then it is possible to fail or lose power during the subsequent operations. A control word mechanism is used to track what step the EEPROM was in if a failure occurs. If not completed, the EESUPP register indicates the partial completion, and the EESUPP_START bit can be written to allow it to continue to completion.

- If a copy buffer erase fails or power is lost while erasing, the EESUPP register indicates it is not complete and allows it to be restarted.

After a reset and prior to writing any data to the EEPROM, software must read the EESUPP register and check for the presence of any error condition which may indicate that a write or erase was in progress when the system was reset due to a voltage drop. If either the PRETRY or ERETRY bits are set, the peripheral should be reset by setting and then clearing the R0 bit in the EEPROM Software Reset (SREEEPROM) register and waiting for the WORKING bit in the EEDONE register to clear before again checking the EESUPP register for error indicators. This procedure should allow the EEPROM to recover from the write or erase error. In very isolated cases, the EESUPP register may continue to register an error after this operation, in which case the reset should be repeated. After recovery, the application should rewrite the data which was being programmed when the initial failure occurred.

**Soft Reset Handling**

The following soft resets should not be asserted during an EEPROM program or erase operation:

- Software reset (SYSRESREQ)
- Software peripheral reset
- Watchdog reset
- MOSC failure reset

The WORKING bit of the EEDONE register can be checked before the reset is asserted to see if an EEPROM program or erase operation is occurring. Soft resets may occur when using a debugger and should be avoided during an EEPROM operation. A reset such as the Watchdog reset can be mapped to an external reset using a GPIO, or Hibernate can be entered, if time is not a concern.

**Endurance**

Endurance is per meta-block which is 2 blocks. Endurance is measured in two ways:

1. To the application, it is the number of writes that can be performed.
2. To the microcontroller, it is the number of erases that can be performed on the meta-block.

Because of the second measure, the number of writes depends on how the writes are performed. For example:
One word can be written more than 500K times, but, these writes impact the meta-block that the word is within. As a result, writing one word 500K times, then trying to write a nearby word 500K times is not assured to work. To ensure success, the words should be written more in parallel.

All words can be written in a sweep with a total of more than 500K sweeps which updates all words more than 500K times.

Different words can be written such that any or all words can be written more than 500K times when write counts per word stay about the same. For example, offset 0 could be written 3 times, then offset 1 could be written 2 times, then offset 2 is written 4 times, then offset 1 is written twice, then offset 0 is written again. As a result, all 3 offsets would have 4 writes at the end of the sequence. This kind of balancing within 7 writes maximizes the endurance of different words within the same meta-block.

8.2.4.2 EEPROM Initialization and Configuration

Before writing to any EEPROM registers, the clock to the EEPROM module must be enabled through the EEPROM Run Mode Clock Gating Control (RCGCEEPROM) register (see page 359) and the following initialization steps must be executed:

1. Insert delay (6 cycles plus function call overhead).

2. Poll the WORKING bit in the EEPROM Done Status (EEDONE) register until it is clear, indicating that the EEPROM has completed its power-on initialization. When WORKING=0, continue.

3. Read the PRETRY and ERETRY bits in the EEPROM Support Control and Status (EESUPP) register. If either of the bits are set, return an error, else continue.

4. Reset the EEPROM module using the EEPROM Software Reset (SREEPROM) register at offset 0x558 in the System Control register space.

5. Insert delay (6 cycles plus function call overhead).

6. Poll the WORKING bit in the EEPROM Done Status (EEDONE) register to determine when it is clear. When WORKING=0, continue.

7. Read the PRETRY and ERETRY bits in the EESUPP register. If either of the bits are set, return an error, else the EEPROM initialization is complete and software may use the peripheral as normal.

Important: Failure to perform these initialization steps after a reset may lead to incorrect operation or permanent data loss if the EEPROM is later written.

If the PRETRY or ERETRY bits are set in the EESUPP register, the EEPROM was unable to recover its state. If power is stable when this occurs, this indicates a fatal error and is likely an indication that the EEPROM memory has exceeded its specified lifetime write/erase specification. If the supply voltage is unstable when this return code is observed, retrying the operation once the voltage is stabilized may clear the error.

The EEPROM initialization function code is named EEPROMinit( ) in TivaWare, which can be downloaded from http://www.ti.com/tivaware.
## 8.3 Register Map

Table 8-3 on page 550 lists the ROM Controller register and the Flash memory and control registers. The offset listed is a hexadecimal increment to the particular memory controller's base address. The Flash memory register offsets are relative to the Flash memory control base address of 0x400F.D000. The EEPROM registers are relative to the EEPROM base address of 0x400A.F000. The ROM and Flash memory protection register offsets are relative to the System Control base address of 0x400F.E000.

### Table 8-3. Flash Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Flash Memory Registers (Flash Control Offset)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x000</td>
<td>FMA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Flash Memory Address</td>
<td>552</td>
</tr>
<tr>
<td>0x004</td>
<td>FMD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Flash Memory Data</td>
<td>553</td>
</tr>
<tr>
<td>0x008</td>
<td>FMC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Flash Memory Control</td>
<td>554</td>
</tr>
<tr>
<td>0x00C</td>
<td>FCRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Flash Controller Raw Interrupt Status</td>
<td>556</td>
</tr>
<tr>
<td>0x010</td>
<td>FCIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Flash Controller Interrupt Mask</td>
<td>559</td>
</tr>
<tr>
<td>0x014</td>
<td>FCMiSC</td>
<td>RW/RO</td>
<td>0x0000.0000</td>
<td>Flash Controller Masked Interrupt Status and Clear</td>
<td>561</td>
</tr>
<tr>
<td>0x020</td>
<td>FMC2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Flash Memory Control 2</td>
<td>564</td>
</tr>
<tr>
<td>0x030</td>
<td>FWBVAL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Flash Write Buffer Valid</td>
<td>565</td>
</tr>
<tr>
<td>0x100 - 0x17C</td>
<td>FWBn</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Flash Write Buffer n</td>
<td>566</td>
</tr>
<tr>
<td>0xFC0</td>
<td>FSIZE</td>
<td>RO</td>
<td>0x0000.007F</td>
<td>Flash Size</td>
<td>567</td>
</tr>
<tr>
<td>0xFC4</td>
<td>SSIZE</td>
<td>RO</td>
<td>0x0000.007F</td>
<td>SRAM Size</td>
<td>568</td>
</tr>
<tr>
<td>0xFCC</td>
<td>ROMSWMAP</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>ROM Software Map</td>
<td>569</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EEPROM Registers (EEPROM Control Offset)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x000</td>
<td>EESIZE</td>
<td>RO</td>
<td>0x0020.0200</td>
<td>EEPROM Size Information</td>
<td>570</td>
</tr>
<tr>
<td>0x004</td>
<td>EEBLOCK</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Current Block</td>
<td>571</td>
</tr>
<tr>
<td>0x008</td>
<td>EEOFFSET</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Current Offset</td>
<td>572</td>
</tr>
<tr>
<td>0x010</td>
<td>EERDWR</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Read-Write</td>
<td>573</td>
</tr>
<tr>
<td>0x014</td>
<td>EERDWRINC</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Read-Write with Increment</td>
<td>574</td>
</tr>
<tr>
<td>0x018</td>
<td>EEDONE</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>EEPROM Done Status</td>
<td>575</td>
</tr>
<tr>
<td>0x01C</td>
<td>EESUPP</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Support Control and Status</td>
<td>577</td>
</tr>
<tr>
<td>0x020</td>
<td>EEUNLOCK</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Unlock</td>
<td>579</td>
</tr>
<tr>
<td>0x030</td>
<td>EEPROT</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Protection</td>
<td>580</td>
</tr>
<tr>
<td>0x034</td>
<td>EEPASS0</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Password</td>
<td>582</td>
</tr>
<tr>
<td>0x038</td>
<td>EE PASS1</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Password</td>
<td>582</td>
</tr>
<tr>
<td>0x03C</td>
<td>EE PASS2</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Password</td>
<td>582</td>
</tr>
</tbody>
</table>
### Table 8-3. Flash Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x040</td>
<td>EEINT</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Interrupt</td>
<td>583</td>
</tr>
<tr>
<td>0x050</td>
<td>EEHIDE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Block Hide</td>
<td>584</td>
</tr>
<tr>
<td>0x080</td>
<td>EEDBGMKE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>EEPROM Debug Mass Erase</td>
<td>585</td>
</tr>
<tr>
<td>0xFC0</td>
<td>EEPROMPP</td>
<td>RO</td>
<td>0x0000.001F</td>
<td>EEPROM Peripheral Properties</td>
<td>586</td>
</tr>
</tbody>
</table>

#### Memory Registers (System Control Offset)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0F0</td>
<td>RMCTL</td>
<td>RW1C</td>
<td>-</td>
<td>ROM Control</td>
<td>587</td>
</tr>
<tr>
<td>0x130</td>
<td>FMPRE0</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Read Enable 0</td>
<td>588</td>
</tr>
<tr>
<td>0x200</td>
<td>FMPRE0</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Read Enable 0</td>
<td>588</td>
</tr>
<tr>
<td>0x134</td>
<td>FMPPE0</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Program Enable 0</td>
<td>589</td>
</tr>
<tr>
<td>0x400</td>
<td>FMPPE0</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Program Enable 0</td>
<td>589</td>
</tr>
<tr>
<td>0x1D0</td>
<td>BOOTCFG</td>
<td>RO</td>
<td>0xFFFF.FFFE</td>
<td>Boot Configuration</td>
<td>591</td>
</tr>
<tr>
<td>0x1E0</td>
<td>USER_REG0</td>
<td>RW</td>
<td>0xFFFF.FFFE</td>
<td>User Register 0</td>
<td>594</td>
</tr>
<tr>
<td>0x1E4</td>
<td>USER_REG1</td>
<td>RW</td>
<td>0xFFFF.FFFE</td>
<td>User Register 1</td>
<td>594</td>
</tr>
<tr>
<td>0x1E8</td>
<td>USER_REG2</td>
<td>RW</td>
<td>0xFFFF.FFFE</td>
<td>User Register 2</td>
<td>594</td>
</tr>
<tr>
<td>0x1EC</td>
<td>USER_REG3</td>
<td>RW</td>
<td>0xFFFF.FFFE</td>
<td>User Register 3</td>
<td>594</td>
</tr>
<tr>
<td>0x204</td>
<td>FMPRE1</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Read Enable 1</td>
<td>588</td>
</tr>
<tr>
<td>0x208</td>
<td>FMPRE2</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Read Enable 2</td>
<td>588</td>
</tr>
<tr>
<td>0x20C</td>
<td>FMPRE3</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Read Enable 3</td>
<td>588</td>
</tr>
<tr>
<td>0x404</td>
<td>FMPPE1</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Program Enable 1</td>
<td>589</td>
</tr>
<tr>
<td>0x408</td>
<td>FMPPE2</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Program Enable 2</td>
<td>589</td>
</tr>
<tr>
<td>0x40C</td>
<td>FMPPE3</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Memory Protection Program Enable 3</td>
<td>589</td>
</tr>
</tbody>
</table>

### 8.4 Flash Memory Register Descriptions (Flash Control Offset)

This section lists and describes the Flash Memory registers, in numerical order by address offset. Registers in this section are relative to the Flash control base address of 0x400F.D000.
Register 1: Flash Memory Address (FMA), offset 0x000

During a single word write operation, this register contains a 4-byte-aligned address and specifies where the data is written. During a write operation that uses the write buffer, this register contains a 128-byte (32-word) aligned address that specifies the start of the 32-word block to be written. During erase operations, this register contains a 1 KB-aligned CPU byte address and specifies which block is erased. Note that the alignment requirements must be met by software or the results of the operation are unpredictable.

Flash Memory Address (FMA)
Base 0x400F.D000
Offset 0x000
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:18</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>17:0</td>
<td>OFFSET</td>
<td>RW</td>
<td>0x0</td>
<td>Address Offset</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Address offset in Flash memory where operation is performed, except for non-volatile registers (see &quot;Non-Volatile Register Programming&quot; on page 542 for details on values for this field).</td>
</tr>
</tbody>
</table>
Register 2: Flash Memory Data (FMD), offset 0x004

This register contains the data to be written during the programming cycle. This register is not used during erase cycles.

Flash Memory Data (FMD)
Base 0x400F.D000
Offset 0x004
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>DATA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Data Value</td>
</tr>
</tbody>
</table>

Data value for write operation.
Register 3: Flash Memory Control (FMC), offset 0x008

When this register is written, the Flash memory controller initiates the appropriate access cycle for the location specified by the Flash Memory Address (FMA) register (see page 552). If the access is a write access, the data contained in the Flash Memory Data (FMD) register (see page 553) is written to the specified address.

This register must be the final register written and initiates the memory operation. The four control bits in the lower byte of this register are used to initiate memory operations.

Care must be taken not to set multiple control bits as the results of such an operation are unpredictable.

Flash Memory Control (FMC)
Base 0x400F.D000
Offset 0x008
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:16     | WRKEY      | WO   | 0x0000| Flash Memory Write Key
This field contains a write key, which is used to minimize the incidence of accidental Flash memory writes. Depending on the value of the KEY bit in the BOOTCFG register, the value 0xA442 or 0x71D5 must be written into this field for a Flash memory write to occur. Writes to the FMC register without this WRKEY value are ignored. A read of this field returns the value 0. |
| 15:4      | reserved   | RO   | 0x00  | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 3         | COMT       | RW   | 0     | Commit Register Value
This bit is used to commit writes to Flash-memory-resident registers and to monitor the progress of that process. |

Value Description
0 A write of 0 has no effect on the state of this bit. When read, a 0 indicates that the previous commit access is complete.
1 Set this bit to commit (write) the register value to a Flash-memory-resident register. When read, a 1 indicates that the previous commit access is not complete.

See “Non-Volatile Register Programming” on page 542 for more information on programming Flash-memory-resident registers.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>MERASE</td>
<td>RW</td>
<td>0</td>
<td>Mass Erase Flash Memory</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is used to mass erase the Flash main memory and to monitor the progress of that process.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>A write of 0 has no effect on the state of this bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, a 0 indicates that the previous mass erase operation is complete.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Set this bit to erase the Flash main memory.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, a 1 indicates that the previous mass erase operation is not complete.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For information on erase time, see “Flash Memory and EEPROM” on page 1421.</td>
</tr>
<tr>
<td>1</td>
<td>ERASE</td>
<td>RW</td>
<td>0</td>
<td>Erase a Page of Flash Memory</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is used to erase a page of Flash memory and to monitor the progress of that process.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>A write of 0 has no effect on the state of this bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, a 0 indicates that the previous page erase operation is complete.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Set this bit to erase the Flash memory page specified by the contents of the FMA register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, a 1 indicates that the previous page erase operation is not complete.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For information on erase time, see “Flash Memory and EEPROM” on page 1421.</td>
</tr>
<tr>
<td>0</td>
<td>WRITE</td>
<td>RW</td>
<td>0</td>
<td>Write a Word into Flash Memory</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is used to write a word into Flash memory and to monitor the progress of that process.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>A write of 0 has no effect on the state of this bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, a 0 indicates that the previous write update operation is complete.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Set this bit to write the data stored in the FMD register into the Flash memory location specified by the contents of the FMA register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, a 1 indicates that the write update operation is not complete.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For information on programming time, see “Flash Memory and EEPROM” on page 1421.</td>
</tr>
</tbody>
</table>
Register 4: Flash Controller Raw Interrupt Status (FCRIS), offset 0x00C

This register indicates that the Flash memory controller has an interrupt condition. An interrupt is sent to the interrupt controller only if the corresponding FCIM register bit is set.

Flash Controller Raw Interrupt Status (FCRIS)

| Base 0x400F.D000 | Offset 0x00C | Type RO, reset 0x0000.0000 |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>PROGRIS</td>
<td>RO</td>
<td>0</td>
<td>Program Verify Error Raw Interrupt Status</td>
</tr>
<tr>
<td>12</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>ERRIS</td>
<td>RO</td>
<td>0</td>
<td>Erase Verify Error Raw Interrupt Status</td>
</tr>
</tbody>
</table>

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is pending because the verify of a PROGRAM operation failed. If this error occurs when using the Flash write buffer, software must inspect the affected words to determine where the error occurred.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the PROGMISC bit in the FCMISC register.

Value | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is pending because the verify of an ERASE operation failed. If this error occurs when using the Flash write buffer, software must inspect the affected words to determine where the error occurred.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the ERMISC bit in the FCMISC register.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>INVDRIS</td>
<td>RO</td>
<td>0</td>
<td>Invalid Data Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is pending because a bit that was previously programmed as a 0 is now being requested to be programmed as a 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the \text{INVMISC} bit in the \text{FCMISC} register.</td>
</tr>
<tr>
<td>9</td>
<td>VOLTRIS</td>
<td>RO</td>
<td>0</td>
<td>Pump Voltage Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is pending because the regulated voltage of the pump went out of spec during the Flash operation and the operation was terminated.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the \text{VOLTMISC} bit in the \text{FCMISC} register.</td>
</tr>
<tr>
<td>8:3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>ERIS</td>
<td>RO</td>
<td>0</td>
<td>EEPROM Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit provides status EEPROM operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>An EEPROM interrupt has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An EEPROM interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the \text{EMISC} bit in the \text{FCMISC} register.</td>
</tr>
<tr>
<td>1</td>
<td>PRIS</td>
<td>RO</td>
<td>0</td>
<td>Programming Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit provides status on programming cycles which are write or erase actions generated through the FMC or FMC2 register bits (see page 554 and page 564).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The programming or erase cycle has not completed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The programming or erase cycle has completed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This status is sent to the interrupt controller when the \text{PMASK} bit in the \text{FCIM} register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the \text{PMISC} bit in the \text{FCMISC} register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>0</td>
<td>ARIS</td>
<td>RO</td>
<td>0</td>
<td>Access Raw Interrupt Status</td>
</tr>
</tbody>
</table>

Value  Description
---  ---
0    No access has tried to improperly program or erase the Flash memory.
1    A program or erase action was attempted on a block of Flash memory that contradicts the protection policy for that block as set in the FMPPEn registers.

This status is sent to the interrupt controller when the AMASK bit in the FCIM register is set.
This bit is cleared by writing a 1 to the AMISC bit in the FCMISC register.
Register 5: Flash Controller Interrupt Mask (FCIM), offset 0x010

This register controls whether the Flash memory controller generates interrupts to the controller.

Flash Controller Interrupt Mask (FCIM)
Base 0x400F.D000
Offset 0x010
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>PROGMASK</td>
<td>RW</td>
<td>0</td>
<td>PROGVER Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>12</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>ERMASK</td>
<td>RW</td>
<td>0</td>
<td>ERVER Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>INVDMAK</td>
<td>RW</td>
<td>0</td>
<td>Invalid Data Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>9</td>
<td>VOLTMASK</td>
<td>RW</td>
<td>0</td>
<td>VOLT Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The VOLTRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the VOLTRIS bit is set.</td>
</tr>
<tr>
<td>8:3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>EMASK</td>
<td>RW</td>
<td>0</td>
<td>EEPROM Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The ERIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the ERIS bit is set.</td>
</tr>
<tr>
<td>1</td>
<td>PMASK</td>
<td>RW</td>
<td>0</td>
<td>Programming Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the reporting of the programming raw interrupt status to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The PRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the PRIS bit is set.</td>
</tr>
<tr>
<td>0</td>
<td>AMASK</td>
<td>RW</td>
<td>0</td>
<td>Access Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit controls the reporting of the access raw interrupt status to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The ARIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the ARIS bit is set.</td>
</tr>
</tbody>
</table>
Register 6: Flash Controller Masked Interrupt Status and Clear (FCMISC), offset 0x014

This register provides two functions. First, it reports the cause of an interrupt by indicating which interrupt source or sources are signalling the interrupt. Second, it serves as the method to clear the interrupt reporting.

Flash Controller Masked Interrupt Status and Clear (FCMISC)
Base 0x400F.D000
Offset 0x014
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>PROGMISC</td>
<td>RW1C</td>
<td>0</td>
<td>PROGVER Masked Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 When read, a 0 indicates that an interrupt has not occurred. A write of 0 has no effect on the state of this bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 When read, a 1 indicates that an unmasked interrupt was signaled. Writing a 1 to this bit clears PROGmisc and also the PROGRIS bit in the FCRIS register (see page 556).</td>
</tr>
<tr>
<td>12</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>ERMISC</td>
<td>RW1C</td>
<td>0</td>
<td>ERVER Masked Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 When read, a 0 indicates that an interrupt has not occurred. A write of 0 has no effect on the state of this bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 When read, a 1 indicates that an unmasked interrupt was signaled. Writing a 1 to this bit clears ERMISC and also the ERRIS bit in the FCRIS register (see page 556).</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>-------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>10</td>
<td>INVDMISC</td>
<td>RW1C</td>
<td>0</td>
<td>Invalid Data Masked Interrupt Status and Clear</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: When read, a 0 indicates that an interrupt has not occurred. A write of 0 has no effect on the state of this bit.
- **1**: When read, a 1 indicates that an unmasked interrupt was signaled. Writing a 1 to this bit clears `INVDMISC` and also the `INVDRIS` bit in the `FCRIS` register (see page 556).

| 9         | VOLTMISC | RW1C  | 0     | VOLT Masked Interrupt Status and Clear           |

**Value Description**

- **0**: When read, a 0 indicates that an interrupt has not occurred. A write of 0 has no effect on the state of this bit.
- **1**: When read, a 1 indicates that an unmasked interrupt was signaled. Writing a 1 to this bit clears `VOLTMISC` and also the `VOLTRIS` bit in the `FCRIS` register (see page 556).

| 8:3       | reserved | RO    | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |

| 2         | EMISC    | RW1C  | 0     | EEPROM Masked Interrupt Status and Clear         |

**Value Description**

- **0**: When read, a 0 indicates that an interrupt has not occurred. A write of 0 has no effect on the state of this bit.
- **1**: When read, a 1 indicates that an unmasked interrupt was signaled. Writing a 1 to this bit clears `EMISC` and also the `ERIS` bit in the `FCRIS` register (see page 556).

| 1         | PMISC    | RW1C  | 0     | Programming Masked Interrupt Status and Clear    |

**Value Description**

- **0**: When read, a 0 indicates that a programming cycle complete interrupt has not occurred. A write of 0 has no effect on the state of this bit.
- **1**: When read, a 1 indicates that an unmasked interrupt was signaled because a programming cycle completed. Writing a 1 to this bit clears `PMISC` and also the `PRIS` bit in the `FCRIS` register (see page 556).
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>AMISC</td>
<td>RW1C</td>
<td>0</td>
<td>Access Masked Interrupt Status and Clear</td>
</tr>
</tbody>
</table>

**Value** | **Description** |
--- | --- |
0 | When read, a 0 indicates that no improper accesses have occurred. A write of 0 has no effect on the state of this bit. |
1 | When read, a 1 indicates that an unmasked interrupt was signaled because a program or erase action was attempted on a block of Flash memory that contradicts the protection policy for that block as set in the FMPPEn registers. Writing a 1 to this bit clears AMISC and also the ARIS bit in the FCRIS register (see page 556). |
Register 7: Flash Memory Control 2 (FMC2), offset 0x020

When this register is written, the Flash memory controller initiates the appropriate access cycle for the location specified by the Flash Memory Address (FMA) register (see page 552). If the access is a write access, the data contained in the Flash Write Buffer (FWB) registers is written.

This register must be the final register written as it initiates the memory operation.

Flash Memory Control 2 (FMC2)
Base 0x400F.D000
Offset 0x020
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:16     | WRKEY            | WO   | 0x0000| Flash Memory Write Key
This field contains a write key, which is used to minimize the incidence of accidental Flash memory writes. Depending on the value of the KEY bit in the Boot configuration register, the value 0xA442 or 0x71D5 must be written into this field for a Flash memory write to occur. Writes to the FMC2 register without this WRKEY value are ignored. A read of this field returns the value 0. |
| 15:1      | reserved         | RO   | 0x0000| Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 0         | WRBUF            | RW   | 0     | Buffered Flash Memory Write
This bit is used to start a buffered write to Flash memory. |

For information on programming time, see "Flash Memory and EEPROM" on page 1421.
Register 8: Flash Write Buffer Valid (FWBVAL), offset 0x030

This register provides a bitwise status of which FWBn registers have been written by the processor since the last write of the Flash memory write buffer. The entries with a 1 are written on the next write of the Flash memory write buffer. This register is cleared after the write operation by hardware. A protection violation on the write operation also clears this status.

Software can program the same 32 words to various Flash memory locations by setting the FWB[n] bits after they are cleared by the write operation. The next write operation then uses the same data as the previous one. In addition, if a FWBn register change should not be written to Flash memory, software can clear the corresponding FWB[n] bit to preserve the existing data when the next write operation occurs.

Flash Write Buffer Valid (FWBVAL)
Base 0x400F.D000
Offset 0x030
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>FWB[n]</td>
<td>RW</td>
<td>0x0</td>
<td>Flash Memory Write Buffer</td>
</tr>
</tbody>
</table>

Value Description
0 The corresponding FWBn register has no new data to be written.
1 The corresponding FWBn register has been updated since the last buffer write operation and is ready to be written to Flash memory.

Bit 0 corresponds to FWB0, offset 0x100, and bit 31 corresponds to FWB31, offset 0x13C.
Register 9: Flash Write Buffer n (FWBn), offset 0x100 - 0x17C

These 32 registers hold the contents of the data to be written into the Flash memory on a buffered Flash memory write operation. The offset selects one of the 32-bit registers. Only FWBn registers that have been updated since the preceding buffered Flash memory write operation are written into the Flash memory, so it is not necessary to write the entire bank of registers in order to write 1 or 2 words. The FWBn registers are written into the Flash memory with the FWB0 register corresponding to the address contained in FMA. FWB1 is written to the address FMA+0x4 etc. Note that only data bits that are 0 result in the Flash memory being modified. A data bit that is 1 leaves the content of the Flash memory bit at its previous value.
Register 10: Flash Size (FSIZE), offset 0xFC0

This register indicates the size of the on-chip Flash memory.

**Important:** This register should be used to determine the size of the Flash memory that is implemented on this microcontroller. However, to support legacy software, the DC0 register is available. A read of the DC0 register correctly identifies legacy memory sizes. Software must use the FSIZE register for memory sizes that are not listed in the DC0 register description.

---

**Flash Size (FSIZE)**
Base 0x400F.D000
Offset 0xFC0
Type RO, reset 0x0000.007F

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>SIZE</td>
<td>RO</td>
<td>0x7F</td>
<td>Flash Size</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Indicates the size of the on-chip Flash memory.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x007F 256 KB of Flash</td>
</tr>
</tbody>
</table>
**Register 11: SRAM Size (SSIZE), offset 0xFC4**

This register indicates the size of the on-chip SRAM.

**Important:** This register should be used to determine the size of the SRAM that is implemented on this microcontroller. However, to support legacy software, the DC0 register is available. A read of the DC0 register correctly identifies legacy memory sizes. Software must use the SSIZE register for memory sizes that are not listed in the DC0 register description.

### SRAM Size (SSIZE)

Base 0x400F.D000  
Offset 0xFC4  
Type RO, reset 0x0000.007F

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 15:0      | SIZE  | RO   | 0x7F  | SRAM Size  
Indicates the size of the on-chip SRAM.  
Value | Description |
|          | 0x007F | 32 KB of SRAM |
Register 12: ROM Software Map (ROMSWMAP), offset 0xFCC

This register indicates the presence of third-party software in the on-chip ROM.

**Important:** This register should be used to determine the presence of third-party software in the on-chip ROM on this microcontroller. However, to support legacy software, the NVMSTAT register is available. A read of the TPSW bit in the NVMSTAT register correctly identifies the presence of legacy third-party software. Software should use the ROMSWMAP register for software that is not on legacy devices.

### ROM Software Map (ROMSWMAP)

<table>
<thead>
<tr>
<th>Base 0x400F.D000</th>
<th>Offset 0xFCC</th>
<th>Type RO, reset 0x0000.0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>31:0</th>
<th>reserved Type</th>
<th>0x0000</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>0</th>
<th>SAFERTOS RO</th>
<th>0x0</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SAFERTOS is not in the on-chip ROM.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SAFERTOS is in the on-chip ROM.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 8.5 EEPROM Register Descriptions (EEPROM Offset)

This section lists and describes the EEPROM registers, in numerical order by address offset. Registers in this section are relative to the EEPROM base address of 0x400A.F000.

Note that the EEPROM module clock must be enabled before the registers can be programmed (see page 359). There must be a delay of 3 system clocks after the EEPROM module clock is enabled before any EEPROM module registers are accessed. In addition, after enabling or resetting the EEPROM module, software must wait until the WORKING bit in the EEDONE register is clear before accessing any EEPROM registers.
Register 13: EEPROM Size Information (EESIZE), offset 0x000

The EESIZE register indicates the number of 16-word blocks and 32-bit words in the EEPROM.

EEPROM Size Information (EESIZE)
Base 0x400A.F000
Offset 0x000
Type RO, reset 0x0020.0200

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:27</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 26:16     | BLKCNT      | RO   | 0x20  | Number of 16-Word Blocks
This value encoded in this field describes the number of 16-word blocks in the EEPROM. |
| 15:0      | WORDCNT     | RO   | 0x200 | Number of 32-Bit Words
This value encoded in this field describes the number of 32-bit words in the EEPROM. |
Register 14: EEPROM Current Block (EEBLOCK), offset 0x004

The EEBLOCK register is used to select the EEPROM block for subsequent reads, writes, and protection control. The value is a block offset into the EEPROM, such that the first block is 0, then second block is 1, etc. Each block contains 16 words. Attempts to set an invalid block causes the BLOCK field to be configured to 0. To verify that the intended block is being accessed, software can read the BLOCK field after it has been written. An invalid block can be either a non-existent block or a block that has been hidden using the EEHIDE register. Note that block 0 cannot be hidden.

**EEPROM Current Block (EEBLOCK)**

Base 0x400A.F000
Offset 0x004
Type RW, reset 0x0000.0000

| 31:16 | reserved | RO | 0x00000 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

| 15:0 | BLOCK | RW | 0x00000 | Current Block

This field specifies the block in the EEPROM that is selected for subsequent accesses. Once this field is configured, the read-write registers operate against the specified block, using the EEOFFSET register to select the word within the block. Additionally, the protection and unlock registers are used for the selected block. The maximum value that can be written into this register is determined by the block count, as indicated by the EESIZE register. Attempts to write this field larger than the maximum number of blocks or to a locked block causes this field to be configured to 0.
Register 15: EEPROM Current Offset (EEOFFSET), offset 0x008

The EEOFFSET register is used to select the EEPROM word to read or write within the block selected by the EEBLOCK register. The value is a word offset into the block. Because accesses to the EERDWRINC register change the offset, software can read the contents of this register to determine the current offset.

EEPROM Current Offset (EEOFFSET)
Base 0x400A.F000
Offset 0x008
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 3:0       | OFFSET     | RW   | 0x0         | Current Address Offset
This value is the current address specified as an offset into the block selected by the EEBLOCK register. Once configured, the read-write registers, EERDRWR and EERDWRINC, operate against that address. The offset is automatically incremented by the EERDWRINC register, with wrap around within the block, which means the offset is incremented from 15 back to 0. |
Register 16: EEPROM Read-Write (EERDWR), offset 0x010

The **EERDWR** register is used to read or write the EEPROM word at the address pointed to by the **EEBLOCK** and **EEOFFSET** registers. If the protection or access rules do not permit access, the operation is handled as follows: if reading is not allowed, the value 0xFFFF.FFFF is returned in all cases; if writing is not allowed, the **EEDONE** register is configured to indicate an error.

### EEPROM Read-Write (EERDWR)

Base 0x400A.F000  
Offset 0x010  
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>VALUE</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Read or Write Data</td>
</tr>
</tbody>
</table>

On a read, this field contains the value at the word pointed to by **EEOFFSET**. On a write, this field contains the data to be stored at the word pointed to by **EEOFFSET**. For writes, configuring this field starts the write process. If protection and access rules do not permit reads, all 1s are returned. If protection and access rules do not permit writes, the write fails and the **EEDONE** register indicates failure.
Register 17: EEPROM Read-Write with Increment (EERDWRINC), offset 0x014

The EERDWRINC register is used to read or write the EEPROM word at the address pointed to by the EEBLOCK and EEOFFSET registers, and then increment the OFFSET field in the EEOFFSET register. If the protection or access rules do not permit access, the operation is handled as follows: if reading is not allowed, the value 0xFFFF.FFFF is returned in all cases; if writing is not allowed, the EEDONE register is configured to indicate an error. In all cases, the OFFSET field is incremented. If the last value is reached, OFFSET wraps around to 0 and points to the first word.

EEPROM Read-Write with Increment (EERDWRINC)
Base 0x400A.F000
Offset 0x014
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>VALUE</td>
<td>RW</td>
<td>-</td>
<td>EEPROM Read or Write Data with Increment</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>On a read, this field contains the value at the word pointed to by EEOFFSET. On a write, this field contains the data to be stored at the word pointed to by EEOFFSET. For writes, configuring this field starts the write process. If protection and access rules do not permit reads, all 1s are returned. If protection and access rules do not permit writes, the write fails and the EEDONE register indicates failure. Regardless of error, the OFFSET field in the EEOFFSET register is incremented by 1, and the value wraps around if the last word is reached.</td>
</tr>
</tbody>
</table>
Register 18: EEPROM Done Status (EEDONE), offset 0x018

The **EEDONE** register indicates the successful or failed completion of a write using the **EERDWR** or **EERDWRINC** register, protection set using the **EEPROT** register, password registered using the **EEPASS** register, copy buffer erase or program retry using the **EESUPP** register, or a debug mass erase using the **EEDBGME** register. The **EEDONE** register can be used with the **EEINT** register to generate an interrupt to report the status. The normal usage is to poll the **EEDONE** register or read the register after an interrupt is triggered. When the **EEDONE** bit 0 is set, then the operation is still in progress. When the **EEDONE** bit 0 is clear, then the value of **EEDONE** indicates the completion status. If **EEDONE**=0, then the write completed successfully. If **EEDONE**!=0, then an error occurred and the source of the error is given by the set bit(s). If an error occurs, corrective action may be taken as explained on page 577.

### EEPROM Done Status (EEDONE)

**Base** 0x400A.F000  
**Offset** 0x018  
**Type** RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>WRBUSY</td>
<td>RO</td>
<td>0</td>
<td>Write Busy</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No error</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>An attempt to access the EEPROM was made while a write was in progress.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| 4         | NOPERM          | RO   | 0     | Write Without Permission                                                     |
| Value     | Description     |      |       |                                                                               |
| 0         | No error        |      |       |                                                                               |
| 1         | An attempt was made to write without permission. This error can result because the block is locked, the write violates the programmed access protection, or when an attempt is made to write a password when the password has already been written. |      |       |
### Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>WKCOPY</td>
<td>RO</td>
<td>0</td>
<td>Working on a Copy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The EEPROM is not copying.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  A write is in progress and is waiting for the EEPROM to copy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>to or from the copy buffer.</td>
</tr>
<tr>
<td>2</td>
<td>WKERASE</td>
<td>RO</td>
<td>0</td>
<td>Working on an Erase</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The EEPROM is not erasing.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  A write is in progress and the original block is being erased after</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>being copied.</td>
</tr>
<tr>
<td>1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>WORKING</td>
<td>RO</td>
<td>0</td>
<td>EEPROM Working</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The EEPROM is not working.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The EEPROM is performing the requested operation.</td>
</tr>
</tbody>
</table>

---

**Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.**
The **EESUPP** register indicates if internal operations are required because an internal copy buffer must be erased or a programming failure has occurred and the operation must be completed. These conditions are explained below as well as in more detail in the section called “Manual Copy Buffer Erase” on page 547 and the section called “Error During Programming” on page 547.

- The **EREQ** bit is set if the internal copy buffer must be erased the next time it is used because it is full. To avoid the delay of waiting for the copy buffer to be erased on the next write, it can be erased manually using this register by setting the **START** bit.

- If either **PRETRY** or **ERETRY** is set indicating that an operation must be completed, setting the **START** bit causes the operation to be performed again.

- The **PRETRY** and **ERETRY** bits are cleared automatically after the failed operation has been successfully completed.

These bits are not changed by reset, so any condition that occurred before a reset is still indicated after a reset.

**EEPROM Support Control and Status (EESUPP)**

Base 0x400A.F000
Offset 0x01C
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>PRETRY</td>
<td>RO</td>
<td>-</td>
<td>Programming Must Be Retried</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Programming has not failed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Programming from a copy in either direction failed to complete and must be restarted by setting the <strong>START</strong> bit.</td>
</tr>
<tr>
<td>2</td>
<td>ERETRY</td>
<td>RO</td>
<td>-</td>
<td>Erase Must Be Retried</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Erasing has not failed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Erasing failed to complete and must be restarted by setting the <strong>START</strong> bit. If the failed erase is due to the erase of a main buffer, the copy will be performed after the erase completes successfully.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>EREQ</td>
<td>RO</td>
<td>-</td>
<td>Erase Required</td>
</tr>
</tbody>
</table>

**Value** | **Description**                                                                                                 |
-----------|---------------------------------------------------------------------------------------------------------------|
0          | The copy buffer has available space.                                                                            |
1          | An erase of the copy buffer is required.                                                                        |

| 0         | START  | RW   | 0     | Start Erase                  |

Setting this bit starts error recovery if the PRETRY or ERETRY bit is set. If both the PRETRY and the ERETRY bits are clear, setting this bit starts erasing the copy buffer if EREQ is set. If none of the other bits in this register are set, setting this bit is ignored. After this bit is set, the WORKING bit in the EEDONE register is set and is cleared when the operation is complete. In addition, the EEINT register can be used to generate an interrupt on completion.

If this bit is set while an operation is in progress, the write is ignored.

The `START` bit is automatically cleared when the operation completes.
Register 20: EEPROM Unlock (EEUNLOCK), offset 0x020

The EEUNLOCK register can be used to unlock the whole EEPROM or a single block using a password. Unlocking is only required if a password is registered using the EEPROM Unlock (EEUNLOCK) registers for the block that is selected by the EEBLOCK register. If block 0 has a password, it locks the remaining blocks from any type of access, but uses its own protection mechanism, for example readable, but not writable when locked. In addition, if block 0 has a password, it must be unlocked before unlocking any other block.

The EEUNLOCK register is written between 1 and 3 times to form the 32-bit, 64-bit, or 96-bit password registered using the EEPROM Unlock (EEUNLOCK) registers. The value used to configure the EEPROM Unlock (EEUNLOCK) register must always be written last. For example, for a 96-bit password, the value used to configure the EEPROM Unlock (EEUNLOCK) registers must be written first followed by the EEPROM Unlock (EEUNLOCK) and EEPROM Unlock (EEUNLOCK) register values. The block or the whole EEPROM can be re-locked by writing 0xFFFF.FFFF to this register.

In the event that an invalid value is written to this register, the block remains locked. The state of the EEPROM lock can be determined by reading back the EEPROM Unlock (EEUNLOCK) register. If a multi-word password is set and the number of words written is incorrect, writing 0xFFFF.FFFF to this register reverts the EEPROM lock to the locked state, and the proper unlock sequence can be retried.

Note that the internal logic is balanced to prevent any electrical or time-based attack being used to find the correct password or its length.

EEPROM Unlock (EEUNLOCK)
Base 0x400A.F000
Offset 0x020
Type RW, reset -
Register 21: EEPROM Protection (EEPROT), offset 0x030

The **EEPROT** register is used to set or read the protection for the current block, as selected by the **EEBLOCK** register. Protection and access control is used to determine when a block's contents can be read or written. The protection level for block 0 sets the minimum protection level for the entire EEPROM. For example, if the **PROT** field is configured to 0x1 for block 0, then block 1 could be configured with the **PROT** field to be 0x1, 0x2, or 0x3, but not 0x0.

EEPROM Protection (EEPROT)

Base 0x400A.F000
Offset 0x030
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>ACC</td>
<td>RW</td>
<td>0</td>
<td>Access Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Both user and supervisor code may access this block of the EEPROM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Only supervisor code may access this block of the EEPROM. μDMA and Debug are also prevented from accessing the EEPROM.</td>
</tr>
</tbody>
</table>

If this bit is set for block 0, then the whole EEPROM may only be accessed by supervisor code.
The Protection bits control what context is needed for reading and writing the block selected by the \texttt{EEBLOCK} register, or if block 0 is selected, all blocks. The following values are allowed:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>This setting is the default. If there is no password, the block is not protected and is readable and writable. If there is a password, the block is readable, but only writable when unlocked.</td>
</tr>
<tr>
<td>0x1</td>
<td>If there is a password, the block is readable or writable only when unlocked. This value has no meaning when there is no password.</td>
</tr>
<tr>
<td>0x2</td>
<td>If there is no password, the block is readable, not writable. If there is a password, the block is readable only when unlocked, but is not writable under any conditions.</td>
</tr>
<tr>
<td>0x3</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>PROT</td>
<td>RW</td>
<td>0x0</td>
<td>Protection Control</td>
</tr>
</tbody>
</table>

The Protection bits control what context is needed for reading and writing the block selected by the \texttt{EEBLOCK} register, or if block 0 is selected, all blocks. The following values are allowed:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>This setting is the default. If there is no password, the block is not protected and is readable and writable. If there is a password, the block is readable, but only writable when unlocked.</td>
</tr>
<tr>
<td>0x1</td>
<td>If there is a password, the block is readable or writable only when unlocked. This value has no meaning when there is no password.</td>
</tr>
<tr>
<td>0x2</td>
<td>If there is no password, the block is readable, not writable. If there is a password, the block is readable only when unlocked, but is not writable under any conditions.</td>
</tr>
<tr>
<td>0x3</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register 22: EEPROM Password (EEPASS0), offset 0x034
Register 23: EEPROM Password (EEPASS1), offset 0x038
Register 24: EEPROM Password (EEPASS2), offset 0x03C

The EEPASSn registers are used to configure a password for a block. A password may only be set once and cannot be changed. The password may be 32-bits, 64-bits, or 96-bits. Each word of the password can be any 32-bit value other than 0xFFFF.FFFF (all 1s). To set a password, the EEPASS0 register is written to with a value other than 0xFFFF.FFFF. When the write completes, as indicated in the EEDONE register, the application may choose to write to the EEPASS1 register with a value other than 0xFFFF.FFFF. When that write completes, the application may choose to write to the EEPASS2 register with a value other than 0xFFFF.FFFF to create a 96-bit password. The registers do not have to be written consecutively, and the EEPASS1 and EEPASS2 registers may be written at a later date. Based on whether 1, 2, or all 3 registers have been written, the unlock code also requires the same number of words to unlock.

Note: Once the password is written, the block is not actually locked until either a reset occurs or 0xFFFF.FFFF is written to EEUNLOCK.

### EEPROM Password (EEPASSn)

**Base**: 0x400A.F000  
**Offset**: 0x034  
**Type**: RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>PASS</td>
<td>RW</td>
<td>-</td>
<td>Password</td>
</tr>
</tbody>
</table>

This register reads as 0x1 if a password is registered for this block and 0x0 if no password is registered. A write to this register if it reads as 0x0 sets the password. If an attempt is made to write to this register when it reads as 0x1, the write is ignored and the NOPERM bit in the EEDONE register is set.
Register 25: EEPROM Interrupt (EEINT), offset 0x040

The **EEINT** register is used to control whether an interrupt should be generated when a write to EEPROM completes as indicated by the **EEDONE** register value changing from 0x1 to any other value. If the **INT** bit in this register is set, the **ERIS** bit in the Flash Controller Raw Interrupt Status (**FCRIS**) register is set whenever the **EEDONE** register value changes from 0x1 as the Flash memory and the EEPROM share an interrupt vector.

### EEPROM Interrupt (EEINT)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x400A.F000</td>
<td>0x040</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

#### Bit/Field Details

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>INT</td>
<td>RW</td>
<td>0</td>
<td>Interrupt Enable</td>
</tr>
</tbody>
</table>

#### Interrupt Enable Details

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt is generated.</td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is generated when the <strong>EEDONE</strong> register transitions from 1 to 0 or an error occurs. The <strong>EEDONE</strong> register provides status after a write to an offset location as well as a write to the password and protection bits.</td>
</tr>
</tbody>
</table>
Register 26: EEPROM Block Hide (EEHIDE), offset 0x050

The **EEHIDE** register is used to hide one or more blocks other than block 0. Once hidden, the block is not accessible until the next reset. This model allows initialization code to have access to data which is not visible to the rest of the application. This register also provides for additional security in that there is no password to search for in the code or data.

EEPROM Block Hide (EEHIDE)
Base 0x400A.F000
Offset 0x050
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>Hn</td>
<td>RW</td>
<td>0x0000.000</td>
<td>Hide Block</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The corresponding block is not hidden.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The block number that corresponds to the bit number is hidden. A hidden block cannot be accessed, and the OFFSET value in the EEBLOCK register cannot be set to that block number. If an attempt is made to configure the OFFSET field to a hidden block, the EEBLOCK register is cleared. Any attempt to clear a bit in this register that is set is ignored.</td>
</tr>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 27: EEPROM Debug Mass Erase (EEDBGME), offset 0x080

The **EEDBGME** register is used to mass erase the EEPROM block back to its default state from the factory. This register is intended to be used only for debug and test purposes, not in production environments. The erase takes place in such a way as to be secure. It first erases all data and then erases the protection mechanism. This register can only be written from supervisor mode by the core, and can also be written by the TM4C123GH6PZ debug controller when enabled. A key is used to avoid accidental use of this mechanism. Note that if a power down takes place while erasing, the mechanism should be used again to complete the operation. Powering off prematurely does not expose secured data.

To start a mass erase, the whole register must be written as 0xE37B.0001. The register reads back as 0x1 until the erase is fully completed at which time it reads as 0x0. The **EEDONE** register is set to 0x1 when the erase is started and changes to 0x0 or an error when the mass erase is complete.

Note that mass erasing the EEPROM block means that the wear-leveling counters are also reset to the factory default.

EEPROM Debug Mass Erase (EEDBGME)
Base 0x400A.F000
Offset 0x080
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>KEY</td>
<td>WO</td>
<td>0x0000</td>
<td>Erase Key&lt;br&gt;This field must be written with 0xE37B for the ME field to be effective.</td>
</tr>
<tr>
<td>15:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>ME</td>
<td>RW</td>
<td>0</td>
<td>Mass Erase&lt;br&gt;Value Description&lt;br&gt;0 No action.&lt;br&gt;1 When written as a 1, the EEPROM is mass erased. This bit continues to read as 1 until the EEPROM is fully erased.</td>
</tr>
</tbody>
</table>
Register 28: EEPROM Peripheral Properties (EEPROMPP), offset 0xFC0

The EEPROMPP register indicates the size of the EEPROM for this part.

EEPROM Peripheral Properties (EEPROMPP)

Base 0x400A.F000  
Offset 0xFC0  
Type RO, reset 0x0000.001F

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4:0</td>
<td>SIZE</td>
<td>RO</td>
<td>0x1F</td>
<td>2-KB EEPROM Size</td>
</tr>
</tbody>
</table>

8.6 Memory Register Descriptions (System Control Offset)

The remainder of this section lists and describes the registers that reside in the System Control address space, in numerical order by address offset. Registers in this section are relative to the System Control base address of 0x400F.E000.
Register 29: ROM Control (RMCTL), offset 0x0F0

This register provides control of the ROM controller state. This register offset is relative to the System Control base address of 0x400F.E000.

At reset, the following sequence is performed:

1. The BOOTCFG register is read. If the EN bit is clear, the ROM Boot Loader is executed.

2. In the ROM Boot Loader, the status of the specified GPIO pin is compared with the specified polarity. If the status matches the specified polarity, the ROM is mapped to address 0x0000.0000 and execution continues out of the ROM Boot Loader.

3. If the EN bit is set or the status doesn't match the specified polarity, the data at address 0x0000.0004 is read, and if the data at this address is 0xFFFF.FFFF, the ROM is mapped to address 0x0000.0000 and execution continues out of the ROM Boot Loader.

4. If there is data at address 0x0000.0004 that is not 0xFFFF.FFFF, the stack pointer (SP) is loaded from Flash memory at address 0x0000.0000 and the program counter (PC) is loaded from address 0x0000.0004. The user application begins executing.

ROM Control (RMCTL)
Base 0x400F.E000
Offset 0x0F0
Type RW1C, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>BA</td>
<td>RW1C</td>
<td>1</td>
<td>Boot Alias</td>
</tr>
</tbody>
</table>

Value  Description
0 The Flash memory is at address 0x0.
1 The microcontroller's ROM appears at address 0x0.

This bit is cleared by writing a 1 to this bit position.
Register 30: Flash Memory Protection Read Enable 0 (FMPRE0), offset 0x130 and 0x200
Register 31: Flash Memory Protection Read Enable 1 (FMPRE1), offset 0x204
Register 32: Flash Memory Protection Read Enable 2 (FMPRE2), offset 0x208
Register 33: Flash Memory Protection Read Enable 3 (FMPRE3), offset 0x20C

Note: The FMPRE0 register is aliased for backwards compatibility.

Note: Offset is relative to System Control base address of 0x400F.E000.

This register stores the read-only protection bits for each 2-KB flash block (FMPPEn stores the execute-only bits).

This register is loaded during the power-on reset sequence. The factory settings for the FMPREn and FMPPEn registers are a value of 1 for all implemented 2-KB blocks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is RW0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the sequence detailed in “Recovering a “Locked” Microcontroller” on page 205.

Each FMPREn register controls a 64-k block of Flash. For additional information, see “Flash Memory Protection” on page 538.

- **FMPRE0**: 0 to 64 KB
- **FMPRE1**: 65 to 128 KB
- **FMPRE2**: 129 to 192 KB
- **FMPRE3**: 193 to 256 KB

Flash Memory Protection Read Enable n (FMPREn)
Base 0x400F.E000
Offset 0x130 and 0x200
Type RW, reset 0xFFFF.FFFF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>READ_ENABLE</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Flash Read Enable</td>
</tr>
</tbody>
</table>

Each bit configures a 2-KB flash block to be read only.
The policies may be combined as shown in Table 8-1 on page 539.
Register 34: Flash Memory Protection Program Enable 0 (FMPPE0), offset 0x134 and 0x400

Register 35: Flash Memory Protection Program Enable 1 (FMPPE1), offset 0x404

Register 36: Flash Memory Protection Program Enable 2 (FMPPE2), offset 0x408

Register 37: Flash Memory Protection Program Enable 3 (FMPPE3), offset 0x40C

Note: The FMPPE0 register is aliased for backwards compatibility.

Note: Offset is relative to System Control base address of 0x400FE000.

This register stores the execute-only protection bits for each 2-KB flash block (FMPREn stores the read-only protection bits).

This register is loaded during the power-on reset sequence. The factory settings for the FMPREn and FMPPEn registers are a value of 1 for all implemented banks. This achieves a policy of open access and programmability. The register bits may be changed by writing the specific register bit. However, this register is RW0; the user can only change the protection bit from a 1 to a 0 (and may NOT change a 0 to a 1). The changes are not permanent until the register is committed (saved), at which point the bit change is permanent. If a bit is changed from a 1 to a 0 and not committed, it may be restored by executing a power-on reset sequence. The reset value shown only applies to power-on reset; any other type of reset does not affect this register. Once committed, the only way to restore the factory default value of this register is to perform the sequence detailed in “Recovering a "Locked" Microcontroller” on page 205. For additional information, see “Flash Memory Protection” on page 538.

Each FMPPEn register controls a 64-k block of Flash. For additional information, see “Flash Memory Protection” on page 538.

- **FMPPE0**: 0 to 64 KB
- **FMPPE1**: 65 to 128 KB
- **FMPPE2**: 129 to 192 KB
- **FMPPE3**: 193 to 256 KB

Flash Memory Protection Program Enable n (FMPPEn)
Base 0x400F.E000
Offset 0x134 and 0x400
Type RW, reset 0xFFFF.FFFF
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:0      | PROG_ENABLE| RW   | 0xFFFF.FFFF | Flash Programming Enable  
Each bit configures a 2-KB flash block to be execute only.  
The policies may be combined as shown in Table 8-1 on page 539. |
Register 38: Boot Configuration (BOOTCFG), offset 0x1D0

Note: Offset is relative to System Control base address of 0x400F.E000.

Note: The Boot Configuration (BOOTCFG) register requires a POR before the committed changes take effect.

This register is not written directly, but instead uses the FMD register as explained in “Non-Volatile Register Programming” on page 542. This register provides configuration of a GPIO pin to enable the ROM Boot Loader as well as a write-once mechanism to disable external debugger access to the device. At reset, the user has the opportunity to direct the core to execute the ROM Boot Loader or the application in Flash memory by using any GPIO signal from Ports A-Q as configured by the bits in this register. At reset, the following sequence is performed:

1. The BOOTCFG register is read. If the EN bit is clear, the ROM Boot Loader is executed.

2. In the ROM Boot Loader, the status of the specified GPIO pin is compared with the specified polarity. If the status matches the specified polarity, the ROM is mapped to address 0x0000.0000 and execution continues out of the ROM Boot Loader.

3. If the EN bit is set or the status doesn’t match the specified polarity, the data at address 0x0000.0004 is read, and if the data at this address is 0xFFFF.FFFF, the ROM is mapped to address 0x0000.0000 and execution continues out of the ROM Boot Loader.

4. If there is data at address 0x0000.0004 that is not 0xFFFF.FFFF, the stack pointer (SP) is loaded from Flash memory at address 0x0000.0000 and the program counter (PC) is loaded from address 0x0000.0004. The user application begins executing.

The DBG0 bit is cleared by the factory and the DBG1 bit is set, which enables external debuggers. Clearing the DBG1 bit disables any external debugger access to the device, starting with the next power-up cycle of the device. The NW bit indicates that bits in the register can be changed from 1 to 0.

By committing the register values using the COMT bit in the FMC register, the register contents become non-volatile and are therefore retained following power cycling. Prior to being committed, bits can only be changed from 1 to 0. The reset value shown only applies to power-on reset when the register is not yet committed; any other type of reset does not affect this register. Once committed, the register retains its value through power-on reset. Once committed, the only way to restore the factory default value of this register is to perform the sequence detailed in “Recovering a "Locked" Microcontroller” on page 205.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>NW</td>
<td>RO</td>
<td>1</td>
<td>Not Written</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, this bit indicates that the values in this register can be changed from 1 to 0. When clear, this bit specifies that the contents of this register cannot be changed.</td>
</tr>
<tr>
<td>30:16</td>
<td>reserved</td>
<td>RO</td>
<td>0xFFFF</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:13</td>
<td>PORT</td>
<td>RO</td>
<td>0x7</td>
<td>Boot GPIO Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field selects the port of the GPIO port pin that enables the ROM boot loader at reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>Port A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>Port B</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>Port C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>Port D</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x4</td>
<td>Port E</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x5</td>
<td>Port F</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x6</td>
<td>Port G</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x7</td>
<td>Port H</td>
</tr>
<tr>
<td>12:10</td>
<td>PIN</td>
<td>RO</td>
<td>0x7</td>
<td>Boot GPIO Pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field selects the pin number of the GPIO port pin that enables the ROM boot loader at reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>Pin 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>Pin 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>Pin 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>Pin 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x4</td>
<td>Pin 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x5</td>
<td>Pin 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x6</td>
<td>Pin 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x7</td>
<td>Pin 7</td>
</tr>
<tr>
<td>9</td>
<td>POL</td>
<td>RO</td>
<td>1</td>
<td>Boot GPIO Polarity</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, this bit selects a high level for the GPIO port pin to enable the ROM boot loader at reset. When clear, this bit selects a low level for the GPIO port pin.</td>
</tr>
<tr>
<td>8</td>
<td>EN</td>
<td>RO</td>
<td>1</td>
<td>Boot GPIO Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Clearing this bit enables the use of a GPIO pin to enable the ROM Boot Loader at reset. When this bit is set, the contents of address 0x0000.0004 are checked to see if the Flash memory has been programmed. If the contents are not 0xFFFF.FFFF, the core executes out of Flash memory. If the Flash has not been programmed, the core executes out of ROM.</td>
</tr>
</tbody>
</table>
Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x7</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>KEY</td>
<td>RO</td>
<td>1</td>
<td>KEY Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit chooses between using the value 0xA442 or 0x71D5 as the WRKEY value in the FMC/FMC2 register.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The value 0x71D5 is used as the WRKEY in the FMC/FMC2 register. Writes to the FMC/FMC2 register with a 0xA442 key are ignored.</td>
</tr>
<tr>
<td>1</td>
<td>0xA442 is used as the WRKEY in the FMC/FMC2 register. Writes to the FMC/FMC2 register with a 0x71D5 key are ignored.</td>
</tr>
</tbody>
</table>

| 3:2 | reserved | RO | 0x3 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 1   | DBG1     | RO | 1   | Debug Control 1  |
|     |          |    |     | The DBG1 bit must be 1 and DBG0 must be 0 for debug to be available. |
| 0   | DBG0     | RO | 0   | Debug Control 0  |
|     |          |    |     | The DBG1 bit must be 1 and DBG0 must be 0 for debug to be available. |
**Register 39:** User Register 0 (USER_REG0), offset 0x1E0

**Register 40:** User Register 1 (USER_REG1), offset 0x1E4

**Register 41:** User Register 2 (USER_REG2), offset 0x1E8

**Register 42:** User Register 3 (USER_REG3), offset 0x1EC

**Note:** Offset is relative to System Control base address of 0x400F.E000.

These registers each provide 32 bits of user-defined data that is non-volatile. Bits can only be changed from 1 to 0. The reset value shown only applies to power-on reset when the register is not yet committed; any other type of reset does not affect this register. Once committed, the register retains its value through power-on reset. Once committed, the only way to restore the factory default value of this register is to perform the sequence detailed in “Recovering a "Locked" Microcontroller” on page 205.

---

### User Register n (USER_REGn)

**Base** 0x400F.E000  
**Offset** 0x1E0  
**Type** RW, reset 0xFFFF.FFFF

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:0 | DATA | RW | 0xFFFF.FFFF | User Data  
Contains the user data value. This field is initialized to all 1s and once committed, retains its value through power-on reset. |
9 Micro Direct Memory Access (μDMA)

The TM4C123GH6PZ microcontroller includes a Direct Memory Access (DMA) controller, known as micro-DMA (μDMA). The μDMA controller provides a way to offload data transfer tasks from the Cortex™-M4F processor, allowing for more efficient use of the processor and the available bus bandwidth. The μDMA controller can perform transfers between memory and peripherals. It has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory as the peripheral is ready to transfer more data.

The μDMA controller provides the following features:

- ARM® PrimeCell® 32-channel configurable μDMA controller
- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory in multiple transfer modes
  - Basic for simple transfer scenarios
  - Ping-pong for continuous data flow
  - Scatter-gather for a programmable list of up to 256 arbitrary transfers initiated from a single request
- Highly flexible and configurable channel operation
  - Independently configured and operated channels
  - Dedicated channels for supported on-chip modules
  - Flexible channel assignments
  - One channel each for receive and transmit path for bidirectional modules
  - Dedicated channel for software-initiated transfers
  - Per-channel configurable priority scheme
  - Optional software-initiated requests for any channel
- Two levels of priority
- Design optimizations for improved bus access performance between μDMA controller and the processor core
  - μDMA controller access is subordinate to core access
  - RAM striping
  - Peripheral bus segmentation
- Data sizes of 8, 16, and 32 bits
- Transfer size is programmable in binary steps from 1 to 1024
- Source and destination address increment size of byte, half-word, word, or no increment
9.1 Block Diagram

Figure 9-1. µDMA Block Diagram

9.2 Functional Description

The µDMA controller is a flexible and highly configurable DMA controller designed to work efficiently with the microcontroller's Cortex-M4F processor core. It supports multiple data sizes and address increment schemes, multiple levels of priority among DMA channels, and several transfer modes to allow for sophisticated programmed data transfers. The µDMA controller's usage of the bus is always subordinate to the processor core, so it never holds up a bus transaction by the processor. Because the µDMA controller is only using otherwise-idle bus cycles, the data transfer bandwidth it provides is essentially free, with no impact on the rest of the system. The bus architecture has been optimized to greatly enhance the ability of the processor core and the µDMA controller to efficiently share the on-chip bus, thus improving performance. The optimizations include RAM striping and peripheral bus segmentation, which in many cases allow both the processor core and the µDMA controller to access the bus and perform simultaneous data transfers.

The µDMA controller can transfer data to and from the on-chip SRAM. However, because the Flash memory and ROM are located on a separate internal bus, it is not possible to transfer data from the Flash memory or ROM with the µDMA controller.

Each peripheral function that is supported has a dedicated channel on the µDMA controller that can be configured independently. The µDMA controller implements a unique configuration method using channel control structures that are maintained in system memory by the processor. While simple transfer modes are supported, it is also possible to build up sophisticated "task" lists in memory that allow the µDMA controller to perform arbitrary-sized transfers to and from arbitrary locations as part of a single transfer request. The µDMA controller also supports the use of ping-pong buffering to accommodate constant streaming of data to or from a peripheral.
Each channel also has a configurable arbitration size. The arbitration size is the number of items that are transferred in a burst before the μDMA controller re-arbitrates for channel priority. Using the arbitration size, it is possible to control exactly how many items are transferred to or from a peripheral each time it makes a μDMA service request.

9.2.1 Channel Assignments

Each DMA channel has up to five possible assignments which are selected using the DMA Channel Map Select n (DMACHMAPn) registers with 4-bit assignment fields for each μDMA channel.

Table 9-1 on page 597 shows the μDMA channel mapping. The Enc. column shows the encoding for the respective DMACHMAPn bit field. Encodings 0x5 - 0xF are all reserved. To support legacy software which uses the DMA Channel Assignment (DMACHASGN) register, Enc. 0 is equivalent to a DMACHASGN bit being clear, and Enc. 1 is equivalent to a DMACHASGN bit being set. If the DMACHASGN register is read, bit fields return 0 if the corresponding DMACHMAPn register field value are equal to 0, otherwise they return 1 if the corresponding DMACHMAPn register field values are not equal to 0. The Type indication in the table indicates if a particular peripheral uses a single request (S), burst request (B) or either (SB).

Note: Channels noted in the table as "Software" may be assigned to peripherals in the future. However, they are currently available for software use. Channel 30 is dedicated for software use.

The USB endpoints mapped to μDMA channels 0-3 can be changed with the USBDMASEL register (see page 1233).

Table 9-1. μDMA Channel Assignments

<table>
<thead>
<tr>
<th>Enc.</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ch #</td>
<td>Peripheral</td>
<td>Type</td>
<td>Peripheral</td>
<td>Type</td>
<td>Peripheral</td>
</tr>
<tr>
<td>0</td>
<td>USBO EP1 RX</td>
<td>SB</td>
<td>UART2 RX</td>
<td>SB</td>
<td>Software</td>
</tr>
<tr>
<td>1</td>
<td>USBO EP1 TX</td>
<td>B</td>
<td>UART2 TX</td>
<td>SB</td>
<td>Software</td>
</tr>
<tr>
<td>2</td>
<td>USBO EP2 RX</td>
<td>B</td>
<td>GPTimer 3A</td>
<td>B</td>
<td>Software</td>
</tr>
<tr>
<td>3</td>
<td>USBO EP2 TX</td>
<td>B</td>
<td>GPTimer 3B</td>
<td>B</td>
<td>Software</td>
</tr>
<tr>
<td>4</td>
<td>USBO EP3 RX</td>
<td>B</td>
<td>GPTimer 2A</td>
<td>B</td>
<td>Software</td>
</tr>
<tr>
<td>5</td>
<td>USBO EP3 TX</td>
<td>B</td>
<td>GPTimer 2B</td>
<td>B</td>
<td>Software</td>
</tr>
<tr>
<td>6</td>
<td>Software</td>
<td>B</td>
<td>GPTimer 2A</td>
<td>B</td>
<td>UART5 RX</td>
</tr>
<tr>
<td>7</td>
<td>Software</td>
<td>B</td>
<td>GPTimer 2B</td>
<td>B</td>
<td>UART5 TX</td>
</tr>
<tr>
<td>8</td>
<td>UART0 RX</td>
<td>SB</td>
<td>UART1 RX</td>
<td>SB</td>
<td>Software</td>
</tr>
<tr>
<td>9</td>
<td>UART0 TX</td>
<td>SB</td>
<td>UART1 TX</td>
<td>SB</td>
<td>Software</td>
</tr>
<tr>
<td>10</td>
<td>SSIO RX</td>
<td>SS1 RX</td>
<td>SB</td>
<td>UART6 RX</td>
<td>SB</td>
</tr>
<tr>
<td>11</td>
<td>SSIO TX</td>
<td>SS1 TX</td>
<td>SB</td>
<td>UART6 TX</td>
<td>SB</td>
</tr>
<tr>
<td>12</td>
<td>Software</td>
<td>B</td>
<td>UART2 RX</td>
<td>SB</td>
<td>SS1 RX</td>
</tr>
<tr>
<td>13</td>
<td>Software</td>
<td>B</td>
<td>UART2 TX</td>
<td>SB</td>
<td>SS1 TX</td>
</tr>
<tr>
<td>14</td>
<td>ADC0 SS0</td>
<td>B</td>
<td>GPTimer 2A</td>
<td>B</td>
<td>SS1 RX</td>
</tr>
<tr>
<td>15</td>
<td>ADC0 SS1</td>
<td>B</td>
<td>GPTimer 2B</td>
<td>B</td>
<td>SS1 RX</td>
</tr>
<tr>
<td>16</td>
<td>ADC0 SS2</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>UART3 RX</td>
</tr>
<tr>
<td>17</td>
<td>ADC0 SS3</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>UART3 TX</td>
</tr>
<tr>
<td>18</td>
<td>GPTimer 0A</td>
<td>B</td>
<td>GPTimer 1A</td>
<td>B</td>
<td>UART4 RX</td>
</tr>
<tr>
<td>19</td>
<td>GPTimer 0B</td>
<td>B</td>
<td>GPTimer 1B</td>
<td>B</td>
<td>UART4 TX</td>
</tr>
<tr>
<td>20</td>
<td>GPTimer 1A</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>UART7 RX</td>
</tr>
</tbody>
</table>
Table 9-1. μDMA Channel Assignments (continued)

<table>
<thead>
<tr>
<th>Enc.</th>
<th>Ch #</th>
<th>Peripheral</th>
<th>Type</th>
<th>Peripheral</th>
<th>Type</th>
<th>Peripheral</th>
<th>Type</th>
<th>Peripheral</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>GPI Timer 1B</td>
<td>B Software</td>
<td>2</td>
<td>UART 7 TX</td>
<td>SB</td>
<td>GPIO J</td>
<td>B Software</td>
<td>B</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>UART 1 RX</td>
<td>SB</td>
<td>2</td>
<td>Software</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>Software</td>
<td>B</td>
</tr>
<tr>
<td>23</td>
<td>UART 1 TX</td>
<td>SB</td>
<td>2</td>
<td>Software</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>Software</td>
<td>B</td>
</tr>
<tr>
<td>24</td>
<td>SS1 RX</td>
<td>SB</td>
<td>2</td>
<td>ADC 1 SS0</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>GP Wide Timer 3A</td>
<td>B</td>
</tr>
<tr>
<td>25</td>
<td>SS1 TX</td>
<td>SB</td>
<td>2</td>
<td>ADC 1 SS1</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>GP Wide Timer 3B</td>
<td>B</td>
</tr>
<tr>
<td>26</td>
<td>Software</td>
<td>B</td>
<td>2</td>
<td>ADC 1 SS2</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>GP Wide Timer 4A</td>
<td>B</td>
</tr>
<tr>
<td>27</td>
<td>Software</td>
<td>B</td>
<td>2</td>
<td>ADC 1 SS3</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>GP Wide Timer 4B</td>
<td>B</td>
</tr>
<tr>
<td>28</td>
<td>Software</td>
<td>B</td>
<td>2</td>
<td>Software</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>GP Wide Timer 5A</td>
<td>B</td>
</tr>
<tr>
<td>29</td>
<td>Software</td>
<td>B</td>
<td>2</td>
<td>Software</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>GP Wide Timer 5B</td>
<td>B</td>
</tr>
<tr>
<td>30</td>
<td>Software</td>
<td>B</td>
<td>2</td>
<td>Software</td>
<td>B</td>
<td>Software</td>
<td>B</td>
<td>Software</td>
<td>B</td>
</tr>
<tr>
<td>31</td>
<td>Reserved</td>
<td>B</td>
<td>2</td>
<td>Reserved</td>
<td>B</td>
<td>Reserved</td>
<td>B</td>
<td>Reserved</td>
<td>B</td>
</tr>
</tbody>
</table>

9.2.2 Priority

The μDMA controller assigns priority to each channel based on the channel number and the priority level bit for the channel. Channel number 0 has the highest priority and as the channel number increases, the priority of a channel decreases. Each channel has a priority level bit to provide two levels of priority: default priority and high priority. If the priority level bit is set, then that channel has higher priority than all other channels at default priority. If multiple channels are set for high priority, then the channel number is used to determine relative priority among all the high priority channels.

The priority bit for a channel can be set using the DMA Channel Priority Set (DMAPRIOSET) register and cleared with the DMA Channel Priority Clear (DMAPRICLR) register.

9.2.3 Arbitration Size

When a μDMA channel requests a transfer, the μDMA controller arbitrates among all the channels making a request and services the μDMA channel with the highest priority. Once a transfer begins, it continues for a selectable number of transfers before rearbitrating among the requesting channels again. The arbitration size can be configured for each channel, ranging from 1 to 1024 item transfers.

If a lower priority μDMA channel uses a large arbitration size, the latency for higher priority channels is increased because the μDMA controller completes the lower priority burst before checking for higher priority requests. Therefore, lower priority channels should not use a large arbitration size for best response on high priority channels.

9.2.4 Request Types

The μDMA controller responds to two types of requests from a peripheral: single or burst. Each peripheral may support either or both types of requests. A single request means that the peripheral...
is ready to transfer one item, while a burst request means that the peripheral is ready to transfer multiple items.

The μDMA controller responds differently depending on whether the peripheral is making a single request or a burst request. If both are asserted, and the μDMA channel has been set up for a burst transfer, then the burst request takes precedence. See Table 9-2 on page 599, which shows how each peripheral supports the two request types.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Event that generates Single Request</th>
<th>Event that generates Burst Request</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>None</td>
<td>FIFO half full</td>
</tr>
<tr>
<td>General-Purpose Timer</td>
<td>None</td>
<td>Trigger event</td>
</tr>
<tr>
<td>GPIO</td>
<td>Raw interrupt pulse</td>
<td>None</td>
</tr>
<tr>
<td>SSI TX</td>
<td>TX FIFO Not Full</td>
<td>TX FIFO Level (fixed at 4)</td>
</tr>
<tr>
<td>SSI RX</td>
<td>RX FIFO Not Empty</td>
<td>RX FIFO Level (fixed at 4)</td>
</tr>
<tr>
<td>UART TX</td>
<td>TX FIFO Not Full</td>
<td>TX FIFO Level (configurable)</td>
</tr>
<tr>
<td>UART RX</td>
<td>RX FIFO Not Full</td>
<td>RX FIFO Level (configurable)</td>
</tr>
<tr>
<td>USB TX</td>
<td>None</td>
<td>FIFO TXRDY</td>
</tr>
<tr>
<td>USB RX</td>
<td>None</td>
<td>FIFO RXRDY</td>
</tr>
</tbody>
</table>

9.2.4.1 Single Request

When a single request is detected, and not a burst request, the μDMA controller transfers one item and then stops to wait for another request.

9.2.4.2 Burst Request

When a burst request is detected, the μDMA controller transfers the number of items that is the lesser of the arbitration size or the number of items remaining in the transfer. Therefore, the arbitration size should be the same as the number of data items that the peripheral can accommodate when making a burst request. For example, the UART generates a burst request based on the FIFO trigger level. In this case, the arbitration size should be set to the amount of data that the FIFO can transfer when the trigger level is reached. A burst transfer runs to completion once it is started, and cannot be interrupted, even by a higher priority channel. Burst transfers complete in a shorter time than the same number of non-burst transfers.

It may be desirable to use only burst transfers and not allow single transfers. For example, perhaps the nature of the data is such that it only makes sense when transferred together as a single unit rather than one piece at a time. The single request can be disabled by using the DMA Channel Useburst Set (DMAUSEBURSTSET) register. By setting the bit for a channel in this register, the μDMA controller only responds to burst requests for that channel.

9.2.5 Channel Configuration

The μDMA controller uses an area of system memory to store a set of channel control structures in a table. The control table may have one or two entries for each μDMA channel. Each entry in the table structure contains source and destination pointers, transfer size, and transfer mode. The control table can be located anywhere in system memory, but it must be contiguous and aligned on a 1024-byte boundary.

Table 9-3 on page 600 shows the layout in memory of the channel control table. Each channel may have one or two control structures in the control table: a primary control structure and an optional alternate control structure. The table is organized so that all of the primary entries are in the first
half of the table, and all the alternate structures are in the second half of the table. The primary entry is used for simple transfer modes where transfers can be reconfigured and restarted after each transfer is complete. In this case, the alternate control structures are not used and therefore only the first half of the table must be allocated in memory; the second half of the control table is not necessary, and that memory can be used for something else. If a more complex transfer mode is used such as ping-pong or scatter-gather, then the alternate control structure is also used and memory space should be allocated for the entire table.

Any unused memory in the control table may be used by the application. This includes the control structures for any channels that are unused by the application as well as the unused control word for each channel.

Table 9-3. Control Structure Memory Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0, Primary</td>
</tr>
<tr>
<td>0x10</td>
<td>1, Primary</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0x1F0</td>
<td>31, Primary</td>
</tr>
<tr>
<td>0x200</td>
<td>0, Alternate</td>
</tr>
<tr>
<td>0x210</td>
<td>1, Alternate</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0x3F0</td>
<td>31, Alternate</td>
</tr>
</tbody>
</table>

Table 9-4 shows an individual control structure entry in the control table. Each entry is aligned on a 16-byte boundary. The entry contains four long words: the source end pointer, the destination end pointer, the control word, and an unused entry. The end pointers point to the ending address of the transfer and are inclusive. If the source or destination is non-incrementing (as for a peripheral register), then the pointer should point to the transfer address.

Table 9-4. Channel Control Structure

<table>
<thead>
<tr>
<th>Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>Source End Pointer</td>
</tr>
<tr>
<td>0x004</td>
<td>Destination End Pointer</td>
</tr>
<tr>
<td>0x008</td>
<td>Control Word</td>
</tr>
<tr>
<td>0x00C</td>
<td>Unused</td>
</tr>
</tbody>
</table>

The control word contains the following fields:

- Source and destination data sizes
- Source and destination address increment size
- Number of transfers before bus arbitration
- Total number of items to transfer
- Useburst flag
- Transfer mode
The control word and each field are described in detail in “μDMA Channel Control Structure” on page 618. The μDMA controller updates the transfer size and transfer mode fields as the transfer is performed. At the end of a transfer, the transfer size indicates 0, and the transfer mode indicates “stopped.” Because the control word is modified by the μDMA controller, it must be reconfigured before each new transfer. The source and destination end pointers are not modified, so they can be left unchanged if the source or destination addresses remain the same.

Prior to starting a transfer, a μDMA channel must be enabled by setting the appropriate bit in the DMA Channel Enable Set (DMAENASET) register. A channel can be disabled by setting the channel bit in the DMA Channel Enable Clear (DMAENACLR) register. At the end of a complete μDMA transfer, the controller automatically disables the channel.

9.2.6 Transfer Modes

The μDMA controller supports several transfer modes. Two of the modes support simple one-time transfers. Several complex modes support a continuous flow of data.

9.2.6.1 Stop Mode

While Stop is not actually a transfer mode, it is a valid value for the mode field of the control word. When the mode field has this value, the μDMA controller does not perform any transfers and disables the channel if it is enabled. At the end of a transfer, the μDMA controller updates the control word to set the mode to Stop.

9.2.6.2 Basic Mode

In Basic mode, the μDMA controller performs transfers as long as there are more items to transfer, and a transfer request is present. This mode is used with peripherals that assert a μDMA request signal whenever the peripheral is ready for a data transfer. Basic mode should not be used in any situation where the request is momentary even though the entire transfer should be completed. For example, a software-initiated transfer creates a momentary request, and in Basic mode, only the number of transfers specified by the ARBSIZE field in the DMA Channel Control Word (DMACHCTL) register is transferred on a software request, even if there is more data to transfer.

When all of the items have been transferred using Basic mode, the μDMA controller sets the mode for that channel to Stop.

9.2.6.3 Auto Mode

Auto mode is similar to Basic mode, except that once a transfer request is received, the transfer runs to completion, even if the μDMA request is removed. This mode is suitable for software-triggered transfers. Generally, Auto mode is not used with a peripheral.

When all the items have been transferred using Auto mode, the μDMA controller sets the mode for that channel to Stop.

9.2.6.4 Ping-Pong

Ping-Pong mode is used to support a continuous data flow to or from a peripheral. To use Ping-Pong mode, both the primary and alternate data structures must be implemented. Both structures are set up by the processor for data transfer between memory and a peripheral. The transfer is started using the primary control structure. When the transfer using the primary control structure is complete, the μDMA controller reads the alternate control structure for that channel to continue the transfer. Each time this happens, an interrupt is generated, and the processor can reload the control structure for the just-completed transfer. Data flow can continue indefinitely this way, using the primary and alternate control structures to switch back and forth between buffers as the data flows to or from the peripheral.
Refer to Figure 9-2 on page 602 for an example showing operation in Ping-Pong mode.

Figure 9-2. Example of Ping-Pong μDMA Transaction

9.2.6.5 Memory Scatter-Gather

Memory Scatter-Gather mode is a complex mode used when data must be transferred to or from varied locations in memory instead of a set of contiguous locations in a memory buffer. For example,
a gather μDMA operation could be used to selectively read the payload of several stored packets of a communication protocol and store them together in sequence in a memory buffer.

In Memory Scatter-Gather mode, the primary control structure is used to program the alternate control structure from a table in memory. The table is set up by the processor software and contains a list of control structures, each containing the source and destination end pointers, and the control word for a specific transfer. The mode of each control word must be set to Scatter-Gather mode. Each entry in the table is copied in turn to the alternate structure where it is then executed. The μDMA controller alternates between using the primary control structure to copy the next transfer instruction from the list and then executing the new transfer instruction. The end of the list is marked by programming the control word for the last entry to use Auto transfer mode. Once the last transfer is performed using Auto mode, the μDMA controller stops. A completion interrupt is generated only after the last transfer. It is possible to loop the list by having the last entry copy the primary control structure to point back to the beginning of the list (or to a new list). It is also possible to trigger a set of other channels to perform a transfer, either directly, by programming a write to the software trigger for another channel, or indirectly, by causing a peripheral action that results in a μDMA request.

By programming the μDMA controller using this method, a set of up to 256 arbitrary transfers can be performed based on a single μDMA request.

Refer to Figure 9-3 on page 604 and Figure 9-4 on page 605, which show an example of operation in Memory Scatter-Gather mode. This example shows a gather operation, where data in three separate buffers in memory is copied together into one buffer. Figure 9-3 on page 604 shows how the application sets up a μDMA task list in memory that is used by the controller to perform three sets of copy operations from different locations in memory. The primary control structure for the channel that is used for the operation is configured to copy from the task list to the alternate control structure.

Figure 9-4 on page 605 shows the sequence as the μDMA controller performs the three sets of copy operations. First, using the primary control structure, the μDMA controller loads the alternate control structure with task A. It then performs the copy operation specified by task A, copying the data from the source buffer A to the destination buffer. Next, the μDMA controller again uses the primary control structure to load task B into the alternate control structure, and then performs the B operation with the alternate control structure. The process is repeated for task C.
NOTES:
1. Application has a need to copy data items from three separate locations in memory into one combined buffer.
2. Application sets up μDMA “task list” in memory, which contains the pointers and control configuration for three μDMA copy “tasks.”
3. Application sets up the channel primary control structure to copy each task configuration, one at a time, to the alternate control structure, where it is executed by the μDMA controller.
4. The SRC and DST pointers in the task list must point to the last location in the corresponding buffer.
Figure 9-4. Memory Scatter-Gather, \(\mu\)DMA Copy Sequence

Using the channel’s primary control structure, the \(\mu\)DMA controller copies task A configuration to the channel’s alternate control structure.

Then, using the channel’s alternate control structure, the \(\mu\)DMA controller copies data from the source buffer A to the destination buffer.

Using the channel’s primary control structure, the \(\mu\)DMA controller copies task B configuration to the channel’s alternate control structure.

Then, using the channel’s alternate control structure, the \(\mu\)DMA controller copies data from the source buffer B to the destination buffer.

Using the channel’s primary control structure, the \(\mu\)DMA controller copies task C configuration to the channel’s alternate control structure.

Then, using the channel’s alternate control structure, the \(\mu\)DMA controller copies data from the source buffer C to the destination buffer.
9.2.6.6 Peripheral Scatter-Gather

Peripheral Scatter-Gather mode is very similar to Memory Scatter-Gather, except that the transfers are controlled by a peripheral making a μDMA request. Upon detecting a request from the peripheral, the μDMA controller uses the primary control structure to copy one entry from the list to the alternate control structure and then performs the transfer. At the end of this transfer, the next transfer is started only if the peripheral again asserts a μDMA request. The μDMA controller continues to perform transfers from the list only when the peripheral is making a request, until the last transfer is complete. A completion interrupt is generated only after the last transfer.

By using this method, the μDMA controller can transfer data to or from a peripheral from a set of arbitrary locations whenever the peripheral is ready to transfer data.

Refer to Figure 9-5 on page 607 and Figure 9-6 on page 608, which show an example of operation in Peripheral Scatter-Gather mode. This example shows a gather operation, where data from three separate buffers in memory is copied to a single peripheral data register. Figure 9-5 on page 607 shows how the application sets up a μDMA task list in memory that is used by the controller to perform three sets of copy operations from different locations in memory. The primary control structure for the channel that is used for the operation is configured to copy from the task list to the alternate control structure.

Figure 9-6 on page 608 shows the sequence as the μDMA controller performs the three sets of copy operations. First, using the primary control structure, the μDMA controller loads the alternate control structure with task A. It then performs the copy operation specified by task A, copying the data from the source buffer A to the peripheral data register. Next, the μDMA controller again uses the primary control structure to load task B into the alternate control structure, and then performs the B operation with the alternate control structure. The process is repeated for task C.
Figure 9-5. Peripheral Scatter-Gather, Setup and Configuration

NOTES:
1. Application has a need to copy data items from three separate locations in memory into a peripheral data register.
2. Application sets up µDMA "task list" in memory, which contains the pointers and control configuration for three µDMA copy "tasks."
3. Application sets up the channel primary control structure to copy each task configuration, one at a time, to the alternate control structure, where it is executed by the µDMA controller.
Using the channel’s primary control structure, the μDMA controller copies task A configuration to the channel’s alternate control structure. Then, using the channel’s alternate control structure, the μDMA controller copies data from the source buffer A to the peripheral data register.

Using the channel’s primary control structure, the μDMA controller copies task B configuration to the channel’s alternate control structure. Then, using the channel’s alternate control structure, the μDMA controller copies data from the source buffer B to the peripheral data register.

Using the channel’s primary control structure, the μDMA controller copies task C configuration to the channel’s alternate control structure. Then, using the channel’s alternate control structure, the μDMA controller copies data from the source buffer C to the peripheral data register.
9.2.7 Transfer Size and Increment

The μDMA controller supports transfer data sizes of 8, 16, or 32 bits. The source and destination data size must be the same for any given transfer. The source and destination address can be auto-incremented by bytes, half-words, or words, or can be set to no increment. The source and destination address increment values can be set independently, and it is not necessary for the address increment to match the data size as long as the increment is the same or larger than the data size. For example, it is possible to perform a transfer using 8-bit data size, but using an address increment of full words (4 bytes). The data to be transferred must be aligned in memory according to the data size (8, 16, or 32 bits).

Table 9-5 shows the configuration to read from a peripheral that supplies 8-bit data.

Table 9-5. μDMA Read Example: 8-Bit Peripheral

<table>
<thead>
<tr>
<th>Field</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source data size</td>
<td>8 bits</td>
</tr>
<tr>
<td>Destination data size</td>
<td>8 bits</td>
</tr>
<tr>
<td>Source address increment</td>
<td>No increment</td>
</tr>
<tr>
<td>Destination address increment</td>
<td>Byte</td>
</tr>
<tr>
<td>Source end pointer</td>
<td>Peripheral read FIFO register</td>
</tr>
<tr>
<td>Destination end pointer</td>
<td>End of the data buffer in memory</td>
</tr>
</tbody>
</table>

9.2.8 Peripheral Interface

Each peripheral that supports μDMA has a single request and/or burst request signal that is asserted when the peripheral is ready to transfer data (see Table 9-2 on page 599). The request signal can be disabled or enabled using the DMA Channel Request Mask Set (DMAREQMASKSET) and DMA Channel Request Mask Clear (DMAREQMASKCLR) registers. The μDMA request signal is disabled, or masked, when the channel request mask bit is set. When the request is not masked, the μDMA channel is configured correctly and enabled, and the peripheral asserts the request signal, the μDMA controller begins the transfer.

Note: When using μDMA to transfer data to and from a peripheral, the peripheral must disable all interrupts to the NVIC.

When a μDMA transfer is complete, the μDMA controller generates an interrupt, see "Interrupts and Errors" on page 610 for more information.

For more information on how a specific peripheral interacts with the μDMA controller, refer to the DMA Operation section in the chapter that discusses that peripheral.

9.2.9 Software Request

One μDMA channel is dedicated to software-initiated transfers. This channel also has a dedicated interrupt to signal completion of a μDMA transfer. A transfer is initiated by software by first configuring and enabling the transfer, and then issuing a software request using the DMA Channel Software Request (DMASWREQ) register. For software-based transfers, the Auto transfer mode should be used.

It is possible to initiate a transfer on any available software channel using the DMASWREQ register. If a request is initiated by software using a peripheral μDMA channel, then the completion interrupt occurs on the interrupt vector for the peripheral instead of the software interrupt vector. Any peripheral channel may be used for software requests as long as the corresponding peripheral is not using μDMA for data transfer.
9.2.10 Interrupts and Errors

Depending on the peripheral, the μDMA can indicate transfer completion at the end of an entire transfer or when a FIFO or buffer reaches a certain level (see Table 9-2 on page 599 and the individual peripheral chapters). When a μDMA transfer is complete, the μDMA controller generates a completion interrupt on the interrupt vector of the peripheral. Therefore, if μDMA is used to transfer data for a peripheral and interrupts are used, then the interrupt handler for that peripheral must be designed to handle the μDMA transfer completion interrupt. If the transfer uses the software μDMA channel, then the completion interrupt occurs on the dedicated software μDMA interrupt vector (see Table 9-6 on page 610).

When μDMA is enabled for a peripheral, the μDMA controller stops the normal transfer interrupts for a peripheral from reaching the interrupt controller (the interrupts are still reported in the peripheral's interrupt registers). Thus, when a large amount of data is transferred using μDMA, instead of receiving multiple interrupts from the peripheral as data flows, the interrupt controller receives only one interrupt when the transfer is complete. Unmasked peripheral error interrupts continue to be sent to the interrupt controller.

When a μDMA channel generates a completion interrupt, the \textit{CHIS} bit corresponding to the peripheral channel is set in the \textit{DMA Channel Interrupt Status (DMACHIS)} register (see page 645). This register can be used by the peripheral interrupt handler code to determine if the interrupt was caused by the μDMA channel or an error event reported by the peripheral's interrupt registers. The completion interrupt request from the μDMA controller is automatically cleared when the interrupt handler is activated.

When transfers are performed from a FIFO of the UART or SSI using the μDMA, and any interrupt is generated from the UART or SSI, the module's status bit in the \textit{DMA Channel Interrupt Status (DMACHIS)} register must be checked at the end of the interrupt service routine. If the status bit is set, clear the interrupt by writing a 1 to it.

If the μDMA controller encounters a bus or memory protection error as it attempts to perform a data transfer, it disables the μDMA channel that caused the error and generates an interrupt on the μDMA error interrupt vector. The processor can read the \textit{DMA Bus Error Clear (DMAERRCLR)} register to determine if an error is pending. The \textit{ERRCLR} bit is set if an error occurred. The error can be cleared by writing a 1 to the \textit{ERRCLR} bit.

Table 9-6 shows the dedicated interrupt assignments for the μDMA controller.

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>46</td>
<td>μDMA Software Channel Transfer</td>
</tr>
<tr>
<td>47</td>
<td>μDMA Error</td>
</tr>
</tbody>
</table>

9.3 Initialization and Configuration

9.3.1 Module Initialization

Before the μDMA controller can be used, it must be enabled in the System Control block and in the peripheral. The location of the channel control structure must also be programmed.

The following steps should be performed one time during system initialization:

1. Enable the μDMA clock using the \textit{RCGCDMA} register (see page 345).
2. Enable the μDMA controller by setting the \texttt{MASTEREN} bit of the \texttt{DMA Configuration (DMACFG)} register.

3. Program the location of the channel control table by writing the base address of the table to the \texttt{DMA Channel Control Base Pointer (DMACTLBASE)} register. The base address must be aligned on a 1024-byte boundary.

9.3.2 Configuring a Memory-to-Memory Transfer

μDMA channel 30 is dedicated for software-initiated transfers. However, any channel can be used for software-initiated, memory-to-memory transfer if the associated peripheral is not being used.

9.3.2.1 Configure the Channel Attributes

First, configure the channel attributes:

1. Program bit 30 of the \texttt{DMA Channel Priority Set (DMAPRIOSET)} or \texttt{DMA Channel Priority Clear (DMAPRIOCLR)} registers to set the channel to High priority or Default priority.

2. Set bit 30 of the \texttt{DMA Channel Primary Alternate Clear (DMAALTCLR)} register to select the primary channel control structure for this transfer.

3. Set bit 30 of the \texttt{DMA Channel Useburst Clear (DMAUSEBURSTCLR)} register to allow the μDMA controller to respond to single and burst requests.

4. Set bit 30 of the \texttt{DMA Channel Request Mask Clear (DMAREQMASKCLR)} register to allow the μDMA controller to recognize requests for this channel.

9.3.2.2 Configure the Channel Control Structure

Now the channel control structure must be configured.

This example transfers 256 words from one memory buffer to another. Channel 30 is used for a software transfer, and the control structure for channel 30 is at offset 0x1E0 of the channel control table. The channel control structure for channel 30 is located at the offsets shown in Table 9-7.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Table Base + 0x1E0</td>
<td>Channel 30 Source End Pointer</td>
</tr>
<tr>
<td>Control Table Base + 0x1E4</td>
<td>Channel 30 Destination End Pointer</td>
</tr>
<tr>
<td>Control Table Base + 0x1E8</td>
<td>Channel 30 Control Word</td>
</tr>
</tbody>
</table>

Configure the Source and Destination

The source and destination end pointers must be set to the last address for the transfer (inclusive).

1. Program the source end pointer at offset 0x1E0 to the address of the source buffer + 0x3FC.

2. Program the destination end pointer at offset 0x1E4 to the address of the destination buffer + 0x3FC.

The control word at offset 0x1E8 must be programmed according to Table 9-8.
Table 9-8. Channel Control Word Configuration for Memory Transfer Example

<table>
<thead>
<tr>
<th>Field in DMACHCTL</th>
<th>Bits</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSTINC</td>
<td>31:30</td>
<td>2</td>
<td>32-bit destination address increment</td>
</tr>
<tr>
<td>DSTSIZE</td>
<td>29:28</td>
<td>2</td>
<td>32-bit destination data size</td>
</tr>
<tr>
<td>SRCINC</td>
<td>27:26</td>
<td>2</td>
<td>32-bit source address increment</td>
</tr>
<tr>
<td>SRCSIZE</td>
<td>25:24</td>
<td>2</td>
<td>32-bit source data size</td>
</tr>
<tr>
<td>reserved</td>
<td>23:18</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>ARBSIZE</td>
<td>17:14</td>
<td>3</td>
<td>Arbitrates after 8 transfers</td>
</tr>
<tr>
<td>XFERSIZE</td>
<td>13:4</td>
<td>255</td>
<td>Transfer 256 items</td>
</tr>
<tr>
<td>NXTUSEBURST</td>
<td>3</td>
<td>0</td>
<td>N/A for this transfer type</td>
</tr>
<tr>
<td>XFERMODE</td>
<td>2:0</td>
<td>2</td>
<td>Use Auto-request transfer mode</td>
</tr>
</tbody>
</table>

9.3.2.3 Start the Transfer

Now the channel is configured and is ready to start.

1. Enable the channel by setting bit 30 of the DMA Channel Enable Set (DMAENASET) register.

2. Issue a transfer request by setting bit 30 of the DMA Channel Software Request (DMASWREQ) register.

The μDMA transfer begins. If the interrupt is enabled, then the processor is notified by interrupt when the transfer is complete. If needed, the status can be checked by reading bit 30 of the DMAENASET register. This bit is automatically cleared when the transfer is complete. The status can also be checked by reading the XFERMODE field of the channel control word at offset 0x1E8. This field is automatically cleared at the end of the transfer.

9.3.3 Configuring a Peripheral for Simple Transmit

This example configures the μDMA controller to transmit a buffer of data to a peripheral. The peripheral has a transmit FIFO with a trigger level of 4. The example peripheral uses μDMA channel 7.

9.3.3.1 Configure the Channel Attributes

First, configure the channel attributes:

1. Configure bit 7 of the DMA Channel Priority Set (DMAPRIOSET) or DMA Channel Priority Clear (DMAPRIOCCLR) registers to set the channel to High priority or Default priority.

2. Set bit 7 of the DMA Channel Primary Alternate Clear (DMAALTCLR) register to select the primary channel control structure for this transfer.

3. Set bit 7 of the DMA Channel Useburst Clear (DMAUSEBURSTCLR) register to allow the μDMA controller to respond to single and burst requests.

4. Set bit 7 of the DMA Channel Request Mask Clear (DMAREQMASKCLR) register to allow the μDMA controller to recognize requests for this channel.
9.3.3.2 Configure the Channel Control Structure

This example transfers 64 bytes from a memory buffer to the peripheral's transmit FIFO register using μDMA channel 7. The control structure for channel 7 is at offset 0x070 of the channel control table. The channel control structure for channel 7 is located at the offsets shown in Table 9-9.

Table 9-9. Channel Control Structure Offsets for Channel 7

<table>
<thead>
<tr>
<th>Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Table Base + 0x070</td>
<td>Channel 7 Source End Pointer</td>
</tr>
<tr>
<td>Control Table Base + 0x074</td>
<td>Channel 7 Destination End Pointer</td>
</tr>
<tr>
<td>Control Table Base + 0x078</td>
<td>Channel 7 Control Word</td>
</tr>
</tbody>
</table>

Configure the Source and Destination

The source and destination end pointers must be set to the last address for the transfer (inclusive). Because the peripheral pointer does not change, it simply points to the peripheral's data register.

1. Program the source end pointer at offset 0x070 to the address of the source buffer + 0x3F.
2. Program the destination end pointer at offset 0x074 to the address of the peripheral's transmit FIFO register.

The control word at offset 0x078 must be programmed according to Table 9-10.

Table 9-10. Channel Control Word Configuration for Peripheral Transmit Example

<table>
<thead>
<tr>
<th>Field in DMACHCTL</th>
<th>Bits</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSTINC</td>
<td>31:30</td>
<td>3</td>
<td>Destination address does not increment</td>
</tr>
<tr>
<td>DSTSIZE</td>
<td>29:28</td>
<td>0</td>
<td>8-bit destination data size</td>
</tr>
<tr>
<td>SRCINC</td>
<td>27:26</td>
<td>0</td>
<td>8-bit source address increment</td>
</tr>
<tr>
<td>SRCSIZE</td>
<td>25:24</td>
<td>0</td>
<td>8-bit source data size</td>
</tr>
<tr>
<td>reserved</td>
<td>23:18</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>ARBSIZE</td>
<td>17:14</td>
<td>2</td>
<td>Arbitrates after 4 transfers</td>
</tr>
<tr>
<td>XFERSIZE</td>
<td>13:4</td>
<td>63</td>
<td>Transfer 64 items</td>
</tr>
<tr>
<td>NXTUSEBURST</td>
<td>3</td>
<td>0</td>
<td>N/A for this transfer type</td>
</tr>
<tr>
<td>XFERMODE</td>
<td>2:0</td>
<td>1</td>
<td>Use Basic transfer mode</td>
</tr>
</tbody>
</table>

Note: In this example, it is not important if the peripheral makes a single request or a burst request. Because the peripheral has a FIFO that triggers at a level of 4, the arbitration size is set to 4. If the peripheral does make a burst request, then 4 bytes are transferred, which is what the FIFO can accommodate. If the peripheral makes a single request (if there is any space in the FIFO), then one byte is transferred at a time. If it is important to the application that transfers only be made in bursts, then the Channel Useburst SET (DMAUSEBURSTSET) register.

9.3.3.3 Start the Transfer

Now the channel is configured and is ready to start.

1. Enable the channel by setting bit 7 of the DMA Channel Enable Set (DMAENASET) register.
The μDMA controller is now configured for transfer on channel 7. The controller makes transfers to
the peripheral whenever the peripheral asserts a μDMA request. The transfers continue until the
entire buffer of 64 bytes has been transferred. When that happens, the μDMA controller disables
the channel and sets the XFERMODE field of the channel control word to 0 (Stopped). The status of
the transfer can be checked by reading bit 7 of the DMA Channel Enable Set (DMAENASET)
register. This bit is automatically cleared when the transfer is complete. The status can also be
checked by reading the XFERMODE field of the channel control word at offset 0x078. This field is
automatically cleared at the end of the transfer.

If peripheral interrupts are enabled, then the peripheral interrupt handler receives an interrupt when
the entire transfer is complete.

9.3.4 Configuring a Peripheral for Ping-Pong Receive

This example configures the μDMA controller to continuously receive 8-bit data from a peripheral
into a pair of 64-byte buffers. The peripheral has a receive FIFO with a trigger level of 8. The example
peripheral uses μDMA channel 8.

9.3.4.1 Configure the Channel Attributes

First, configure the channel attributes:

1. Configure bit 8 of the DMA Channel Priority Set (DMAPRIOSSET) or DMA Channel Priority
   Clear (DMAPRIOCLR) registers to set the channel to High priority or Default priority.

2. Set bit 8 of the DMA Channel Primary Alternate Clear (DMAALTCLEAR) register to select the
   primary channel control structure for this transfer.

3. Set bit 8 of the DMA Channel Useburst Clear (DMAUSEBURSTCLR) register to allow the
   μDMA controller to respond to single and burst requests.

4. Set bit 8 of the DMA Channel Request Mask Clear (DMAREQMASKCLR) register to allow
   the μDMA controller to recognize requests for this channel.

9.3.4.2 Configure the Channel Control Structure

This example transfers bytes from the peripheral's receive FIFO register into two memory buffers
of 64 bytes each. As data is received, when one buffer is full, the μDMA controller switches to use
the other.

To use Ping-Pong buffering, both primary and alternate channel control structures must be used. The
primary control structure for channel 8 is at offset 0x080 of the channel control table, and the
alternate channel control structure is at offset 0x280. The channel control structures for channel 8
are located at the offsets shown in Table 9-11.

Table 9-11. Primary and Alternate Channel Control Structure Offsets for Channel 8

<table>
<thead>
<tr>
<th>Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Table Base + 0x080</td>
<td>Channel 8 Primary Source End Pointer</td>
</tr>
<tr>
<td>Control Table Base + 0x084</td>
<td>Channel 8 Primary Destination End Pointer</td>
</tr>
<tr>
<td>Control Table Base + 0x088</td>
<td>Channel 8 Primary Control Word</td>
</tr>
<tr>
<td>Control Table Base + 0x280</td>
<td>Channel 8 Alternate Source End Pointer</td>
</tr>
<tr>
<td>Control Table Base + 0x284</td>
<td>Channel 8 Alternate Destination End Pointer</td>
</tr>
<tr>
<td>Control Table Base + 0x288</td>
<td>Channel 8 Alternate Control Word</td>
</tr>
</tbody>
</table>
Configure the Source and Destination

The source and destination end pointers must be set to the last address for the transfer (inclusive). Because the peripheral pointer does not change, it simply points to the peripheral's data register. Both the primary and alternate sets of pointers must be configured.

1. Program the primary source end pointer at offset 0x080 to the address of the peripheral's receive buffer.

2. Program the primary destination end pointer at offset 0x084 to the address of ping-pong buffer A + 0x3F.

3. Program the alternate source end pointer at offset 0x280 to the address of the peripheral's receive buffer.

4. Program the alternate destination end pointer at offset 0x284 to the address of ping-pong buffer B + 0x3F.

The primary control word at offset 0x088 and the alternate control word at offset 0x288 are initially programmed the same way.

1. Program the primary channel control word at offset 0x088 according to Table 9-12.

2. Program the alternate channel control word at offset 0x288 according to Table 9-12.

Table 9-12. Channel Control Word Configuration for Peripheral Ping-Pong Receive Example

<table>
<thead>
<tr>
<th>Field in DMACHCTL</th>
<th>Bits</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSTINC</td>
<td>31:30</td>
<td>0</td>
<td>8-bit destination address increment</td>
</tr>
<tr>
<td>DSTSIZE</td>
<td>29:28</td>
<td>0</td>
<td>8-bit destination data size</td>
</tr>
<tr>
<td>SRCINC</td>
<td>27:26</td>
<td>3</td>
<td>Source address does not increment</td>
</tr>
<tr>
<td>SRCSIZE</td>
<td>25:24</td>
<td>0</td>
<td>8-bit source data size</td>
</tr>
<tr>
<td>reserved</td>
<td>23:18</td>
<td>0</td>
<td>Reserved</td>
</tr>
<tr>
<td>ARBSIZE</td>
<td>17:14</td>
<td>3</td>
<td>Arbitrates after 8 transfers</td>
</tr>
<tr>
<td>XFERSIZE</td>
<td>13:4</td>
<td>63</td>
<td>Transfer 64 items</td>
</tr>
<tr>
<td>NXTUSEBURST</td>
<td>3</td>
<td>0</td>
<td>N/A for this transfer type</td>
</tr>
<tr>
<td>XFERMODE</td>
<td>2:0</td>
<td>3</td>
<td>Use Ping-Pong transfer mode</td>
</tr>
</tbody>
</table>

Note: In this example, it is not important if the peripheral makes a single request or a burst request. Because the peripheral has a FIFO that triggers at a level of 8, the arbitration size is set to 8. If the peripheral does make a burst request, then 8 bytes are transferred, which is what the FIFO can accommodate. If the peripheral makes a single request (if there is any data in the FIFO), then one byte is transferred at a time. If it is important to the application that transfers only be made in bursts, then the Channel Useburst SET[8] bit should be set in the DMA Channel Useburst Set (DMAUSEBURSTSET) register.

9.3.4.3 Configure the Peripheral Interrupt

An interrupt handler should be configured when using μDMA Ping-Pong mode, it is best to use an interrupt handler. However, the Ping-Pong mode can be configured without interrupts by polling. The interrupt handler is triggered after each buffer is complete.

1. Configure and enable an interrupt handler for the peripheral.
9.3.4.4 Enable the μDMA Channel

Now the channel is configured and is ready to start.

1. Enable the channel by setting bit 8 of the DMA Channel Enable Set (DMAENASET) register.

9.3.4.5 Process Interrupts

The μDMA controller is now configured and enabled for transfer on channel 8. When the peripheral asserts the μDMA request signal, the μDMA controller makes transfers into buffer A using the primary channel control structure. When the primary transfer to buffer A is complete, it switches to the alternate channel control structure and makes transfers into buffer B. At the same time, the primary channel control word mode field is configured to indicate Stopped, and an interrupt is pending.

When an interrupt is triggered, the interrupt handler must determine which buffer is complete and process the data or set a flag that the data must be processed by non-interrupt buffer processing code. Then the next buffer transfer must be set up.

In the interrupt handler:

1. Read the primary channel control word at offset 0x088 and check the XFERMODE field. If the field is 0, this means buffer A is complete. If buffer A is complete, then:
   a. Process the newly received data in buffer A or signal the buffer processing code that buffer A has data available.
   b. Reprogram the primary channel control word at offset 0x88 according to Table 9-12 on page 615.

2. Read the alternate channel control word at offset 0x288 and check the XFERMODE field. If the field is 0, this means buffer B is complete. If buffer B is complete, then:
   a. Process the newly received data in buffer B or signal the buffer processing code that buffer B has data available.
   b. Reprogram the alternate channel control word at offset 0x288 according to Table 9-12 on page 615.

9.3.5 Configuring Channel Assignments

Channel assignments for each μDMA channel can be changed using the DMACHMAPn registers. Each 4-bit field represents a μDMA channel.

Refer to Table 9-1 on page 597 for channel assignments.

9.4 Register Map

Table 9-13 on page 617 lists the μDMA channel control structures and registers. The channel control structure shows the layout of one entry in the channel control table. The channel control table is located in system memory, and the location is determined by the application, thus the base address is n/a (not applicable) and noted as such above the register descriptions. In the table below, the offset for the channel control structures is the offset from the entry in the channel control table. See “Channel Configuration” on page 599 and Table 9-3 on page 600 for a description of how the entries in the channel control table are located in memory. The μDMA register addresses are given as a hexadecimal increment, relative to the μDMA base address of 0x400F.F000. Note that the μDMA module clock must be enabled before the registers can be programmed (see page 345). There must
be a delay of 3 system clocks after the μDMA module clock is enabled before any μDMA module registers are accessed.

Table 9-13. μDMA Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>DMASRCENDP</td>
<td>RW</td>
<td>-</td>
<td>DMA Channel Source Address End Pointer</td>
<td>619</td>
</tr>
<tr>
<td>0x004</td>
<td>DAMDSTENDP</td>
<td>RW</td>
<td>-</td>
<td>DMA Channel Destination Address End Pointer</td>
<td>620</td>
</tr>
<tr>
<td>0x008</td>
<td>DMACHCTL</td>
<td>RW</td>
<td>-</td>
<td>DMA Channel Control Word</td>
<td>621</td>
</tr>
<tr>
<td>0x000</td>
<td>DMASTAT</td>
<td>RO</td>
<td>0x001F.0000</td>
<td>DMA Status</td>
<td>626</td>
</tr>
<tr>
<td>0x004</td>
<td>DMACFG</td>
<td>WO</td>
<td>-</td>
<td>DMA Configuration</td>
<td>628</td>
</tr>
<tr>
<td>0x008</td>
<td>DMACTLBASE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Control Base Pointer</td>
<td>629</td>
</tr>
<tr>
<td>0x00C</td>
<td>DMAALTBASE</td>
<td>RO</td>
<td>0x0000.0200</td>
<td>DMA Alternate Channel Control Base Pointer</td>
<td>630</td>
</tr>
<tr>
<td>0x010</td>
<td>DMAWAITSTAT</td>
<td>RO</td>
<td>0x03C3.CF00</td>
<td>DMA Channel Wait-on-Request Status</td>
<td>631</td>
</tr>
<tr>
<td>0x014</td>
<td>DMASWREQ</td>
<td>WO</td>
<td>-</td>
<td>DMA Channel Software Request</td>
<td>632</td>
</tr>
<tr>
<td>0x018</td>
<td>DMAUSEBURSTSET</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Useburst Set</td>
<td>633</td>
</tr>
<tr>
<td>0x01C</td>
<td>DMAUSEBURSTCLR</td>
<td>WO</td>
<td>-</td>
<td>DMA Channel Useburst Clear</td>
<td>634</td>
</tr>
<tr>
<td>0x020</td>
<td>DMAREQMASKSET</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Request Mask Set</td>
<td>635</td>
</tr>
<tr>
<td>0x024</td>
<td>DMAREQMASKCLR</td>
<td>WO</td>
<td>-</td>
<td>DMA Channel Request Mask Clear</td>
<td>636</td>
</tr>
<tr>
<td>0x028</td>
<td>DMAENASET</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Enable Set</td>
<td>637</td>
</tr>
<tr>
<td>0x02C</td>
<td>DMAENACLRR</td>
<td>WO</td>
<td>-</td>
<td>DMA Channel Enable Clear</td>
<td>638</td>
</tr>
<tr>
<td>0x030</td>
<td>DMAALTSET</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Primary Alternate Set</td>
<td>639</td>
</tr>
<tr>
<td>0x034</td>
<td>DMAALTCLR</td>
<td>WO</td>
<td>-</td>
<td>DMA Channel Primary Alternate Clear</td>
<td>640</td>
</tr>
<tr>
<td>0x038</td>
<td>DAMPROIOSET</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Priority Set</td>
<td>641</td>
</tr>
<tr>
<td>0x03C</td>
<td>DAMPROICLR</td>
<td>WO</td>
<td>-</td>
<td>DMA Channel Priority Clear</td>
<td>642</td>
</tr>
<tr>
<td>0x04C</td>
<td>DMAERRCLR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Bus Error Clear</td>
<td>643</td>
</tr>
<tr>
<td>0x500</td>
<td>DACHASHGN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Assignment</td>
<td>644</td>
</tr>
<tr>
<td>0x504</td>
<td>DMACHIS</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>DMA Channel Interrupt Status</td>
<td>645</td>
</tr>
<tr>
<td>0x510</td>
<td>DMACHMAP0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Map Select 0</td>
<td>646</td>
</tr>
<tr>
<td>0x514</td>
<td>DMACHMAP1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Map Select 1</td>
<td>647</td>
</tr>
<tr>
<td>0x518</td>
<td>DMACHMAP2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Map Select 2</td>
<td>648</td>
</tr>
<tr>
<td>0x51C</td>
<td>DMACHMAP3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>DMA Channel Map Select 3</td>
<td>649</td>
</tr>
<tr>
<td>0xFD0</td>
<td>DMAPeriphId4</td>
<td>RO</td>
<td>0x0000.0004</td>
<td>DMA Peripheral Identification 4</td>
<td>654</td>
</tr>
<tr>
<td>0xFE0</td>
<td>DMAPeriphId0</td>
<td>RO</td>
<td>0x0000.0030</td>
<td>DMA Peripheral Identification 0</td>
<td>650</td>
</tr>
</tbody>
</table>
Table 9-13. μDMA Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFE4</td>
<td>DMAPeriphID1</td>
<td>RO</td>
<td>0x0000.00B2</td>
<td>DMA Peripheral Identification 1</td>
<td>651</td>
</tr>
<tr>
<td>0xFE8</td>
<td>DMAPeriphID2</td>
<td>RO</td>
<td>0x0000.00B</td>
<td>DMA Peripheral Identification 2</td>
<td>652</td>
</tr>
<tr>
<td>0xFEC</td>
<td>DMAPeriphID3</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>DMA Peripheral Identification 3</td>
<td>653</td>
</tr>
<tr>
<td>0xFF0</td>
<td>DMACellID0</td>
<td>RO</td>
<td>0x0000.00D</td>
<td>DMA PrimeCell Identification 0</td>
<td>655</td>
</tr>
<tr>
<td>0xFF4</td>
<td>DMACellID1</td>
<td>RO</td>
<td>0x0000.00F0</td>
<td>DMA PrimeCell Identification 1</td>
<td>656</td>
</tr>
<tr>
<td>0xFF8</td>
<td>DMACellID2</td>
<td>RO</td>
<td>0x0000.0005</td>
<td>DMA PrimeCell Identification 2</td>
<td>657</td>
</tr>
<tr>
<td>0xFFC</td>
<td>DMACellID3</td>
<td>RO</td>
<td>0x0000.00B1</td>
<td>DMA PrimeCell Identification 3</td>
<td>658</td>
</tr>
</tbody>
</table>

9.5 μDMA Channel Control Structure

The μDMA Channel Control Structure holds the transfer settings for a μDMA channel. Each channel has two control structures, which are located in a table in system memory. Refer to “Channel Configuration” on page 599 for an explanation of the Channel Control Table and the Channel Control Structure.

The channel control structure is one entry in the channel control table. Each channel has a primary and alternate structure. The primary control structures are located at offsets 0x0, 0x10, 0x20 and so on. The alternate control structures are located at offsets 0x200, 0x210, 0x220, and so on.
Register 1: DMA Channel Source Address End Pointer (DMASRCENDP), offset 0x000

DMA Channel Source Address End Pointer (DMASRCENDP) is part of the Channel Control Structure and is used to specify the source address for a μDMA transfer.

The μDMA controller can transfer data to and from the on-chip SRAM. However, because the Flash memory and ROM are located on a separate internal bus, it is not possible to transfer data to/from the Flash memory or ROM with the μDMA controller.

**Note:** The offset specified is from the base address of the control structure in system memory, not the μDMA module base address.

### DMA Channel Source Address End Pointer (DMASRCENDP)

**Base n/a**

**Offset 0x000**

**Type RW, reset -**

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDR 31:0</td>
<td>ADDR</td>
<td>RW</td>
<td>-</td>
<td>Source Address End Pointer</td>
</tr>
</tbody>
</table>

This field points to the last address of the μDMA transfer source (inclusive). If the source address is not incrementing (the SRCINC field in the DMACHCTL register is 0x3), then this field points at the source location itself (such as a peripheral data register).
Register 2: DMA Channel Destination Address End Pointer (DMADSTENDP), offset 0x004

DMA Channel Destination Address End Pointer (DMADSTENDP) is part of the Channel Control Structure and is used to specify the destination address for a μDMA transfer.

**Note:** The offset specified is from the base address of the control structure in system memory, not the μDMA module base address.

### DMA Channel Destination Address End Pointer (DMADSTENDP)

- **Base**: n/a
- **Offset**: 0x004
- **Type**: RW, reset -

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>ADDR</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Description**: Destination Address End Pointer

This field points to the last address of the μDMA transfer destination (inclusive). If the destination address is not incrementing (the DSTINC field in the DMACHCTL register is 0x3), then this field points at the destination location itself (such as a peripheral data register).
Register 3: DMA Channel Control Word (DMACHCTL), offset 0x008

DMA Channel Control Word (DMACHCTL) is part of the Channel Control Structure and is used to specify parameters of a μDMA transfer.

**Note:** The offset specified is from the base address of the control structure in system memory, not the μDMA module base address.

DMA Channel Control Word (DMACHCTL)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Destination Address Increment</td>
<td>0x0</td>
<td>Increment by 8-bit locations</td>
</tr>
<tr>
<td></td>
<td>0x1</td>
<td>Increment by 16-bit locations</td>
</tr>
<tr>
<td></td>
<td>0x2</td>
<td>Increment by 32-bit locations</td>
</tr>
<tr>
<td></td>
<td>0x3</td>
<td>No increment</td>
</tr>
</tbody>
</table>

Address remains set to the value of the Destination Address End Pointer (DMADSTENDP) for the channel.
**Micro Direct Memory Access (μDMA)**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 29:28     | DSTSIZE| RW   | -     | Destination Data Size. This field configures the destination item data size.  
Note: DSTSIZE must be the same as SRCSIZE. |
|           |        |      |       | Value Description                                |
|           |        |      |       | 0x0 Byte 8-bit data size                         |
|           |        |      |       | 0x1 Half-word 16-bit data size                   |
|           |        |      |       | 0x2 Word 32-bit data size                        |
|           |        |      |       | 0x3 Reserved                                     |
| 27:26     | SRCINC | RW   | -     | Source Address Increment. This field configures the source address increment.  
The address increment value must be equal or greater than the value of the source size (SRCSIZE). |
|           |        |      |       | Value Description                                |
|           |        |      |       | 0x0 Byte Increment by 8-bit locations            |
|           |        |      |       | 0x1 Half-word Increment by 16-bit locations      |
|           |        |      |       | 0x2 Word Increment by 32-bit locations           |
|           |        |      |       | 0x3 No increment Address remains set to the value of the Source Address End Pointer (DMASRCENDP) for the channel |
| 25:24     | SRCSIZE| RW   | -     | Source Data Size. This field configures the source item data size.  
Note: DSTSIZE must be the same as SRCSIZE. |
|           |        |      |       | Value Description                                |
|           |        |      |       | 0x0 Byte 8-bit data size                         |
|           |        |      |       | 0x1 Half-word 16-bit data size                   |
|           |        |      |       | 0x2 Word 32-bit data size                        |
|           |        |      |       | 0x3 Reserved                                     |
| 23:18     | reserved| RO   | -      | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
### Bit/Field Information

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>17:14</td>
<td>ARBSIZE</td>
<td>RW</td>
<td>-</td>
<td><strong>Arbitration Size</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field configures the number of transfers that can occur before the μDMA controller re-arbitrates. The possible arbitration rate configurations represent powers of 2 and are shown below.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
</tbody>
</table>
|           |           |      |       | 0x0 | 1 Transfer
|           |           |      |       |     | Arbitrates after each μDMA transfer |
|           |           |      |       | 0x1 | 2 Transfers
|           |           |      |       | 0x2 | 4 Transfers
|           |           |      |       | 0x3 | 8 Transfers
|           |           |      |       | 0x4 | 16 Transfers
|           |           |      |       | 0x5 | 32 Transfers
|           |           |      |       | 0x6 | 64 Transfers
|           |           |      |       | 0x7 | 128 Transfers
|           |           |      |       | 0x8 | 256 Transfers
|           |           |      |       | 0x9 | 512 Transfers
|           |           |      |       | 0xA-0xF | 1024 Transfers
|           |           |      |       |     | In this configuration, no arbitration occurs during the μDMA transfer because the maximum transfer size is 1024. |
| 13:4      | XFERSIZE  | RW   | -     | **Transfer Size (minus 1)**          |
|           |           |      |       | This field configures the total number of items to transfer. The value of this field is 1 less than the number to transfer (value 0 means transfer 1 item). The maximum value for this 10-bit field is 1023 which represents a transfer size of 1024 items. |
|           |           |      |       | The transfer size is the number of items, not the number of bytes. If the data size is 32 bits, then this value is the number of 32-bit words to transfer. |
|           |           |      |       | The μDMA controller updates this field immediately prior to entering the arbitration process, so it contains the number of outstanding items that is necessary to complete the μDMA cycle. |
| 3         | NXTUSEBURST | RW | -    | **Next Useburst**                    |
|           |           |      |       | This field controls whether the Useburst SET[n] bit is automatically set for the last transfer of a peripheral scatter-gather operation. Normally, for the last transfer, if the number of remaining items to transfer is less than the arbitration size, the μDMA controller uses single transfers to complete the transaction. If this bit is set, then the controller uses a burst transfer to complete the last transfer. |
μDMA Transfer Mode

This field configures the operating mode of the μDMA cycle. Refer to “Transfer Modes” on page 601 for a detailed explanation of transfer modes.

Because this register is in system RAM, it has no reset value. Therefore, this field should be initialized to 0 before the channel is enabled.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Stop</td>
</tr>
<tr>
<td>0x1</td>
<td>Basic</td>
</tr>
<tr>
<td>0x2</td>
<td>Auto-Request</td>
</tr>
<tr>
<td>0x3</td>
<td>Ping-Pong</td>
</tr>
<tr>
<td>0x4</td>
<td>Memory Scatter-Gather</td>
</tr>
<tr>
<td>0x5</td>
<td>Alternate Memory Scatter-Gather</td>
</tr>
<tr>
<td>0x6</td>
<td>Peripheral Scatter-Gather</td>
</tr>
<tr>
<td>0x7</td>
<td>Alternate Peripheral Scatter-Gather</td>
</tr>
</tbody>
</table>

**XFERMODE Bit Field Values.**

**Stop**
Channel is stopped or configuration data is invalid. No more transfers can occur.

**Basic**
For each trigger (whether from a peripheral or a software request), the μDMA controller performs the number of transfers specified by the ARBSIZE field.

**Auto-Request**
The initial request (software- or peripheral-initiated) is sufficient to complete the entire transfer of XFERSIZE items without any further requests.

**Ping-Pong**
This mode uses both the primary and alternate control structures for this channel. When the number of transfers specified by the XFERSIZE field have completed for the current control structure (primary or alternate), the μDMA controller switches to the other one. These switches continue until one of the control structures is not set to ping-pong mode. At that point, the μDMA controller stops. An interrupt is generated on completion of the transfers configured by each control structure. See “Ping-Pong” on page 601.

**Memory Scatter-Gather**
When using this mode, the primary control structure for the channel is configured to allow a list of operations (tasks) to be performed. The source address pointer specifies the start of a table of tasks to be copied to the alternate control structure for this channel. The XFERMODE field for the alternate control structure should be configured to 0x5 (Alternate memory scatter-gather) to perform the task. When the task completes, the μDMA switches back to the primary channel control structure, which then copies the next task to the alternate control structure. This process continues until the table of tasks is empty. The last task must have an XFERMODE value other than 0x5. Note that for continuous operation, the last task can update the primary channel control structure back to the start of the list or to another list. See “Memory Scatter-Gather” on page 602.
Alternate Memory Scatter-Gather
This value must be used in the alternate channel control data structure when the μDMA controller operates in Memory Scatter-Gather mode.

Peripheral Scatter-Gather
This value must be used in the primary channel control data structure when the μDMA controller operates in Peripheral Scatter-Gather mode. In this mode, the μDMA controller operates exactly the same as in Memory Scatter-Gather mode, except that instead of performing the number of transfers specified by the `XFERSIZE` field in the alternate control structure at one time, the μDMA controller only performs the number of transfers specified by the `ARBSIZE` field per trigger; see Basic mode for details. See “Peripheral Scatter-Gather” on page 606.

Alternate Peripheral Scatter-Gather
This value must be used in the alternate channel control data structure when the μDMA controller operates in Peripheral Scatter-Gather mode.

9.6 μDMA Register Descriptions

The register addresses given are relative to the μDMA base address of 0x400F.F000.
Register 4: DMA Status (DMASTAT), offset 0x000

The DMA Status (DMASTAT) register returns the status of the μDMA controller. You cannot read this register when the μDMA controller is in the reset state.

DMA Status (DMASTAT)

Base 0x400F.F000
Offset 0x000
Type RO, reset 0x001F.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:21</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>20:16</td>
<td>DMACHANS</td>
<td>RO</td>
<td>0x1F</td>
<td>Available μDMA Channels Minus 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field contains a value equal to the number of μDMA channels the μDMA controller is configured to use, minus one. The value of 0x1F corresponds to 32 μDMA channels.</td>
</tr>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:4</td>
<td>STATE</td>
<td>RO</td>
<td>0x0</td>
<td>Control State Machine Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field shows the current status of the control state machine. Status can be one of the following.</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0x0</td>
<td>Idle</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>Reading channel controller data.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2</td>
<td>Reading source end pointer.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x3</td>
<td>Reading destination end pointer.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x4</td>
<td>Reading source data.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x5</td>
<td>Writing destination data.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x6</td>
<td>Waiting for μDMA request to clear.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x7</td>
<td>Writing channel controller data.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x8</td>
<td>Stalled</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x9</td>
<td>Done</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xA-0xF</td>
<td>Undefined</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>MASTEN</td>
<td>RO</td>
<td>0</td>
<td>Master Enable Status</td>
</tr>
</tbody>
</table>

Value | Description            
---    |------------------------|
0     | The μDMA controller is disabled. |
1     | The μDMA controller is enabled. |
Register 5: DMA Configuration (DMACFG), offset 0x004

The DMACFG register controls the configuration of the μDMA controller.

### DMA Configuration (DMACFG)

Base 0x400F.F000
Offset 0x004
Type WO, reset -

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>WO</td>
<td>-</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>MASTEN</td>
<td>WO</td>
<td>-</td>
<td>Controller Master Enable</td>
</tr>
</tbody>
</table>

Value Description

- 0 Disables the μDMA controller.
- 1 Enables μDMA controller.
Register 6: DMA Channel Control Base Pointer (DMACTLBASE), offset 0x008

The DMACTLBASE register must be configured so that the base pointer points to a location in system memory.

The amount of system memory that must be assigned to the μDMA controller depends on the number of μDMA channels used and whether the alternate channel control data structure is used. See “Channel Configuration” on page 599 for details about the Channel Control Table. The base address must be aligned on a 1024-byte boundary. This register cannot be read when the μDMA controller is in the reset state.

### DMA Channel Control Base Pointer (DMACTLBASE)

Base 0x400F.F000  
Offset 0x008  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>ADDR</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:10 | ADDR | RW | 0x0000.00 | Channel Control Base Address  
This field contains the pointer to the base address of the channel control table. The base address must be 1024-byte aligned. |
| 9:0 | reserved | RO | 0x00 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
Register 7: DMA Alternate Channel Control Base Pointer (DMAALTBASE), offset 0x00C

The DMAALTBASE register returns the base address of the alternate channel control data. This register removes the necessity for application software to calculate the base address of the alternate channel control structures. This register cannot be read when the μDMA controller is in the reset state.

DMA Alternate Channel Control Base Pointer (DMAALTBASE)

Base 0x400F.F000
Offset 0x00C
Type RO, reset 0x0000.0200

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:0      | ADDR           | RO   | 0x0000.0200 | Alternate Channel Address Pointer  
This field provides the base address of the alternate channel control structures. |
Register 8: DMA Channel Wait-on-Request Status (DMAWAITSTAT), offset 0x010

This read-only register indicates that the μDMA channel is waiting on a request. A peripheral can hold off the μDMA from performing a single request until the peripheral is ready for a burst request to enhance the μDMA performance. The use of this feature is dependent on the design of the peripheral and is not controllable by software in any way. This register cannot be read when the μDMA controller is in the reset state.

DMA Channel Wait-on-Request Status (DMAWAITSTAT)

Base 0x400F.F000
Offset 0x010
Type RO, reset 0x03C3.CF00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WAITREQ[n]</td>
<td>RO</td>
<td>0x3C3.CF00</td>
<td>Channel [n] Wait Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>These bits provide the channel wait-on-request status. Bit 0 corresponds to channel 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 9: DMA Channel Software Request (DMASWREQ), offset 0x014

Each bit of the DMASWREQ register represents the corresponding μDMA channel. Setting a bit generates a request for the specified μDMA channel.

### DMA Channel Software Request (DMASWREQ)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>No request generated.</td>
<td>0</td>
</tr>
<tr>
<td>Generate a software request for the corresponding channel.</td>
<td>1</td>
</tr>
</tbody>
</table>

These bits are automatically cleared when the software request has been completed.
Register 10: DMA Channel Useburst Set (DMAUSEBURSTSET), offset 0x018

Each bit of the DMAUSEBURSTSET register represents the corresponding μDMA channel. Setting a bit disables the channel's single request input from generating requests, configuring the channel to only accept burst requests. Reading the register returns the status of USEBURST.

If the amount of data to transfer is a multiple of the arbitration (burst) size, the corresponding SET\[n\] bit is cleared after completing the final transfer. If there are fewer items remaining to transfer than the arbitration (burst) size, the μDMA controller automatically clears the corresponding SET\[n\] bit, allowing the remaining items to transfer using single requests. In order to resume transfers using burst requests, the corresponding bit must be set again. A bit should not be set if the corresponding peripheral does not support the burst request model.

Refer to "Request Types" on page 598 for more details about request types.

### DMA Channel Useburst Set (DMAUSEBURSTSET)

<table>
<thead>
<tr>
<th>Base 0x400F.F000</th>
<th>Offset 0x018</th>
<th>Type RW, reset 0x0000.0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Type/RW</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET[n]</td>
<td>0000.0000</td>
<td>Channel [n] Useburst Set</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>SET[n]</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Channel [n] Useburst Set</td>
</tr>
</tbody>
</table>

Value Description

- 0 μDMA channel [n] responds to single or burst requests.
- 1 μDMA channel [n] responds only to burst requests.

Bit 0 corresponds to channel 0. This bit is automatically cleared as described above. A bit can also be manually cleared by setting the corresponding CLR\[n\] bit in the DMAUSEBURSTCLR register.
Register 11: DMA Channel Useburst Clear (DMAUSEBURSTCLR), offset 0x01C

Each bit of the DMAUSEBURSTCLR register represents the corresponding µDMA channel. Setting a bit clears the corresponding SET[n] bit in the DMAUSEBURSTSET register.

DMA Channel Useburst Clear (DMAUSEBURSTCLR)
Base 0x400F.F000
Offset 0x01C
Type WO, reset -

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>CLR[n]</td>
<td>WO</td>
<td>-</td>
<td>Channel [n] Useburst Clear</td>
</tr>
</tbody>
</table>

Value Description

0  No effect.
1  Setting a bit clears the corresponding SET[n] bit in the DMAUSEBURSTSET register meaning that µDMA channel [n] responds to single and burst requests.
Register 12: DMA Channel Request Mask Set (DMAREQMASKSET), offset 0x020

Each bit of the DMAREQMASKSET register represents the corresponding μDMA channel. Setting a bit disables μDMA requests for the channel. Reading the register returns the request mask status. When a μDMA channel’s request is masked, that means the peripheral can no longer request μDMA transfers. The channel can then be used for software-initiated transfers.

### DMA Channel Request Mask Set (DMAREQMASKSET)

**Base** 0x400F.F000  
**Offset** 0x020  
**Type** RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>0000</td>
<td>31:0</td>
<td>SET[n]</td>
<td>RW</td>
<td>0000</td>
<td>Channel [n] Request Mask Set</td>
</tr>
</tbody>
</table>

- **Value Description**
  - 0: The peripheral associated with channel [n] is enabled to request μDMA transfers.
  - 1: The peripheral associated with channel [n] is not able to request μDMA transfers. Channel [n] may be used for software-initiated transfers.

Bit 0 corresponds to channel 0. A bit can only be cleared by setting the corresponding CLR[n] bit in the DMAREQMASKCLR register.
Register 13: DMA Channel Request Mask Clear (DMAREQMASKCLR), offset 0x024

Each bit of the DMAREQMASKCLR register represents the corresponding μDMA channel. Setting a bit clears the corresponding SET[n] bit in the DMAREQMASKSET register.

### DMA Channel Request Mask Clear (DMAREQMASKCLR)

Base 0x400F.F000  
Offset 0x024  
Type WO, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>CLR[n]</td>
<td>WO</td>
<td>-</td>
<td>Channel [n] Request Mask Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 14: DMA Channel Enable Set (DMAENASET), offset 0x028

Each bit of the DMAENASET register represents the corresponding µDMA channel. Setting a bit enables the corresponding µDMA channel. Reading the register returns the enable status of the channels. If a channel is enabled but the request mask is set (DMAREQMASKSET), then the channel can be used for software-initiated transfers.

### DMA Channel Enable Set (DMAENASET)

- **Base**: 0x400F.F000
- **Offset**: 0x028
- **Type**: RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>SET[n]</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Channel [n] Enable Set</td>
</tr>
</tbody>
</table>

Value Description

- 0  µDMA Channel [n] is disabled.
- 1  µDMA Channel [n] is enabled.

Bit 0 corresponds to channel 0. A bit can only be cleared by setting the corresponding CLR[n] bit in the DMAENACLRL register or when the end of a µDMA transfer occurs.
Register 15: DMA Channel Enable Clear (DMAENACLR), offset 0x02C

Each bit of the DMAENACLR register represents the corresponding µDMA channel. Setting a bit clears the corresponding SET[n] bit in the DMAENASET register.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear Channel [n] Enable Clear</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Value</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No effect.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Setting a bit clears the corresponding SET[n] bit in the DMAENASET register meaning that channel [n] is disabled for µDMA transfers.</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** The controller disables a channel when it completes the µDMA cycle.

### DMA Channel Enable Clear (DMAENACLR)

Base 0x400F.F000  
Offset 0x02C  
Type WO, reset -

<table>
<thead>
<tr>
<th>CLR[n]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>CLR[n]</td>
<td>WO</td>
<td>-</td>
<td>Clear Channel [n] Enable Clear</td>
</tr>
</tbody>
</table>

- **Value Description**
  - 0: No effect.
  - 1: Setting a bit clears the corresponding SET[n] bit in the DMAENASET register meaning that channel [n] is disabled for µDMA transfers.

**Note:** The controller disables a channel when it completes the µDMA cycle.
Register 16: DMA Channel Primary Alternate Set (DMAALTSET), offset 0x030

Each bit of the DMAALTSET register represents the corresponding µDMA channel. Setting a bit configures the µDMA channel to use the alternate control data structure. Reading the register returns the status of which control data structure is in use for the corresponding µDMA channel.

**Description**

- **Bit 0 corresponds to channel 0. A bit can only be cleared by setting the corresponding CLR[n] bit in the DMAALTCLR register.**

**Note:** For Ping-Pong and Scatter-Gather cycle types, the µDMA controller automatically sets these bits to select the alternate channel control data structure.
Register 17: DMA Channel Primary Alternate Clear (DMAALTCLR), offset 0x034

Each bit of the DMAALTCLR register represents the corresponding μDMA channel. Setting a bit clears the corresponding SET[n] bit in the DMAALTSET register.

### DMA Channel Primary Alternate Clear (DMAALTCLR)

- **Base**: 0x400F.F000
- **Offset**: 0x034
- **Type**: WO, reset -1

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>CLR[n]</td>
<td>WO</td>
<td>-</td>
<td>Channel [n] Alternate Clear</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No effect.</td>
</tr>
<tr>
<td>1</td>
<td>Setting a bit clears the corresponding SET[n] bit in the DMAALTSET register meaning that channel [n] is using the primary control structure.</td>
</tr>
</tbody>
</table>

**Note:** For Ping-Pong and Scatter-Gather cycle types, the μDMA controller automatically sets these bits to select the alternate channel control data structure.
Register 18: DMA Channel Priority Set (DMAPRIOSSET), offset 0x038

Each bit of the DMAPRIOSSET register represents the corresponding µDMA channel. Setting a bit configures the µDMA channel to have a high priority level. Reading the register returns the status of the channel priority mask.

DMA Channel Priority Set (DMAPRIOSSET)
Base 0x400F.F000
Offset 0x038
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>SET[n]</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Channel [n] Priority Set</td>
</tr>
</tbody>
</table>

Value Description
0   µDMA channel [n] is using the default priority level.
1   µDMA channel [n] is using a high priority level.

Bit 0 corresponds to channel 0. A bit can only be cleared by setting the corresponding CLR[n] bit in the DMAPRIOCLR register.
Register 19: DMA Channel Priority Clear (DMAPRIOCLR), offset 0x03C

Each bit of the DMAPRIOCLR register represents the corresponding µDMA channel. Setting a bit clears the corresponding SET[n] bit in the DMAPRIOSET register.

**DMA Channel Priority Clear (DMAPRIOCLR)**

Base 0x400F.F000
Offset 0x03C
Type WO, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>CLR[n]</td>
<td>WO</td>
<td>-</td>
<td>Channel [n] Priority Clear</td>
</tr>
</tbody>
</table>

Value Description

0 No effect.
1 Setting a bit clears the corresponding SET[n] bit in the DMAPRIOSET register meaning that channel [n] is using the default priority level.
Register 20: DMA Bus Error Clear (DMAERRCLR), offset 0x04C

The DMAERRCLR register is used to read and clear the µDMA bus error status. The error status is set if the µDMA controller encountered a bus error while performing a transfer. If a bus error occurs on a channel, that channel is automatically disabled by the µDMA controller. The other channels are unaffected.

**DMA Bus Error Clear (DMAERRCLR)**

Base 0x400F.F000
Offset 0x04C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>ERRCLR</td>
<td>RW1C</td>
<td>0</td>
<td>µDMA Bus Error Status</td>
</tr>
</tbody>
</table>

  - Value Description
    - 0  No bus error is pending.
    - 1  A bus error is pending.

This bit is cleared by writing a 1 to it.
Register 21: DMA Channel Assignment (DMACHASGN), offset 0x500

Each bit of the DMACHASGN register represents the corresponding µDMA channel. Setting a bit selects the secondary channel assignment as specified in Table 9-1 on page 597.

**Note:** This register is provided to support legacy software. New software should use the DMACHMAPn registers. If a bit is clear in this register, the corresponding field in the DMACHMAPn registers is configured to 0x0. If a bit is set in this register, the corresponding field is configured to 0x1. If this register is read, a bit reads as 0 if the corresponding DMACHMAPn register field value is equal to 0, otherwise it reads as 1 if the corresponding DMACHMAPn register field value is not equal to 0.

### DMA Channel Assignment (DMACHASGN)

Base 0x400F.F000
Offset 0x500
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0 CHASGN[n]</td>
<td>RW</td>
<td>-</td>
<td>Channel [n] Assignment Select</td>
</tr>
</tbody>
</table>

Value Description

- 0 Use the primary channel assignment.
- 1 Use the secondary channel assignment.
Register 22: DMA Channel Interrupt Status (DMACHIS), offset 0x504

Each bit of the DMACHIS register represents the corresponding μDMA channel. A bit is set when that μDMA channel causes a completion interrupt. The bits are cleared by a writing a 1.

**Note:** When transfers are performed from a FIFO of the UART or SSI using the μDMA, and any interrupt is generated from the UART or SSI, the module’s status bit in the DMACHIS register must be checked at the end of the interrupt service routine. If the status bit is set, clear the interrupt by writing a 1 to it.

**DMA Channel Interrupt Status (DMACHIS)**

Base 0x400F.F000
Offset 0x504
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>CHIS[n]</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>Channel [n] Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value  Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to it.</td>
</tr>
</tbody>
</table>
Register 23: DMA Channel Map Select 0 (DMACHMAP0), offset 0x510

Each 4-bit field of the DMACHMAP0 register configures the μDMA channel assignment as specified in Table 9-1 on page 597.

**Note:** To support legacy software which uses the DMA Channel Assignment (DMACHASGN) register, a value of 0x0 is equivalent to a DMACHASGN bit being clear, and a value of 0x1 is equivalent to a DMACHASGN bit being set.

DMA Channel Map Select 0 (DMACHMAP0)
Base 0x400F.F000
Offset 0x510
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Channel 0</th>
<th>Channel 1</th>
<th>Channel 2</th>
<th>Channel 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit/Field | Name  | Type | Reset | Description
---|-------|------|-------|----------------------------------
31:28 | CH7SEL | RW   | 0x00  | μDMA Channel 7 Source Select
|       |       |      |       | See Table 9-1 on page 597 for channel assignments.
27:24 | CH6SEL | RW   | 0x00  | μDMA Channel 6 Source Select
|       |       |      |       | See Table 9-1 on page 597 for channel assignments.
23:20 | CH5SEL | RW   | 0x00  | μDMA Channel 5 Source Select
|       |       |      |       | See Table 9-1 on page 597 for channel assignments.
19:16 | CH4SEL | RW   | 0x00  | μDMA Channel 4 Source Select
|       |       |      |       | See Table 9-1 on page 597 for channel assignments.
15:12 | CH3SEL | RW   | 0x00  | μDMA Channel 3 Source Select
|       |       |      |       | See Table 9-1 on page 597 for channel assignments.
11:8 | CH2SEL | RW   | 0x00  | μDMA Channel 2 Source Select
|       |       |      |       | See Table 9-1 on page 597 for channel assignments.
7:4  | CH1SEL | RW   | 0x00  | μDMA Channel 1 Source Select
|       |       |      |       | See Table 9-1 on page 597 for channel assignments.
3:0  | CH0SEL | RW   | 0x00  | μDMA Channel 0 Source Select
|       |       |      |       | See Table 9-1 on page 597 for channel assignments.
Register 24: DMA Channel Map Select 1 (DMACHMAP1), offset 0x514

Each 4-bit field of the DMACHMAP1 register configures the μDMA channel assignment as specified in Table 9-1 on page 597.

**Note:** To support legacy software which uses the DMA Channel Assignment (DMACHASGN) register, a value of 0x0 is equivalent to a DMACHASGN bit being clear, and a value of 0x1 is equivalent to a DMACHASGN bit being set.

### DMA Channel Map Select 1 (DMACHMAP1)

Base 0x400F.F000
Offset 0x514
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>CH15SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 15 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>27:24</td>
<td>CH14SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 14 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>23:20</td>
<td>CH13SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 13 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>19:16</td>
<td>CH12SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 12 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>15:12</td>
<td>CH11SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 11 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>11:8</td>
<td>CH10SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 10 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>7:4</td>
<td>CH9SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 9 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>3:0</td>
<td>CH8SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 8 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
Register 25: DMA Channel Map Select 2 (DMACHMAP2), offset 0x518

Each 4-bit field of the DMACHMAP2 register configures the μDMA channel assignment as specified in Table 9-1 on page 597.

**Note:** To support legacy software which uses the DMA Channel Assignment (DMACHASGN) register, a value of 0x0 is equivalent to a DMACHASGN bit being clear, and a value of 0x1 is equivalent to a DMACHASGN bit being set.

### DMA Channel Map Select 2 (DMACHMAP2)

Base 0x400F.F000
Offset 0x518
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>CH23SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 23 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>27:24</td>
<td>CH22SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 22 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>23:20</td>
<td>CH21SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 21 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>19:16</td>
<td>CH20SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 20 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>15:12</td>
<td>CH19SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 19 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>11:8</td>
<td>CH18SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 18 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>7:4</td>
<td>CH17SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 17 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>3:0</td>
<td>CH16SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 16 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
</tbody>
</table>
Register 26: DMA Channel Map Select 3 (DMACHMAP3), offset 0x51C

Each 4-bit field of the DMACHMAP3 register configures the μDMA channel assignment as specified in Table 9-1 on page 597.

**Note:** To support legacy software which uses the DMA Channel Assignment (DMACHASGN) register, a value of 0x0 is equivalent to a DMACHASGN bit being clear, and a value of 0x1 is equivalent to a DMACHASGN bit being set.

### DMA Channel Map Select 3 (DMACHMAP3)

<table>
<thead>
<tr>
<th>Base 0x400F.F000</th>
<th>Offset 0x51C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RW, reset 0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CH31SEL</th>
<th>CH30SEL</th>
<th>CH29SEL</th>
<th>CH28SEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CH27SEL</th>
<th>CH26SEL</th>
<th>CH25SEL</th>
<th>CH24SEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>CH31SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 31 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>27:24</td>
<td>CH30SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 30 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>23:20</td>
<td>CH29SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 29 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>19:16</td>
<td>CH28SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 28 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>15:12</td>
<td>CH27SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 27 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>11:8</td>
<td>CH26SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 26 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>7:4</td>
<td>CH25SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 25 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
<tr>
<td>3:0</td>
<td>CH24SEL</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Channel 24 Source Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 9-1 on page 597 for channel assignments.</td>
</tr>
</tbody>
</table>
Register 27: DMA Peripheral Identification 0 (DMAPeriphID0), offset 0xFE0

The DMAPeriphIDn registers are hard-coded, and the fields within the registers determine the reset values.

DMA Peripheral Identification 0 (DMAPeriphID0)
Base 0x400F.F000
Offset 0xFE0
Type RO, reset 0x0000.0030

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID0</td>
<td>RO</td>
<td>0x30</td>
<td>μDMA Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 28: DMA Peripheral Identification 1 (DMAPeriphID1), offset 0xFE4

The DMAPeriphIDn registers are hard-coded, and the fields within the registers determine the reset values.

### DMA Peripheral Identification 1 (DMAPeriphID1)

- **Base**: 0x400F.F000
- **Offset**: 0xFE4
- **Type**: RO, reset 0x0000.00B2

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID1</td>
<td>RO</td>
<td>0xB2</td>
<td>μDMA Peripheral ID Register [15:8] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 29: DMA Peripheral Identification 2 (DMAPeriphID2), offset 0xFE8

The DMAPeriphIDn registers are hard-coded, and the fields within the registers determine the reset values.

### DMA Peripheral Identification 2 (DMAPeriphID2)

Base 0x400F.F000  
Offset 0xFE8  
Type RO, reset 0x0000.000B

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID2</td>
<td>RO</td>
<td>0x0B</td>
<td>μDMA Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
### Register 30: DMA Peripheral Identification 3 (DMAPeriphID3), offset 0xFEC

The **DMAPeriphIDn** registers are hard-coded and the fields within the registers determine the reset values.

#### DMA Peripheral Identification 3 (DMAPeriphID3)
- **Base**: 0x400F.F000
- **Offset**: 0xFEC
- **Type**: RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID3</td>
<td>RO</td>
<td>0x00</td>
<td>μDMA Peripheral ID Register [31:24] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 31: DMA Peripheral Identification 4 (DMAPeriphID4), offset 0xFD0

The DMAPeriphIDn registers are hard-coded, and the fields within the registers determine the reset values.

DMA Peripheral Identification 4 (DMAPeriphID4)
Base 0x400F.F000
Offset 0xFD0
Type RO, reset 0x0000.0004

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID4</td>
<td>RO</td>
<td>0x04</td>
<td>μDMA Peripheral ID Register Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 32: DMA PrimeCell Identification 0 (DMAPCellID0), offset 0xFF0

The DMAPCellIDn registers are hard-coded, and the fields within the registers determine the reset values.

DMA PrimeCell Identification 0 (DMAPCellID0)
Base 0x400F.F000
Offset 0xFF0
Type RO, reset 0x0000.000D

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID0</td>
<td>RO</td>
<td>0x0D</td>
<td>μDMA PrimeCell ID Register [7:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 33: DMA PrimeCell Identification 1 (DMAPCellID1), offset 0xFF4

The DMAPCellIDn registers are hard-coded, and the fields within the registers determine the reset values.

DMA PrimeCell Identification 1 (DMAPCellID1)

Base 0x400F.F000
Offset 0xFF4
Type RO, reset 0x0000.00F0

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID1</td>
<td>RO</td>
<td>0xF0</td>
<td>μDMA PrimeCell ID Register [15:8] Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 34: DMA PrimeCell Identification 2 (DMAPCellID2), offset 0xFF8

The **DMAPCellIDn** registers are hard-coded, and the fields within the registers determine the reset values.

**DMA PrimeCell Identification 2 (DMAPCellID2)**

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x400F.F000</td>
<td>0xFF8</td>
<td>RO</td>
<td>0x0000.0005</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID2</td>
<td>RO</td>
<td>0x05</td>
<td>μDMA PrimeCell ID Register [23:16] Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 35: DMA PrimeCell Identification 3 (DMAPCellID3), offset 0xFFC

The DMAPCellIDn registers are hard-coded, and the fields within the registers determine the reset values.

DMA PrimeCell Identification 3 (DMAPCellID3)
Base 0x400F.F000
Offset 0xFFC
Type RO, reset 0x0000.00B1

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID3</td>
<td>RO</td>
<td>0xB1</td>
<td>μDMA PrimeCell ID Register [31:24] Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
General-Purpose Input/Outputs (GPIOs)

The GPIO module is composed of ten physical GPIO blocks, each corresponding to an individual GPIO port (Port A, Port B, Port C, Port D, Port E, Port F, Port G, Port H, Port J, Port K, Port L). The GPIO module supports up to 69 programmable input/output pins, depending on the peripherals being used.

The GPIO module has the following features:

- Up to 69 GPIOs, depending on configuration
- Highly flexible pin muxing allows use as GPIO or one of several peripheral functions
- 5-V-tolerant in input configuration
- Fast toggle capable of a change every clock cycle for ports on AHB, every two clock cycles for ports on APB
- Programmable control for GPIO interrupts
  - Interrupt generation masking
  - Edge-triggered on rising, falling, or both
  - Level-sensitive on High or Low values
- Bit masking in both read and write operations through address lines
- Can be used to initiate an ADC sample sequence or a μDMA transfer
- Pin state can be retained during Hibernation mode
- Pins configured as digital inputs are Schmitt-triggered
- Programmable control for GPIO pad configuration
  - Weak pull-up or pull-down resistors
  - 2-mA, 4-mA, and 8-mA pad drive for digital communication; up to four pads can sink 18-mA for high-current applications
  - Slew rate control for 8-mA pad drive
  - Open drain enables
  - Digital input enables

Signal Description

GPIO signals have alternate hardware functions. The following table lists the GPIO pins and their analog and digital alternate functions. All GPIO signals are 5-V tolerant when configured as inputs except for PJ0, PJ1, PB0 and PB1, which are limited to 3.6 V. The digital alternate hardware functions are enabled by setting the appropriate bit in the GPIO Alternate Function Select (GPIOAFSEL) and GPIODEN registers and configuring the PMCx bit field in the GPIO Port Control (GPIOPCTL) register to the numeric encoding shown in the table below. Analog signals in the table below are
also 5-V tolerant and are configured by clearing the **DEN** bit in the **GPIO Digital Enable (GPIODEN)** register. The **AINx** analog signals have internal circuitry to protect them from voltages over **V_{DD}** (up to the maximum specified in Table 24-1 on page 1395), but analog performance specifications are only guaranteed if the input signal swing at the I/O pad is kept inside the range 0 V < **V_{IN}** < **V_{DD}**. Note that each pin must be programmed individually; no type of grouping is implied by the columns in the table. Table entries that are shaded gray are the default values for the corresponding GPIO pin.

---

**Important:** The table below shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL**=0, **GPIODEN**=0, **GPIOPDR**=0, **GPIOPUR**=0, and **GPIOPCTL**=0). Special consideration pins may be programmed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (**POR**) or asserting **RST** returns these GPIO to their original special consideration state.

### Table 10-1. GPIO Pins With Special Considerations

<table>
<thead>
<tr>
<th>GPIO Pins</th>
<th>Default Reset State</th>
<th>GPIOAFSEL</th>
<th>GPIODEN</th>
<th>GPIOPDR</th>
<th>GPIOPUR</th>
<th>GPIOPCTL</th>
<th>GPIOCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[1:0]</td>
<td>UART0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x1</td>
<td>1</td>
</tr>
<tr>
<td>PA[5:2]</td>
<td>SSI0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x2</td>
<td>1</td>
</tr>
<tr>
<td>PB[3:2]</td>
<td>I2C0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x3</td>
<td>1</td>
</tr>
<tr>
<td>PC[3:0]</td>
<td>JTAG/SWD</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0x1</td>
<td>0</td>
</tr>
<tr>
<td>PD[7]</td>
<td>GPIO^a</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
<tr>
<td>PF[0]</td>
<td>GPIO^a</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
</tbody>
</table>

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the **GPIOLOCK** register and uncommitting it by setting the **GPIOCR** register.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware signals including the GPIO pins that can function as JTAG/SWD signals and the **NMI** signal. The commit control process must be followed for these pins, even if they are programmed as alternate functions other than JTAG/SWD or NMI; see "Commit Control" on page 667.

### Table 10-2. GPIO Pins and Alternate Functions (100LQFP)

<table>
<thead>
<tr>
<th>IO</th>
<th>Pin</th>
<th>Analog Function</th>
<th>Digital Function (GPIOPCTL PMCx Bit Field Encoding)^a</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>1  2  3  4  5  6  7  8  9  14 15</td>
</tr>
<tr>
<td>PA0</td>
<td>26</td>
<td>U0Rx</td>
<td>-   -   -   -   -   -   -     CAN1Rx     -   -   -</td>
</tr>
<tr>
<td>PA1</td>
<td>27</td>
<td>U0Tx</td>
<td>-   -   -   -   -   -   -     CAN1Tx     -   -   -</td>
</tr>
<tr>
<td>PA2</td>
<td>28</td>
<td>SSI0Clk</td>
<td>-   -   -   -   -   -   -     CAN1Rx     -   -   -</td>
</tr>
<tr>
<td>PA3</td>
<td>29</td>
<td>SSI0Pax</td>
<td>-   -   -   -   -   -   -     CAN1Tx     -   -   -</td>
</tr>
<tr>
<td>PA4</td>
<td>30</td>
<td>SSI0Rx</td>
<td>-   -   -   -   -   -   -     CAN1Rx     -   -   -</td>
</tr>
<tr>
<td>PA5</td>
<td>31</td>
<td>SSI0Txx</td>
<td>-   -   -   -   -   -   -     CAN1Tx     -   -   -</td>
</tr>
<tr>
<td>PA6</td>
<td>34</td>
<td>I2C1SCL</td>
<td>-   -   -   -   -   -   -     M1PWM2     -   -   -</td>
</tr>
<tr>
<td>PA7</td>
<td>35</td>
<td>I2C1SDA</td>
<td>-   -   -   -   -   -   -     M1PWM3     -   -   -</td>
</tr>
<tr>
<td>PB0</td>
<td>70</td>
<td>USB0ID</td>
<td>-   -   -   -   -   -   -     T2CCPO     -   -   -</td>
</tr>
<tr>
<td>PB1</td>
<td>71</td>
<td>USB0VBUS</td>
<td>-   -   -   -   -   -   -     T2CCPO     -   -   -</td>
</tr>
<tr>
<td>IO</td>
<td>Pin</td>
<td>Analog Function</td>
<td>Digital Function (GPIOCTL PMCx Bit Field Encoding)</td>
</tr>
<tr>
<td>----</td>
<td>-----</td>
<td>----------------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 2 3 4 5 6 7 8 9 14 15</td>
</tr>
<tr>
<td>PB2</td>
<td>72</td>
<td>-</td>
<td>I2C0SCL</td>
</tr>
<tr>
<td>PB3</td>
<td>73</td>
<td>-</td>
<td>I2C0SDA</td>
</tr>
<tr>
<td>PB4</td>
<td>92</td>
<td>AIN10</td>
<td>SS12C1k</td>
</tr>
<tr>
<td>PB5</td>
<td>91</td>
<td>AIN11</td>
<td>SS12FSx</td>
</tr>
<tr>
<td>PC0</td>
<td>85</td>
<td>TCK SWCLK</td>
<td>-</td>
</tr>
<tr>
<td>PC1</td>
<td>84</td>
<td>TMS SWDIO</td>
<td>-</td>
</tr>
<tr>
<td>PC2</td>
<td>83</td>
<td>TD1</td>
<td>-</td>
</tr>
<tr>
<td>PC3</td>
<td>82</td>
<td>TDO SWO</td>
<td>-</td>
</tr>
<tr>
<td>PC4</td>
<td>25</td>
<td>Cl-</td>
<td>U4Rx</td>
</tr>
<tr>
<td>PC5</td>
<td>24</td>
<td>Cl+</td>
<td>U4Tx</td>
</tr>
<tr>
<td>PC6</td>
<td>23</td>
<td>CO+</td>
<td>U3Rx</td>
</tr>
<tr>
<td>PC7</td>
<td>22</td>
<td>CO-</td>
<td>U3Tx</td>
</tr>
<tr>
<td>PB0</td>
<td>1</td>
<td>AIN15</td>
<td>SS13C1k</td>
</tr>
<tr>
<td>PB1</td>
<td>2</td>
<td>AIN14</td>
<td>SS13FSs</td>
</tr>
<tr>
<td>PC2</td>
<td>3</td>
<td>AIN13</td>
<td>SS13Rx</td>
</tr>
<tr>
<td>PC3</td>
<td>4</td>
<td>AIN12</td>
<td>SS13Tx</td>
</tr>
<tr>
<td>PC4</td>
<td>97</td>
<td>AIN7</td>
<td>U6Rx</td>
</tr>
<tr>
<td>PC5</td>
<td>98</td>
<td>AIN6</td>
<td>U6Tx</td>
</tr>
<tr>
<td>PB6</td>
<td>99</td>
<td>AIN5</td>
<td>U2Rx</td>
</tr>
<tr>
<td>PB7</td>
<td>100</td>
<td>AIN4</td>
<td>U2Tx</td>
</tr>
<tr>
<td>PB0</td>
<td>15</td>
<td>AIN3</td>
<td>U7Rx</td>
</tr>
<tr>
<td>PB1</td>
<td>14</td>
<td>AIN2</td>
<td>U7Tx</td>
</tr>
<tr>
<td>PB2</td>
<td>13</td>
<td>AIN1</td>
<td>-</td>
</tr>
<tr>
<td>PB3</td>
<td>12</td>
<td>AIN0</td>
<td>-</td>
</tr>
<tr>
<td>PB4</td>
<td>95</td>
<td>AIN9</td>
<td>U5Rx</td>
</tr>
<tr>
<td>PB5</td>
<td>96</td>
<td>AIN8</td>
<td>U5Tx</td>
</tr>
<tr>
<td>PB6</td>
<td>89</td>
<td>AIN21</td>
<td>-</td>
</tr>
<tr>
<td>PB7</td>
<td>90</td>
<td>AIN20</td>
<td>U1RI</td>
</tr>
<tr>
<td>PF0</td>
<td>40</td>
<td>U1RTS</td>
<td>SS11Rx</td>
</tr>
<tr>
<td>PF1</td>
<td>41</td>
<td>U1CTS</td>
<td>SS11Tx</td>
</tr>
<tr>
<td>PF2</td>
<td>42</td>
<td>U1DDC</td>
<td>SS11C1k</td>
</tr>
<tr>
<td>PF3</td>
<td>43</td>
<td>U1DDR</td>
<td>SS11FSs</td>
</tr>
<tr>
<td>PF4</td>
<td>39</td>
<td>U1DTR</td>
<td>-</td>
</tr>
<tr>
<td>PF5</td>
<td>37</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PF6</td>
<td>36</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Table 10-2. GPIO Pins and Alternate Functions (100LQFP) (continued)

<table>
<thead>
<tr>
<th>IO</th>
<th>Pin</th>
<th>Analog Function</th>
<th>Digital Function (GPIOCCTL PMCx Bit Field Encoding)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF7</td>
<td>58</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG0</td>
<td>62</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG1</td>
<td>61</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG2</td>
<td>60</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG3</td>
<td>59</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG4</td>
<td>74</td>
<td>-</td>
<td>U2Rx</td>
</tr>
<tr>
<td>PG5</td>
<td>75</td>
<td>-</td>
<td>U2Tx</td>
</tr>
<tr>
<td>PG6</td>
<td>87</td>
<td>C2+</td>
<td>-</td>
</tr>
<tr>
<td>PG7</td>
<td>88</td>
<td>C2-</td>
<td>-</td>
</tr>
<tr>
<td>PH0</td>
<td>16</td>
<td>AIN16</td>
<td>-</td>
</tr>
<tr>
<td>PH1</td>
<td>17</td>
<td>AIN17</td>
<td>-</td>
</tr>
<tr>
<td>PH2</td>
<td>18</td>
<td>AIN18</td>
<td>-</td>
</tr>
<tr>
<td>PH3</td>
<td>19</td>
<td>AIN19</td>
<td>-</td>
</tr>
<tr>
<td>PH4</td>
<td>79</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PH5</td>
<td>78</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PH6</td>
<td>77</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PH7</td>
<td>76</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PJ0</td>
<td>68</td>
<td>USB0DM</td>
<td>U4Rx</td>
</tr>
<tr>
<td>PJ1</td>
<td>69</td>
<td>USB0DP</td>
<td>U4Tx</td>
</tr>
<tr>
<td>PJ2</td>
<td>11</td>
<td>-</td>
<td>U3Rx</td>
</tr>
<tr>
<td>PK0</td>
<td>49</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PK1</td>
<td>48</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PK2</td>
<td>47</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PK3</td>
<td>46</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

a. The digital signals that are shaded gray are the power-on default values for the corresponding GPIO pin. Encodings 10-13 are not used on this device.

10.2 Functional Description

Each GPIO port is a separate hardware instantiation of the same physical block (see Figure 10-1 on page 663 and Figure 10-2 on page 664). The TM4C123GH6PZ microcontroller contains ten ports and thus ten of these physical GPIO blocks. Note that not all pins are implemented on every block. Some GPIO pins can function as I/O signals for the on-chip peripheral modules. For information on which GPIO pins are used for alternate hardware functions, refer to Table 23-5 on page 1386.
Figure 10-1. Digital I/O Pads
10.2.1 Data Control

The data control registers allow software to configure the operational modes of the GPIOs. The data direction register configures the GPIO as an input or an output while the data register either captures incoming data or drives it out to the pads.

Caution – It is possible to create a software sequence that prevents the debugger from connecting to the TM4C123GH6PZ microcontroller. If the program code loaded into flash immediately changes the JTAG pins to their GPIO functionality, the debugger may not have enough time to connect and halt the controller before the JTAG pin functionality switches. As a result, the debugger may be locked out of the part. This issue can be avoided with a software routine that restores JTAG functionality based on an external or software trigger. In the case that the software routine is not implemented and the device is locked out of the part, this issue can be solved by using the TM4C123GH6PZ Flash Programmer "Unlock" feature. Please refer to LMFLASHPROGRAMMER on the TI web for more information.

10.2.1.1 Data Direction Operation

The GPIO Direction (GPIODIR) register (see page 675) is used to configure each individual pin as an input or output. When the data direction bit is cleared, the GPIO is configured as an input, and the corresponding data register bit captures and stores the value on the GPIO port. When the data
direction bit is set, the GPIO is configured as an output, and the corresponding data register bit is driven out on the GPIO port.

10.2.1.2 Data Register Operation

To aid in the efficiency of software, the GPIO ports allow for the modification of individual bits in the GPIO Data (GPIODATA) register (see page 673) by using bits [9:2] of the address bus as a mask. In this manner, software drivers can modify individual GPIO pins in a single instruction without affecting the state of the other pins. This method is more efficient than the conventional method of performing a read-modify-write operation to set or clear an individual GPIO pin. To implement this feature, the GPIODATA register covers 256 locations in the memory map.

During a write, if the address bit associated with that data bit is set, the value of the GPIODATA register is altered. If the address bit is cleared, the data bit is left unchanged. For example, writing a value of 0xEB to the address GPIODATA + 0x098 has the results shown in Figure 10-3, where u indicates that data is unchanged by the write. This example demonstrates how GPIODATA bits 5, 2, and 1 are written.

![Figure 10-3. GPIODATA Write Example](image)

During a read, if the address bit associated with the data bit is set, the value is read. If the address bit associated with the data bit is cleared, the data bit is read as a zero, regardless of its actual value. For example, reading address GPIODATA + 0x0C4 yields as shown in Figure 10-4. This example shows how to read GPIODATA bits 5, 4, and 0.

![Figure 10-4. GPIODATA Read Example](image)

10.2.2 Interrupt Control

The interrupt capabilities of each GPIO port are controlled by a set of seven registers. These registers are used to select the source of the interrupt, its polarity, and the edge properties. When one or more GPIO inputs cause an interrupt, a single interrupt output is sent to the interrupt controller for the entire GPIO port. For edge-triggered interrupts, software must clear the interrupt to enable any
further interrupts. For a level-sensitive interrupt, the external source must hold the level constant for the interrupt to be recognized by the controller.

Three registers define the edge or sense that causes interrupts:

- **GPIO Interrupt Sense (GPIOIS)** register (see page 676)
- **GPIO Interrupt Both Edges (GPIOIBE)** register (see page 677)
- **GPIO Interrupt Event (GPIOIEV)** register (see page 679)

Interrupts are enabled/disabled via the **GPIO Interrupt Mask (GPIOIM)** register (see page 680).

When an interrupt condition occurs, the state of the interrupt signal can be viewed in two locations: the **GPIO Raw Interrupt Status (GPIORIS)** and **GPIO Masked Interrupt Status (GPIOMIS)** registers (see page 681 and page 682). As the name implies, the **GPIOMIS** register only shows interrupt conditions that are allowed to be passed to the interrupt controller. The **GPIORIS** register indicates that a GPIO pin meets the conditions for an interrupt, but has not necessarily been sent to the interrupt controller.

For a GPIO level-detect interrupt, the interrupt signal generating the interrupt must be held until serviced. Once the input signal deasserts from the interrupt generating logical sense, the corresponding **RIS** bit in the **GPIORIS** register clears. For a GPIO edge-detect interrupt, the **RIS** bit in the **GPIORIS** register is cleared by writing a “1” to the corresponding bit in the **GPIO Interrupt Clear (GPIOICR)** register (see page 683). The corresponding **GPIOMIS** bit reflects the masked value of the **RIS** bit.

When programming the interrupt control registers (**GPIOIS, GPIOIBE, or GPIOIEV**), the interrupts should be masked (**GPIOIM** cleared). Writing any value to an interrupt control register can generate a spurious interrupt if the corresponding bits are enabled.

### 10.2.2.1 ADC Trigger Source

Any GPIO pin can be configured to be an external trigger for the ADC using the **GPIO ADC Control (GPIOADCCTL)** register. If any GPIO is configured as a non-masked interrupt pin (the appropriate bit of **GPIOIM** is set), and an interrupt for that port is generated, a trigger signal is sent to the ADC. If the **ADC Event Multiplexer Select (ADCEMUX)** register is configured to use the external trigger, an ADC conversion is initiated. See page 847.

Note that if the Port B **GPIOADCCTL** register is cleared, PB4 can still be used as an external trigger for the ADC. This is a legacy mode which allows code written for previous devices to operate on this microcontroller.

### 10.2.2.2 μDMA Trigger Source

Any GPIO pin can be configured to be an external trigger for the μDMA using the **GPIO DMA Control (GPIODMACCTL)** register. If any GPIO is configured as a non-masked interrupt pin (the appropriate bit of **GPIOIM** is set), an interrupt for that port is generated and an external trigger signal is sent to the μDMA. If the μDMA is configured to start a transfer based on the GPIO signal, a transfer is initiated.

### 10.2.3 Mode Control

The GPIO pins can be controlled by either software or hardware. Software control is the default for most signals and corresponds to the GPIO mode, where the **GPIODATA** register is used to read or write the corresponding pins. When hardware control is enabled via the **GPIO Alternate Function**
Select (GPIOAFSEL) register (see page 684), the pin state is controlled by its alternate function (that is, the peripheral).

Further pin muxing options are provided through the GPIO Port Control (GPIOPCTL) register which selects one of several peripheral functions for each GPIO. For information on the configuration options, refer to Table 23-5 on page 1386.

**Note:** If any pin is to be used as an ADC input, the appropriate bit in the GPIOAMSEL register must be set to disable the analog isolation circuit.

### 10.2.4 Commit Control

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is provided for the GPIO pins that can be used as the four JTAG/SWD pins and the NMI pin (see “Signal Tables” on page 1354 for pin numbers). Writes to protected bits of the GPIO Alternate Function Select (GPIOAFSEL) register (see page 684), GPIO Pull Up Select (GPIOPUR) register (see page 690), GPIO Pull-Down Select (GPIOPDR) register (see page 692), and GPIO Digital Enable (GPIODEN) register (see page 695) are not committed to storage unless the GPIO Lock (GPIOLOCK) register (see page 697) has been unlocked and the appropriate bits of the GPIO Commit (GPIOCR) register (see page 698) have been set.

### 10.2.5 Pad Control

The pad control registers allow software to configure the GPIO pads based on the application requirements. The pad control registers include the GPIO2R, GPIO4R, GPIO8R, GPIO4R, GPIOUPR, GPIOPD, GPIO2R, and GPIODEN registers. These registers control drive strength, open-drain configuration, pull-up and pull-down resistors, slew-rate control and digital input enable for each GPIO. If 5 V is applied to a GPIO configured as an open-drain output, the output voltage will depend on the strength of your pull-up resistor. The GPIO pad is not electrically configured to output 5 V.

### 10.2.6 Identification

The identification registers configured at reset allow software to detect and identify the module as a GPIO block. The identification registers include the GPIOPeriphID0-GPIOPeriphID7 registers as well as the GPIOPCellID0-GPIOPCellID3 registers.

### 10.3 Initialization and Configuration

The GPIO modules may be accessed via two different memory apertures. The legacy aperture, the Advanced Peripheral Bus (APB), is backwards-compatible with previous devices. The other aperture, the Advanced High-Performance Bus (AHB), offers the same register map but provides better back-to-back access performance than the APB bus. These apertures are mutually exclusive. The aperture enabled for a given GPIO port is controlled by the appropriate bit in the GPIOHBCTL register (see page 258). Note that GPIO port K can only be accessed through the AHB aperture.

To configure the GPIO pins of a particular port, follow these steps:

1. Enable the clock to the port by setting the appropriate bits in the RCGCGPIO register (see page 342). In addition, the SCGCGPIO and DCGCGPIO registers can be programmed in the same manner to enable clocking in Sleep and Deep-Sleep modes.

2. Set the direction of the GPIO port pins by programming the GPIODIR register. A write of a 1 indicates output and a write of a 0 indicates input.
3. Configure the GPIOAFSEL register to program each bit as a GPIO or alternate pin. If an alternate pin is chosen for a bit, then the PMCx field must be programmed in the GPIOPCTL register for the specific peripheral required. There are also two registers, GPIOADCCTL and GPIODMCTL, which can be used to program a GPIO pin as an ADC or μDMA trigger, respectively.

4. Set the drive strength for each of the pins through the GPIODR2R, GPIODR4R, and GPIODR8R registers.

5. Program each pad in the port to have either pull-up, pull-down, or open drain functionality through the GPIOPUR, GPIOPDR, GPIOODR register. Slew rate may also be programmed, if needed, through the GPIOSLR register.

6. To enable GPIO pins as digital I/Os, set the appropriate DEN bit in the GIODEN register. To enable GPIO pins to their analog function (if available), set the GPIOAMSEL bit in the GPIOAMSEL register.

7. Program the GPIO, GPIOIBE, GPIOEV, and GPIOIM registers to configure the type, event, and mask of the interrupts for each port.

     **Note:** To prevent false interrupts, the following steps should be taken when re-configuring GPIO edge and interrupt sense registers:

     a. Mask the corresponding port by clearing the IME field in the GPIOIM register.

     b. Configure the IS field in the GPIOIS register and the IBE field in the GPIOIBE register.

     c. Clear the GPIOISR register.

     d. Unmask the port by setting the IME field in the GPIOIM register.

8. Optionally, software can lock the configurations of the NMI and JTAG/SWD pins on the GPIO port pins, by setting the LOCK bits in the GPIOLOCK register.

When the internal POR signal is asserted and until otherwise configured, all GPIO pins are configured to be undriven (tristate): GPIOAFSEL=0, GIODEN=0, GPIOPDR=0, and GPIOPUR=0, except for the pins shown in Table 10-1 on page 660. Table 10-3 on page 668 shows all possible configurations of the GPIO pads and the control register settings required to achieve them. Table 10-4 on page 669 shows how a rising edge interrupt is configured for pin 2 of a GPIO port.

**Table 10-3. GPIO Pad Configuration Examples**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>GPIO Register Bit Valuea</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AFSEL</td>
</tr>
<tr>
<td>Digital Input (GPIO)</td>
<td>0</td>
</tr>
<tr>
<td>Digital Output (GPIO)</td>
<td>0</td>
</tr>
<tr>
<td>Open Drain Output (GPIO)</td>
<td>0</td>
</tr>
<tr>
<td>Open Drain Input/Output (I2CSDA)</td>
<td>1</td>
</tr>
<tr>
<td>Digital Input/Output (I2CSCl)</td>
<td>1</td>
</tr>
<tr>
<td>Digital Input (Timer CCP)</td>
<td>1</td>
</tr>
</tbody>
</table>

Texas Instruments-Production Data

June 12, 2014
Table 10-3. GPIO Pad Configuration Examples (continued)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>GPIO Register Bit Value(^a)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AFSEL</td>
</tr>
<tr>
<td>Digital Input (QEI)</td>
<td>1</td>
</tr>
<tr>
<td>Digital Output (PWM)</td>
<td>1</td>
</tr>
<tr>
<td>Digital Output (Timer PWM)</td>
<td>1</td>
</tr>
<tr>
<td>Analog Input (Comparator)</td>
<td>0</td>
</tr>
<tr>
<td>Digital Output (Comparator)</td>
<td>1</td>
</tr>
</tbody>
</table>

\(^a\) X=Ignored (don't care bit)

? = Can be either 0 or 1, depending on the configuration

Table 10-4. GPIO Interrupt Configuration Example

<table>
<thead>
<tr>
<th>Register</th>
<th>Desired Interrupt Event Trigger</th>
<th>Pin 2 Bit Value(^a)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>GPIOIS</td>
<td>0=edge</td>
<td>1=level</td>
</tr>
<tr>
<td>GPIOIBE</td>
<td>0=single edge</td>
<td>1=both edges</td>
</tr>
<tr>
<td>GPIOIEV</td>
<td>0=Low level, or falling edge</td>
<td>1=High level, or rising edge</td>
</tr>
<tr>
<td>GPIOIM</td>
<td>0=masked</td>
<td>1=not masked</td>
</tr>
</tbody>
</table>

\(^a\) X=Ignored (don't care bit)

10.4 Register Map

Table 10-6 on page 671 lists the GPIO registers. Each GPIO port can be accessed through one of two bus apertures. The legacy aperture, the Advanced Peripheral Bus (APB), is backwards-compatible with previous devices. The other aperture, the Advanced High-Performance Bus (AHB), offers the same register map but provides better back-to-back access performance than the APB bus.

**Important:** The GPIO registers in this chapter are duplicated in each GPIO block; however, depending on the block, all eight bits may not be connected to a GPIO pad. In those cases, writing to unconnected bits has no effect, and reading unconnected bits returns no meaningful data. See “Signal Description” on page 659 for the GPIOs included on this device.

The offset listed is a hexadecimal increment to the register's address, relative to that GPIO port's base address:

- GPIO Port A (APB): 0x4000.4000
Note that each GPIO module clock must be enabled before the registers can be programmed (see page 342). There must be a delay of 3 system clocks after the GPIO module clock is enabled before any GPIO module registers are accessed.

**Important:** The table below shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (GPIOAFSEL=0, GPIODEN=0, GPIOPDR=0, GPIOPUR=0, and GPIOPCTL=0). Special consideration pins may be programmed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (POR) or asserting RST returns these GPIO to their original special consideration state.

<table>
<thead>
<tr>
<th>GPIO Pins</th>
<th>Default State</th>
<th>Default Reset</th>
<th>GPIOAFSEL</th>
<th>GPIODEN</th>
<th>GPIOPDR</th>
<th>GPIOPUR</th>
<th>GPIOPCTL</th>
<th>GPIOCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[1:0]</td>
<td>UART0</td>
<td>0 0 0 0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PA[5:2]</td>
<td>SSI0</td>
<td>0 0 0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x2</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>PB[3:2]</td>
<td>I²C0</td>
<td>0 0 0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x3</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>PC[3:0]</td>
<td>JTAG/SWD</td>
<td>0 0 0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>PD[7]</td>
<td>GPIOa</td>
<td>0 0 0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>PF[0]</td>
<td>GPIOb</td>
<td>0 0 0 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the GPIOLOCK register and uncommitting it by setting the GPIOCR register.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware signals including the GPIO pins that can function as JTAG/SWD signals and the NMI signal. The commit control process must be followed for these pins, even if they are programmed as alternate functions other than JTAG/SWD or NMI; see “Commit Control” on page 667.

The default register type for the GPIOCR register is RO for all GPIO pins with the exception of the NMI pin and the four JTAG/SWD pins (see “Signal Tables” on page 1354 for pin numbers). These six
pins are the only GPIOs that are protected by the GPIOCR register. Because of this, the register type for the corresponding GPIO Ports is RW.

The default reset value for the GPIOCR register is 0x0000.00FF for all GPIO pins, with the exception of the NMI and JTAG/SWD pins (see “Signal Tables” on page 1354 for pin numbers). To ensure that the JTAG and NMI pins are not accidentally programmed as GPIO pins, these pins default to non-committable. Because of this, the default reset value of GPIOCR changes for the corresponding ports.

Table 10-6. GPIO Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>GPIODATA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Data</td>
<td>673</td>
</tr>
<tr>
<td>0x040</td>
<td>GPIODIR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Direction</td>
<td>675</td>
</tr>
<tr>
<td>0x044</td>
<td>GPIOIS</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Interrupt Sense</td>
<td>676</td>
</tr>
<tr>
<td>0x048</td>
<td>GPIOIBE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Interrupt Both Edges</td>
<td>677</td>
</tr>
<tr>
<td>0x04C</td>
<td>GPIOIEV</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Interrupt Event</td>
<td>679</td>
</tr>
<tr>
<td>0x100</td>
<td>GPIOIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Interrupt Mask</td>
<td>680</td>
</tr>
<tr>
<td>0x144</td>
<td>GIORIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPIO Raw Interrupt Status</td>
<td>681</td>
</tr>
<tr>
<td>0x148</td>
<td>GIORIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPIO Masked Interrupt Status</td>
<td>682</td>
</tr>
<tr>
<td>0x14C</td>
<td>GPIOICR</td>
<td>W1C</td>
<td>0x0000.0000</td>
<td>GPIO Interrupt Clear</td>
<td>683</td>
</tr>
<tr>
<td>0x200</td>
<td>GPIOAFSEL</td>
<td>RW</td>
<td>-</td>
<td>GPIO Alternate Function Select</td>
<td>684</td>
</tr>
<tr>
<td>0x500</td>
<td>GPIO2R</td>
<td>RW</td>
<td>0x0000.00FF</td>
<td>GPIO 2-mA Drive Select</td>
<td>685</td>
</tr>
<tr>
<td>0x504</td>
<td>GPIO4R</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO 4-mA Drive Select</td>
<td>687</td>
</tr>
<tr>
<td>0x508</td>
<td>GPIO8R</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO 8-mA Drive Select</td>
<td>688</td>
</tr>
<tr>
<td>0x50C</td>
<td>GPIOODR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Open Drain Select</td>
<td>689</td>
</tr>
<tr>
<td>0x510</td>
<td>GPIOPUR</td>
<td>RW</td>
<td>-</td>
<td>GPIO Pull-Up Select</td>
<td>690</td>
</tr>
<tr>
<td>0x514</td>
<td>GPIOPDR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Pull-Down Select</td>
<td>692</td>
</tr>
<tr>
<td>0x518</td>
<td>GPIOSLR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Slew Rate Control Select</td>
<td>694</td>
</tr>
<tr>
<td>0x51C</td>
<td>GIODEN</td>
<td>RW</td>
<td>-</td>
<td>GPIO Digital Enable</td>
<td>695</td>
</tr>
<tr>
<td>0x520</td>
<td>GPIOLOCK</td>
<td>RW</td>
<td>0x0000.0001</td>
<td>GPIO Lock</td>
<td>697</td>
</tr>
<tr>
<td>0x524</td>
<td>GPIOCR</td>
<td>-</td>
<td>-</td>
<td>GPIO Commit</td>
<td>698</td>
</tr>
<tr>
<td>0x528</td>
<td>GPIOAMSEL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO Analog Mode Select</td>
<td>700</td>
</tr>
<tr>
<td>0x52C</td>
<td>GIOPCCTL</td>
<td>RW</td>
<td>-</td>
<td>GPIO Port Control</td>
<td>702</td>
</tr>
<tr>
<td>0x530</td>
<td>GPIOADCCCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO ADC Control</td>
<td>704</td>
</tr>
<tr>
<td>0x534</td>
<td>GPIODMACTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPIO DMA Control</td>
<td>705</td>
</tr>
<tr>
<td>0xFD0</td>
<td>GPIOPeriphID4</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPIO Peripheral Identification 4</td>
<td>706</td>
</tr>
<tr>
<td>0xFD4</td>
<td>GPIOPeriphID5</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPIO Peripheral Identification 5</td>
<td>707</td>
</tr>
</tbody>
</table>
### Table 10-6. GPIO Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFD8</td>
<td>GPIOPeriphID6</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPIO Peripheral Identification 6</td>
<td>708</td>
</tr>
<tr>
<td>0xFD0</td>
<td>GPIOPeriphID7</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPIO Peripheral Identification 7</td>
<td>709</td>
</tr>
<tr>
<td>0xFE0</td>
<td>GPIOPeriphID0</td>
<td>RO</td>
<td>0x0000.0061</td>
<td>GPIO Peripheral Identification 0</td>
<td>710</td>
</tr>
<tr>
<td>0xFE4</td>
<td>GPIOPeriphID1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPIO Peripheral Identification 1</td>
<td>711</td>
</tr>
<tr>
<td>0xFE8</td>
<td>GPIOPeriphID2</td>
<td>RO</td>
<td>0x0000.0018</td>
<td>GPIO Peripheral Identification 2</td>
<td>712</td>
</tr>
<tr>
<td>0xFEC</td>
<td>GPIOPeriphID3</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>GPIO Peripheral Identification 3</td>
<td>713</td>
</tr>
<tr>
<td>0xFF0</td>
<td>GPIOPrimeCellID0</td>
<td>RO</td>
<td>0x0000.00D</td>
<td>GPIO PrimeCell Identification 0</td>
<td>714</td>
</tr>
<tr>
<td>0xFF4</td>
<td>GPIOPrimeCellID1</td>
<td>RO</td>
<td>0x0000.00F0</td>
<td>GPIO PrimeCell Identification 1</td>
<td>715</td>
</tr>
<tr>
<td>0xFF8</td>
<td>GPIOPrimeCellID2</td>
<td>RO</td>
<td>0x0000.0005</td>
<td>GPIO PrimeCell Identification 2</td>
<td>716</td>
</tr>
<tr>
<td>0xFFC</td>
<td>GPIOPrimeCellID3</td>
<td>RO</td>
<td>0x0000.00B1</td>
<td>GPIO PrimeCell Identification 3</td>
<td>717</td>
</tr>
</tbody>
</table>

#### 10.5 Register Descriptions

The remainder of this section lists and describes the GPIO registers, in numerical order by address offset.
Register 1: GPIO Data (GPIODATA), offset 0x000

The GPIODATA register is the data register. In software control mode, values written in the GPIODATA register are transferred onto the GPIO port pins if the respective pins have been configured as outputs through the GPIO Direction (GPIODIR) register (see page 675).

In order to write to GPIODATA, the corresponding bits in the mask, resulting from the address bus bits [9:2], must be set. Otherwise, the bit values remain unchanged by the write.

Similarly, the values read from this register are determined for each bit by the mask bit derived from the address used to access the data register, bits [9:2]. Bits that are set in the address mask cause the corresponding bits in GPIODATA to be read, and bits that are clear in the address mask cause the corresponding bits in GPIODATA to be read as 0, regardless of their value.

A read from GPIODATA returns the last bit value written if the respective pins are configured as outputs, or it returns the value on the corresponding input pin when these are configured as inputs. All bits are cleared by a reset.

GPIO Data (GPIODATA)

| GPIO Port A (APB) base: 0x4000.4000 |
| GPIO Port A (AHB) base: 0x4005.8000 |
| GPIO Port B (APB) base: 0x4000.5000 |
| GPIO Port B (AHB) base: 0x4005.9000 |
| GPIO Port C (APB) base: 0x4000.6000 |
| GPIO Port C (AHB) base: 0x4005.A000 |
| GPIO Port D (APB) base: 0x4000.7000 |
| GPIO Port D (AHB) base: 0x4005.B000 |
| GPIO Port E (APB) base: 0x4002.4000 |
| GPIO Port E (AHB) base: 0x4005.C000 |
| GPIO Port F (APB) base: 0x4002.5000 |
| GPIO Port F (AHB) base: 0x4005.D000 |
| GPIO Port G (APB) base: 0x4002.6000 |
| GPIO Port G (AHB) base: 0x4005.E000 |
| GPIO Port H (APB) base: 0x4002.7000 |
| GPIO Port H (AHB) base: 0x4005.F000 |
| GPIO Port J (APB) base: 0x4003.D000 |
| GPIO Port J (AHB) base: 0x4006.0000 |
| GPIO Port K (AHB) base: 0x4006.1000 |
| Offset 0x000
| Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:8      | reserved | RO   | 0x0000.00 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
### GPIO Data

This register is virtually mapped to 256 locations in the address space. To facilitate the reading and writing of data to these registers by independent drivers, the data read from and written to the registers are masked by the eight address lines [9:2]. Reads from this register return its current state. Writes to this register only affect bits that are not masked by ADDR[9:2] and are configured as outputs. See “Data Register Operation” on page 665 for examples of reads and writes.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>DATA</td>
<td>RW</td>
<td>0x00</td>
<td>GPIO Data</td>
</tr>
</tbody>
</table>
Register 2: GPIO Direction (GPIODIR), offset 0x400

The GPIODIR register is the data direction register. Setting a bit in the GPIODIR register configures the corresponding pin to be an output, while clearing a bit configures the corresponding pin to be an input. All bits are cleared by a reset, meaning all GPIO pins are inputs by default.

GPIO Direction (GPIODIR)

<table>
<thead>
<tr>
<th>GPIO Port A (APB) base:</th>
<th>0x4000.4000</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO Port A (AHB) base:</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>GPIO Port B (APB) base:</td>
<td>0x4000.5000</td>
</tr>
<tr>
<td>GPIO Port B (AHB) base:</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>GPIO Port C (APB) base:</td>
<td>0x4000.6000</td>
</tr>
<tr>
<td>GPIO Port C (AHB) base:</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>GPIO Port D (APB) base:</td>
<td>0x4000.7000</td>
</tr>
<tr>
<td>GPIO Port D (AHB) base:</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>GPIO Port E (APB) base:</td>
<td>0x4002.4000</td>
</tr>
<tr>
<td>GPIO Port E (AHB) base:</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>GPIO Port F (APB) base:</td>
<td>0x4002.5000</td>
</tr>
<tr>
<td>GPIO Port F (AHB) base:</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>GPIO Port G (APB) base:</td>
<td>0x4002.6000</td>
</tr>
<tr>
<td>GPIO Port G (AHB) base:</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>GPIO Port H (APB) base:</td>
<td>0x4002.7000</td>
</tr>
<tr>
<td>GPIO Port H (AHB) base:</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>GPIO Port J (APB) base:</td>
<td>0x4003.D000</td>
</tr>
<tr>
<td>GPIO Port J (AHB) base:</td>
<td>0x4006.0000</td>
</tr>
<tr>
<td>GPIO Port K (AHB) base:</td>
<td>0x4006.1000</td>
</tr>
</tbody>
</table>

Offset 0x400
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>DIR</td>
<td>RW</td>
<td>0x00</td>
<td>GPIO Data Direction</td>
</tr>
</tbody>
</table>

Value Description
0  Corresponding pin is an input.
1  Corresponding pins is an output.
Register 3: GPIO Interrupt Sense (GPIOIS), offset 0x404

The GPIOIS register is the interrupt sense register. Setting a bit in the GPIOIS register configures the corresponding pin to detect levels, while clearing a bit configures the corresponding pin to detect edges. All bits are cleared by a reset.

Note: To prevent false interrupts, the following steps should be taken when re-configuring GPIO edge and interrupt sense registers:

1. Mask the corresponding port by clearing the IME field in the GPIOIM register.
2. Configure the IS field in the GPIOIS register and the IBE field in the GPIOIBE register.
3. Clear the GPIORIS register.
4. Unmask the port by setting the IME field in the GPIOIM register.

GPIO Interrupt Sense (GPIOIS)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>IS</td>
<td>RW</td>
<td>0x00</td>
<td>GPIO Interrupt Sense</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 4: GPIO Interrupt Both Edges (GPIOIBE), offset 0x408

The GPIOIBE register allows both edges to cause interrupts. When the corresponding bit in the GPIO Interrupt Sense (GPIOIS) register (see page 676) is set to detect edges, setting a bit in the GPIOIBE register configures the corresponding pin to detect both rising and falling edges, regardless of the corresponding bit in the GPIO Interrupt Event (GPIOIEV) register (see page 679). Clearing a bit configures the pin to be controlled by the GPIOIEV register. All bits are cleared by a reset.

**Note:** To prevent false interrupts, the following steps should be taken when re-configuring GPIO edge and interrupt sense registers:

1. Mask the corresponding port by clearing the IME field in the GPIOIM register.
2. Configure the IS field in the GPIOIS register and the IBE field in the GPIOIBE register.
3. Clear the GPIORIS register.
4. Unmask the port by setting the IME field in the GPIOIM register.

**GPIO Interrupt Both Edges (GPIOIBE)**

- GPIO Port A (APB) base: 0x4000.4000
- GPIO Port A (AHB) base: 0x4005.8000
- GPIO Port B (APB) base: 0x4000.5000
- GPIO Port B (AHB) base: 0x4005.9000
- GPIO Port C (APB) base: 0x4000.6000
- GPIO Port C (AHB) base: 0x4005.A000
- GPIO Port D (APB) base: 0x4000.7000
- GPIO Port D (AHB) base: 0x4005.B000
- GPIO Port E (APB) base: 0x4002.4000
- GPIO Port E (AHB) base: 0x4005.C000
- GPIO Port F (APB) base: 0x4002.5000
- GPIO Port F (AHB) base: 0x4005.D000
- GPIO Port G (APB) base: 0x4002.6000
- GPIO Port G (AHB) base: 0x4005.E000
- GPIO Port H (APB) base: 0x4002.7000
- GPIO Port H (AHB) base: 0x4005.F000
- GPIO Port J (APB) base: 0x4003.D000
- GPIO Port J (AHB) base: 0x4006.0000
- GPIO Port K (AHB) base: 0x4006.1000

Offset 0x408
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
**General-Purpose Input/Outputs (GPIOs)**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>IBE</td>
<td>RW</td>
<td>0x00</td>
<td>GPIO Interrupt Both Edges</td>
</tr>
</tbody>
</table>

Value Description

- **0** Interrupt generation is controlled by the **GPIO Interrupt Event (GPIOIEV)** register (see page 679).
- **1** Both edges on the corresponding pin trigger an interrupt.
Register 5: GPIO Interrupt Event (GPIOIEV), offset 0x40C

The GPIOIEV register is the interrupt event register. Setting a bit in the GPIOIEV register configures the corresponding pin to detect rising edges or high levels, depending on the corresponding bit value in the GPIO Interrupt Sense (GPIOIS) register (see page 676). Clearing a bit configures the pin to detect falling edges or low levels, depending on the corresponding bit value in the GPIOIS register. All bits are cleared by a reset.

### GPIO Interrupt Event (GPIOIEV)

<table>
<thead>
<tr>
<th>GPIO Port A (APB) base: 0x4000.4000</th>
<th>GPIO Port A (AHB) base: 0x4005.8000</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO Port B (APB) base: 0x4000.5000</td>
<td>GPIO Port B (AHB) base: 0x4005.9000</td>
</tr>
<tr>
<td>GPIO Port C (APB) base: 0x4000.6000</td>
<td>GPIO Port C (AHB) base: 0x4005.A000</td>
</tr>
<tr>
<td>GPIO Port D (APB) base: 0x4000.7000</td>
<td>GPIO Port D (AHB) base: 0x4005.B000</td>
</tr>
<tr>
<td>GPIO Port E (APB) base: 0x4002.4000</td>
<td>GPIO Port E (AHB) base: 0x4005.C000</td>
</tr>
<tr>
<td>GPIO Port F (APB) base: 0x4002.5000</td>
<td>GPIO Port F (AHB) base: 0x4005.D000</td>
</tr>
<tr>
<td>GPIO Port G (APB) base: 0x4002.6000</td>
<td>GPIO Port G (AHB) base: 0x4005.E000</td>
</tr>
<tr>
<td>GPIO Port H (APB) base: 0x4002.7000</td>
<td>GPIO Port H (AHB) base: 0x4005.F000</td>
</tr>
<tr>
<td>GPIO Port J (APB) base: 0x4003.D000</td>
<td>GPIO Port J (AHB) base: 0x4006.0000</td>
</tr>
<tr>
<td>GPIO Port K (AHB) base: 0x4006.1000</td>
<td>Offset 0x40C</td>
</tr>
</tbody>
</table>

Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
</tr>
</tbody>
</table>

### Bit/Field Details

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>IEV</td>
<td>RW</td>
<td>0x00</td>
<td>GPIO Interrupt Event</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 A falling edge or a Low level on the corresponding pin triggers an interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A rising edge or a High level on the corresponding pin triggers an interrupt.</td>
</tr>
</tbody>
</table>
Register 6: GPIO Interrupt Mask (GPIOIM), offset 0x410

The GPIOIM register is the interrupt mask register. Setting a bit in the GPIOIM register allows interrupts that are generated by the corresponding pin to be sent to the interrupt controller on the combined interrupt signal. Clearing a bit prevents an interrupt on the corresponding pin from being sent to the interrupt controller. All bits are cleared by a reset.

GPIO Interrupt Mask (GPIOIM)

<table>
<thead>
<tr>
<th>Port</th>
<th>APB Base</th>
<th>AHB Base</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0x4000.4000</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>B</td>
<td>0x4000.5000</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>C</td>
<td>0x4000.6000</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>D</td>
<td>0x4000.7000</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>E</td>
<td>0x4002.4000</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>F</td>
<td>0x4002.5000</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>G</td>
<td>0x4002.6000</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>H</td>
<td>0x4002.7000</td>
<td>0x4006.0000</td>
</tr>
<tr>
<td>J</td>
<td>0x4003.D000</td>
<td>0x4006.1000</td>
</tr>
</tbody>
</table>

Offset 0x410
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>IME</td>
<td>RW</td>
<td>0x00</td>
<td>GPIO Interrupt Mask Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 7: GPIO Raw Interrupt Status (GPIORIS), offset 0x414

The GPIORIS register is the raw interrupt status register. A bit in this register is set when an interrupt condition occurs on the corresponding GPIO pin. If the corresponding bit in the GPIO Interrupt Mask (GPIOIM) register (see page 680) is set, the interrupt is sent to the interrupt controller. Bits read as zero indicate that corresponding input pins have not initiated an interrupt. For a GPIO level-detect interrupt, the interrupt signal generating the interrupt must be held until serviced. Once the input signal deasserts from the interrupt generating logical sense, the corresponding RIS bit in the GPIORIS register clears. For a GPIO edge-detect interrupt, the RIS bit in the GPIORIS register is cleared by writing a ‘1’ to the corresponding bit in the GPIO Interrupt Clear (GPIOICR) register. The corresponding GPIOIS bit reflects the masked value of the RIS bit.

GPIO Raw Interrupt Status (GPIORIS)

| GPIO Port A (APB) base: 0x4000.4000 |
| GPIO Port A (AHB) base: 0x4005.8000 |
| GPIO Port B (APB) base: 0x4000.5000 |
| GPIO Port B (AHB) base: 0x4005.9000 |
| GPIO Port C (APB) base: 0x4000.6000 |
| GPIO Port C (AHB) base: 0x4005.A000 |
| GPIO Port D (APB) base: 0x4000.7000 |
| GPIO Port D (AHB) base: 0x4005.B000 |
| GPIO Port E (APB) base: 0x4002.4000 |
| GPIO Port E (AHB) base: 0x4005.C000 |
| GPIO Port F (APB) base: 0x4002.5000 |
| GPIO Port F (AHB) base: 0x4005.D000 |
| GPIO Port G (APB) base: 0x4002.6000 |
| GPIO Port G (AHB) base: 0x4005.E000 |
| GPIO Port H (APB) base: 0x4002.7000 |
| GPIO Port H (AHB) base: 0x4005.F000 |
| GPIO Port J (APB) base: 0x4003.D000 |
| GPIO Port J (AHB) base: 0x4006.0000 |
| GPIO Port K (AHB) base: 0x4006.1000 |

Offset 0x414
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>RIS</td>
<td>RO</td>
<td>0x00</td>
<td>GPIO Interrupt Raw Status</td>
</tr>
</tbody>
</table>

Value Description

0 An interrupt condition has not occurred on the corresponding pin.

1 An interrupt condition has occurred on the corresponding pin.

For edge-detect interrupts, this bit is cleared by writing a 1 to the corresponding bit in the GPIOICR register.
For a GPIO level-detect interrupt, the bit is cleared when the level is deasserted.
Register 8: GPIO Masked Interrupt Status (GPIOMIS), offset 0x418

The GPIOMIS register is the masked interrupt status register. If a bit is set in this register, the corresponding interrupt has triggered an interrupt to the interrupt controller. If a bit is clear, either no interrupt has been generated, or the interrupt is masked.

Note that if the Port B GPIOADCCCTL register is cleared, PB4 can still be used as an external trigger for the ADC. This is a legacy mode which allows code written for previous devices to operate on this microcontroller.

GPIOMIS is the state of the interrupt after masking.

**GPIO Masked Interrupt Status (GPIOMIS)**

| GPIO Port A (APB) base: 0x4000.4000 |
| GPIO Port A (AHB) base: 0x4005.8000 |
| GPIO Port B (APB) base: 0x4000.5000 |
| GPIO Port B (AHB) base: 0x4005.9000 |
| GPIO Port C (APB) base: 0x4000.6000 |
| GPIO Port C (AHB) base: 0x4005.A000 |
| GPIO Port D (APB) base: 0x4000.7000 |
| GPIO Port D (AHB) base: 0x4005.B000 |
| GPIO Port E (APB) base: 0x4002.4000 |
| GPIO Port E (AHB) base: 0x4005.C000 |
| GPIO Port F (APB) base: 0x4002.5000 |
| GPIO Port F (AHB) base: 0x4005.D000 |
| GPIO Port G (APB) base: 0x4002.6000 |
| GPIO Port G (AHB) base: 0x4005.E000 |
| GPIO Port H (APB) base: 0x4002.7000 |
| GPIO Port H (AHB) base: 0x4005.F000 |
| GPIO Port J (APB) base: 0x4003.D000 |
| GPIO Port J (AHB) base: 0x4006.0000 |
| GPIO Port K (AHB) base: 0x4006.1000 |

Offset 0x418
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>MIS</td>
<td>RO</td>
<td>0x00</td>
<td>GPIO Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For edge-detect interrupts, this bit is cleared by writing a 1 to the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>corresponding bit in the GPIOICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For a GPIO level-detect interrupt, the bit is cleared when the level is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>deasserted.</td>
</tr>
</tbody>
</table>

Texas Instruments-Production Data

June 12, 2014
Register 9: GPIO Interrupt Clear (GPIOICR), offset 0x41C

The GPIOICR register is the interrupt clear register. For edge-detect interrupts, writing a 1 to the IC bit in the GPIOICR register clears the corresponding bit in the GPIORIS and GPIOMIS registers. If the interrupt is a level-detect, the IC bit in this register has no effect. In addition, writing a 0 to any of the bits in the GPIOICR register has no effect.

**GPIO Interrupt Clear (GPIOICR)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>W1C</td>
<td>GPIO Interrupt Clear</td>
<td>0x00</td>
<td>The corresponding interrupt is unaffected.</td>
</tr>
<tr>
<td>W1C</td>
<td>GPIO Interrupt Clear</td>
<td>0x01</td>
<td>The corresponding interrupt is cleared.</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
Register 10: GPIO Alternate Function Select (GPIOAFSEL), offset 0x420

The GPIOAFSEL register is the mode control select register. If a bit is clear, the pin is used as a GPIO and is controlled by the GPIO registers. Setting a bit in this register configures the corresponding GPIO line to be controlled by an associated peripheral. Several possible peripheral functions are multiplexed on each GPIO. The GPIO Port Control (GPIOPCCTL) register is used to select one of the possible functions. Table 23-5 on page 1386 details which functions are muxed on each GPIO pin. The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in the table below.

**Important:** The table below shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (GPIOAFSEL=0, GPIODEN=0, GPIOPDR=0, GPIOPUR=0, and GPIOPCCTL=0). Special consideration pins may be programmed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (POR) or asserting RST returns these GPIO to their original special consideration state.

### Table 10-7. GPIO Pins With Special Considerations

<table>
<thead>
<tr>
<th>GPIO Pins</th>
<th>Default Reset State</th>
<th>GPIOAFSEL</th>
<th>GPIODEN</th>
<th>GPIOPDR</th>
<th>GPIOPUR</th>
<th>GPIOPCCTL</th>
<th>GPIOCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[1:0]</td>
<td>UART0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x1</td>
<td>1</td>
</tr>
<tr>
<td>PA[5:2]</td>
<td>SSI0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x2</td>
<td>1</td>
</tr>
<tr>
<td>PB[3:2]</td>
<td>I^2C0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x3</td>
<td>1</td>
</tr>
<tr>
<td>PC[3:0]</td>
<td>JTAG/SWD</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0x1</td>
<td>0</td>
</tr>
<tr>
<td>PD[7]</td>
<td>GPIO8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
<tr>
<td>PF[0]</td>
<td>GPIO9</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
</tbody>
</table>

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the GPIOLOCK register and uncommitting it by setting the GPIOCR register.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware signals including the GPIO pins that can function as JTAG/SWD signals and the NMI signal. The commit control process must be followed for these pins, even if they are programmed as alternate functions other than JTAG/SWD or NMI; see “Commit Control” on page 667.

Caution – It is possible to create a software sequence that prevents the debugger from connecting to the TM4C123GH6PZ microcontroller. If the program code loaded into flash immediately changes the JTAG pins to their GPIO functionality, the debugger may not have enough time to connect and halt the controller before the JTAG pin functionality switches. As a result, the debugger may be locked out of the part. This issue can be avoided with a software routine that restores JTAG functionality based on an external or software trigger. In the case that the software routine is not implemented and the device is locked out of the part, this issue can be solved by using the TM4C123GH6PZ Flash Programmer "Unlock" feature. Please refer to LMFLASHPROGRAMMER on the TI web for more information.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is provided for the GPIO pins that can be used as the four JTAG/SWD pins and the NMI pin (see “Signal Tables” on page 1354 for pin numbers). Writes to protected bits of the GPIO Alternate Function Select (GPIOAFSEL) register (see page 684), GPIO Pull Up Select (GPIOPUR) register (see page 690), GPIO Pull-Down Select (GPIOPDR) register (see page 692), and GPIO Digital Enable (GPIODEN) register (see page 695) are not committed to storage unless the GPIO Lock (GPIOLOCK) register (see page 697) has been unlocked and the appropriate bits of the GPIO Commit (GPIOCR) register (see page 698) have been set.
When using the I²C module, in addition to setting the GPIOAFSEL register bits for the I²C clock and data pins, the data pins should be set to open drain using the GPIO Open Drain Select (GPIOODR) register (see examples in “Initialization and Configuration” on page 667).

GPIO Alternate Function Select (GPIOAFSEL)
GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000
Offset 0x420
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>AFSEL</td>
<td>RW</td>
<td>-</td>
<td>GPIO Alternate Function Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The associated pin functions as a GPIO and is controlled by the GPIO registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The associated pin functions as a peripheral signal and is controlled by the alternate hardware function. The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in Table 10-1 on page 660.</td>
</tr>
</tbody>
</table>
Register 11: GPIO 2-mA Drive Select (GPIODR2R), offset 0x500

The GPIODR2R register is the 2-mA drive control register. Each GPIO signal in the port can be individually configured without affecting the other pads. When setting the DRV2 bit for a GPIO signal, the corresponding DRV4 bit in the GPIODR4R register and DRV8 bit in the GPIODR8R register are automatically cleared by hardware. By default, all GPIO pins have 2-mA drive.

GPIO 2-mA Drive Select (GPIODR2R)

<table>
<thead>
<tr>
<th>GPIO Port</th>
<th>APB base</th>
<th>AHB base</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0x4000.4000</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>B</td>
<td>0x4000.5000</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>C</td>
<td>0x4000.6000</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>D</td>
<td>0x4000.7000</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>E</td>
<td>0x4000.8000</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>F</td>
<td>0x4000.9000</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>G</td>
<td>0x4005.E000</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>H</td>
<td>0x4005.F000</td>
<td>0x4006.0000</td>
</tr>
<tr>
<td>I</td>
<td>0x4006.0000</td>
<td>0x4006.1000</td>
</tr>
</tbody>
</table>

Offset 0x500
Type RW, reset 0x0000.00FF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>DRV2</td>
<td>RW</td>
<td>0xFF</td>
<td>Output Pad 2-mA Drive Enable</td>
</tr>
</tbody>
</table>

Value Description

0 The drive for the corresponding GPIO pin is controlled by the GPIODR4R or GPIODR8R register.
1 The corresponding GPIO pin has 2-mA drive.

Setting a bit in either the GPIODR4 register or the GPIODR8 register clears the corresponding 2-mA enable bit. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.
Register 12: GPIO 4-mA Drive Select (GPIO4R), offset 0x504

The GPIO4R register is the 4-mA drive control register. Each GPIO signal in the port can be individually configured without affecting the other pads. When setting the DRV4 bit for a GPIO signal, the corresponding DRV2 bit in the GPIO2R register and DRV8 bit in the GPIO8R register are automatically cleared by hardware.

GPIO 4-mA Drive Select (GPIO4R)

<table>
<thead>
<tr>
<th>Port</th>
<th>APB Base</th>
<th>AHB Base</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port A</td>
<td>0x4000.4000</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>Port B</td>
<td>0x4000.5000</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>Port C</td>
<td>0x4000.6000</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>Port D</td>
<td>0x4000.7000</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>Port E</td>
<td>0x4000.8000</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>Port F</td>
<td>0x4000.9000</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>Port G</td>
<td>0x4000.A000</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>Port H</td>
<td>0x4000.B000</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>Port J</td>
<td>0x4000.C000</td>
<td>0x4005.0000</td>
</tr>
<tr>
<td>Port K</td>
<td>0x4000.D000</td>
<td>0x4005.1000</td>
</tr>
</tbody>
</table>

Offset 0x504
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>DRV4</td>
<td>RW</td>
<td>0x00</td>
<td>Output Pad 4-mA Drive Enable</td>
</tr>
</tbody>
</table>

Value Description

0 The drive for the corresponding GPIO pin is controlled by the GPIO2R or GPIO8R register.
1 The corresponding GPIO pin has 4-mA drive.

Setting a bit in either the GPIO2R register or the GPIO8R register clears the corresponding 4-mA enable bit. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.
Register 13: GPIO 8-mA Drive Select (GPIODR8R), offset 0x508

The **GPIODR8R** register is the 8-mA drive control register. Each GPIO signal in the port can be individually configured without affecting the other pads. When setting the **DRV8** bit for a GPIO signal, the corresponding **DRV2** bit in the **GPIODR2R** register and **DRV4** bit in the **GPIODR4R** register are automatically cleared by hardware. The 8-mA setting is also used for high-current operation.

**Note:** There is no configuration difference between 8-mA and high-current operation. The additional current capacity results from a shift in the $V_{OH}/V_{OL}$ levels. See “Recommended Operating Conditions” on page 1397 for further information.

### GPIO 8-mA Drive Select (GPIODR8R)

| GPIO Port A (APB) base: 0x4000.4000 |
| GPIO Port A (AHB) base: 0x4005.8000 |
| GPIO Port B (APB) base: 0x4000.5000 |
| GPIO Port B (AHB) base: 0x4005.9000 |
| GPIO Port C (APB) base: 0x4000.6000 |
| GPIO Port C (AHB) base: 0x4005.A000 |
| GPIO Port D (APB) base: 0x4000.7000 |
| GPIO Port D (AHB) base: 0x4005.B000 |
| GPIO Port E (APB) base: 0x4002.4000 |
| GPIO Port E (AHB) base: 0x4005.C000 |
| GPIO Port F (APB) base: 0x4002.5000 |
| GPIO Port F (AHB) base: 0x4005.D000 |
| GPIO Port G (APB) base: 0x4002.6000 |
| GPIO Port G (AHB) base: 0x4005.E000 |
| GPIO Port H (APB) base: 0x4002.7000 |
| GPIO Port H (AHB) base: 0x4005.F000 |
| GPIO Port J (APB) base: 0x4003.D000 |
| GPIO Port J (AHB) base: 0x4006.0000 |
| GPIO Port K (AHB) base: 0x4006.1000 |

Offset 0x508

Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Pad 8-mA Drive Enable</td>
<td>0x00</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

**Setting a bit in either the GPIODR2 register or the GPIODR4 register clears the corresponding 8-mA enable bit. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.**
Register 14: GPIO Open Drain Select (GPIOODR), offset 0x50C

The GPIOODR register is the open drain control register. Setting a bit in this register enables the open-drain configuration of the corresponding GPIO pad. When open-drain mode is enabled, the corresponding bit should also be set in the GPIO Digital Enable (GPIODEN) register (see page 695). Corresponding bits in the drive strength and slew rate control registers (GPIODR2R, GPIODR4R, GPIODR8R, and GPIOSLR) can be set to achieve the desired fall times. The GPIO acts as an input if the corresponding bit in the GPIODIR register is cleared. If open drain is selected while the GPIO is configured as an input, the GPIO will remain an input and the open-drain selection has no effect until the GPIO is changed to an output.

When using the I²C module, in addition to configuring the data pin to open drain, the GPIO Alternate Function Select (GPIOAFSEL) register bits for the I²C clock and data pins should be set (see examples in "Initialization and Configuration" on page 667).

GPIO Open Drain Select (GPIOODR)

| GPIO Port A (APB) base: 0x4000.4000 |
| GPIO Port A (AHB) base: 0x4005.8000 |
| GPIO Port B (APB) base: 0x4000.5000 |
| GPIO Port B (AHB) base: 0x4005.9000 |
| GPIO Port C (APB) base: 0x4000.6000 |
| GPIO Port C (AHB) base: 0x4005.4000 |
| GPIO Port D (APB) base: 0x4000.7000 |
| GPIO Port D (AHB) base: 0x4005.B000 |
| GPIO Port E (APB) base: 0x4002.4000 |
| GPIO Port E (AHB) base: 0x4005.C000 |
| GPIO Port F (APB) base: 0x4002.5000 |
| GPIO Port F (AHB) base: 0x4005.D000 |
| GPIO Port G (APB) base: 0x4002.6000 |
| GPIO Port G (AHB) base: 0x4005.E000 |
| GPIO Port H (APB) base: 0x4002.7000 |
| GPIO Port H (AHB) base: 0x4005.F000 |
| GPIO Port J (APB) base: 0x4003.D000 |
| GPIO Port J (AHB) base: 0x4006.0000 |
| GPIO Port K (AHB) base: 0x4006.1000 |
| Offset 0x50C |

Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>ODE</td>
<td>RW</td>
<td>0x00</td>
<td>Output Pad Open Drain Enable</td>
</tr>
</tbody>
</table>

Value Description

0  The corresponding pin is not configured as open drain.
1  The corresponding pin is configured as open drain.
Register 15: GPIO Pull-Up Select (GPIOPUR), offset 0x510

The GPIOPUR register is the pull-up control register. When a bit is set, a weak pull-up resistor on the corresponding GPIO signal is enabled. Setting a bit in GPIOPUR automatically clears the corresponding bit in the GPIO Pull-Down Select (GPIOPDR) register (see page 692). Write access to this register is protected with the GPIOCR register. Bits in GPIOCR that are cleared prevent writes to the equivalent bit in this register.

**Important:** The table below shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (GPIOAFSEL=0, GPIODEN=0, GPIOPDR=0, GPIOPUR=0, and GPIOPCTL=0). Special consideration pins may be programmed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (POR) or asserting RST returns these GPIO to their original special consideration state.

**Table 10-8. GPIO Pins With Special Considerations**

<table>
<thead>
<tr>
<th>GPIO Pins</th>
<th>Default Reset State</th>
<th>GPIOAFSEL</th>
<th>GPIODEN</th>
<th>GPIOPDR</th>
<th>GPIOPUR</th>
<th>GPIOPCTL</th>
<th>GPIOCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[1:0]</td>
<td>UART0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x1</td>
<td>1</td>
</tr>
<tr>
<td>PA[5:2]</td>
<td>SSI0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x2</td>
<td>1</td>
</tr>
<tr>
<td>PB[3:2]</td>
<td>I²C0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x3</td>
<td>1</td>
</tr>
<tr>
<td>PC[3:0]</td>
<td>JTAG/SWD</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0x1</td>
<td>0</td>
</tr>
<tr>
<td>PD[7]</td>
<td>GPIOa</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
<tr>
<td>PF[0]</td>
<td>GPIOa</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
</tbody>
</table>

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the GPIOLOCK register and uncommitting it by setting the GPIOCR register.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware signals including the GPIO pins that can function as JTAG/SWD signals and the NMI signal. The commit control process must be followed for these pins, even if they are programmed as alternate functions other than JTAG/SWD or NMI; see “Commit Control” on page 667.

**Note:** The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is provided for the GPIO pins that can be used as the four JTAG/SWD pins and the NMI pin (see “Signal Tables” on page 1354 for pin numbers). Writes to protected bits of the GPIO Alternate Function Select (GPIOAFSEL) register (see page 684), GPIO Pull Up Select (GPIOPUR) register (see page 690), GPIO Pull-Down Select (GPIOPDR) register (see page 692), and GPIO Digital Enable (GPIODEN) register (see page 695) are not committed to storage unless the GPIO Lock (GPIOLOCK) register (see page 697) has been unlocked and the appropriate bits of the GPIO Commit (GPIOCR) register (see page 698) have been set.
GPIO Pull-Up Select (GPIOPUR)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000
Offset 0x510

Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PUE</td>
<td>RW</td>
<td>-</td>
<td>Pad Weak Pull-Up Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The corresponding pin's weak pull-up resistor is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The corresponding pin's weak pull-up resistor is enabled.</td>
</tr>
</tbody>
</table>

Setting a bit in the GPIOPDR register clears the corresponding bit in the GPIOPUR register. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.

The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in Table 10-1 on page 660.
Register 16: GPIO Pull-Down Select (GPIOPDR), offset 0x514

The GPIOPDR register is the pull-down control register. When a bit is set, a weak pull-down resistor on the corresponding GPIO signal is enabled. Setting a bit in GPIOPDR automatically clears the corresponding bit in the GPIO Pull-Up Select (GPIOPUR) register (see page 690).

Important: The table below shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (GPIOAFSEL=0, GPIODEN=0, GPIOPDR=0, GPIOPUR=0, and GPIOPCTL=0). Special consideration pins may be programmed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (POR) or asserting RST returns these GPIO to their original special consideration state.

<table>
<thead>
<tr>
<th>GPIO Pins</th>
<th>Default Reset State</th>
<th>GPIOAFSEL</th>
<th>GPIODEN</th>
<th>GPIOPDR</th>
<th>GPIOPUR</th>
<th>GPIOPCTL</th>
<th>GPIOCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[1:0]</td>
<td>UART0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x1</td>
<td>1</td>
</tr>
<tr>
<td>PA[5:2]</td>
<td>SSI0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x2</td>
<td>1</td>
</tr>
<tr>
<td>PB[3:2]</td>
<td>I²C0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x3</td>
<td>1</td>
</tr>
<tr>
<td>PC[3:0]</td>
<td>JTAG/SWD</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0x1</td>
<td>0</td>
</tr>
<tr>
<td>PD[7]</td>
<td>GPIO3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
<tr>
<td>PF[0]</td>
<td>GPIO3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
</tbody>
</table>

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the GPIOLOCK register and uncommitting it by setting the GPIOCR register.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware signals including the GPIO pins that can function as JTAG/SWD signals and the NMI signal. The commit control process must be followed for these pins, even if they are programmed as alternate functions other than JTAG/SWD or NMI; see “Commit Control” on page 667.

Note: The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is provided for the GPIO pins that can be used as the four JTAG/SWD pins and the NMI pin (see “Signal Tables” on page 1354 for pin numbers). Writes to protected bits of the GPIO Alternate Function Select (GPIOAFSEL) register (see page 684), GPIO Pull Up Select (GPIOPUR) register (see page 690), GPIO Pull-Down Select (GPIOPDR) register (see page 692), and GPIO Digital Enable (GPIODEN) register (see page 695) are not committed to storage unless the GPIO Lock (GPIOLOCK) register (see page 697) has been unlocked and the appropriate bits of the GPIO Commit (GPIOCR) register (see page 698) have been set.
### GPIO Pull-Down Select (GPIOPDR)

GPIO Port A (APB) base: 0x4000.4000  
GPIO Port A (AHB) base: 0x4005.8000  
GPIO Port B (APB) base: 0x4000.5000  
GPIO Port B (AHB) base: 0x4005.9000  
GPIO Port C (APB) base: 0x4000.6000  
GPIO Port C (AHB) base: 0x4005.A000  
GPIO Port D (APB) base: 0x4000.7000  
GPIO Port D (AHB) base: 0x4005.B000  
GPIO Port E (APB) base: 0x4002.4000  
GPIO Port E (AHB) base: 0x4005.C000  
GPIO Port F (APB) base: 0x4002.5000  
GPIO Port F (AHB) base: 0x4005.D000  
GPIO Port G (APB) base: 0x4002.6000  
GPIO Port G (AHB) base: 0x4005.E000  
GPIO Port H (APB) base: 0x4002.7000  
GPIO Port H (AHB) base: 0x4005.F000  
GPIO Port J (APB) base: 0x4003.D000  
GPIO Port J (AHB) base: 0x4006.0000  
GPIO Port K (AHB) base: 0x4006.1000  
Offset 0x514  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PDE</td>
<td>RW</td>
<td>0x00</td>
<td>Pad Weak Pull-Down Enable</td>
</tr>
</tbody>
</table>

**Value | Description**
--- | ---
0    | The corresponding pin's weak pull-down resistor is disabled.  
1    | The corresponding pin's weak pull-down resistor is enabled.  

Setting a bit in the GPIOPUR register clears the corresponding bit in the GPIOPDR register. The change is effective on the second clock cycle after the write if accessing GPIO via the APB memory aperture. If using AHB access, the change is effective on the next clock cycle.
Register 17: GPIO Slew Rate Control Select (GPIOSLR), offset 0x518

The GPIOSLR register is the slew rate control register. Slew rate control is only available when using the 8-mA drive strength option. The selection of drive strength is done through the GPIO 8-mA Drive Select (GPIO8mA) register.

GPIO Slew Rate Control Select (GPIOSLR)

<table>
<thead>
<tr>
<th>Port</th>
<th>APB Base</th>
<th>AHB Base</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0x4000.4000</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>B</td>
<td>0x4000.5000</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>C</td>
<td>0x4000.6000</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>D</td>
<td>0x4000.7000</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>E</td>
<td>0x4000.8000</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>F</td>
<td>0x4000.9000</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>G</td>
<td>0x4000.1000</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>H</td>
<td>0x4000.1100</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>J</td>
<td>0x4002.4000</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>K</td>
<td>0x4002.5000</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>L</td>
<td>0x4002.6000</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>M</td>
<td>0x4002.7000</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>N</td>
<td>0x4003.4000</td>
<td>0x4006.0000</td>
</tr>
<tr>
<td>O</td>
<td>0x4003.5000</td>
<td>0x4006.1000</td>
</tr>
</tbody>
</table>

Offset 0x518
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>SRL</td>
<td>RW</td>
<td>0x00</td>
<td>Slew Rate Limit Enable (8-mA drive only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 18: GPIO Digital Enable (GPIODEN), offset 0x51C

**Note:** Pins configured as digital inputs are Schmitt-triggered.

The **GPIODEN** register is the digital enable register. By default, all GPIO signals except those listed below are configured out of reset to be undriven (tristate). Their digital function is disabled; they do not drive a logic value on the pin and they do not allow the pin voltage into the GPIO receiver. To use the pin as a digital input or output (either GPIO or alternate function), the corresponding **GPIODEN** bit must be set.

**Important:** The table below shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL**=0, **GPIODEN**=0, **GPIOPDR**=0, **GPIOPUR**=0, and **GPIOPCTL**=0). Special consideration pins may be programed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (POR) or asserting **RST** returns these GPIO to their original special consideration state.

### Table 10-10. GPIO Pins With Special Considerations

<table>
<thead>
<tr>
<th>GPIO Pins</th>
<th>Default Reset State</th>
<th>GPIOAFSEL</th>
<th>GPIODEN</th>
<th>GPIOPDR</th>
<th>GPIOPUR</th>
<th>GPIOPCTL</th>
<th>GPIOCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[1:0]</td>
<td>UART0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x1</td>
<td>1</td>
</tr>
<tr>
<td>PA[5:2]</td>
<td>SSI0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x2</td>
<td>1</td>
</tr>
<tr>
<td>PB[3:2]</td>
<td>I²C0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x3</td>
<td>1</td>
</tr>
<tr>
<td>PC[3:0]</td>
<td>JTAG/SWD</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0x1</td>
<td>0</td>
</tr>
<tr>
<td>PD[7]</td>
<td>GPIO²</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
<tr>
<td>PF[0]</td>
<td>GPIO²</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
</tbody>
</table>

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the **GPIOLOCK** register and uncommitting it by setting the **GPIOCR** register.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware signals including the GPIO pins that can function as JTAG/SWD pins and the **NMI** signal. The commit control process must be followed for these pins, even if they are programmed as alternate functions other than JTAG/SWD or NMI; see “Commit Control” on page 667.

**Note:** The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware peripherals. Protection is provided for the GPIO pins that can be used as the four JTAG/SWD pins and the **NMI** pin (see “Signal Tables” on page 1354 for pin numbers). Writes to protected bits of the **GPIO Alternate Function Select (GPIOAFSEL)** register (see page 684), **GPIO Pull Up Select (GPIOPUR)** register (see page 690), **GPIO Pull-Down Select (GPIOPDR)** register (see page 692), and **GPIO Digital Enable (GPIODEN)** register (see page 695) are not committed to storage unless the **GPIO Lock (GPIOLOCK)** register (see page 697) has been unlocked and the appropriate bits of the **GPIO Commit (GPIOCR)** register (see page 698) have been set.
GPIO Digital Enable (GPIODEN)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>-</td>
</tr>
<tr>
<td>Digital Enable</td>
<td>-</td>
</tr>
</tbody>
</table>

Value Description

0  
The digital functions for the corresponding pin are disabled.

1  
The digital functions for the corresponding pin are enabled.

The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in Table 10-1 on page 660.
Register 19: GPIO Lock (GPIOLOCK), offset 0x520

The GPIOLOCK register enables write access to the GPIOCR register (see page 698). Writing 0x4C4F.434B to the GPIOLOCK register unlocks the GPIOCR register. Writing any other value to the GPIOLOCK register re-enables the locked state. Reading the GPIOLOCK register returns the lock status rather than the 32-bit value that was previously written. Therefore, when write accesses are disabled, or locked, reading the GPIOLOCK register returns 0x0000.0001. When write accesses are enabled, or unlocked, reading the GPIOLOCK register returns 0x0000.0000.

GPIO Lock (GPIOLOCK)

| GPIO Port A (APB) base: 0x4000.4000 |
| GPIO Port A (AHB) base: 0x4005.8000 |
| GPIO Port B (APB) base: 0x4000.5000 |
| GPIO Port B (AHB) base: 0x4005.9000 |
| GPIO Port C (APB) base: 0x4000.6000 |
| GPIO Port C (AHB) base: 0x4005.4000 |
| GPIO Port D (APB) base: 0x4000.7000 |
| GPIO Port D (AHB) base: 0x4005.5000 |
| GPIO Port E (APB) base: 0x4002.4000 |
| GPIO Port E (AHB) base: 0x4005.C000 |
| GPIO Port F (APB) base: 0x4002.5000 |
| GPIO Port F (AHB) base: 0x4005.D000 |
| GPIO Port G (APB) base: 0x4002.6000 |
| GPIO Port G (AHB) base: 0x4005.E000 |
| GPIO Port H (APB) base: 0x4002.7000 |
| GPIO Port H (AHB) base: 0x4005.F000 |
| GPIO Port I (APB) base: 0x4003.D000 |
| GPIO Port J (AHB) base: 0x4006.0000 |
| GPIO Port K (AHB) base: 0x4006.1000 |

Offset 0x520
Type RW, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO Lock</td>
<td>LOCK</td>
<td>31:0</td>
<td>RW</td>
<td>0x0000.0001</td>
<td>0x1</td>
<td>The GPIOCR register is locked and may not be modified.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>The GPIOCR register is unlocked and may be modified.</td>
</tr>
</tbody>
</table>
Register 20: GPIO Commit (GPIOCR), offset 0x524

The GPIOCR register is the commit register. The value of the GPIOCR register determines which bits of the GPIOAFSEL, GPIOPUR, GPIOPDR, and GPIODEN registers are committed when a write to these registers is performed. If a bit in the GPIOCR register is cleared, the data being written to the corresponding bit in the GPIOAFSEL, GPIOPUR, GPIOPDR, or GPIODEN registers cannot be committed and retains its previous value. If a bit in the GPIOCR register is set, the data being written to the corresponding bit of the GPIOAFSEL, GPIOPUR, GPIOPDR, or GPIODEN registers is committed to the register and reflects the new value.

The contents of the GPIOCR register can only be modified if the status in the GPIOLOCK register is unlocked. Writes to the GPIOCR register are ignored if the status in the GPIOLOCK register is locked.

**Important:** This register is designed to prevent accidental programming of the registers that control connectivity to the NMI and JTAG/SWD debug hardware. By initializing the bits of the GPIOCR register to 0 for the NMI and JTAG/SWD pins (see “Signal Tables” on page 1354 for pin numbers), the NMI and JTAG/SWD debug port can only be converted to GPIOs through a deliberate set of writes to the GPIOLOCK, GPIOCR, and the corresponding registers.

Because this protection is currently only implemented on the NMI and JTAG/SWD pins (see “Signal Tables” on page 1354 for pin numbers), all of the other bits in the GPIOCR registers cannot be written with 0x0. These bits are hardwired to 0x1, ensuring that it is always possible to commit new values to the GPIOAFSEL, GPIOPUR, GPIOPDR, or GPIODEN register bits of these other pins.
Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CR</td>
<td>-</td>
<td>-</td>
<td>GPIO Commit</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The corresponding GPIOAFSEL, GPIOPUR, GPIOPDR, or GPIODEN bits cannot be written.</td>
</tr>
<tr>
<td>1</td>
<td>The corresponding GPIOAFSEL, GPIOPUR, GPIOPDR, or GPIODEN bits can be written.</td>
</tr>
</tbody>
</table>

**Note:** The default register type for the GPIOCR register is RO for all GPIO pins with the exception of the NMI pin and the four JTAG/SWD pins (see “Signal Tables” on page 1354 for pin numbers). These six pins are the only GPIOs that are protected by the GPIOCR register. Because of this, the register type for the corresponding GPIO Ports is RW.

The default reset value for the GPIOCR register is 0x0000.00FF for all GPIO pins, with the exception of the NMI and JTAG/SWD pins (see “Signal Tables” on page 1354 for pin numbers). To ensure that the JTAG and NMI pins are not accidentally programmed as GPIO pins, these pins default to non-committable. Because of this, the default reset value of GPIOCR changes for the corresponding ports.
## Register 21: GPIO Analog Mode Select (GPIOAMSEL), offset 0x528

**Important:** This register is only valid for ports and pins that can be used as ADC AINx inputs. If any pin is to be used as an ADC input, the appropriate bit in GPIOAMSEL must be set to disable the analog isolation circuit.

The **GPIOAMSEL** register controls isolation circuits to the analog side of a unified I/O pad. Because the GPIOs may be driven by a 5-V source and affect analog operation, analog circuitry requires isolation from the pins when they are not used in their analog function.

Each bit of this register controls the isolation circuitry for the corresponding GPIO signal. For information on which GPIO pins can be used for ADC functions, refer to Table 23-5 on page 1386.

### GPIO Analog Mode Select (GPIOAMSEL)

| GPIO Port A (APB) base: 0x4000.4000 | GPIO Port A (AHB) base: 0x4005.8000 |
| GPIO Port B (APB) base: 0x4000.5000 | GPIO Port B (AHB) base: 0x4005.9000 |
| GPIO Port C (APB) base: 0x4000.6000 | GPIO Port C (AHB) base: 0x4005.A000 |
| GPIO Port D (APB) base: 0x4000.7000 | GPIO Port D (AHB) base: 0x4005.B000 |
| GPIO Port E (APB) base: 0x4002.4000 | GPIO Port E (AHB) base: 0x4005.C000 |
| GPIO Port F (APB) base: 0x4002.5000 | GPIO Port F (AHB) base: 0x4005.D000 |
| GPIO Port G (APB) base: 0x4002.6000 | GPIO Port G (AHB) base: 0x4005.E000 |
| GPIO Port H (APB) base: 0x4002.7000 | GPIO Port H (AHB) base: 0x4005.F000 |
| GPIO Port J (APB) base: 0x4003.D000 | GPIO Port J (AHB) base: 0x4006.0000 |
| GPIO Port K (AHB) base: 0x4006.1000 | Offset 0x528 |

Type RW, reset 0x0000.0000

### Description

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>GPIOAMSEL</td>
<td>RW</td>
<td>0x00</td>
<td>GPIO Analog Mode Select</td>
</tr>
</tbody>
</table>

**Value Description**

0  The analog function of the pin is disabled, the isolation is enabled, and the pin is capable of digital functions as specified by the other GPIO configuration registers.

1  The analog function of the pin is enabled, the isolation is disabled, and the pin is capable of analog functions.

**Note:** This register and bits are only valid for GPIO signals that share analog function through a unified I/O pad.

The reset state of this register is 0 for all signals.
Register 22: GPIO Port Control (GPIOPCTL), offset 0x52C

The GPIOPCTL register is used in conjunction with the GPIOAFSEL register and selects the specific peripheral signal for each GPIO pin when using the alternate function mode. Most bits in the GPIOAFSEL register are cleared on reset, therefore most GPIO pins are configured as GPIOs by default. When a bit is set in the GPIOAFSEL register, the corresponding GPIO signal is controlled by an associated peripheral. The GPIOPCTL register selects one out of a set of peripheral functions for each GPIO, providing additional flexibility in signal definition. For information on the defined encodings for the bit fields in this register, refer to Table 23-5 on page 1386. The reset value for this register is 0x0000.0000 for GPIO ports that are not listed in the table below.

Note: If a particular input signal to a peripheral is assigned to two different GPIO port pins, the signal is assigned to the port with the lowest letter and the assignment to the higher letter port is ignored. If a particular output signal from a peripheral is assigned to two different GPIO port pins, the signal will output to both pins. Assigning an output signal from a peripheral to two different GPIO pins is not recommended.

Important: The table below shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (GPIOAFSEL=0, GPIODEN=0, GPIOPDR=0, GPIOPUR=0, and GPIOPCTL=0). Special consideration pins may be programed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (POR) or asserting RST returns these GPIO to their original special consideration state.

Table 10-11. GPIO Pins With Special Considerations

<table>
<thead>
<tr>
<th>GPIO Pins</th>
<th>Default Reset State</th>
<th>GPIOAFSEL</th>
<th>GPIODEN</th>
<th>GPIOPDR</th>
<th>GPIOPUR</th>
<th>GPIOPCTL</th>
<th>GPIOCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[1:0]</td>
<td>UART0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x1</td>
<td>1</td>
</tr>
<tr>
<td>PA[5:2]</td>
<td>SSI0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x2</td>
<td>1</td>
</tr>
<tr>
<td>PB[3:2]</td>
<td>I2C0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x3</td>
<td>1</td>
</tr>
<tr>
<td>PC[3:0]</td>
<td>JTAG/SWD</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0x1</td>
<td>0</td>
</tr>
<tr>
<td>PD[7]</td>
<td>GPIO5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
<tr>
<td>PF[0]</td>
<td>GPIO6</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
</tbody>
</table>

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the GPIOLOCK register and uncommitting it by setting the GPIOCR register.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware signals including the GPIO pins that can function as JTAG/SWD signals and the NMI signal. The commit control process must be followed for these pins, even if they are programmed as alternate functions other than JTAG/SWD or NMI; see “Commit Control” on page 667.
GPIO Port Control (GPIOPCTL)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000
Offset 0x52C
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:28     | PMC7  | RW   | -     | Port Mux Control 7  
This field controls the configuration for GPIO pin 7. |
| 27:24     | PMC6  | RW   | -     | Port Mux Control 6  
This field controls the configuration for GPIO pin 6. |
| 23:20     | PMC5  | RW   | -     | Port Mux Control 5  
This field controls the configuration for GPIO pin 5. |
| 19:16     | PMC4  | RW   | -     | Port Mux Control 4  
This field controls the configuration for GPIO pin 4. |
| 15:12     | PMC3  | RW   | -     | Port Mux Control 3  
This field controls the configuration for GPIO pin 3. |
| 11:8      | PMC2  | RW   | -     | Port Mux Control 2  
This field controls the configuration for GPIO pin 2. |
| 7:4       | PMC1  | RW   | -     | Port Mux Control 1  
This field controls the configuration for GPIO pin 1. |
| 3:0       | PMC0  | RW   | -     | Port Mux Control 0  
This field controls the configuration for GPIO pin 0. |
Register 23: GPIO ADC Control (GPIOADCCTL), offset 0x530

This register is used to configure a GPIO pin as a source for the ADC trigger.

Note that if the Port B GPIOADCCTL register is cleared, PB4 can still be used as an external trigger for the ADC. This is a legacy mode which allows code written for previous devices to operate on this microcontroller.

GPIO ADC Control (GPIOADCCTL)
GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000

Offset 0x530
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>ADCEN</td>
<td>RW</td>
<td>0x00</td>
<td>ADC Trigger Enable</td>
</tr>
</tbody>
</table>

Value  Description
0      The corresponding pin is not used to trigger the ADC.
1      The corresponding pin is used to trigger the ADC.
Register 24: GPIO DMA Control (GPIODMACCTL), offset 0x534

This register is used to configure a GPIO pin as a source for the μDMA trigger.

### GPIO DMA Control (GPIODMACCTL)

| GPIO Port A (APB) base: 0x4000.4000 | GPIO Port A (AHB) base: 0x4005.8000 |
| GPIO Port B (APB) base: 0x4000.5000 | GPIO Port B (AHB) base: 0x4005.9000 |
| GPIO Port C (APB) base: 0x4000.6000 | GPIO Port C (AHB) base: 0x4005.A000 |
| GPIO Port D (APB) base: 0x4000.7000 | GPIO Port D (AHB) base: 0x4005.B000 |
| GPIO Port E (APB) base: 0x4002.4000 | GPIO Port E (AHB) base: 0x4005.C000 |
| GPIO Port F (APB) base: 0x4002.5000 | GPIO Port F (AHB) base: 0x4005.D000 |
| GPIO Port G (APB) base: 0x4002.6000 | GPIO Port G (AHB) base: 0x4005.E000 |
| GPIO Port H (APB) base: 0x4002.7000 | GPIO Port H (AHB) base: 0x4005.F000 |
| GPIO Port J (APB) base: 0x4003.D000 | GPIO Port J (AHB) base: 0x4006.0000 |
| GPIO Port K (AHB) base: 0x4006.1000 |

Offset 0x534
- Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>DMAEN</td>
<td>RW</td>
<td>0x00</td>
<td>μDMA Trigger Enable</td>
</tr>
</tbody>
</table>

Value  Description
0      The corresponding pin is not used to trigger the μDMA.
1      The corresponding pin is used to trigger the μDMA.
The **GPIO Peripheral Identification 4** (GPIOPeriphID4), **GPIO Peripheral Identification 5** (GPIOPeriphID5), **GPIO Peripheral Identification 6** (GPIOPeriphID6), and **GPIO Peripheral Identification 7** (GPIOPeriphID7) registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

### GPIO Peripheral Identification 4 (GPIOPeriphID4)

<table>
<thead>
<tr>
<th>Port</th>
<th>APB Base</th>
<th>AHB Base</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port A</td>
<td>0x4000.4000</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>Port B</td>
<td>0x4000.5000</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>Port C</td>
<td>0x4000.6000</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>Port D</td>
<td>0x4000.7000</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>Port E</td>
<td>0x4002.4000</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>Port F</td>
<td>0x4002.5000</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>Port G</td>
<td>0x4002.6000</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>Port H</td>
<td>0x4002.7000</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>Port I</td>
<td>0x4003.D000</td>
<td>0x4006.0000</td>
</tr>
<tr>
<td>Port J</td>
<td>0x4006.1000</td>
<td>0x4006.1000</td>
</tr>
</tbody>
</table>

Offset **0xFD0**

**Type RO, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibil</td>
</tr>
<tr>
<td>7:0</td>
<td>PID4</td>
<td>RO</td>
<td>0x00</td>
<td>GPIO Peripheral ID Register [7:0]</td>
</tr>
</tbody>
</table>
Register 26: GPIO Peripheral Identification 5 (GPIOPeriphID5), offset 0xFD4

The GPIOPeriphID4, GPIOPeriphID5, GPIOPeriphID6, and GPIOPeriphID7 registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

GPIO Peripheral Identification 5 (GPIOPeriphID5)

<table>
<thead>
<tr>
<th>Description</th>
<th>Reset</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 31:8 reserved</td>
<td>0x0000.00</td>
<td>RO</td>
</tr>
<tr>
<td>Software should not rely on the value of the reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 7:0</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>PID5</td>
<td>0x00</td>
<td>RO</td>
</tr>
<tr>
<td>GPIO Peripheral ID Register [15:8]</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Tiva™ TM4C123GH6PZ Microcontroller

June 12, 2014

Texas Instruments-Production Data
Register 27: GPIO Peripheral Identification 6 (GPIOPeriphID6), offset 0xFD8

The GPIOPeriphID4, GPIOPeriphID5, GPIOPeriphID6, and GPIOPeriphID7 registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

### GPIO Peripheral Identification 6 (GPIOPeriphID6)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000
Offset 0xFD8
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID6</td>
<td>RO</td>
<td>0x00</td>
<td>GPIO Peripheral ID Register [23:16]</td>
</tr>
</tbody>
</table>
Register 28: GPIO Peripheral Identification 7 (GPIOPeriphID7), offset 0xFDC

The GPIOPeriphID4, GPIOPeriphID5, GPIOPeriphID6, and GPIOPeriphID7 registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

### GPIO Peripheral Identification 7 (GPIOPeriphID7)

<table>
<thead>
<tr>
<th>Description</th>
<th>Reset Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>RO</td>
<td>0x0000.00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>GPIO Peripheral ID Register [31:24]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>PID7</td>
<td>RO</td>
<td>0x00</td>
<td></td>
</tr>
</tbody>
</table>
Register 29: GPIO Peripheral Identification 0 (GPIOPeriphID0), offset 0xFE0

The **GPIOPeriphID0**, **GPIOPeriphID1**, **GPIOPeriphID2**, and **GPIOPeriphID3** registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

### GPIO Peripheral Identification 0 (GPIOPeriphID0)

<table>
<thead>
<tr>
<th>GPIO Port A (APB) base</th>
<th>0x4000.4000</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO Port A (AHB) base</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>GPIO Port B (APB) base</td>
<td>0x4000.5000</td>
</tr>
<tr>
<td>GPIO Port B (AHB) base</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>GPIO Port C (APB) base</td>
<td>0x4000.6000</td>
</tr>
<tr>
<td>GPIO Port C (AHB) base</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>GPIO Port D (APB) base</td>
<td>0x4000.7000</td>
</tr>
<tr>
<td>GPIO Port D (AHB) base</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>GPIO Port E (APB) base</td>
<td>0x4002.4000</td>
</tr>
<tr>
<td>GPIO Port E (AHB) base</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>GPIO Port F (APB) base</td>
<td>0x4002.5000</td>
</tr>
<tr>
<td>GPIO Port F (AHB) base</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>GPIO Port G (APB) base</td>
<td>0x4002.6000</td>
</tr>
<tr>
<td>GPIO Port G (AHB) base</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>GPIO Port H (APB) base</td>
<td>0x4002.7000</td>
</tr>
<tr>
<td>GPIO Port H (AHB) base</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>GPIO Port J (APB) base</td>
<td>0x4003.D000</td>
</tr>
<tr>
<td>GPIO Port J (AHB) base</td>
<td>0x4006.0000</td>
</tr>
<tr>
<td>GPIO Port K (AHB) base</td>
<td>0x4006.1000</td>
</tr>
<tr>
<td>Offset 0xFE0 Type RO, reset 0x0000.0061</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID0</td>
<td>RO</td>
<td>0x61</td>
<td>GPIO Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 30: GPIO Peripheral Identification 1 (GPIOPeriphID1), offset 0xFE4

The GPIOPeriphID0, GPIOPeriphID1, GPIOPeriphID2, and GPIOPeriphID3 registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

GPIO Peripheral Identification 1 (GPIOPeriphID1)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000
Offset 0xFE4
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID1</td>
<td>RO</td>
<td>0x00</td>
<td>GPIO Peripheral ID Register [15:8] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 31: GPIO Peripheral Identification 2 (GPIOPeriphID2), offset 0xFE8

The GPIOPeriphID0, GPIOPeriphID1, GPIOPeriphID2, and GPIOPeriphID3 registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

**GPIO Peripheral Identification 2 (GPIOPeriphID2)**

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000
Offset 0xFE8
Type RO, reset 0x0000.0018

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID2</td>
<td>RO</td>
<td>0x18</td>
<td>GPIO Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 32: GPIO Peripheral Identification 3 (GPIOPeriphID3), offset 0xFEC

The GPIOPeriphID0, GPIOPeriphID1, GPIOPeriphID2, and GPIOPeriphID3 registers can conceptually be treated as one 32-bit register; each register contains eight bits of the 32-bit register, used by software to identify the peripheral.

GPIO Peripheral Identification 3 (GPIOPeriphID3)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000
Offset 0xFEC
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID3</td>
<td>RO</td>
<td>0x01</td>
<td>GPIO Peripheral ID Register [31:24] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 33: GPIO PrimeCell Identification 0 (GPIOPCellID0), offset 0xFF0

The GPIOPCellID0, GPIOPCellID1, GPIOPCellID2, and GPIOPCellID3 registers are four 8-bit wide registers, that can conceptually be treated as one 32-bit register. The register is used as a standard cross-peripheral identification system.

GPIO PrimeCell Identification 0 (GPIOPCellID0)

<table>
<thead>
<tr>
<th>GPIO Port A (APB) base</th>
<th>0x4000.4000</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO Port A (AHB) base</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>GPIO Port B (APB) base</td>
<td>0x4000.5000</td>
</tr>
<tr>
<td>GPIO Port B (AHB) base</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>GPIO Port C (APB) base</td>
<td>0x4000.6000</td>
</tr>
<tr>
<td>GPIO Port C (AHB) base</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>GPIO Port D (APB) base</td>
<td>0x4000.7000</td>
</tr>
<tr>
<td>GPIO Port D (AHB) base</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>GPIO Port E (APB) base</td>
<td>0x4002.4000</td>
</tr>
<tr>
<td>GPIO Port E (AHB) base</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>GPIO Port F (APB) base</td>
<td>0x4002.5000</td>
</tr>
<tr>
<td>GPIO Port F (AHB) base</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>GPIO Port G (APB) base</td>
<td>0x4002.6000</td>
</tr>
<tr>
<td>GPIO Port G (AHB) base</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>GPIO Port H (APB) base</td>
<td>0x4002.7000</td>
</tr>
<tr>
<td>GPIO Port H (AHB) base</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>GPIO Port J (APB) base</td>
<td>0x4003.D000</td>
</tr>
<tr>
<td>GPIO Port J (AHB) base</td>
<td>0x4006.0000</td>
</tr>
<tr>
<td>GPIO Port K (AHB) base</td>
<td>0x4006.1000</td>
</tr>
<tr>
<td>Offset 0xFF0</td>
<td>Type RO, reset 0x0000.000D</td>
</tr>
</tbody>
</table>

8-bit: 31:0

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000000D</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td>7:0</td>
<td>CID0</td>
<td>RO</td>
<td>0x0D</td>
<td>GPIO PrimeCell ID Register [7:0] Provides software a standard cross-</td>
</tr>
</tbody>
</table>

Texas Instruments-Production Data
Register 34: GPIO PrimeCell Identification 1 (GPIOPCellID1), offset 0xFF4

The GPIOPCellID0, GPIOPCellID1, GPIOPCellID2, and GPIOPCellID3 registers are four 8-bit wide registers, that can conceptually be treated as one 32-bit register. The register is used as a standard cross-peripheral identification system.

GPIO PrimeCell Identification 1 (GPIOPCellID1)

<table>
<thead>
<tr>
<th>GPIO Port A (APB) base</th>
<th>GPIO Port A (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4000.4000</td>
<td>0x4005.8000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port B (APB) base</th>
<th>GPIO Port B (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4000.5000</td>
<td>0x4005.9000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port C (APB) base</th>
<th>GPIO Port C (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4000.6000</td>
<td>0x4005.A000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port D (APB) base</th>
<th>GPIO Port D (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4000.7000</td>
<td>0x4005.B000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port E (APB) base</th>
<th>GPIO Port E (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4002.4000</td>
<td>0x4005.C000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port F (APB) base</th>
<th>GPIO Port F (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4002.5000</td>
<td>0x4005.D000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port G (APB) base</th>
<th>GPIO Port G (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4002.6000</td>
<td>0x4005.E000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port H (APB) base</th>
<th>GPIO Port H (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4002.7000</td>
<td>0x4005.F000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port J (APB) base</th>
<th>GPIO Port J (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4003.D000</td>
<td>0x4006.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO Port K (AHB) base</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4006.1000</td>
</tr>
</tbody>
</table>

Offset 0xFF4
Type RO, reset 0x0000.00F0

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID1</td>
<td>RO</td>
<td>0xF0</td>
<td>GPIO PrimeCell ID Register [15:8] Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 35: GPIO PrimeCell Identification 2 (GPIOPCellID2), offset 0xFF8

The GPIOPCellID0, GPIOPCellID1, GPIOPCellID2, and GPIOPCellID3 registers are four 8-bit wide registers, that can conceptually be treated as one 32-bit register. The register is used as a standard cross-peripheral identification system.

GPIO PrimeCell Identification 2 (GPIOPCellID2)

GPIO Port A (APB) base: 0x4000.4000
GPIO Port A (AHB) base: 0x4005.8000
GPIO Port B (APB) base: 0x4000.5000
GPIO Port B (AHB) base: 0x4005.9000
GPIO Port C (APB) base: 0x4000.6000
GPIO Port C (AHB) base: 0x4005.A000
GPIO Port D (APB) base: 0x4000.7000
GPIO Port D (AHB) base: 0x4005.B000
GPIO Port E (APB) base: 0x4002.4000
GPIO Port E (AHB) base: 0x4005.C000
GPIO Port F (APB) base: 0x4002.5000
GPIO Port F (AHB) base: 0x4005.D000
GPIO Port G (APB) base: 0x4002.6000
GPIO Port G (AHB) base: 0x4005.E000
GPIO Port H (APB) base: 0x4002.7000
GPIO Port H (AHB) base: 0x4005.F000
GPIO Port J (APB) base: 0x4003.D000
GPIO Port J (AHB) base: 0x4006.0000
GPIO Port K (AHB) base: 0x4006.1000
Offset 0xFF8
Type RO, reset 0x0000.0005

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td></td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td>CID2</td>
<td>RO</td>
<td>0x05</td>
<td>GPIO PrimeCell Identification ID Register [23:16]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 36: GPIO PrimeCell Identification 3 (GPIOPCellID3), offset 0xFFC

The GPIOPCellID0, GPIOPCellID1, GPIOPCellID2, and GPIOPCellID3 registers are four 8-bit wide registers, that can conceptually be treated as one 32-bit register. The register is used as a standard cross-peripheral identification system.

### GPIOP PrimeCell Identification 3 (GPIOPCellID3)

<table>
<thead>
<tr>
<th>GPIO Port</th>
<th>APB base</th>
<th>AHB base</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0x4000.4000</td>
<td>0x4005.8000</td>
</tr>
<tr>
<td>B</td>
<td>0x4000.5000</td>
<td>0x4005.9000</td>
</tr>
<tr>
<td>C</td>
<td>0x4000.6000</td>
<td>0x4005.A000</td>
</tr>
<tr>
<td>D</td>
<td>0x4000.7000</td>
<td>0x4005.B000</td>
</tr>
<tr>
<td>E</td>
<td>0x4000.8000</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>F</td>
<td>0x4000.9000</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>G</td>
<td>0x4000.A000</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>H</td>
<td>0x4000.B000</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>J</td>
<td>0x4002.4000</td>
<td>0x4005.C000</td>
</tr>
<tr>
<td>K</td>
<td>0x4002.5000</td>
<td>0x4005.D000</td>
</tr>
<tr>
<td>L</td>
<td>0x4002.6000</td>
<td>0x4005.E000</td>
</tr>
<tr>
<td>M</td>
<td>0x4002.7000</td>
<td>0x4005.F000</td>
</tr>
<tr>
<td>N</td>
<td>0x4002.8000</td>
<td>0x4006.0000</td>
</tr>
<tr>
<td>O</td>
<td>0x4002.9000</td>
<td>0x4006.1000</td>
</tr>
</tbody>
</table>

Offset 0xFFC

Type RO, reset 0x0000.00B1

---

### Register Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID3</td>
<td>RO</td>
<td>0xB1</td>
<td>GPIO PrimeCell ID Register [31:24] Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
11 General-Purpose Timers

Programmable timers can be used to count or time external events that drive the Timer input pins. The TM4C123GH6PZ General-Purpose Timer Module (GPTM) contains six 16/32-bit GPTM blocks and six 32/64-bit Wide GPTM blocks. Each 16/32-bit GPTM block provides two 16-bit timers/counters (referred to as Timer A and Timer B) that can be configured to operate independently as timers or event counters, or concatenated to operate as one 32-bit timer or one 32-bit Real-Time Clock (RTC). Each 32/64-bit Wide GPTM block provides 32-bit timers for Timer A and Timer B that can be concatenated to operate as a 64-bit timer. Timers can also be used to trigger μDMA transfers.

In addition, timers can be used to trigger analog-to-digital conversions (ADC) when a time-out occurs in periodic and one-shot modes. The ADC trigger signals from all of the general-purpose timers are ORed together before reaching the ADC module, so only one timer should be used to trigger ADC events.

The GPT Module is one timing resource available on the Tiva™ C Series microcontrollers. Other timer resources include the System Timer (SysTick) (see 123) and the PWM timer in the PWM modules (see “PWM Timer” on page 1256).

The General-Purpose Timer Module (GPTM) contains six 16/32-bit GPTM blocks and six 32/64-bit Wide GPTM blocks with the following functional options:

■ 16/32-bit operating modes:
  – 16- or 32-bit programmable one-shot timer
  – 16- or 32-bit programmable periodic timer
  – 16-bit general-purpose timer with an 8-bit prescaler
  – 32-bit Real-Time Clock (RTC) when using an external 32.768-KHz clock as the input
  – 16-bit input-edge count- or time-capture modes with an 8-bit prescaler
  – 16-bit PWM mode with an 8-bit prescaler and software-programmable output inversion of the PWM signal

■ 32/64-bit operating modes:
  – 32- or 64-bit programmable one-shot timer
  – 32- or 64-bit programmable periodic timer
  – 32-bit general-purpose timer with a 16-bit prescaler
  – 64-bit Real-Time Clock (RTC) when using an external 32.768-KHz clock as the input
  – 32-bit input-edge count- or time-capture modes with a 16-bit prescaler
  – 32-bit PWM mode with a 16-bit prescaler and software-programmable output inversion of the PWM signal

■ Count up or down

■ Twelve 16/32-bit Capture Compare PWM pins (CCP)
- Twelve 32/64-bit Capture Compare PWM pins (CCP)
- Daisy chaining of timer modules to allow a single timer to initiate multiple timing events
- Timer synchronization allows selected timers to start counting on the same clock cycle
- ADC event trigger
- User-enabled stalling when the microcontroller asserts CPU Halt flag during debug (excluding RTC mode)
- Ability to determine the elapsed time between the assertion of the timer interrupt and entry into the interrupt service routine
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Dedicated channel for each timer
  - Burst request generated on timer interrupt

11.1 Block Diagram

In the block diagram, the specific Capture Compare PWM (CCP) pins available depend on the TM4C123GH6PZ device. See Table 11-1 on page 720 for the available CCP pins and their timer assignments.
### Table 11-1. Available CCP Pins

<table>
<thead>
<tr>
<th>Timer</th>
<th>Up/Down Counter</th>
<th>Even CCP Pin</th>
<th>Odd CCP Pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>16/32-Bit Timer 0</td>
<td>Timer A</td>
<td>T0CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>T0CCP1</td>
</tr>
<tr>
<td>16/32-Bit Timer 1</td>
<td>Timer A</td>
<td>T1CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>T1CCP1</td>
</tr>
<tr>
<td>16/32-Bit Timer 2</td>
<td>Timer A</td>
<td>T2CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>T2CCP1</td>
</tr>
<tr>
<td>16/32-Bit Timer 3</td>
<td>Timer A</td>
<td>T3CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>T3CCP1</td>
</tr>
<tr>
<td>16/32-Bit Timer 4</td>
<td>Timer A</td>
<td>T4CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>T4CCP1</td>
</tr>
<tr>
<td>16/32-Bit Timer 5</td>
<td>Timer A</td>
<td>T5CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>T5CCP1</td>
</tr>
<tr>
<td>32/64-Bit Wide Timer 0</td>
<td>Timer A</td>
<td>WT0CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>WT0CCP1</td>
</tr>
<tr>
<td>32/64-Bit Wide Timer 1</td>
<td>Timer A</td>
<td>WT1CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>WT1CCP1</td>
</tr>
<tr>
<td>32/64-Bit Wide Timer 2</td>
<td>Timer A</td>
<td>WT2CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>WT2CCP1</td>
</tr>
<tr>
<td>32/64-Bit Wide Timer 3</td>
<td>Timer A</td>
<td>WT3CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>WT3CCP1</td>
</tr>
<tr>
<td>32/64-Bit Wide Timer 4</td>
<td>Timer A</td>
<td>WT4CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>WT4CCP1</td>
</tr>
<tr>
<td>32/64-Bit Wide Timer 5</td>
<td>Timer A</td>
<td>WT5CCP0</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Timer B</td>
<td>-</td>
<td>WT5CCP1</td>
</tr>
</tbody>
</table>

### 11.2 Signal Description

The following table lists the external signals of the GP Timer module and describes the function of each. The GP Timer signals are alternate functions for some GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for these GP Timer signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the GP Timer function. The number in parentheses is the encoding that must be programmed into the PMCn field in the GPIO Port Control (GPIOPCTL) register (page 702) to assign the GP Timer signal to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659.

#### Table 11-2. General-Purpose Timers Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T0CCP0</td>
<td>40</td>
<td>PF0 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T0CCP1</td>
<td>41</td>
<td>PF1 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 0 Capture/Compare/PWM 1.</td>
</tr>
</tbody>
</table>
Table 11-2. General-Purpose Timers Signals (100LQFP) *(continued)*

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type*</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1CCP0</td>
<td>42, 68, 92</td>
<td>PF2 (7), PJ0 (7), PB4 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T1CCP1</td>
<td>43, 69, 91</td>
<td>PF3 (7), PJ1 (7), PB5 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T2CCP0</td>
<td>11, 39, 70</td>
<td>PJ2 (7), PF4 (7), PB0 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T2CCP1</td>
<td>37, 71</td>
<td>PF5 (7), PB1 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T3CCP0</td>
<td>36, 72</td>
<td>PF6 (7), PB2 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T3CCP1</td>
<td>58, 73</td>
<td>PF7 (7), PB3 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T4CCP0</td>
<td>62, 85</td>
<td>PG0 (7), PC0 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T4CCP1</td>
<td>61, 84</td>
<td>PG1 (7), PC1 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T5CCP0</td>
<td>60, 83</td>
<td>PG2 (7), PC2 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T5CCP1</td>
<td>59, 82</td>
<td>PG3 (7), PC3 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT0CCP0</td>
<td>25, 74</td>
<td>PC4 (7), PG4 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT0CCP1</td>
<td>24, 75</td>
<td>PC5 (7), PG5 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT1CCP0</td>
<td>23, 87</td>
<td>PC6 (7), PG6 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT1CCP1</td>
<td>22, 88</td>
<td>PC7 (7), PG7 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT2CCP0</td>
<td>1, 16</td>
<td>PD0 (7), PH0 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT2CCP1</td>
<td>2, 17</td>
<td>PD1 (7), PH1 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT3CCP0</td>
<td>3, 79</td>
<td>PD2 (7), PH4 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT3CCP1</td>
<td>4, 78</td>
<td>PD3 (7), PH5 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT4CCP0</td>
<td>77, 97</td>
<td>PH6 (7), PD4 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT4CCP1</td>
<td>76, 98</td>
<td>PH7 (7), PD5 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT5CCP0</td>
<td>18, 99</td>
<td>PH2 (7), PD6 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT5CCP1</td>
<td>19, 100</td>
<td>PH3 (7), PD7 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 1.</td>
</tr>
</tbody>
</table>

* The TTL designation indicates the pin has TTL-compatible voltage levels.
11.3 Functional Description

The main components of each GPTM block are two free-running up/down counters (referred to as Timer A and Timer B), two prescaler registers, two match registers, two prescaler match registers, two shadow registers, and two load/initialization registers and their associated control functions. The exact functionality of each GPTM is controlled by software and configured through the register interface. Timer A and Timer B can be used individually, in which case they have a 16-bit counting range for the 16/32-bit GPTM blocks and a 32-bit counting range for 32/64-bit Wide GPTM blocks. In addition, Timer A and Timer B can be concatenated to provide a 32-bit counting range for the 16/32-bit GPTM blocks and a 64-bit counting range for the 32/64-bit Wide GPTM blocks. Note that the prescaler can only be used when the timers are used individually.

The available modes for each GPTM block are shown in Table 11-3 on page 722. Note that when counting down in one-shot or periodic modes, the prescaler acts as a true prescaler and contains the least-significant bits of the count. When counting up in one-shot or periodic modes, the prescaler acts as a timer extension and holds the most-significant bits of the count. In input edge count, input edge time and PWM mode, the prescaler always acts as a timer extension, regardless of the count direction.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Timer Use</th>
<th>Count Direction</th>
<th>Counter Size</th>
<th>Prescaler Sizea</th>
<th>Prescaler Behavior (Count Direction)</th>
</tr>
</thead>
<tbody>
<tr>
<td>One-shot</td>
<td>Individual</td>
<td>Up or Down</td>
<td>16-bit</td>
<td>16-bit</td>
<td>Timer Extension (Up), Prescaler (Down)</td>
</tr>
<tr>
<td></td>
<td>Concatenated</td>
<td>Up or Down</td>
<td>32-bit</td>
<td>16-bit</td>
<td>Timer Extension (Up), Prescaler (Down)</td>
</tr>
<tr>
<td>Periodic</td>
<td>Individual</td>
<td>Up or Down</td>
<td>16-bit</td>
<td>16-bit</td>
<td>Timer Extension (Up), Prescaler (Down)</td>
</tr>
<tr>
<td></td>
<td>Concatenated</td>
<td>Up or Down</td>
<td>32-bit</td>
<td>16-bit</td>
<td>N/A</td>
</tr>
<tr>
<td>RTC</td>
<td>Concatenated</td>
<td>Up</td>
<td>32-bit</td>
<td>16-bit</td>
<td>N/A</td>
</tr>
<tr>
<td>Edge Count</td>
<td>Individual</td>
<td>Up or Down</td>
<td>16-bit</td>
<td>16-bit</td>
<td>Timer Extension (Both)</td>
</tr>
<tr>
<td></td>
<td>Individual</td>
<td>Up or Down</td>
<td>32-bit</td>
<td>16-bit</td>
<td>Timer Extension (Both)</td>
</tr>
<tr>
<td>PWM</td>
<td>Individual</td>
<td>Down</td>
<td>16-bit</td>
<td>16-bit</td>
<td>Timer Extension</td>
</tr>
</tbody>
</table>

a. The prescaler is only available when the timers are used individually

Software configures the GPTM using the GPTM Configuration (GPTMCFG) register (see page 741), the GPTM Timer A Mode (GPTMTAMR) register (see page 743), and the GPTM Timer B Mode (GPTMTBMGR) register (see page 747). When in one of the concatenated modes, Timer A and Timer B can only operate in one mode. However, when configured in an individual mode, Timer A and Timer B can be independently configured in any combination of the individual modes.

11.3.1 GPTM Reset Conditions

After reset has been applied to the GPTM module, the module is in an inactive state, and all control registers are cleared and in their default states. Counters Timer A and Timer B are initialized to all 1s, along with their corresponding registers:

- Load Registers:
  - GPTM Timer A Interval Load (GPTMTAILR) register (see page 770)
- GPTM Timer B Interval Load (GPTMTBILR) register (see page 771)

**Shadow Registers:**
- GPTM Timer A Value (GPTMTAV) register (see page 780)
- GPTM Timer B Value (GPTMTBV) register (see page 781)

The following prescale counters are initialized to all 0s:
- GPTM Timer A Prescale (GPTMTAPR) register (see page 774)
- GPTM Timer B Prescale (GPTMTBPR) register (see page 775)
- GPTM Timer A Prescale Snapshot (GPTMTAPS) register (see page 783)
- GPTM Timer B Prescale Snapshot (GPTMTBPS) register (see page 784)
- GPTM Timer A Prescale Value (GPTMTAPV) register (see page 785)
- GPTM Timer B Prescale Value (GPTMTBPV) register (see page 786)

### 11.3.2 Timer Modes

This section describes the operation of the various timer modes. When using Timer A and Timer B in concatenated mode, only the Timer A control and status bits must be used; there is no need to use Timer B control and status bits. The GPTM is placed into individual/split mode by writing a value of 0x4 to the GPTM Configuration (GPTMCFG) register (see page 741). In the following sections, the variable “n” is used in bit field and register names to imply either a Timer A function or a Timer B function. Throughout this section, the timeout event in down-count mode is 0x0 and in up-count mode is the value in the GPTM Timer n Interval Load (GPTMTnILR) and the optional GPTM Timer n Prescale (GPTMTnPR) registers, with the exception of RTC mode.

#### 11.3.2.1 One-Shot/Periodic Timer Mode

The selection of one-shot or periodic mode is determined by the value written to the TnMR field of the GPTM Timer n Mode (GPTMTnMR) register (see page 743). The timer is configured to count up or down using the TnCDIR bit in the GPTMTnMR register.

When software sets the TnEN bit in the GPTM Control (GPTMCTL) register (see page 751), the timer begins counting up from 0x0 or down from its preloaded value. Alternatively, if the TnWOT bit is set in the GPTMnMR register, once the TnEN bit is set, the timer waits for a trigger to begin counting (see “Wait-for-Trigger Mode” on page 732). Table 11-4 on page 723 shows the values that are loaded into the timer registers when the timer is enabled.

**Table 11-4. Counter Values When the Timer is Enabled in Periodic or One-Shot Modes**

<table>
<thead>
<tr>
<th>Register</th>
<th>Count Down Mode</th>
<th>Count Up Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPTMTnR</td>
<td>GPTMTnILR</td>
<td>0x0</td>
</tr>
<tr>
<td>GPTMTnV</td>
<td>GPTMTnILR in concatenated mode; GPTMTnPR in combination with GPTMTnILR in individual mode</td>
<td>0x0</td>
</tr>
<tr>
<td>GPTMTnPS</td>
<td>GPTMTnPR in individual mode; not available in concatenated mode</td>
<td>0x0 in individual mode; not available in concatenated mode</td>
</tr>
<tr>
<td>GPTMTnPV</td>
<td>GPTMTnPR in individual mode; not available in concatenated mode</td>
<td>0x0 in individual mode; not available in concatenated mode</td>
</tr>
</tbody>
</table>
When the timer is counting down and it reaches the timeout event (0x0), the timer reloads its start value from the GPTMTnILR and the GPTMTnPR registers on the next cycle. When the timer is counting up and it reaches the timeout event (the value in the GPTMTnILR and the optional GPTMTnPR registers), the timer reloads with 0x0. If configured to be a one-shot timer, the timer stops counting and clears the TnEN bit in the GPTMCTL register. If configured as a periodic timer, the timer starts counting again on the next cycle.

In periodic, snap-shot mode (TnMR field is 0x2 and the TnSNAPS bit is set in the GPTMTnMR register), the value of the timer at the time-out event is loaded into the GPTMTnR register and the value of the prescaler is loaded into the GPTMTnPS register. The free-running counter value is shown in the GPTMTnV register and the free-running prescaler value is shown in the GPTMTnPv register. In this manner, software can determine the time elapsed from the interrupt assertion to the ISR entry by examining the snapshot values and the current value of the free-running timer. Snapshot mode is not available when the timer is configured in one-shot mode.

In addition to reloading the count value, the GPTM can generate interrupts, CCP outputs and triggers when it reaches the time-out event. The GPTM sets the TnTORIS bit in the GPTM Raw Interrupt Status (GPTMRIS) register (see page 762), and holds it until it is cleared by writing the GPTM Interrupt Clear (GPTMICR) register (see page 768). If the time-out interrupt is enabled in the GPTM Interrupt Mask (GPTMIMR) register (see page 759), the GPTM also sets the TnTOMIS bit in the GPTM Masked Interrupt Status (GPTMMIS) register (see page 765).

By setting the TnMIE bit in the GPTMTnMR register, an interrupt condition can also be generated when the Timer value equals the value loaded into the GPTM Timer n Match (GPTMTnMATCHR) and GPTM Timer n Prescale Match (GPTMTnPMR) registers. This interrupt has the same status, masking, and clearing functions as the time-out interrupt, but uses the match interrupt bits instead (for example, the raw interrupt status is monitored via TnRIS bit in the GPTM Raw Interrupt Status (GPTMRIS) register). Note that the interrupt status bits are not updated by the hardware unless the TnMIE bit in the GPTMTnMR register is set, which is different than the behavior for the time-out interrupt. The ADC trigger is enabled by setting the TnOTE bit in GPTMCTL. If the ADC trigger is enabled, only a one-shot or periodic time-out event can produce an ADC trigger assertion. The µDMA trigger is enabled by configuring and enabling the appropriate µDMA channel. See “Channel Configuration” on page 599.

If software updates the GPTMTnILR or the GPTMTnPR register while the counter is counting down, the counter loads the new value on the next clock cycle and continues counting from the new value if the TnILD bit in the GPTMTnMR register is clear. If the TnILD bit is set, the counter loads the new value after the next timeout. If software updates the GPTMTnILR or the GPTMTnPR register while the counter is counting up or down, the timeout event is changed on the next cycle to the new value. If software updates the GPTM Timer n Value (GPTMTnV) register while the counter is counting up or down, the counter loads the new value on the next clock cycle and continues counting from the new value. If software updates the GPTMTnMATCHR or the GPTMTnPMR registers, the new values are reflected on the next clock cycle if the TnMRSU bit in the GPTMTnMR register is clear. If the TnMRSU bit is set, the new value will not take effect until the next timeout.

When using a 32/64-bit wide timer block in a 64-bit mode, certain registers must be accessed in the manner described in “Accessing Concatenated 32/64-Bit Wide GPTM Register Values” on page 734.

If the TnSTALL bit in the GPTMCTL register is set and the RTCEN bit is not set in the GPTMCTL register, the timer freezes counting while the processor is halted by the debugger. The timer resumes counting when the processor resumes execution. If the RTCEN bit is set, it prevents the TnSTALL bit from freezing the count when the processor is halted by the debugger.

The following table shows a variety of configurations for a 16-bit free-running timer while using the prescaler. All values assume an 80-MHz clock with Tc=12.5 ns (clock period). The prescaler can
only be used when a 16/32-bit timer is configured in 16-bit mode and when a 32/64-bit timer is configured in 32-bit mode.

Table 11-5. 16-Bit Timer With Prescaler Configurations

<table>
<thead>
<tr>
<th>Prescale (8-bit value)</th>
<th># of Timer Clocks (Tc) (^a)</th>
<th>Max Time</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000000</td>
<td>1</td>
<td>0.8192</td>
<td>ms</td>
</tr>
<tr>
<td>00000001</td>
<td>2</td>
<td>1.6384</td>
<td>ms</td>
</tr>
<tr>
<td>00000010</td>
<td>3</td>
<td>2.4576</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11111101</td>
<td>254</td>
<td>208.0768</td>
<td>ms</td>
</tr>
<tr>
<td>11111110</td>
<td>255</td>
<td>208.896</td>
<td>ms</td>
</tr>
<tr>
<td>11111111</td>
<td>256</td>
<td>209.7152</td>
<td>ms</td>
</tr>
</tbody>
</table>

\(a.\) Tc is the clock period.

The following table shows a variety of configurations for a 32-bit free-running timer using the prescaler while configured in 32/64-bit mode. All values assume an 80-MHz clock with Tc=12.5 ns (clock period).

Table 11-6. 32-Bit Timer (configured in 32/64-bit mode) With Prescaler Configurations

<table>
<thead>
<tr>
<th>Prescale (16-bit value)</th>
<th># of Timer Clocks (Tc) (^a)</th>
<th>Max Time</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000</td>
<td>1</td>
<td>53.687</td>
<td>s</td>
</tr>
<tr>
<td>0x0001</td>
<td>2</td>
<td>107.374</td>
<td>s</td>
</tr>
<tr>
<td>0x0002</td>
<td>3</td>
<td>214.748</td>
<td>s</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xFFFF</td>
<td>65534</td>
<td>0.879</td>
<td>10^6 s</td>
</tr>
<tr>
<td>0xFFFFE</td>
<td>65535</td>
<td>1.759</td>
<td>10^6 s</td>
</tr>
<tr>
<td>0xFFFFFF</td>
<td>65536</td>
<td>3.518</td>
<td>10^6 s</td>
</tr>
</tbody>
</table>

\(a.\) Tc is the clock period.

11.3.2.2 Real-Time Clock Timer Mode

In Real-Time Clock (RTC) mode, the concatenated versions of the Timer A and Timer B registers are configured as an up-counter. When RTC mode is selected for the first time after reset, the counter is loaded with a value of 0x1. All subsequent load values must be written to the GPTM Timer n Interval Load (GPTMTnILR) registers (see page 770). If the GPTMTnILR register is loaded with a new value, the counter begins counting at that value and rolls over at the fixed value of 0xFFFFFFFF. Table 11-7 on page 725 shows the values that are loaded into the timer registers when the timer is enabled.

Table 11-7. Counter Values When the Timer is Enabled in RTC Mode

<table>
<thead>
<tr>
<th>Register</th>
<th>Count Down Mode</th>
<th>Count Up Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPTMTnR</td>
<td>Not available</td>
<td>0x1</td>
</tr>
<tr>
<td>GPTMTnV</td>
<td>Not available</td>
<td>0x1</td>
</tr>
<tr>
<td>GPTMTnPS</td>
<td>Not available</td>
<td>Not available</td>
</tr>
<tr>
<td>GPTMTnPV</td>
<td>Not available</td>
<td>Not available</td>
</tr>
</tbody>
</table>

The input clock on a CCP0 input is required to be 32.768 KHz in RTC mode. The clock signal is then divided down to a 1-Hz rate and is passed along to the input of the counter.
When software writes the \texttt{TAEN} bit in the \texttt{GPTMCTL} register, the counter starts counting up from its preloaded value of 0x1. When the current count value matches the preloaded value in the \texttt{GPTMTnMATCHR} registers, the GPTM asserts the \texttt{RTCRI} bit in \texttt{GPTMRIS} and continues counting until either a hardware reset, or it is disabled by software (clearing the \texttt{TAEN} bit). When the timer value reaches the terminal count, the timer rolls over and continues counting up from 0x0. If the RTC interrupt is enabled in \texttt{GPTMIMR}, the GPTM also sets the \texttt{RTCMI} bit in \texttt{GPTMMIS} and generates a controller interrupt. The status flags are cleared by writing the \texttt{RTCCINT} bit in \texttt{GPTMICR}.

In this mode, the \texttt{GPTMTnR} and \texttt{GPTMTnV} registers always have the same value.

When using a 32/64-bit wide timer block in a RTC mode, certain registers must be accessed in the manner described in “Accessing Concatenated 32/64-Bit Wide GPTM Register Values” on page 734.

The value of the RTC predivider can be read in the \texttt{GPTM RTC Predivide (GPTMRTCPD)} register. To ensure that the RTC value is coherent, software should follow the process detailed in Figure 11-2 on page 726.

**Figure 11-2. Reading the RTC Value**

In addition to generating interrupts, the RTC can generate a \(\mu\)DMA trigger. The \(\mu\)DMA trigger is enabled by configuring and enabling the appropriate \(\mu\)DMA channel. See “Channel Configuration” on page 599.
### 11.3.2.3 Input Edge-Count Mode

**Note:** For rising-edge detection, the input signal must be High for at least two system clock periods following the rising edge. Similarly, for falling-edge detection, the input signal must be Low for at least two system clock periods following the falling edge. Based on this criteria, the maximum input frequency for edge detection is 1/4 of the system frequency.

In Edge-Count mode, the timer is configured as a 24-bit or 48-bit up- or down-counter including the optional prescaler with the upper count value stored in the GPTM Timer n Prescale (GPTMTnPR) register and the lower bits in the GPTMTnR register. In this mode, the timer is capable of capturing three types of events: rising edge, falling edge, or both. To place the timer in Edge-Count mode, the TnCMR bit of the GPTMTnMR register must be cleared. The type of edge that the timer counts is determined by the TnEVENT fields of the GPTMCTL register. During initialization in down-count mode, the GPTMTnMATCHR and GPTMTnPMR registers are configured so that the difference between the value in the GPTMTnILR and GPTMTnPR registers and the GPTMTnMATCHR and GPTMTnPMR registers equals the number of edge events that must be counted. In up-count mode, the timer counts from 0x0 to the value in the GPTMTnMATCHR and GPTMTnPMR registers. Note that when executing an up-count, that the value of GPTMTnPR and GPTMTnILR must be greater than the value of GPTMTnPMR and GPTMTnMATCHR. Table 11-8 on page 727 shows the values that are loaded into the timer registers when the timer is enabled.

**Table 11-8. Counter Values When the Timer is Enabled in Input Edge-Count Mode**

<table>
<thead>
<tr>
<th>Register</th>
<th>Count Down Mode</th>
<th>Count Up Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPTMTnR</td>
<td>GPTMTnPR in combination with GPTMTnILR</td>
<td>0x0</td>
</tr>
<tr>
<td>GPTMTnV</td>
<td>GPTMTnPR in combination with GPTMTnILR</td>
<td>0x0</td>
</tr>
<tr>
<td>GPTMTnPS</td>
<td>GPTMTnPR</td>
<td>0x0</td>
</tr>
<tr>
<td>GPTMTnPv</td>
<td>GPTMTnPR</td>
<td>0x0</td>
</tr>
</tbody>
</table>

When software writes the TnEN bit in the GPTM Control (GPTMCTL) register, the timer is enabled for event capture. Each input event on the CCP pin decrements or increments the counter by 1 until the event count matches GPTMTnMATCHR and GPTMTnPMR. When the counts match, the GPTM asserts the CnMRIS bit in the GPTM Raw Interrupt Status (GPTMRS) register, and holds it until it is cleared by writing the GPTM Interrupt Clear (GPTMICR) register. If the capture mode match interrupt is enabled in the GPTM Interrupt Mask (GPTMMR) register, the GPTM also sets the CnMMIS bit in the GPTM Masked Interrupt Status (GPTMMIS) register. In this mode, the GPTMTnPR and GPTMTnPS registers hold the count of the input events while the GPTMTnV and GPTMTnPv registers hold the free-running timer value and the free-running prescaler value. In up count mode, the current count of input events is held in both the GPTMTnR and GPTMTnV registers.

In addition to generating interrupts, a μDMA trigger can be generated. The μDMA trigger is enabled by configuring and enabling the appropriate μDMA channel. See "Channel Configuration" on page 599.

After the match value is reached in down-count mode, the counter is then reloaded using the value in GPTMTnILR and GPTMTnPR registers, and stopped because the GPTM automatically clears the TnEN bit in the GPTMCTL register. Once the event count has been reached, all further events are ignored until TnEN is re-enabled by software. In up-count mode, the timer is reloaded with 0x0 and continues counting.

Figure 11-3 on page 728 shows how Input Edge-Count mode works. In this case, the timer start value is set to GPTMTnILR = 0x000A and the match value is set to GPTMTnMATCHR = 0x0006 so that four edge events are counted. The counter is configured to detect both edges of the input signal.

Note that the last two edges are not counted because the timer automatically clears the TnEN bit after the current count matches the value in the GPTMTnMATCHR register.
11.3.2.4 Input Edge-Time Mode

Note: For rising-edge detection, the input signal must be High for at least two system clock periods following the rising edge. Similarly, for falling edge detection, the input signal must be Low for at least two system clock periods following the falling edge. Based on this criteria, the maximum input frequency for edge detection is 1/4 of the system frequency.

In Edge-Time mode, the timer is configured as a 24-bit or 48-bit up- or down-counter including the optional prescaler with the upper timer value stored in the GPTMTnPR register and the lower bits in the GPTMTnILR register. In this mode, the timer is initialized to the value loaded in the GPTMTnILR and GPTMTnPR registers when counting down and 0x0 when counting up. The timer is capable of capturing three types of events: rising edge, falling edge, or both. The timer is placed into Edge-Time mode by setting the TnCMR bit in the GPTMTRnMR register, and the type of event that the timer captures is determined by the TnEVENT fields of the GPTMCTL register. Table 11-9 on page 728 shows the values that are loaded into the timer registers when the timer is enabled.

<table>
<thead>
<tr>
<th>Register</th>
<th>Count Down Mode</th>
<th>Count Up Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>TnR</td>
<td>GPTMTnILR</td>
<td>0x0</td>
</tr>
<tr>
<td>TnV</td>
<td>GPTMTnILR</td>
<td>0x0</td>
</tr>
<tr>
<td>TnPS</td>
<td>GPTMTnPR</td>
<td>0x0</td>
</tr>
<tr>
<td>TnPv</td>
<td>GPTMTnPR</td>
<td>0x0</td>
</tr>
</tbody>
</table>

When software writes the TnEN bit in the GPTMCTL register, the timer is enabled for event capture. When the selected input event is detected, the current timer counter value is captured in the GPTMTnR and GPTMTnPS register and is available to be read by the microcontroller. The GPTM then asserts the CnERIS bit in the GPTM Raw Interrupt Status (GPTMRIS) register, and holds it until it is cleared by writing the GPTM Interrupt Clear (GPTMICR) register. If the capture mode event interrupt is enabled in the GPTM Interrupt Mask (GPTMIMR) register, the GPTM also sets the CnEMIS bit in the GPTM Masked Interrupt Status (GPTMMIS) register. In this mode, the
GPTMTnR and GPTMTnPS registers hold the time at which the selected input event occurred while the GPTMTnV and GPTMTnPV registers hold the free-running timer value and the free-running prescaler value. These registers can be read to determine the time that elapsed between the interrupt assertion and the entry into the ISR.

In addition to generating interrupts, a μDMA trigger can be generated. The μDMA trigger is enabled by configuring the appropriate μDMA channel. See “Channel Configuration” on page 599.

After an event has been captured, the timer does not stop counting. It continues to count until the TnEN bit is cleared. When the timer reaches the timeout value, it is reloaded with 0x0 in up-count mode and the value from the GPTMTnILR and GPTMTnPR registers in down-count mode.

Figure 11-4 on page 729 shows how input edge timing mode works. In the diagram, it is assumed that the start value of the timer is the default value of 0xFFFF, and the timer is configured to capture rising edge events.

Each time a rising edge event is detected, the current count value is loaded into the GPTMTnR and GPTMTnPS registers, and is held there until another rising edge is detected (at which point the new count value is loaded into the GPTMTnR and GPTMTnPS registers).

**Figure 11-4. 16-Bit Input Edge-Time Mode Example**

**Note:** When operating in Edge-time mode, the counter uses a modulo $2^{24}$ count if prescaler is enabled or $2^{16}$, if not. If there is a possibility the edge could take longer than the count, then another timer configured in periodic-timer mode can be implemented to ensure detection of the missed edge. The periodic timer should be configured in such a way that:

- The periodic timer cycles at the same rate as the edge-time timer.
- The periodic timer interrupt has a higher interrupt priority than the edge-time timeout interrupt.
- If the periodic timer interrupt service routine is entered, software must check if an edge-time interrupt is pending and if it is, the value of the counter must be subtracted by 1 before being used to calculate the snapshot time of the event.
11.3.2.5 PWM Mode

The GPTM supports a simple PWM generation mode. In PWM mode, the timer is configured as a 24-bit or 48-bit down-counter with a start value (and thus period) defined by the GPTMTnILR and GPTMTnPR registers. In this mode, the PWM frequency and period are synchronous events and therefore guaranteed to be glitch free. PWM mode is enabled with the GPTMTnMR register by setting the TnAMS bit to 0x1, the TnCMR bit to 0x0, and the TnMR field to 0x2. Table 11-10 on page 730 shows the values that are loaded into the timer registers when the timer is enabled.

Table 11-10. Counter Values When the Timer is Enabled in PWM Mode

<table>
<thead>
<tr>
<th>Register</th>
<th>Count Down Mode</th>
<th>Count Up Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPTMTnR</td>
<td>GPTMTnILR</td>
<td>Not available</td>
</tr>
<tr>
<td>GPTMTnV</td>
<td>GPTMTnILR</td>
<td>Not available</td>
</tr>
<tr>
<td>GPTMTnP</td>
<td>GPTMTnPR</td>
<td>Not available</td>
</tr>
<tr>
<td>GPTMTnP</td>
<td>GPTMTnPR</td>
<td>Not available</td>
</tr>
</tbody>
</table>

When software writes the TnEN bit in the GPTMCTL register, the counter begins counting down until it reaches the 0x0 state. Alternatively, if the TnWOT bit is set in the GPTMTnMR register, once the TnEN bit is set, the timer waits for a trigger to begin counting (see “Wait-for-Trigger Mode” on page 732). On the next counter cycle in periodic mode, the counter reloads its start value from the GPTMTnILR and GPTMTnPR registers and continues counting until disabled by software clearing the TnEN bit in the GPTMCTL register. The timer is capable of generating interrupts based on three types of events: rising edge, falling edge, or both. The event is configured by the TnEVENT field of the GPTMCTL register, and the interrupt is enabled by setting the TnPWMIE bit in the GPTMTnMR register. When the event occurs, the CnERIS bit is set in the GPTM Raw Interrupt Status (GPTMRIS) register, and holds it until it is cleared by writing the GPTM Interrupt Clear (GPTMIMR) register. If the capture mode event interrupt is enabled in the GPTM Interrupt Mask (GPTMMIS) register, the GPTM also sets the CnEMIS bit in the GPTM Masked Interrupt Status (GPTMMIS) register. Note that the interrupt status bits are not updated unless the TnPWMIE bit is set.

In this mode, the GPTMTnR and GPTMTnV registers always have the same value, as do the GPTMPnPS and the GPTMTnPV registers.

The output PWM signal asserts when the counter is at the value of the GPTMTnILR and GPTMTnPR registers (its start state), and is deasserted when the counter value equals the value in the GPTMTnMATCHR and GPTMTnPMR registers. Software has the capability of inverting the output PWM signal by setting the TnPWML bit in the GPTMCTL register.

**Note:** If PWM output inversion is enabled, edge detection interrupt behavior is reversed. Thus, if a positive-edge interrupt trigger has been set and the PWM inversion generates a positive edge, no event-trigger interrupt asserts. Instead, the interrupt is generated on the negative edge of the PWM signal.

Figure 11-5 on page 731 shows how to generate an output PWM with a 1-ms period and a 66% duty cycle assuming a 50-MHz input clock and TnPWML =0 (duty cycle would be 33% for the TnPWML =1 configuration). For this example, the start value is GPTMTnILR=0xC350 and the match value is GPTMTnMATCHR=0x411A.
When synchronizing the timers using the `GPTMSYNC` register, the timer must be properly configured to avoid glitches on the CCP outputs. Both the `TnPLO` and the `TnMRSU` bits must be set in the `GPTMTnMR` register. Figure 11-6 on page 731 shows how the CCP output operates when the `TnPLO` and `TnMRSU` bits are set and the `GPTMTnMATCHR` value is greater than the `GPTMTnILR` value.

Figure 11-7 on page 732 shows how the CCP output operates when the `PLO` and `MRSU` bits are set and the `GPTMTnMATCHR` value is the same as the `GPTMTnILR` value. In this situation, if the `PLO` bit is 0, the CCP signal goes high when the `GPTMTnILR` value is loaded and the match would be essentially ignored.
11.3.3 Wait-for-Trigger Mode

The Wait-for-Trigger mode allows daisy chaining of the timer modules such that once configured, a single timer can initiate multiple timing events using the Timer triggers. Wait-for-Trigger mode is enabled by setting the TnWOT bit in the GPTMnMR register. When the TnWOT bit is set, Timer N+1 does not begin counting until the timer in the previous position in the daisy chain (Timer N) reaches its time-out event. The daisy chain is configured such that GPTM1 always follows GPTM0, GPTM2 follows GPTM1, and so on. If Timer A is configured as a 32-bit (16/32-bit mode) or 64-bit (32/64-bit wide mode) timer (controlled by the GPTMCFG field in the GPTMCFG register), it triggers Timer A in the next module. If Timer A is configured as a 16-bit (16/32-bit mode) or 32-bit (32/64-bit wide mode) timer, it triggers Timer B in the same module, and Timer B triggers Timer A in the next module. Care must be taken that the TAWOT bit is never set in GPTM0. Figure 11-9 on page 733 shows how the GPTMCFG bit affects the daisy chain. This function is valid for one-shot, periodic, and PWM modes.
11.3.4 Synchronizing GP Timer Blocks

The GPTM Synchronizer Control (GPTMSYNC) register in the GPTM0 block can be used to synchronize selected timers to begin counting at the same time. Setting a bit in the GPTMSYNC register causes the associated timer to perform the actions of a timeout event. An interrupt is not generated when the timers are synchronized. If a timer is being used in concatenated mode, only the bit for Timer A must be set in the GPTMSYNC register.

Note: All timers must use the same clock source for this feature to work correctly.

Table 11-11 on page 733 shows the actions for the timeout event performed when the timers are synchronized in the various timer modes.

Table 11-11. Timeout Actions for GPTM Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Count Dir</th>
<th>Time Out Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>32- and 64-bit One-Shot (concatenated timers)</td>
<td>—</td>
<td>N/A</td>
</tr>
<tr>
<td>32- and 64-bit Periodic (concatenated timers)</td>
<td>Down</td>
<td>Count value = ILR</td>
</tr>
<tr>
<td></td>
<td>Up</td>
<td>Count value = 0</td>
</tr>
<tr>
<td>32- and 64-bit RTC (concatenated timers)</td>
<td>Up</td>
<td>Count value = 0</td>
</tr>
<tr>
<td>16- and 32-bit One Shot (individual/split timers)</td>
<td>—</td>
<td>N/A</td>
</tr>
<tr>
<td>16- and 32-bit Periodic (individual/split timers)</td>
<td>Down</td>
<td>Count value = ILR</td>
</tr>
<tr>
<td></td>
<td>Up</td>
<td>Count value = 0</td>
</tr>
<tr>
<td>16- and 32-bit Edge-Count (individual/split timers)</td>
<td>Down</td>
<td>Count value = ILR</td>
</tr>
<tr>
<td></td>
<td>Up</td>
<td>Count value = 0</td>
</tr>
<tr>
<td>16- and 32-bit Edge-Time (individual/split timers)</td>
<td>Down</td>
<td>Count value = ILR</td>
</tr>
<tr>
<td></td>
<td>Up</td>
<td>Count value = 0</td>
</tr>
<tr>
<td>16- and 32-bit PWM</td>
<td>Down</td>
<td>Count value = ILR</td>
</tr>
</tbody>
</table>
11.3.5 DMA Operation

The timers each have a dedicated μDMA channel and can provide a request signal to the μDMA controller. The request is a burst type and occurs whenever a timer raw interrupt condition occurs. The arbitration size of the μDMA transfer should be set to the amount of data that should be transferred whenever a timer event occurs.

For example, to transfer 256 items, 8 items at a time every 10 ms, configure a timer to generate a periodic timeout at 10 ms. Configure the μDMA transfer for a total of 256 items, with a burst size of 8 items. Each time the timer times out, the μDMA controller transfers 8 items, until all 256 items have been transferred.

No other special steps are needed to enable Timers for μDMA operation. Refer to "Micro Direct Memory Access (μDMA)" on page 595 for more details about programming the μDMA controller.

11.3.6 Accessing Concatenated 16/32-Bit GPTM Register Values

The GPTM is placed into concatenated mode by writing a 0x0 or a 0x1 to the GPTMCFG bit field in the GPTM Configuration (GPTMCFG) register. In both configurations, certain 16/32-bit GPTM registers are concatenated to form pseudo 32-bit registers. These registers include:

- GPTM Timer A Interval Load (GPTMTAILR) register [15:0], see page 770
- GPTM Timer B Interval Load (GPTMTBILR) register [15:0], see page 771
- GPTM Timer A (GPTMTAR) register [15:0], see page 778
- GPTM Timer B (GPTMTBR) register [15:0], see page 779
- GPTM Timer A Value (GPTMTAV) register [15:0], see page 780
- GPTM Timer B Value (GPTMTBV) register [15:0], see page 781
- GPTM Timer A Match (GPTMTAMATCHR) register [15:0], see page 772
- GPTM Timer B Match (GPTMTBMATCHR) register [15:0], see page 773

In the 32-bit modes, the GPTM translates a 32-bit write access to GPTMTAILR into a write access to both GPTMTAILR and GPTMTBILR. The resulting word ordering for such a write operation is:

GPTMTBILR[15:0]:GPTMTAILR[15:0]

Likewise, a 32-bit read access to GPTMTAR returns the value:

GPTMTBR[15:0]:GPTMTAR[15:0]

A 32-bit read access to GPTMTAV returns the value:

GPTMTBV[15:0]:GPTMTAV[15:0]

11.3.7 Accessing Concatenated 32/64-Bit Wide GPTM Register Values

On the 32/64-bit wide GPTM blocks, concatenated register values (64-bits and 48-bits) are not readily available as the bit width for these accesses is greater than the bus width of the processor core. In the concatenated timer modes and the individual timer modes when using the prescaler, software must perform atomic accesses for the value to be coherent. When reading timer values that are greater than 32 bits, software should follow these steps:
1. Read the appropriate Timer B register or prescaler register.
2. Read the corresponding Timer A register.
3. Re-read the Timer B register or prescaler register.
4. Compare the Timer B or prescaler values from the first and second reads. If they are the same, the timer value is coherent. If they are not the same, repeat steps 1-4 once more so that they are the same.

The following pseudo code illustrates this process:

```c
high = timer_high;
low = timer_low;
if (high != timer_high);  //low overflowed into high
{
    high = timer_high;
    low = timer_low;
}
```

The registers that must be read in this manner are shown below:

- **64-bit reads**
  - GPTMTAV and GPTMTBV
  - GPTMTAR and GPTMTBR

- **48-bit reads**
  - GPTMTAR and GPTMTAPS
  - GPTMTBR and GPTMTBPS
  - GPTMTAV and GPTMTAPV
  - GPTMTBV and GPTMTBPV

Similarly, write accesses must also be performed by writing the upper bits prior to writing the lower bits as follows:

1. Write the appropriate Timer B register or prescaler register.
2. Write the corresponding Timer A register.

The registers that must be written in this manner are shown below:

- **64-bit writes**
  - GPTMTAV and GPTMTBV
- \text{GPTMTAMATCHR} \text{ and GPTMTBMATCHR}
- \text{GPTMTAILR} \text{ and GPTMTBLIR}

\text{48-bit writes}
- \text{GPTMTAV} \text{ and GPTMTAPV}
- \text{GPTMTBV} \text{ and GPTMTBPV}
- \text{GPTMTAMATCHR} \text{ and GPTMTAPMR}
- \text{GPTMTBMATCHR} \text{ and GPTMTBPMR}
- \text{GPTMTAILR} \text{ and GPTMTAPR}
- \text{GPTMTBILR} \text{ and GPTMTBPR}

When writing a 64-bit value, if there are two consecutive writes to any of the registers listed above under the "48-bit writes" heading, whether the register is in Timer A or Timer B, or if a register Timer A is written prior to writing the corresponding register in Timer B, then an error is reported using the \text{WUERIS} bit in the \text{GPTMRIS} register. This error can be promoted to interrupt if it is not masked. Note that this error is not reported for the prescaler registers because use of the prescaler is optional. As a result, programmers must take care to follow the protocol outlined above.

### 11.4 Initialization and Configuration

To use a GPTM, the appropriate \text{TIMEn} bit must be set in the \text{RCGCTIMER} or \text{RCGCWTIMER} register (see page 340 and page 360). If using any CCP pins, the clock to the appropriate GPIO module must be enabled via the \text{RCGGCGPIO} register (see page 342). To find out which GPIO port to enable, refer to Table 23-4 on page 1377. Configure the \text{PMCn} fields in the \text{GPIOPCTL} register to assign the CCP signals to the appropriate pins (see page 702 and Table 23-5 on page 1386).

This section shows module initialization and configuration examples for each of the supported timer modes.

#### 11.4.1 One-Shot/Periodic Timer Mode

The GPTM is configured for One-Shot and Periodic modes by the following sequence:

1. Ensure the timer is disabled (the \text{TnEN} bit in the \text{GPTMCTL} register is cleared) before making any changes.

2. Write the \text{GPTM Configuration Register} (\text{GPTMCFG}) with a value of 0x0000.0000.

3. Configure the \text{TnMR} field in the \text{GPTM Timer n Mode Register} (\text{GPTMTnMR}):
   a. Write a value of 0x1 for One-Shot mode.
   b. Write a value of 0x2 for Periodic mode.

4. Optionally configure the \text{TnSNAPS}, \text{TnWOT}, \text{TnMTE}, and \text{TnCDIR} bits in the \text{GPTMTnMR} register to select whether to capture the value of the free-running timer at time-out, use an external trigger to start counting, configure an additional trigger or interrupt, and count up or down.

5. Load the start value into the \text{GPTM Timer n Interval Load Register} (\text{GPTMTnILR}).
6. If interrupts are required, set the appropriate bits in the GPTM Interrupt Mask Register (GPTMIMR).

7. Set the TnEN bit in the GPTMCTL register to enable the timer and start counting.

8. Poll the GPTMRIS register or wait for the interrupt to be generated (if enabled). In both cases, the status flags are cleared by writing a 1 to the appropriate bit of the GPTM Interrupt Clear Register (GPTMICR).

If the TnMIE bit in the GPTMTnMR register is set, the RTCRIS bit in the GPTMRIS register is set, and the timer continues counting. In One-Shot mode, the timer stops counting after the time-out event. To re-enable the timer, repeat the sequence. A timer configured in Periodic mode reloads the timer and continues counting after the time-out event.

11.4.2 Real-Time Clock (RTC) Mode

To use the RTC mode, the timer must have a 32.768-KHz input signal on an even CCP input. To enable the RTC feature, follow these steps:

1. Ensure the timer is disabled (the TAEN bit is cleared) before making any changes.

2. If the timer has been operating in a different mode prior to this, clear any residual set bits in the GPTM Timer n Mode (GPTMTnMR) register before reconfiguring.

3. Write the GPTM Configuration Register (GPTMCFG) with a value of 0x0000.0001.

4. Write the match value to the GPTM Timer n Match Register (GPTMTnMATCHR).

5. Set/clear the RTCEN and TnSTALL bit in the GPTM Control Register (GPTMCTL) as needed.

6. If interrupts are required, set the RTCIM bit in the GPTM Interrupt Mask Register (GPTMIMR).

7. Set the TAEN bit in the GPTMCTL register to enable the timer and start counting.

When the timer count equals the value in the GPTMTnMATCHR register, the GPTM asserts the RTCRIS bit in the GPTMRIS register and continues counting until Timer A is disabled or a hardware reset. The interrupt is cleared by writing the RTCCINT bit in the GPTMICR register. Note that if the GPTMTnILR register is loaded with a new value, the timer begins counting at this new value and continues until it reaches 0xFFFF.FFFF, at which point it rolls over.

11.4.3 Input Edge-Count Mode

A timer is configured to Input Edge-Count mode by the following sequence:

1. Ensure the timer is disabled (the TnEN bit is cleared) before making any changes.

2. Write the GPTM Configuration (GPTMCFG) register with a value of 0x0000.0004.

3. In the GPTM Timer Mode (GPTMTnMR) register, write the TnCMR field to 0x0 and the TnMR field to 0x3.

4. Configure the type of event(s) that the timer captures by writing the TnEVENT field of the GPTM Control (GPTMCTL) register.

5. Program registers according to count direction:
■ In down-count mode, the GPTMTnMATCHR and GPTMTnPMR registers are configured so that the difference between the value in the GPTMTnILR and GPTMTnPR registers and the GPTMTnMATCHR and GPTMTnPMR registers equals the number of edge events that must be counted.

■ In up-count mode, the timer counts from 0x0 to the value in the GPTMTnMATCHR and GPTMTnPMR registers. Note that when executing an up-count, the value of the GPTMTnPR and GPTMTnILR must be greater than the value of GPTMTnPMR and GPTMTnMATCHR.

6. If interrupts are required, set the CnMIM bit in the GPTM Interrupt Mask (GPTMIMR) register.

7. Set the TnEN bit in the GPTMCTL register to enable the timer and begin waiting for edge events.

8. Poll the CnMRIS bit in the GPTMRIS register or wait for the interrupt to be generated (if enabled). In both cases, the status flags are cleared by writing a 1 to the CnMCINT bit of the GPTM Interrupt Clear (GPTMICR) register.

When counting down in Input Edge-Count Mode, the timer stops after the programmed number of edge events has been detected. To re-enable the timer, ensure that the TnEN bit is cleared and repeat steps 4 through 8.

11.4.4 Input Edge Time Mode
A timer is configured to Input Edge Time mode by the following sequence:

1. Ensure the timer is disabled (the TnEN bit is cleared) before making any changes.

2. Write the GPTM Configuration (GPTMCFG) register with a value of 0x0000.0004.

3. In the GPTM Timer Mode (GPTMnMR) register, write the TnCMR field to 0x1 and the TnMR field to 0x3 and select a count direction by programming the TnCDIR bit.

4. Configure the type of event that the timer captures by writing the TnEVENT field of the GPTM Control (GPTMCTL) register.

5. If a prescaler is to be used, write the prescale value to the GPTM Timer n Prescale Register (GPTMTnPR).

6. Load the timer start value into the GPTM Timer n Interval Load (GPTMTnILR) register.

7. If interrupts are required, set the CnEIM bit in the GPTM Interrupt Mask (GPTMIMR) register.

8. Set the TnEN bit in the GPTM Control (GPTMCTL) register to enable the timer and start counting.

9. Poll the CnERIS bit in the GPTMRIS register or wait for the interrupt to be generated (if enabled). In both cases, the status flags are cleared by writing a 1 to the CnECINT bit of the GPTM Interrupt Clear (GPTMICR) register. The time at which the event happened can be obtained by reading the GPTM Timer n (GPTMnR) register.

In Input Edge Timing mode, the timer continues running after an edge event has been detected, but the timer interval can be changed at any time by writing the GPTMTnILR register and clearing the TnILD bit in the GPTMnMR register. The change takes effect at the next cycle after the write.

11.4.5 PWM Mode
A timer is configured to PWM mode using the following sequence:
1. Ensure the timer is disabled (the TnEN bit is cleared) before making any changes.

2. Write the GPTM Configuration (GPTMCFG) register with a value of 0x0000.0004.

3. In the GPTM Timer Mode (GPTMTnMR) register, set the TnAMS bit to 0x1, the TnCMR bit to 0x0, and the TnMR field to 0x2.

4. Configure the output state of the PWM signal (whether or not it is inverted) in the TnPWML field of the GPTM Control (GPTMCTL) register.

5. If a prescaler is to be used, write the prescale value to the GPTM Timer n Prescale Register (GPTMTnPR).

6. If PWM interrupts are used, configure the interrupt condition in the TnEVENT field in the GPTMCTL register and enable the interrupts by setting the TnPWMIE bit in the GPTMTnMR register. Note that edge detect interrupt behavior is reversed when the PWM output is inverted (see page 751).

7. Load the timer start value into the GPTM Timer n Interval Load (GPTMTnILR) register.

8. Load the GPTM Timer n Match (GPTMTnMATCHR) register with the match value.

9. Set the TnEN bit in the GPTM Control (GPTMCTL) register to enable the timer and begin generation of the output PWM signal.

In PWM Time mode, the timer continues running after the PWM signal has been generated. The PWM period can be adjusted at any time by writing the GPTMTnILR register, and the change takes effect at the next cycle after the write.

11.5 Register Map

Table 11-12 on page 740 lists the GPTM registers. The offset listed is a hexadecimal increment to the register's address, relative to that timer's base address:

- 16/32-bit Timer 0: 0x4003.0000
- 16/32-bit Timer 1: 0x4003.1000
- 16/32-bit Timer 2: 0x4003.2000
- 16/32-bit Timer 3: 0x4003.3000
- 16/32-bit Timer 4: 0x4003.4000
- 16/32-bit Timer 5: 0x4003.5000
- 32/64-bit Wide Timer 0: 0x4003.6000
- 32/64-bit Wide Timer 1: 0x4003.7000
- 32/64-bit Wide Timer 2: 0x4004.C000
- 32/64-bit Wide Timer 3: 0x4004.D000
- 32/64-bit Wide Timer 4: 0x4004.E000
- 32/64-bit Wide Timer 5: 0x4004.F000

The SIZE field in the GPTM Peripheral Properties (GPTMPP) register identifies whether a module has a 16/32-bit or 32/64-bit wide timer.

Note that the GP Timer module clock must be enabled before the registers can be programmed (see page 340 or page 360). There must be a delay of 3 system clocks after the Timer module clock is enabled before any Timer module registers are accessed.
Table 11-12. Timers Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>GPTMCFG</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM Configuration</td>
<td>741</td>
</tr>
<tr>
<td>0x004</td>
<td>GPTMTAMR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM Timer A Mode</td>
<td>743</td>
</tr>
<tr>
<td>0x008</td>
<td>GPTMTBMR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM Timer B Mode</td>
<td>747</td>
</tr>
<tr>
<td>0x00C</td>
<td>GPTMCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM Control</td>
<td>751</td>
</tr>
<tr>
<td>0x010</td>
<td>GPTMSYNC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM Synchronize</td>
<td>755</td>
</tr>
<tr>
<td>0x018</td>
<td>GPTMIMR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM Interrupt Mask</td>
<td>759</td>
</tr>
<tr>
<td>0x01C</td>
<td>GPTMRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPTM Raw Interrupt Status</td>
<td>762</td>
</tr>
<tr>
<td>0x020</td>
<td>GPTMIMIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPTM Masked Interrupt Status</td>
<td>765</td>
</tr>
<tr>
<td>0x024</td>
<td>GPTMICR</td>
<td>W1C</td>
<td>0x0000.0000</td>
<td>GPTM Interrupt Clear</td>
<td>768</td>
</tr>
<tr>
<td>0x028</td>
<td>GPTMTAILR</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>GPTM Timer A Interval Load</td>
<td>770</td>
</tr>
<tr>
<td>0x02C</td>
<td>GPTMTBILR</td>
<td>RW</td>
<td>-</td>
<td>GPTM Timer B Interval Load</td>
<td>771</td>
</tr>
<tr>
<td>0x030</td>
<td>GPTMTAMATCHR</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>GPTM Timer A Match</td>
<td>772</td>
</tr>
<tr>
<td>0x034</td>
<td>GPTMTRBMATCHR</td>
<td>RW</td>
<td>-</td>
<td>GPTM Timer B Match</td>
<td>773</td>
</tr>
<tr>
<td>0x038</td>
<td>GPTMTAPR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM Timer A Prescale</td>
<td>774</td>
</tr>
<tr>
<td>0x03C</td>
<td>GPTMTPR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM Timer B Prescale</td>
<td>775</td>
</tr>
<tr>
<td>0x040</td>
<td>GPTMTAPMR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM TimerA Prescale Match</td>
<td>776</td>
</tr>
<tr>
<td>0x044</td>
<td>GPTMTBPMR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>GPTM TimerB Prescale Match</td>
<td>777</td>
</tr>
<tr>
<td>0x048</td>
<td>GPTMTAR</td>
<td>RO</td>
<td>0xFFFF.FFFF</td>
<td>GPTM Timer A</td>
<td>778</td>
</tr>
<tr>
<td>0x04C</td>
<td>GPTMTBR</td>
<td>RO</td>
<td>-</td>
<td>GPTM Timer B</td>
<td>779</td>
</tr>
<tr>
<td>0x050</td>
<td>GPTMTAV</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>GPTM Timer A Value</td>
<td>780</td>
</tr>
<tr>
<td>0x054</td>
<td>GPTMTBV</td>
<td>RW</td>
<td>-</td>
<td>GPTM Timer B Value</td>
<td>781</td>
</tr>
<tr>
<td>0x058</td>
<td>GPTMRTCPSD</td>
<td>RO</td>
<td>0x0000.7FFF</td>
<td>GPTM RTC Predivide</td>
<td>782</td>
</tr>
<tr>
<td>0x05C</td>
<td>GPTMTAPS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPTM Timer A Prescale Snapshot</td>
<td>783</td>
</tr>
<tr>
<td>0x060</td>
<td>GPTMTBPS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPTM Timer B Prescale Snapshot</td>
<td>784</td>
</tr>
<tr>
<td>0x064</td>
<td>GPTMTAPV</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPTM Timer A Prescale Value</td>
<td>785</td>
</tr>
<tr>
<td>0x068</td>
<td>GPTMTBV</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPTM Timer B Prescale Value</td>
<td>786</td>
</tr>
<tr>
<td>0xFC0</td>
<td>GPTMPP</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>GPTM Peripheral Properties</td>
<td>787</td>
</tr>
</tbody>
</table>

11.6 Register Descriptions

The remainder of this section lists and describes the GPTM registers, in numerical order by address offset.
Register 1: GPTM Configuration (GPTMCFG), offset 0x000

This register configures the global operation of the GPTM module. The value written to this register determines whether the GPTM is in 32- or 64-bit mode (concatenated timers) or in 16- or 32-bit mode (individual, split timers).

**Important:** Bits in this register should only be changed when the \textit{TAEN} and \textit{TBEN} bits in the \textit{GPTMCTL} register are cleared.

GPTM Configuration (GPTMCFG)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Type** RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
## GPTM Configuration

The `GPTMCFG` values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>For a 16/32-bit timer, this value selects the 32-bit timer configuration. For a 32/64-bit wide timer, this value selects the 64-bit timer configuration.</td>
</tr>
<tr>
<td>0x1</td>
<td>For a 16/32-bit timer, this value selects the 32-bit real-time clock (RTC) counter configuration. For a 32/64-bit wide timer, this value selects the 64-bit real-time clock (RTC) counter configuration.</td>
</tr>
<tr>
<td>0x2-0x3</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x4</td>
<td>For a 16/32-bit timer, this value selects the 16-bit timer configuration. For a 32/64-bit wide timer, this value selects the 32-bit timer configuration. The function is controlled by bits 1:0 of <code>GPTMTAMR</code> and <code>GPTMTBMR</code>.</td>
</tr>
<tr>
<td>0x5-0x7</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

### Bit/Field Table

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>GPTMCFG</td>
<td>RW</td>
<td>0x0</td>
<td>Description</td>
</tr>
</tbody>
</table>

The `GPTMCFG` values are defined as follows:

- **Value**: Description
- **0x0**: For a 16/32-bit timer, this value selects the 32-bit timer configuration. For a 32/64-bit wide timer, this value selects the 64-bit timer configuration.
- **0x1**: For a 16/32-bit timer, this value selects the 32-bit real-time clock (RTC) counter configuration. For a 32/64-bit wide timer, this value selects the 64-bit real-time clock (RTC) counter configuration.
- **0x2-0x3**: Reserved
- **0x4**: For a 16/32-bit timer, this value selects the 16-bit timer configuration. For a 32/64-bit wide timer, this value selects the 32-bit timer configuration. The function is controlled by bits 1:0 of `GPTMTAMR` and `GPTMTBMR`.
- **0x5-0x7**: Reserved
Register 2: GPTM Timer A Mode (GPTMTAMR), offset 0x004

This register configures the GPTM based on the configuration selected in the GPTMCFG register. When in PWM mode, set the TAAMS bit, clear the TACMR bit, and configure the TAMR field to 0x1 or 0x2.

This register controls the modes for Timer A when it is used individually. When Timer A and Timer B are concatenated, this register controls the modes for both Timer A and Timer B, and the contents of GPTMTBMR are ignored.

**Important:** Bits in this register should only be changed when the TAEN bit in the GPTMCTL register is cleared.

---

GPTM Timer A Mode (GPTMTAMR)

<table>
<thead>
<tr>
<th>16/32-bit Timer 0 base: 0x4003.0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>16/32-bit Timer 1 base: 0x4003.1000</td>
</tr>
<tr>
<td>16/32-bit Timer 2 base: 0x4003.2000</td>
</tr>
<tr>
<td>16/32-bit Timer 3 base: 0x4003.3000</td>
</tr>
<tr>
<td>16/32-bit Timer 4 base: 0x4003.4000</td>
</tr>
<tr>
<td>16/32-bit Timer 5 base: 0x4003.5000</td>
</tr>
<tr>
<td>32/64-bit Wide Timer 0 base: 0x4003.6000</td>
</tr>
<tr>
<td>32/64-bit Wide Timer 1 base: 0x4003.7000</td>
</tr>
<tr>
<td>32/64-bit Wide Timer 2 base: 0x4004.C000</td>
</tr>
<tr>
<td>32/64-bit Wide Timer 3 base: 0x4004.D000</td>
</tr>
<tr>
<td>32/64-bit Wide Timer 4 base: 0x4004.E000</td>
</tr>
<tr>
<td>32/64-bit Wide Timer 5 base: 0x4004.F000</td>
</tr>
</tbody>
</table>

Offset 0x004
Type RW, reset 0x0000.0000

---

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>TAPLO</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A PWM Legacy Operation</td>
</tr>
</tbody>
</table>

Value Description

0 Legacy operation with CCP pin driven Low when the GPTMTAILR is reloaded after the timer reaches 0.

1 CCP is driven High when the GPTMTAILR is reloaded after the timer reaches 0.

This bit is only valid in PWM mode.
**GPTM Timer A Match Register Update**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>TAMRSU</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Match Register Update</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Update the GPTMTAMATCHR register and the GPTMTAPR register, if used, on the next cycle.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Update the GPTMTAMATCHR register and the GPTMTAPR register, if used, on the next timeout.</td>
</tr>
</tbody>
</table>

If the timer is disabled (TAEN is clear) when this bit is set, GPTMTAMATCHR and GPTMTAPR are updated when the timer is enabled. If the timer is stalled (TASTALL is set), GPTMTAMATCHR and GPTMTAPR are updated according to the configuration of this bit.

**GPTM Timer A PWM Interrupt Enable**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>TAPWMIE</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A PWM Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Capture event interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Capture event interrupt is enabled.</td>
</tr>
</tbody>
</table>

This bit is only valid in PWM mode.

**GPTM Timer A Interval Load Write**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>TAILD</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Interval Load Write</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Update the GPTMTAR and GPTMTAV registers with the value in the GPTMTAILR register on the next cycle. Also update the GPTMTAPS and GPTMTAPV registers with the value in the GPTMTAPR register on the next cycle.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Update the GPTMTAR and GPTMTAV registers with the value in the GPTMTAILR register on the next timeout. Also update the GPTMTAPS and GPTMTAPV registers with the value in the GPTMTAPR register on the next timeout.</td>
</tr>
</tbody>
</table>

Note the state of this bit has no effect when counting up.

The bit descriptions above apply if the timer is enabled and running. If the timer is disabled (TAEN is clear) when this bit is set, GPTMTAR, GPTMTAV, GPTMTAPS, and GPTMTAPV are updated when the timer is enabled. If the timer is stalled (TASTALL is set), GPTMTAR and GPTMTAPS are updated according to the configuration of this bit.

**GPTM Timer A Snap-Shot Mode**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>TASNAPS</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Snap-Shot Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Snap-shot mode is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 If Timer A is configured in the periodic mode, the actual free-running, capture or snapshot value of Timer A is loaded at the time-out event/capture or snapshot event into the GPTM Timer A (GPTMTAR) register. If the timer prescaler is used, the prescaler snapshot is loaded into the GPTM Timer A (GPTMTAPR).</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>---------------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>6</td>
<td>TAWOT</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Wait-on-Trigger</td>
</tr>
<tr>
<td>5</td>
<td>TAMIE</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Match Interrupt Enable</td>
</tr>
<tr>
<td>4</td>
<td>TACDIR</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Count Direction</td>
</tr>
<tr>
<td>3</td>
<td>TAAMS</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Alternate Mode Select</td>
</tr>
<tr>
<td>2</td>
<td>TACMR</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Capture Mode</td>
</tr>
</tbody>
</table>

**Value | Description**
--- | ---
0 | Timer A begins counting as soon as it is enabled.
1 | If Timer A is enabled (TAEN is set in the GPTMCTL register), Timer A does not begin counting until it receives a trigger from the timer in the previous position in the daisy chain, see Figure 11-9 on page 733. This function is valid for one-shot, periodic, and PWM modes.

This bit must be clear for GP Timer Module 0, Timer A.

**Value | Description**
--- | ---
0 | The match interrupt is disabled for match events.
1 | An interrupt is generated when the match value in the GPTMTAMATCHR register is reached in the one-shot and periodic modes.

**Value | Description**
--- | ---
0 | The timer counts down.
1 | The timer counts up. When counting up, the timer starts from a value of 0x0.

When in PWM or RTC mode, the status of this bit is ignored. PWM mode always counts down and RTC mode always counts up.

**Value | Description**
--- | ---
0 | Capture or compare mode is enabled.
1 | PWM mode is enabled.

**Note:** To enable PWM mode, you must also clear the TACMR bit and configure the TAMR field to 0x1 or 0x2.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>TAMR</td>
<td>RW</td>
<td>0x0</td>
<td>GPTM Timer A Mode</td>
</tr>
</tbody>
</table>

The TAMR values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x1</td>
<td>One-Shot Timer mode</td>
</tr>
<tr>
<td>0x2</td>
<td>Periodic Timer mode</td>
</tr>
<tr>
<td>0x3</td>
<td>Capture mode</td>
</tr>
</tbody>
</table>

The Timer mode is based on the timer configuration defined by bits 2:0 in the GPTMCFG register.
Register 3: GPTM Timer B Mode (GPTMTBMR), offset 0x008

This register configures the GPTM based on the configuration selected in the GPTMCFG register. When in PWM mode, set the TBAMS bit, clear the TBCMR bit, and configure the TBMR field to 0x1 or 0x2.

This register controls the modes for Timer B when it is used individually. When Timer A and Timer B are concatenated, this register is ignored and GPTMTAMR controls the modes for both Timer A and Timer B.

Important: Bits in this register should only be changed when the TBEN bit in the GPTMCTL register is cleared.

GPTM Timer B Mode (GPTMTBMR)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Legacy operation with CCP pin driven Low when the GPTMTAILR is reloaded after the timer reaches 0.</td>
<td>0</td>
</tr>
<tr>
<td>CCP is driven High when the GPTMTAILR is reloaded after the timer reaches 0.</td>
<td>1</td>
</tr>
</tbody>
</table>

This bit is only valid in PWM mode.
### GPTM Timer B Match Register Update

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>TBMRSU</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Match Register Update</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: Update the `GPTMTBMATCHR` register and the `GPTMTBPR` register, if used, on the next cycle.
- **1**: Update the `GPTMTBMATCHR` register and the `GPTMTBPR` register, if used, on the next timeout.

If the timer is disabled (`TBEN` is clear) when this bit is set, `GPTMTBMATCHR` and `GPTMTBPR` are updated when the timer is enabled. If the timer is stalled (`TBSTALL` is set), `GPTMTBMATCHR` and `GPTMTBPR` are updated according to the configuration of this bit.

### GPTM Timer B PWM Interrupt Enable

**Description**

- **9**: TBPWMIE

This bit enables interrupts in PWM mode on rising, falling, or both edges of the CCP output as defined by the `TBEVENT` field in the `GPTMCTL` register.

**Value Description**

- **0**: Capture event interrupt is disabled.
- **1**: Capture event is enabled.

This bit is only valid in PWM mode.

### GPTM Timer B Interval Load Write

**Description**

- **8**: TBILD

Update the `GPTMTBR` and `GPTMTBV` registers with the value in the `GPTMTBILR` register on the next cycle. Also update the `GPTMTBPS` and `GPTMTBPV` registers with the value in the `GPTMTBPR` register on the next cycle.

- **1**: Update the `GPTMTBR` and `GPTMTBV` registers with the value in the `GPTMTBILR` register on the next timeout. Also update the `GPTMTBPS` and `GPTMTBPV` registers with the value in the `GPTMTBPR` register on the next timeout.

**Note**: The state of this bit has no effect when counting up.

The bit descriptions above apply if the timer is enabled and running. If the timer is disabled (`TBEN` is clear) when this bit is set, `GPTMTBR`, `GPTMTBV`, `GPTMTBPS`, and `GPTMTBPV` are updated when the timer is enabled. If the timer is stalled (`TBSTALL` is set), `GPTMTBR` and `GPTMTBPS` are updated according to the configuration of this bit.

### GPTM Timer B Snap-Shot Mode

**Description**

- **7**: TBSNAPS

If Timer B is configured in the periodic mode, the actual free-running value of Timer B is loaded at the time-out event into the `GPTM Timer B (GPTMTBR)` register. If the timer prescaler is used, the prescaler snapshot is loaded into the `GPTM Timer B (GPTMTBPR)`.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>TBWOT</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Wait-on-Trigger</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>0</strong>  Timer B begins counting as soon as it is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>1</strong>  If Timer B is enabled (TBEN is set in the GPTMCTL register), Timer B does not begin counting until it receives a trigger from the timer in the previous position in the daisy chain, see Figure 11-9 on page 733. This function is valid for one-shot, periodic, and PWM modes.</td>
</tr>
<tr>
<td>5</td>
<td>TBMIE</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Match Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>0</strong>  The match interrupt is disabled for match events.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>1</strong>  An interrupt is generated when the match value in the GPTMTBMATCHR register is reached in the one-shot and periodic modes.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> Clearing the TBMIE bit in the GPTMTBMR register prevents assertion of µDMA or ADC requests generated on a match event. Even if the TBTODMAEN bit is set in the GPTMDMAEV register or the TBTOADCEN bit is set in the GPTMADCEV register, a µDMA or ADC match trigger is not sent to the µDMA or ADC, respectively, when the TBMIE bit is clear.</td>
</tr>
<tr>
<td>4</td>
<td>TBCDIR</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Count Direction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>0</strong>  The timer counts down.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>1</strong>  The timer counts up. When counting up, the timer starts from a value of 0x0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When in PWM or RTC mode, the status of this bit is ignored. PWM mode always counts down and RTC mode always counts up.</td>
</tr>
<tr>
<td>3</td>
<td>TBAMS</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Alternate Mode Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>The TBAMS values are defined as follows:</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>0</strong>  Capture or compare mode is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>1</strong>  PWM mode is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> To enable PWM mode, you must also clear the TBCMR bit and configure the TBCMR field to 0x1 or 0x2.</td>
</tr>
<tr>
<td>2</td>
<td>TBCMR</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Capture Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>The TBCMR values are defined as follows:</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>0</strong>  Edge-Count mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>1</strong>  Edge-Time mode</td>
</tr>
</tbody>
</table>
**General-Purpose Timers**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>TBMR</td>
<td>RW</td>
<td>0x0</td>
<td>GPTM Timer B Mode</td>
</tr>
</tbody>
</table>

The TBMR values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x1</td>
<td>One-Shot Timer mode</td>
</tr>
<tr>
<td>0x2</td>
<td>Periodic Timer mode</td>
</tr>
<tr>
<td>0x3</td>
<td>Capture mode</td>
</tr>
</tbody>
</table>

The timer mode is based on the timer configuration defined by bits 2:0 in the GPTMCFG register.
Register 4: GPTM Control (GPTMCTL), offset 0x00C

This register is used alongside the GPTMCFG and GMTMTnMR registers to fine-tune the timer configuration, and to enable other features such as timer stall and the output trigger. The output trigger can be used to initiate transfers on the ADC module.

**Important:** Bits in this register should only be changed when the TnEN bit for the respective timer is cleared.

GPTM Control (GPTMCTL)

| 16/32-bit Timer 0 base: 0x4003.0000 |
| 16/32-bit Timer 1 base: 0x4003.1000 |
| 16/32-bit Timer 2 base: 0x4003.2000 |
| 16/32-bit Timer 3 base: 0x4003.3000 |
| 16/32-bit Timer 4 base: 0x4003.4000 |
| 16/32-bit Timer 5 base: 0x4003.5000 |
| 32/64-bit Wide Timer 0 base: 0x4003.6000 |
| 32/64-bit Wide Timer 1 base: 0x4003.7000 |
| 32/64-bit Wide Timer 2 base: 0x4004.C000 |
| 32/64-bit Wide Timer 3 base: 0x4004.D000 |
| 32/64-bit Wide Timer 4 base: 0x4004.E000 |
| 32/64-bit Wide Timer 5 base: 0x4004.F000 |
| Offset 0x00C |
| Type RW, reset 0x0000.0000 |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:15</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>14</td>
<td>TBPWML</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B PWM Output Level</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The TBPWML values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Output is unaffected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Output is inverted.</td>
</tr>
</tbody>
</table>
The TBOTE values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The output Timer B ADC trigger is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>The output Timer B ADC trigger is enabled.</td>
</tr>
</tbody>
</table>

**Note:** The timer must be configured for one-shot or periodic time-out mode to produce an ADC trigger assertion. The GPTM does not generate triggers for match, compare events or compare match events.

In addition, the ADC must be enabled and the timer selected as a trigger source with the EMn bit in the ADCEMUX register (see page 847).

The TBEVENT values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Positive edge</td>
</tr>
<tr>
<td>0x1</td>
<td>Negative edge</td>
</tr>
<tr>
<td>0x2</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>Both edges</td>
</tr>
</tbody>
</table>

**Note:** If PWM output inversion is enabled, edge detection interrupt behavior is reversed. Thus, if a positive-edge interrupt trigger has been set and the PWM inversion generates a positive edge, no event-trigger interrupt asserts. Instead, the interrupt is generated on the negative edge of the PWM signal.

The TBSTALL values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Timer B continues counting while the processor is halted by the debugger.</td>
</tr>
<tr>
<td>1</td>
<td>Timer B freezes counting while the processor is halted by the debugger.</td>
</tr>
</tbody>
</table>

If the processor is executing normally, the TBSTALL bit is ignored.

The TBEN values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Timer B is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>Timer B is enabled and begins counting or the capture logic is enabled based on the GPTMCFG register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>-----------</td>
<td>---------------</td>
</tr>
<tr>
<td>7</td>
<td>reserved</td>
</tr>
<tr>
<td>6</td>
<td>TAPWML</td>
</tr>
</tbody>
</table>

The TAPWML values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Output is unaffected.</td>
</tr>
<tr>
<td>1</td>
<td>Output is inverted.</td>
</tr>
</tbody>
</table>

| 5      | TAOTE             | RW   | 0     | GPTM Timer A Output Trigger Enable |

The TAOTE values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The output Timer A ADC trigger is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>The output Timer A ADC trigger is enabled.</td>
</tr>
</tbody>
</table>

**Note:** The timer must be configured for one-shot or periodic time-out mode to produce an ADC trigger assertion. The GPTM does not generate triggers for match, compare events or compare match events.

In addition, the ADC must be enabled and the timer selected as a trigger source with the EM<sub>n</sub> bit in the ADCEMUX register (see page 847).

| 4      | RTCEN           | RW   | 0     | GPTM RTC Stall Enable |

The RTCEN values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RTC counting freezes while the processor is halted by the debugger.</td>
</tr>
<tr>
<td>1</td>
<td>RTC counting continues while the processor is halted by the debugger.</td>
</tr>
</tbody>
</table>

If the RTCEN bit is set, it prevents the timer from stalling in all operating modes, even if TnSTALL is set.

| 3:2    | TAEVENT       | RW   | 0x0   | GPTM Timer A Event Mode |

The TAEVENT values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Positive edge</td>
</tr>
<tr>
<td>0x1</td>
<td>Negative edge</td>
</tr>
<tr>
<td>0x2</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>Both edges</td>
</tr>
</tbody>
</table>

**Note:** If PWM output inversion is enabled, edge detection interrupt behavior is reversed. Thus, if a positive-edge interrupt trigger has been set and the PWM inversion generates a positive edge, no event-trigger interrupt asserts. Instead, the interrupt is generated on the negative edge of the PWM signal.
General-Purpose Timers

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TASTALL</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Stall Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The TASTALL values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>TAEN</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The TAEN values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

Texas Instruments-Production Data

June 12, 2014
Register 5: GPTM Synchronize (GPTMSYNC), offset 0x010

Note: This register is only implemented on GPTM Module 0 only.

This register allows software to synchronize a number of timers.

GPTM Synchronize (GPTMSYNC)

16/32-bit Timer 0 base: 0x4003.0000
16/32-bit Timer 1 base: 0x4003.1000
16/32-bit Timer 2 base: 0x4003.2000
16/32-bit Timer 3 base: 0x4003.3000
16/32-bit Timer 4 base: 0x4003.4000
16/32-bit Timer 5 base: 0x4003.5000
32/64-bit Wide Timer 0 base: 0x4003.6000
32/64-bit Wide Timer 1 base: 0x4003.7000
32/64-bit Wide Timer 2 base: 0x4004.C000
32/64-bit Wide Timer 3 base: 0x4004.D000
32/64-bit Wide Timer 4 base: 0x4004.E000
32/64-bit Wide Timer 5 base: 0x4004.F000

Offset 0x010
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23:22</td>
<td>SYNCWT5</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 32/64-Bit Timer 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The SYNCWT5 values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0x0</td>
<td>GPTM 32/64-Bit Timer 5 is not affected.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 32/64-Bit Timer 5 is triggered.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 32/64-Bit Timer 5 is triggered.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 32/64-Bit Timer 5 is triggered.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
General-Purpose Timers

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>21:20</td>
<td>SYNCWT4</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 32/64-Bit Timer 4</td>
<td>0x0</td>
<td>GPTM 32/64-Bit Timer 4 is not affected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 32/64-Bit Timer 4 is triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 32/64-Bit Timer 4 is triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 32/64-Bit Timer 4 is triggered.</td>
</tr>
<tr>
<td>19:18</td>
<td>SYNCWT3</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 32/64-Bit Timer 3</td>
<td>0x0</td>
<td>GPTM 32/64-Bit Timer 3 is not affected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 32/64-Bit Timer 3 is triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 32/64-Bit Timer 3 is triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 32/64-Bit Timer 3 is triggered.</td>
</tr>
<tr>
<td>17:16</td>
<td>SYNCWT2</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 32/64-Bit Timer 2</td>
<td>0x0</td>
<td>GPTM 32/64-Bit Timer 2 is not affected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 32/64-Bit Timer 2 is triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 32/64-Bit Timer 2 is triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 32/64-Bit Timer 2 is triggered.</td>
</tr>
<tr>
<td>15:14</td>
<td>SYNCWT1</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 32/64-Bit Timer 1</td>
<td>0x0</td>
<td>GPTM 32/64-Bit Timer 1 is not affected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 32/64-Bit Timer 1 is triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 32/64-Bit Timer 1 is triggered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 32/64-Bit Timer 1 is triggered.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----------</td>
<td>-----------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------------------------------------------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13:12</td>
<td>SYNCWT0</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 32/64-Bit Timer 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <strong>SYNCWT0</strong> values are defined as follows:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>GPTM 32/64-Bit Timer 0 is not affected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 32/64-Bit Timer 0 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 32/64-Bit Timer 0 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 32/64-Bit Timer 0 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:10</td>
<td>SYNCT5</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 16/32-Bit Timer 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <strong>SYNCT5</strong> values are defined as follows:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>GPTM 16/32-Bit Timer 5 is not affected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 16/32-Bit Timer 5 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 16/32-Bit Timer 5 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 16/32-Bit Timer 5 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9:8</td>
<td>SYNCT4</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 16/32-Bit Timer 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <strong>SYNCT4</strong> values are defined as follows:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>GPTM 16/32-Bit Timer 4 is not affected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 16/32-Bit Timer 4 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 16/32-Bit Timer 4 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 16/32-Bit Timer 4 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:6</td>
<td>SYNCT3</td>
<td>RW</td>
<td>0x0</td>
<td>Synchronize GPTM 16/32-Bit Timer 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <strong>SYNCT3</strong> values are defined as follows:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>GPTM 16/32-Bit Timer 3 is not affected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 16/32-Bit Timer 3 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 16/32-Bit Timer 3 is triggered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 16/32-Bit Timer 3 is triggered.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Synchronize GPTM 16/32-Bit Timer 2

The SYNCT2 values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>GPTM 16/32-Bit Timer 2 is not affected.</td>
</tr>
<tr>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 16/32-Bit Timer 2 is triggered.</td>
</tr>
<tr>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 16/32-Bit Timer 2 is triggered.</td>
</tr>
<tr>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 16/32-Bit Timer 2 is triggered.</td>
</tr>
</tbody>
</table>

Synchronize GPTM 16/32-Bit Timer 1

The SYNCT1 values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>GPTM 16/32-Bit Timer 1 is not affected.</td>
</tr>
<tr>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 16/32-Bit Timer 1 is triggered.</td>
</tr>
<tr>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 16/32-Bit Timer 1 is triggered.</td>
</tr>
<tr>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 16/32-Bit Timer 1 is triggered.</td>
</tr>
</tbody>
</table>

Synchronize GPTM 16/32-Bit Timer 0

The SYNCT0 values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>GPTM 16/32-Bit Timer 0 is not affected.</td>
</tr>
<tr>
<td>0x1</td>
<td>A timeout event for Timer A of GPTM 16/32-Bit Timer 0 is triggered.</td>
</tr>
<tr>
<td>0x2</td>
<td>A timeout event for Timer B of GPTM 16/32-Bit Timer 0 is triggered.</td>
</tr>
<tr>
<td>0x3</td>
<td>A timeout event for both Timer A and Timer B of GPTM 16/32-Bit Timer 0 is triggered.</td>
</tr>
</tbody>
</table>
Register 6: GPTM Interrupt Mask (GPTMIMR), offset 0x018

This register allows software to enable/disable GPTM controller-level interrupts. Setting a bit enables the corresponding interrupt, while clearing a bit disables it.

GPTM Interrupt Mask (GPTMIMR)

- 16/32-bit Timer 0 base: 0x4003.0000
- 16/32-bit Timer 1 base: 0x4003.1000
- 16/32-bit Timer 2 base: 0x4003.2000
- 16/32-bit Timer 3 base: 0x4003.3000
- 16/32-bit Timer 4 base: 0x4003.4000
- 16/32-bit Timer 5 base: 0x4003.5000
- 32/64-bit Wide Timer 0 base: 0x4003.6000
- 32/64-bit Wide Timer 1 base: 0x4003.7000
- 32/64-bit Wide Timer 2 base: 0x4004.C000
- 32/64-bit Wide Timer 3 base: 0x4004.D000
- 32/64-bit Wide Timer 4 base: 0x4004.E000
- 32/64-bit Wide Timer 5 base: 0x4004.F000

Offset 0x018
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type/Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>WUEIM</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide GPTM Write Update Error Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>15:12</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>TBMIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Match Interrupt Mask</td>
</tr>
</tbody>
</table>

Value Description

- 0: Interrupt is disabled.
- 1: Interrupt is enabled.

June 12, 2014

Texas Instruments-Production Data
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>CBEIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Capture Mode Event Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The CBEIM values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value  Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0      Interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1      Interrupt is enabled.</td>
</tr>
<tr>
<td>9</td>
<td>CBMIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Capture Mode Match Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The CBMIM values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value  Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0      Interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1      Interrupt is enabled.</td>
</tr>
<tr>
<td>8</td>
<td>TBTOIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer B Time-Out Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The TBTOIM values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value  Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0      Interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1      Interrupt is enabled.</td>
</tr>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>TAMIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Match Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The TAMIM values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value  Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0      Interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1      Interrupt is enabled.</td>
</tr>
<tr>
<td>3</td>
<td>RTCIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM RTC Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The RTCIM values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value  Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0      Interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1      Interrupt is enabled.</td>
</tr>
<tr>
<td>2</td>
<td>CAEIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Capture Mode Event Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The CAEIM values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value  Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0      Interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1      Interrupt is enabled.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>CAMIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Capture Mode Match Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The CAMIM values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value   Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       Interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       Interrupt is enabled.</td>
</tr>
<tr>
<td>0</td>
<td>TATOIM</td>
<td>RW</td>
<td>0</td>
<td>GPTM Timer A Time-Out Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The TATOIM values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value   Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       Interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       Interrupt is enabled.</td>
</tr>
</tbody>
</table>
Register 7: GPTM Raw Interrupt Status (GPTMRIS), offset 0x01C

This register shows the state of the GPTM's internal interrupt signal. These bits are set whether or not the interrupt is masked in the GPTMIMR register. Each bit can be cleared by writing a 1 to its corresponding bit in GPTMICR.

**Note:** The state of the GPTMRIS register is not affected by disabling and then re-enabling the timer using the TnEN bits in the GPTM Control (GPTMCTL) register. If an application requires that all or certain status bits should not carry over after re-enabling the timer, then the appropriate bits in the GPTMRIS register should be cleared using the GPTMICR register prior to re-enabling the timer. If this is not done, any status bits set in the GPTMRIS register and unmasked in the GPTMIMR register generate an interrupt once the timer is re-enabled.

### GPTM Raw Interrupt Status (GPTMRIS)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>No error.</td>
<td>0</td>
</tr>
<tr>
<td>Either a Timer A register or a Timer B register was written twice in a row or a Timer A register was written before the corresponding Timer B register was written.</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>WUERIS</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide GPTM Write Update Error Raw Interrupt Status</td>
</tr>
</tbody>
</table>

Value Description

0  No error.
1  Either a Timer A register or a Timer B register was written twice in a row or a Timer A register was written before the corresponding Timer B register was written.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>TBMRIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer B Match Raw Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The match value has not been reached.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The TBMIE bit is set in the GPTMTBMR register, and the match values in</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the GPTMTBMR and (optionally) GPTMTBPMR registers have been reached when</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>configured in one-shot or periodic mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the TBMCEINT bit in the GPTMCR</td>
</tr>
<tr>
<td>10</td>
<td>CBERIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer B Capture Mode Event Raw Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The capture mode event for Timer B has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  A capture mode event has occurred for Timer B. This interrupt asserts</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>when the subtimer is configured in Input Edge-Time mode or when configured</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>in PWM mode with the PWM interrupt enabled by setting the TBPWMIE bit in</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the GPTMTBMR.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CBECINT bit in the GPTMCR</td>
</tr>
<tr>
<td>9</td>
<td>CBMRIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer B Capture Mode Match Raw Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The capture mode match for Timer B has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The capture mode match has occurred for Timer B. This interrupt asserts</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>when the values in the GPTMTBR and GPTMTBPR match the values in the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GPTMTBMR and GPTMTBPMR when configured in Input Edge-Time mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CBMCINT bit in the GPTMCR</td>
</tr>
<tr>
<td>8</td>
<td>TBTORIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer B Time-Out Raw Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Timer B has not timed out.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Timer B has timed out. This interrupt is asserted when a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>one-shot or periodic mode timer reaches it's count limit (0 or the value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>loaded into GPTMTBILR, depending on the count direction).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the TBTOCRINT bit in the GPTMCR</td>
</tr>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------------------</td>
<td>------</td>
<td>-------</td>
<td>-------------------------------------------------------</td>
</tr>
</tbody>
</table>
| 4         | TAMRIS             | RO   | 0     | GPTM Timer A Match Raw Interrupt

**Value Description**

- **0**: The match value has not been reached.
- **1**: The TAMIE bit is set in the GPTMTAMR register, and the match value in the GPTMTAMATCHR and (optionally) GPTMTAPMR registers have been reached when configured in one-shot or periodic mode.

This bit is cleared by writing a 1 to the TAMCINT bit in the GPTMICR register.

| 3         | RTCRIS             | RO   | 0     | GPTM RTC Raw Interrupt

**Value Description**

- **0**: The RTC event has not occurred.
- **1**: The RTC event has occurred.

This bit is cleared by writing a 1 to the RTCCINT bit in the GPTMICR register.

| 2         | CAERIS             | RO   | 0     | GPTM Timer A Capture Mode Event Raw Interrupt

**Value Description**

- **0**: The capture mode event for Timer A has not occurred.
- **1**: A capture mode event has occurred for Timer A. This interrupt asserts when the subtimer is configured in Input Edge-Time mode or when configured in PWM mode with the PWM interrupt enabled by setting the TAPWMIE bit in the GPTMTAMR.

This bit is cleared by writing a 1 to the CAECINT bit in the GPTMICR register.

| 1         | CAMRIS             | RO   | 0     | GPTM Timer A Capture Mode Match Raw Interrupt

**Value Description**

- **0**: The capture mode match for Timer A has not occurred.
- **1**: A capture mode match has occurred for Timer A. This interrupt asserts when the values in the GPTMTAR and GPTMTAPR match the values in the GPTMTAMATCHR and GPTMTAPMR when configured in Input Edge-Time mode.

This bit is cleared by writing a 1 to the CAMCINT bit in the GPTMICR register.

| 0         | TATORIS            | RO   | 0     | GPTM Timer A Time-Out Raw Interrupt

**Value Description**

- **0**: Timer A has not timed out.
- **1**: Timer A has timed out. This interrupt is asserted when a one-shot or periodic mode timer reaches its count limit (0 or the value loaded into GPTMTAILR, depending on the count direction).

This bit is cleared by writing a 1 to the TATOCINT bit in the GPTMICR register.
Register 8: GPTM Masked Interrupt Status (GPTMMIS), offset 0x020

This register show the state of the GPTM's controller-level interrupt. If an interrupt is unmasked in GPTMIMR, and there is an event that causes the interrupt to be asserted, the corresponding bit is set in this register. All bits are cleared by writing a 1 to the corresponding bit in GPTMICR.

GPTM Masked Interrupt Status (GPTMMIS)

16/32-bit Timer 0 base: 0x4003.0000
16/32-bit Timer 1 base: 0x4003.1000
16/32-bit Timer 2 base: 0x4003.2000
16/32-bit Timer 3 base: 0x4003.3000
16/32-bit Timer 4 base: 0x4003.4000
16/32-bit Timer 5 base: 0x4003.5000
32/64-bit Wide Timer 0 base: 0x4003.6000
32/64-bit Wide Timer 1 base: 0x4003.7000
32/64-bit Wide Timer 2 base: 0x4004.C000
32/64-bit Wide Timer 3 base: 0x4004.D000
32/64-bit Wide Timer 4 base: 0x4004.E000
32/64-bit Wide Timer 5 base: 0x4004.F000
Offset 0x020
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>WUEMIS</td>
<td>RO</td>
<td>0</td>
<td>32/64-Bit Wide GPTM Write Update Error Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An unmasked Write Update Error has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked Write Update Error has occurred.</td>
</tr>
<tr>
<td>15:12</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>TBMMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer B Match Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 A Timer B Mode Match interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked Timer B Mode Match interrupt has occurred.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the TBMCINT bit in the GPTMICR register.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>CBEMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer B Capture Mode Event Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   A Capture B event interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An unmasked Capture B event interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CBECINT bit in the GPTMICR register.</td>
</tr>
<tr>
<td>9</td>
<td>CBMMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer B Capture Mode Match Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   A Capture B Mode Match interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An unmasked Capture B Match interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CBMCINT bit in the GPTMICR register.</td>
</tr>
<tr>
<td>8</td>
<td>TBTOMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer B Time-Out Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   A Timer B Time-Out interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An unmasked Timer B Time-Out interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the TBTOCINT bit in the GPTMICR register.</td>
</tr>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>TAMMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer A Match Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   A Timer A Mode Match interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An unmasked Timer A Mode Match interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the TAMCINT bit in the GPTMICR register.</td>
</tr>
<tr>
<td>3</td>
<td>RTCMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM RTC Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   An RTC event interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An unmasked RTC event interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the RTCINT bit in the GPTMICR register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>CAEMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer A Capture Mode Event Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 A Capture A event interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked Capture A event interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CAECINT bit in the GPTMICR register.</td>
</tr>
<tr>
<td>1</td>
<td>CAMMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer A Capture Mode Match Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 A Capture A Mode Match interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked Capture A Match interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CAMCINT bit in the GPTMICR register.</td>
</tr>
<tr>
<td>0</td>
<td>TATOMIS</td>
<td>RO</td>
<td>0</td>
<td>GPTM Timer A Time-Out Masked Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 A Timer A Time-Out interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked Timer A Time-Out interrupt has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the TATOCINT bit in the GPTMICR register.</td>
</tr>
</tbody>
</table>
Register 9: GPTM Interrupt Clear (GPTMICR), offset 0x024

This register is used to clear the status bits in the GPTMRIS and GPTMMIS registers. Writing a 1 to a bit clears the corresponding bit in the GPTMRIS and GPTMMIS registers.

### GPTM Interrupt Clear (GPTMICR)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x024</td>
<td>GPTM Interrupt Clear (GPTMICR)</td>
</tr>
</tbody>
</table>

#### Register Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>WUECINT</td>
<td>RW</td>
<td>0</td>
<td>32/64-Bit Wide GPTM Write Update Error Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the WUERIS bit in the GPTMRIS register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and the WUEMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>15:12</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>TBMCINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM Timer B Match Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the TBMRIS bit in the GPTMRIS register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and the TBMMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>10</td>
<td>CBECINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM Timer B Capture Mode Event Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the CBERIS bit in the GPTMRIS register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and the CBEMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>9</td>
<td>CBMCINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM Timer B Capture Mode Match Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the CBMORIS bit in the GPTMRIS register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and the CBMMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>8</td>
<td>TBTOCINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM Timer B Time-Out Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the TBTORIS bit in the GPTMRIS register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and the TBTOMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------------------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>TAMCINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM Timer A Match Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the TAMRIS bit in the GPTMRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the TAMMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>3</td>
<td>RTCCINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM RTC Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the RTCRIS bit in the GPTMRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the RTCMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>2</td>
<td>CAECINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM Timer A Capture Mode Event Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the CAERIS bit in the GPTMRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the CAEMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>1</td>
<td>CAMCINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM Timer A Capture Mode Match Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the CAMRIS bit in the GPTMRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the CAMMIS bit in the GPTMMIS register.</td>
</tr>
<tr>
<td>0</td>
<td>TATOCINT</td>
<td>W1C</td>
<td>0</td>
<td>GPTM Timer A Time-Out Raw Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the TATORIS bit in the GPTMRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the TATOMIS bit in the GPTMMIS register.</td>
</tr>
</tbody>
</table>
Register 10: GPTM Timer A Interval Load (GPTMTAILR), offset 0x028

When the timer is counting down, this register is used to load the starting count value into the timer. When the timer is counting up, this register sets the upper bound for the timeout event.

When a 16/32-bit GPTM is configured to one of the 32-bit modes, GPTMTAILR appears as a 32-bit register (the upper 16-bits correspond to the contents of the GPTM Timer B Interval Load (GPTMTBILR) register). In a 16-bit mode, the upper 16 bits of this register read as 0s and have no effect on the state of GPTMTBILR.

When a 32/64-bit Wide GPTM is configured to one of the 64-bit modes, GPTMTAILR contains bits 31:0 of the 64-bit count and the GPTM Timer B Interval Load (GPTMTBILR) register contains bits 63:32.

### GPTM Timer A Interval Load (GPTMTAILR)

- **Type**: RW, reset 0xFFFF.FFFF
- **Register**: 31:0 TAILR

#### Bit/Field Information

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>TAILR</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>GPTM Timer A Interval Load Register</td>
</tr>
</tbody>
</table>

Writing this field loads the counter for Timer A. A read returns the current value of GPTMTAILR.

---

Texas Instruments-Production Data
Register 11: GPTM Timer B Interval Load (GPTMTBILR), offset 0x02C

When the timer is counting down, this register is used to load the starting count value into the timer. When the timer is counting up, this register sets the upper bound for the timeout event.

When a 16/32-bit GPTM is configured to one of the 32-bit modes, the contents of bits 15:0 in this register are loaded into the upper 16 bits of the \textbf{GPTMTAILR} register. Reads from this register return the current value of Timer B and writes are ignored. In a 16-bit mode, bits 15:0 are used for the load value. Bits 31:16 are reserved in both cases.

When a 32/64-bit Wide GPTM is configured to one of the 64-bit modes, \textbf{GPTMTAILR} contains bits 31:0 of the 64-bit count and the \textbf{GPTMTBILR} register contains bits 63:32.

\begin{verbatim}
GPTM Timer B Interval Load (GPTMTBILR)
16/32-bit Timer 0 base: 0x4003.0000
16/32-bit Timer 1 base: 0x4003.1000
16/32-bit Timer 2 base: 0x4003.2000
16/32-bit Timer 3 base: 0x4003.3000
16/32-bit Timer 4 base: 0x4003.4000
16/32-bit Timer 5 base: 0x4003.5000
32/64-bit Wide Timer 0 base: 0x4003.6000
32/64-bit Wide Timer 1 base: 0x4003.7000
32/64-bit Wide Timer 2 base: 0x4004.C000
32/64-bit Wide Timer 3 base: 0x4004.D000
32/64-bit Wide Timer 4 base: 0x4004.E000
32/64-bit Wide Timer 5 base: 0x4004.F000
Offset 0x02C
Type RW, reset -
\end{verbatim}

\begin{tabular}{cccccccccccccccc}
\hline
Reset & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 1 & 1 \\
\hline
Reset & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \\
\end{tabular}

\begin{verbatim}
Bit/Field Name Type Reset Description
31:0 TBILR RW 0x0000.FFFF (for 16/32-bit) Writing this field loads the counter for Timer B. A read returns the current value of \textbf{GPTMTBILR}. When a 16/32-bit GPTM is in 32-bit mode, writes are ignored, and reads return the current value of \textbf{GPTMTBILR}. 
0xFFFF.FFFF (for 32/64-bit)
\end{verbatim}
Register 12: GPTM Timer A Match (GPTMTAMATCHR), offset 0x030

This register is loaded with a match value. Interrupts can be generated when the timer value is equal to the value in this register in one-shot or periodic mode.

In Edge-Count mode, this register along with GPTMTAILR, determines how many edge events are counted. The total number of edge events counted is equal to the value in GPTMTAILR minus this value. Note that in edge-count mode, when executing an up-count, the value of GPTMTnPR and GPTMTnILR must be greater than the value of GPTMTnPMR and GPTMTnMATCHR.

In PWM mode, this value along with GPTMTAILR, determines the duty cycle of the output PWM signal.

When a 16/32-bit GPTM is configured to one of the 32-bit modes, GPTMTAMATCHR appears as a 32-bit register (the upper 16-bits correspond to the contents of the GPTM Timer B Match (GPTMTBMATCHR) register). In a 16-bit mode, the upper 16 bits of this register read as 0s and have no effect on the state of GPTMTBMATCHR.

When a 32/64-bit Wide GPTM is configured to one of the 64-bit modes, GPTMTAMATCHR contains bits 31:0 of the 64-bit match value and the GPTM Timer B Match (GPTMTBMATCHR) register contains bits 63:32.

GPTM Timer A Match (GPTMTAMATCHR)
16/32-bit Timer 0 base: 0x4003.0000
16/32-bit Timer 1 base: 0x4003.1000
16/32-bit Timer 2 base: 0x4003.2000
16/32-bit Timer 3 base: 0x4003.3000
16/32-bit Timer 4 base: 0x4003.4000
16/32-bit Timer 5 base: 0x4003.5000
32/64-bit Wide Timer 0 base: 0x4003.6000
32/64-bit Wide Timer 1 base: 0x4003.7000
32/64-bit Wide Timer 2 base: 0x4004.C000
32/64-bit Wide Timer 3 base: 0x4004.D000
32/64-bit Wide Timer 4 base: 0x4004.E000
32/64-bit Wide Timer 5 base: 0x4004.F000
Offset 0x030

Type RW, reset 0xFFFF.FFFF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>TAMR</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>GPTM Timer A Match Register</td>
</tr>
</tbody>
</table>

This value is compared to the GPTMTAR register to determine match events.
Register 13: GPTM Timer B Match (GPTMTBMATCHR), offset 0x034

This register is loaded with a match value. Interrupts can be generated when the timer value is equal to the value in this register in one-shot or periodic mode.

In Edge-Count mode, this register along with GPTMTBILR determines how many edge events are counted. The total number of edge events counted is equal to the value in GPTMTBILR minus this value. Note that in edge-count mode, when executing an up-count, the value of GPTMTnPR and GPTMTnILR must be greater than the value of GPTMTnPMR and GPTMTnMATCHR.

In PWM mode, this value along with GPTMTBILR, determines the duty cycle of the output PWM signal.

When a 16/32-bit GPTM is configured to one of the 32-bit modes, the contents of bits 15:0 in this register are loaded into the upper 16 bits of the GPTMTAMATCHR register. Reads from this register return the current match value of Timer B and writes are ignored. In a 16-bit mode, bits 15:0 are used for the match value. Bits 31:16 are reserved in both cases.

When a 32/64-bit Wide GPTM is configured to one of the 64-bit modes, GPTMTAMATCHR contains bits 31:0 of the 64-bit match value and the GPTMTBMATCHR register contains bits 63:32.

GPTM Timer B Match (GPTMTBMATCHR)

| 16/32-bit Timer 0 base: 0x4003.0000 |
| 16/32-bit Timer 1 base: 0x4003.1000 |
| 16/32-bit Timer 2 base: 0x4003.2000 |
| 16/32-bit Timer 3 base: 0x4003.3000 |
| 16/32-bit Timer 4 base: 0x4003.4000 |
| 16/32-bit Timer 5 base: 0x4003.5000 |
| 32/64-bit Wide Timer 0 base: 0x4003.6000 |
| 32/64-bit Wide Timer 1 base: 0x4003.7000 |
| 32/64-bit Wide Timer 2 base: 0x4004.C000 |
| 32/64-bit Wide Timer 3 base: 0x4004.D000 |
| 32/64-bit Wide Timer 4 base: 0x4004.E000 |
| 32/64-bit Wide Timer 5 base: 0x4004.F000 |

Offset 0x034
Type RW, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>TBMR</td>
<td>RW</td>
<td>0x0000.FFFF (for 16/32-bit) 0xFFFF.FFFF (for 32/64-bit)</td>
<td>GPTM Timer B Match Register This value is compared to the GPTMTBR register to determine match events.</td>
</tr>
</tbody>
</table>
Register 14: GPTM Timer A Prescale (GPTMTAPR), offset 0x038

This register allows software to extend the range of the timers when they are used individually. When in one-shot or periodic down count modes, this register acts as a true prescaler for the timer counter. When acting as a true prescaler, the prescaler counts down to 0 before the value in the GPTMTAR and GPTMTAV registers are incremented. In all other individual/split modes, this register is a linear extension of the upper range of the timer counter, holding bits 23:16 in the 16/32-bit modes of the 16/32-bit GPTM and bits 47:32 in the 32-bit modes of the 32/64-bit Wide GPTM.

GPTM Timer A Prescale (GPTMTAPR)

| 16/32-bit Timer 0 base: 0x4003.0000 |
| 16/32-bit Timer 1 base: 0x4003.1000 |
| 16/32-bit Timer 2 base: 0x4003.2000 |
| 16/32-bit Timer 3 base: 0x4003.3000 |
| 16/32-bit Timer 4 base: 0x4003.4000 |
| 16/32-bit Timer 5 base: 0x4003.5000 |
| 32/64-bit Wide Timer 0 base: 0x4003.6000 |
| 32/64-bit Wide Timer 1 base: 0x4003.7000 |
| 32/64-bit Wide Timer 2 base: 0x4004.C000 |
| 32/64-bit Wide Timer 3 base: 0x4004.D000 |
| 32/64-bit Wide Timer 4 base: 0x4004.E000 |
| 32/64-bit Wide Timer 5 base: 0x4004.F000 |
| Offset 0x038 |

Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Bit/Field Name Type Reset Description
--- --- ---- ---- ----
31:16 reserved RO 0 Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

15:8 TAPSRH RW 0x00 GPTM Timer A Prescale High Byte
The register loads this value on a write. A read returns the current value of the register.
For the 16/32-bit GPTM, this field is reserved. For the 32/64-bit Wide GPTM, this field contains the upper 8-bits of the 16-bit prescaler.
Refer to Table 11-5 on page 725 for more details and an example.

7:0 TAPSR RW 0x00 GPTM Timer A Prescale
The register loads this value on a write. A read returns the current value of the register.
For the 16/32-bit GPTM, this field contains the entire 8-bit prescaler.
For the 32/64-bit Wide GPTM, this field contains the lower 8-bits of the 16-bit prescaler.
Refer to Table 11-5 on page 725 for more details and an example.
Register 15: GPTM Timer B Prescale (GPTMTBPR), offset 0x03C

This register allows software to extend the range of the timers when they are used individually. When in one-shot or periodic down count modes, this register acts as a true prescaler for the timer counter. When acting as a true prescaler, the prescaler counts down to 0 before the value in the GPTMTBR and GPTMTBV registers are incremented. In all other individual/split modes, this register is a linear extension of the upper range of the timer counter, holding bits 23:16 in the 16/32-bit modes of the 16/32-bit GPTM and bits 47:32 in the 32-bit modes of the 32/64-bit Wide GPTM.

GPTM Timer B Prescale (GPTMTBPR)

<table>
<thead>
<tr>
<th>Description</th>
<th>Bit(s)</th>
<th>Type</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide</td>
<td>31:16</td>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>compatibility with future products, the value of a reserved bit should be</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>preserved across a read-modify-write operation.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPTM Timer B Prescale High Byte</td>
<td>15:8</td>
<td>RW</td>
<td>0x00</td>
</tr>
<tr>
<td>The register loads this value on a write. A read returns the current value</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>of the register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For the 16/32-bit GPTM, this field is reserved. For the 32/64-bit Wide</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPTM, this field contains the upper 8-bits of the 16-bit prescaler.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Refer to Table 11-5 on page 725 for more details and an example.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GPTM Timer B Prescale</td>
<td>7:0</td>
<td>RW</td>
<td>0x00</td>
</tr>
<tr>
<td>The register loads this value on a write. A read returns the current value</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>of this register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For the 16/32-bit GPTM, this field contains the entire 8-bit prescaler.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For the 32/64-bit Wide GPTM, this field contains the lower 8-bits of the</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16-bit prescaler.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Refer to Table 11-5 on page 725 for more details and an example.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 16: GPTM TimerA Prescale Match (GPTMTAPMR), offset 0x040

This register allows software to extend the range of the GPTMTAMATCHR when the timers are used individually. This register holds bits 23:16 in the 16-bit modes of the 16/32-bit GPTM and bits 47:32 in the 32-bit modes of the 32/64-bit Wide GPTM.

GPTM TimerA Prescale Match (GPTMTAPMR)

16/32-bit Timer 0 base: 0x4003.0000
16/32-bit Timer 1 base: 0x4003.1000
16/32-bit Timer 2 base: 0x4003.2000
16/32-bit Timer 3 base: 0x4003.3000
16/32-bit Timer 4 base: 0x4003.4000
16/32-bit Timer 5 base: 0x4003.5000
32/64-bit Wide Timer 0 base: 0x4003.6000
32/64-bit Wide Timer 1 base: 0x4003.7000
32/64-bit Wide Timer 2 base: 0x4004.C000
32/64-bit Wide Timer 3 base: 0x4004.D000
32/64-bit Wide Timer 4 base: 0x4004.E000
32/64-bit Wide Timer 5 base: 0x4004.F000
Offset 0x040
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:8</td>
<td>TAPSMRH</td>
<td>RW</td>
<td>0x00</td>
<td>GPTM Timer A Prescale Match High Byte</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This value is used alongside GPTMTAMATCHR to detect timer match events while using a prescaler.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For the 16/32-bit GPTM, this field is reserved. For the 32/64-bit Wide GPTM, this field contains the upper 8-bits of the 16-bit prescaler match value.</td>
</tr>
<tr>
<td>7:0</td>
<td>TAPSMR</td>
<td>RW</td>
<td>0x00</td>
<td>GPTM TimerA Prescale Match</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This value is used alongside GPTMTAMATCHR to detect timer match events while using a prescaler.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For the 16/32-bit GPTM, this field contains the entire 8-bit prescaler match value. For the 32/64-bit Wide GPTM, this field contains the lower 8-bits of the 16-bit prescaler match value.</td>
</tr>
</tbody>
</table>
Register 17: GPTM TimerB Prescale Match (GPTMTBPMR), offset 0x044

This register allows software to extend the range of the GPTMTBPMATCHR when the timers are used individually. This register holds bits 23:16 in the 16-bit modes of the 16/32-bit GPTM and bits 47:32 in the 32-bit modes of the 32/64-bit Wide GPTM.

GPTM TimerB Prescale Match (GPTMTBPMR)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>TBPSMH</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>0x00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>TBPSM</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>0x00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

GPTM Timer B Prescale Match High Byte

This value is used alongside GPTMTBPMATCHR to detect timer match events while using a prescaler.

For the 16/32-bit GPTM, this field is reserved. For the 32/64-bit Wide GPTM, this field contains the upper 8-bits of the 16-bit prescaler match value.

GPTM TimerB Prescale Match

This value is used alongside GPTMTBPMATCHR to detect timer match events while using a prescaler.

For the 16/32-bit GPTM, this field contains the entire 8-bit prescaler match value. For the 32/64-bit Wide GPTM, this field contains the lower 8-bits of the 16-bit prescaler match value.
Register 18: GPTM Timer A (GPTMTAR), offset 0x048

This register shows the current value of the Timer A counter in all cases except for Input Edge Count and Time modes. In the Input Edge Count mode, this register contains the number of edges that have occurred. In the Input Edge Time mode, this register contains the time at which the last edge event took place.

When a 16/32-bit GPTM is configured to one of the 32-bit modes, GPTMTAR appears as a 32-bit register (the upper 16-bits correspond to the contents of the GPTM Timer B (GPTMTBR) register). In the 16-bit Input Edge Count, Input Edge Time, and PWM modes, bits 15:0 contain the value of the counter and bits 23:16 contain the value of the prescaler, which is the upper 8 bits of the count. Bits 31:24 always read as 0. To read the value of the prescaler in 16-bit One-Shot and Periodic modes, read bits [23:16] in the GPTMTAV register. To read the value of the prescaler in periodic snapshot mode, read the Timer A Prescale Snapshot (GPTMTAPS) register.

When a 32/64-bit Wide GPTM is configured to one of the 64-bit modes, GPTMTAR contains bits 31:0 of the 64-bit timer value and the GPTMTimerB (GPTMTBR) register contains bits 63:32. In a 32-bit mode, the value of the prescaler is stored in the GPTM Timer A Prescale Snapshot (GPTMTAPS) register.
Register 19: GPTM Timer B (GPTMTBR), offset 0x04C

This register shows the current value of the Timer B counter in all cases except for Input Edge Count and Time modes. In the Input Edge Count mode, this register contains the number of edges that have occurred. In the Input Edge Time mode, this register contains the time at which the last edge event took place.

When a 16/32-bit GPTM is configured to one of the 32-bit modes, the contents of bits 15:0 in this register are loaded into the upper 16 bits of the GPTMTAR register. Reads from this register return the current value of Timer B. In a 16-bit mode, bits 15:0 contain the value of the counter and bits 23:16 contain the value of the prescaler in Input Edge Count, Input Edge Time, and PWM modes, which is the upper 8 bits of the count. Bits 31:24 always read as 0. To read the value of the prescaler in 16-bit One-Shot and Periodic modes, read bits [23:16] in the GPTMTBV register. To read the value of the prescaler in periodic snapshot mode, read the Timer B Prescale Snapshot (GPTMTBPS) register.

When a 32/64-bit Wide GPTM is configured to one of the 64-bit modes, GPTMTAR contains bits 31:0 of the 64-bit timer value and the GPTM Timer B (GPTMTBR) register contains bits 63:32. In a 32-bit mode, the value of the prescaler is stored in the GPTM Timer B Prescale Snapshot (GPTMTBPS) register.
Register 20: GPTM Timer A Value (GPTMTAV), offset 0x050

When read, this register shows the current, free-running value of Timer A in all modes. Software can use this value to determine the time elapsed between an interrupt and the ISR entry when using the snapshot feature with the periodic operating mode. When written, the value written into this register is loaded into the GPTMTAR register on the next clock cycle.

When a 16/32-bit GPTM is configured to one of the 32-bit modes, GPTMTAV appears as a 32-bit register (the upper 16-bits correspond to the contents of the GPTM Timer B Value (GPTMTBV) register). In a 16-bit mode, bits 15:0 contain the value of the counter and bits 23:16 contain the current, free-running value of the prescaler, which is the upper 8 bits of the count in Input Edge Count, Input Edge Time, PWM and one-shot or periodic up count modes. In one-shot or periodic down count modes, the prescaler stored in 23:16 is a true prescaler, meaning bits 23:16 count down before decrementing the value in bits 15:0. The prescaler in bits 31:24 always reads as 0.

When a 32/64-bit Wide GPTM is configured to one of the 64-bit modes, GPTMTAV contains bits 31:0 of the 64-bit timer value and the GPTMTimerBValue (GPTMTBV) register contains bits 63:32. In a 32-bit mode, the current, free-running value of the prescaler is stored in the GPTM Timer A Prescale Value (GPTMTAPV) register.

GPTM Timer A Value (GPTMTAV)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>TAV</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>A read returns the current, free-running value of Timer A in all modes. When written, the value written into this register is loaded into the GPTMTAR register on the next clock cycle. Note: In 16-bit mode, only the lower 16-bits of the GPTMTAV register can be written with a new value. Writes to the prescaler bits have no effect.</td>
</tr>
</tbody>
</table>
Register 21: GPTM Timer B Value (GPTMTBV), offset 0x054

When read, this register shows the current, free-running value of Timer B in all modes. Software can use this value to determine the time elapsed between an interrupt and the ISR entry. When written, the value written into this register is loaded into the GPTMTBR register on the next clock cycle.

When a 16/32-bit GPTM is configured to one of the 32-bit modes, the contents of bits 15:0 in this register are loaded into the upper 16 bits of the GPTMTAV register. Reads from this register return the current free-running value of Timer B. In a 16-bit mode, bits 15:0 contain the value of the counter and bits 23:16 contain the current, free-running value of the prescaler, which is the upper 8 bits of the count in Input Edge Count, Input Edge Time, PWM and one-shot or periodic up count modes. In one-shot or periodic down count modes, the prescaler stored in 23:16 is a true prescaler, meaning bits 23:16 count down before decrementing the value in bits 15:0. The prescaler in bits 31:24 always reads as 0.

When a 32/64-bit Wide GPTM is configured to one of the 64-bit modes, GPTMTBV contains bits 63:32 of the 64-bit timer value and the GPTM Timer A Value (GPTMTAV) register contains bits 31:0. In a 32-bit mode, the current, free-running value of the prescaler is stored in the GPTM Timer B Prescale Value (GPTMTBPV) register.

### Description

A read returns the current, free-running value of Timer A in all modes. When written, the value written into this register is loaded into the GPTMTAR register on the next clock cycle.

**Note:** In 16-bit mode, only the lower 16-bits of the GPTMTBV register can be written with a new value. Writes to the prescaler bits have no effect.

---

**GPTM Timer B Value (GPTMTBV)**

<table>
<thead>
<tr>
<th></th>
<th>16/32-bit Timer 0 base: 0x4003.0000</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>16/32-bit Timer 1 base: 0x4003.1000</td>
</tr>
<tr>
<td></td>
<td>16/32-bit Timer 2 base: 0x4003.2000</td>
</tr>
<tr>
<td></td>
<td>16/32-bit Timer 3 base: 0x4003.3000</td>
</tr>
<tr>
<td></td>
<td>16/32-bit Timer 4 base: 0x4003.4000</td>
</tr>
<tr>
<td></td>
<td>16/32-bit Timer 5 base: 0x4003.5000</td>
</tr>
<tr>
<td></td>
<td>32/64-bit Wide Timer 0 base: 0x4003.6000</td>
</tr>
<tr>
<td></td>
<td>32/64-bit Wide Timer 1 base: 0x4003.7000</td>
</tr>
<tr>
<td></td>
<td>32/64-bit Wide Timer 2 base: 0x4004.C000</td>
</tr>
<tr>
<td></td>
<td>32/64-bit Wide Timer 3 base: 0x4004.D000</td>
</tr>
<tr>
<td></td>
<td>32/64-bit Wide Timer 4 base: 0x4004.E000</td>
</tr>
<tr>
<td></td>
<td>32/64-bit Wide Timer 5 base: 0x4004.F000</td>
</tr>
<tr>
<td>Offset</td>
<td>0x054</td>
</tr>
<tr>
<td>Type</td>
<td>RW, reset -</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Type</strong></td>
</tr>
<tr>
<td>Reset</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Bit/Field Names, Types, and Descriptions

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>TBV</td>
<td>RW</td>
<td>0x0000.FFFF (for 16/32-bit) 0xFFFF.FFFF (for 32/64-bit)</td>
<td>GPTM Timer B Value A read returns the current, free-running value of Timer A in all modes. When written, the value written into this register is loaded into the GPTMTAR register on the next clock cycle. <strong>Note:</strong> In 16-bit mode, only the lower 16-bits of the GPTMTBV register can be written with a new value. Writes to the prescaler bits have no effect.</td>
</tr>
</tbody>
</table>
Register 22: GPTM RTC Predivide (GPTMRTCPD), offset 0x058

This register provides the current RTC predivider value when the timer is operating in RTC mode. Software must perform an atomic access with consecutive reads of the GPTMTAR, GPTMTBR, and GPTMRTCPD registers, see Figure 11-2 on page 726 for more information.

GPTM RTC Predivide (GPTMRTCPD)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>0x0000.7FFF</td>
<td>RTC Predivide Counter Value</td>
</tr>
</tbody>
</table>

The current RTC predivider value when the timer is operating in RTC mode. This field has no meaning in other timer modes.
Register 23: GPTM Timer A Prescale Snapshot (GPTMTAPS), offset 0x05C

For the 32/64-bit Wide GPTM, this register shows the current value of the Timer A prescaler in the 32-bit modes. For 16-/32-bit wide GPTM, this register shows the current value of the Timer A prescaler for periodic snapshot mode.

**GPTM Timer A Prescale Snapshot (GPTMTAPS)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>PSS</td>
<td>0x0000</td>
<td>GPTM Timer A Prescaler Snapshot</td>
</tr>
</tbody>
</table>

**Register 23: GPTM Timer A Prescale Snapshot (GPTMTAPS)**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>PSS</td>
<td>RO</td>
<td>0x0000</td>
<td>GPTM Timer A Prescaler Snapshot</td>
</tr>
</tbody>
</table>
Register 24: GPTM Timer B Prescale Snapshot (GPTMTBPS), offset 0x060

For the 32/64-bit Wide GPTM, this register shows the current value of the Timer B prescaler in the 32-bit modes. For 16-/32-bit wide GPTM, this register shows the current value of the Timer B prescaler for periodic snapshot mode.

GPTM Timer B Prescale Snapshot (GPTMTBPS)

<table>
<thead>
<tr>
<th>Description</th>
<th>Reset</th>
<th>Type</th>
<th>Bit/Field</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>0x0000</td>
<td>RO</td>
<td>31:16</td>
<td>reserved</td>
</tr>
<tr>
<td>A read returns the current value of the GPTM Timer A Prescaler.</td>
<td>0x0000</td>
<td>RO</td>
<td>15:0</td>
<td>PSS</td>
</tr>
</tbody>
</table>

Offset 0x060
Type RO, reset 0x0000.0000
Register 25: GPTM Timer A Prescale Value (GPTMTAPV), offset 0x064

For the 32/64-bit Wide GPTM, this register shows the current free-running value of the Timer A prescaler in the 32-bit modes. Software can use this value in conjunction with the GPTMTAV register to determine the time elapsed between an interrupt and the ISR entry. This register is unused in 16/32-bit GPTM mode.

### GPTM Timer A Prescale Value (GPTMTAPV)

| 16/32-bit Timer 0 base: 0x4003.0000 |
| 16/32-bit Timer 1 base: 0x4003.1000 |
| 16/32-bit Timer 2 base: 0x4003.2000 |
| 16/32-bit Timer 3 base: 0x4003.3000 |
| 16/32-bit Timer 4 base: 0x4003.4000 |
| 16/32-bit Timer 5 base: 0x4003.5000 |
| 32/64-bit Wide Timer 0 base: 0x4003.6000 |
| 32/64-bit Wide Timer 1 base: 0x4003.7000 |
| 32/64-bit Wide Timer 2 base: 0x4004.C000 |
| 32/64-bit Wide Timer 3 base: 0x4004.D000 |
| 32/64-bit Wide Timer 4 base: 0x4004.E000 |
| 32/64-bit Wide Timer 5 base: 0x4004.F000 |

Offset 0x064
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>PSV</td>
<td>RO</td>
<td>0x0000</td>
<td>GPTM Timer A Prescaler Value</td>
</tr>
</tbody>
</table>

A read returns the current, free-running value of the Timer A prescaler.
Register 26: GPTM Timer B Prescale Value (GPTMTBPV), offset 0x068

For the 32/64-bit Wide GPTM, this register shows the current free-running value of the Timer B prescaler in the 32-bit modes. Software can use this value in conjunction with the GPTMTBV register to determine the time elapsed between an interrupt and the ISR entry. This register is unused in 16/32-bit GPTM mode.

GPTM Timer B Prescale Value (GPTMTBPV)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

A read returns the current, free-running value of the Timer B prescaler.
Register 27: GPTM Peripheral Properties (GPTMPP), offset 0xFC0

The GPTMPP register provides information regarding the properties of the General-Purpose Timer module.

GPTM Peripheral Properties (GPTMPP)
16/32-bit Timer 0 base: 0x4003.0000
16/32-bit Timer 1 base: 0x4003.1000
16/32-bit Timer 2 base: 0x4003.2000
16/32-bit Timer 3 base: 0x4003.3000
16/32-bit Timer 4 base: 0x4003.4000
16/32-bit Timer 5 base: 0x4003.5000
32/64-bit Wide Timer 0 base: 0x4003.6000
32/64-bit Wide Timer 1 base: 0x4003.7000
32/64-bit Wide Timer 2 base: 0x4004.C000
32/64-bit Wide Timer 3 base: 0x4004.D000
32/64-bit Wide Timer 4 base: 0x4004.E000
32/64-bit Wide Timer 5 base: 0x4004.F000
Offset 0xFC0
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3:0</td>
<td>SIZE</td>
<td>RO</td>
<td>0x0</td>
<td>Count Size</td>
</tr>
</tbody>
</table>

Value Description

0  Timer A and Timer B counters are 16 bits each with an 8-bit prescale counter.
1  Timer A and Timer B counters are 32 bits each with a 16-bit prescale counter.
Watchdog Timers

A watchdog timer can generate a non-maskable interrupt (NMI), a regular interrupt or a reset when a time-out value is reached. The watchdog timer is used to regain control when a system has failed due to a software error or due to the failure of an external device to respond in the expected way. The TM4C123GH6PZ microcontroller has two Watchdog Timer Modules, one module is clocked by the system clock (Watchdog Timer 0) and the other (Watchdog Timer 1) is clocked by the PIOSC. The two modules are identical except that WDT1 is in a different clock domain, and therefore requires synchronizers. As a result, WDT1 has a bit defined in the Watchdog Timer Control (WDTCTL) register to indicate when a write to a WDT1 register is complete. Software can use this bit to ensure that the previous access has completed before starting the next access.

The TM4C123GH6PZ controller has two Watchdog Timer modules with the following features:

- 32-bit down counter with a programmable load register
- Separate watchdog clock with an enable
- Programmable interrupt generation logic with interrupt masking and optional NMI function
- Lock register protection from runaway software
- Reset generation logic with an enable/disable
- User-enabled stalling when the microcontroller asserts the CPU Halt flag during debug

The Watchdog Timer can be configured to generate an interrupt to the controller on its first time-out, and to generate a reset signal on its second time-out. Once the Watchdog Timer has been configured, the lock register can be written to prevent the timer configuration from being inadvertently altered.
12.1 Block Diagram

Figure 12-1. WDT Module Block Diagram

12.2 Functional Description

The Watchdog Timer module generates the first time-out signal when the 32-bit counter reaches the zero state after being enabled; enabling the counter also enables the watchdog timer interrupt. The watchdog interrupt can be programmed to be a non-maskable interrupt (NMI) using the INTTYPE bit in the WDTCTL register. After the first time-out event, the 32-bit counter is re-loaded with the value of the Watchdog Timer Load (WDTLOAD) register, and the timer resumes counting down from that value. Once the Watchdog Timer has been configured, the Watchdog Timer Lock (WDTLOCK) register is written, which prevents the timer configuration from being inadvertently altered by software.

If the timer counts down to its zero state again before the first time-out interrupt is cleared, and the reset signal has been enabled by setting the RESEN bit in the WDTCTL register, the Watchdog timer asserts its reset signal to the system. If the interrupt is cleared before the 32-bit counter reaches its second time-out, the 32-bit counter is loaded with the value in the WDTLOAD register, and counting resumes from that value.

If WDTLOAD is written with a new value while the Watchdog Timer counter is counting, then the counter is loaded with the new value and continues counting.
Writing to **WDTLOAD** does not clear an active interrupt. An interrupt must be specifically cleared by writing to the **Watchdog Interrupt Clear (WDTICR)** register.

The Watchdog module interrupt and reset generation can be enabled or disabled as required. When the interrupt is re-enabled, the 32-bit counter is preloaded with the load register value and not its last state.

The watchdog timer is disabled by default out of reset. To achieve maximum watchdog protection of the device, the watchdog timer can be enabled at the start of the reset vector.

### 12.2.1 Register Access Timing

Because the Watchdog Timer 1 module has an independent clocking domain, its registers must be written with a timing gap between accesses. Software must guarantee that this delay is inserted between back-to-back writes to WDT1 registers or between a write followed by a read to the registers. The timing for back-to-back reads from the WDT1 module has no restrictions. The **WRC** bit in the **Watchdog Control (WDTCTL)** register for WDT1 indicates that the required timing gap has elapsed. This bit is cleared on a write operation and set once the write completes, indicating to software that another write or read may be started safely. Software should poll **WDTCTL** for **WRC=1** prior to accessing another register. Note that WDT0 does not have this restriction as it runs off the system clock.

### 12.3 Initialization and Configuration

To use the WDT, its peripheral clock must be enabled by setting the **Rn** bit in the **Watchdog Timer Run Mode Clock Gating Control (RCGCWD)** register, see page 339.

The Watchdog Timer is configured using the following sequence:

1. Load the **WDTLOAD** register with the desired timer load value.
2. If WDT1, wait for the **WRC** bit in the **WDTCTL** register to be set.
3. If the Watchdog is configured to trigger system resets, set the **RESEN** bit in the **WDTCTL** register.
4. If WDT1, wait for the **WRC** bit in the **WDTCTL** register to be set.
5. Set the **INTEN** bit in the **WDTCTL** register to enable the Watchdog, enable interrupts, and lock the control register.

If software requires that all of the watchdog registers are locked, the Watchdog Timer module can be fully locked by writing any value to the **WDTLOCK** register. To unlock the Watchdog Timer, write a value of 0x1ACC.E551.

To service the watchdog, periodically reload the count value into the **WDTLOAD** register to restart the count. The interrupt can be enabled using the **INTEN** bit in the **WDTCTL** register to allow the processor to attempt corrective action if the watchdog is not serviced often enough. The **RESEN** bit in **WDTCTL** can be set so that the system resets if the failure is not recoverable using the ISR.

### 12.4 Register Map

Table 12-1 on page 791 lists the Watchdog registers. The offset listed is a hexadecimal increment to the register's address, relative to the Watchdog Timer base address:

- WDT0: 0x4000.0000
- WDT1: 0x4000.1000
Note that the Watchdog Timer module clock must be enabled before the registers can be programmed (see page 339).

Table 12-1. Watchdog Timers Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>WDTLOAD</td>
<td>RW</td>
<td>0xFFF.FFFF</td>
<td>Watchdog Load</td>
<td>792</td>
</tr>
<tr>
<td>0x004</td>
<td>WDTVALUE</td>
<td>RO</td>
<td>0xFFF.FFFF</td>
<td>Watchdog Value</td>
<td>793</td>
</tr>
<tr>
<td>0x008</td>
<td>WDTCTL</td>
<td>RW</td>
<td>0x0000.0000 (WDT0) 0x8000.0000 (WDT1)</td>
<td>Watchdog Control</td>
<td>794</td>
</tr>
<tr>
<td>0x00C</td>
<td>WDTICR</td>
<td>WO</td>
<td>-</td>
<td>Watchdog Interrupt Clear</td>
<td>796</td>
</tr>
<tr>
<td>0x010</td>
<td>WDTRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Watchdog Raw Interrupt Status</td>
<td>797</td>
</tr>
<tr>
<td>0x014</td>
<td>WDTMIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Watchdog Masked Interrupt Status</td>
<td>798</td>
</tr>
<tr>
<td>0x418</td>
<td>WDTTEST</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Watchdog Test</td>
<td>799</td>
</tr>
<tr>
<td>0xCO0</td>
<td>WDTLOCK</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Watchdog Lock</td>
<td>800</td>
</tr>
<tr>
<td>0xFD0</td>
<td>WDTPeriphID4</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Watchdog Peripheral Identification 4</td>
<td>801</td>
</tr>
<tr>
<td>0xFD4</td>
<td>WDTPeriphID5</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Watchdog Peripheral Identification 5</td>
<td>802</td>
</tr>
<tr>
<td>0xFD8</td>
<td>WDTPeriphID6</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Watchdog Peripheral Identification 6</td>
<td>803</td>
</tr>
<tr>
<td>0xFDc</td>
<td>WDTPeriphID7</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Watchdog Peripheral Identification 7</td>
<td>804</td>
</tr>
<tr>
<td>0xFE0</td>
<td>WDTPeriphID0</td>
<td>RO</td>
<td>0x0000.0005</td>
<td>Watchdog Peripheral Identification 0</td>
<td>805</td>
</tr>
<tr>
<td>0xFE4</td>
<td>WDTPeriphID1</td>
<td>RO</td>
<td>0x0000.018</td>
<td>Watchdog Peripheral Identification 1</td>
<td>806</td>
</tr>
<tr>
<td>0xFE8</td>
<td>WDTPeriphID2</td>
<td>RO</td>
<td>0x0000.018</td>
<td>Watchdog Peripheral Identification 2</td>
<td>807</td>
</tr>
<tr>
<td>0xFEc</td>
<td>WDTPeriphID3</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>Watchdog Peripheral Identification 3</td>
<td>808</td>
</tr>
<tr>
<td>0xFF0</td>
<td>WDTPrimeCellID0</td>
<td>RO</td>
<td>0x0000.000D</td>
<td>Watchdog PrimeCell Identification 0</td>
<td>809</td>
</tr>
<tr>
<td>0xFF4</td>
<td>WDTPrimeCellID1</td>
<td>RO</td>
<td>0x0000.00F0</td>
<td>Watchdog PrimeCell Identification 1</td>
<td>810</td>
</tr>
<tr>
<td>0xFF8</td>
<td>WDTPrimeCellID2</td>
<td>RO</td>
<td>0x0000.0006</td>
<td>Watchdog PrimeCell Identification 2</td>
<td>811</td>
</tr>
<tr>
<td>0xFFC</td>
<td>WDTPrimeCellID3</td>
<td>RO</td>
<td>0x0000.00B1</td>
<td>Watchdog PrimeCell Identification 3</td>
<td>812</td>
</tr>
</tbody>
</table>

12.5 Register Descriptions

The remainder of this section lists and describes the WDT registers, in numerical order by address offset.
### Register 1: Watchdog Load (WDTLOAD), offset 0x000

This register is the 32-bit interval value used by the 32-bit counter. When this register is written, the value is immediately loaded and the counter restarts counting down from the new value. If the **WDTLOAD** register is loaded with 0x0000.0000, an interrupt is immediately generated.

**Watchdog Load (WDTLOAD)**

WDT0 base: 0x4000.0000  
WDT1 base: 0x4000.1000  
Offset 0x000  
Type RW, reset 0xFFFF.FFFF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WDTLOAD</td>
<td>RW</td>
<td>0xFFFF.FFFF</td>
<td>Watchdog Load Value</td>
</tr>
</tbody>
</table>
Register 2: Watchdog Value (WDTVALUE), offset 0x004

This register contains the current count value of the timer.

Watchdog Value (WDTVALUE)
WDT0 base: 0x4000.0000
WDT1 base: 0x4000.1000
Offset 0x004
Type RO, reset 0xFFFF.FFFF

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WDTVALUE</td>
<td>RO</td>
<td>0xFFFF.FFFF</td>
<td>Watchdog Value</td>
</tr>
</tbody>
</table>

Current value of the 32-bit down counter.
Register 3: Watchdog Control (WDTCTL), offset 0x008

This register is the watchdog control register. The watchdog timer can be configured to generate a reset signal (on second time-out) or an interrupt on time-out.

When the watchdog interrupt has been enabled by setting the INTEN bit, all subsequent writes to the INTEN bit are ignored. The only mechanisms that can re-enable writes to this bit are a hardware reset or a software reset initiated by setting the appropriate bit in the Watchdog Timer Software Reset (SRWD) register.

**Important:** Because the Watchdog Timer 1 module has an independent clocking domain, its registers must be written with a timing gap between accesses. Software must guarantee that this delay is inserted between back-to-back writes to WDT1 registers or between a write followed by a read to the registers. The timing for back-to-back reads from the WDT1 module has no restrictions. The WRC bit in the Watchdog Control (WDTCTL) register for WDT1 indicates that the required timing gap has elapsed. This bit is cleared on a write operation and set once the write completes, indicating to software that another write or read may be started safely. Software should poll WDTCTL for WRC=1 prior to accessing another register. Note that WDT0 does not have this restriction as it runs off the system clock and therefore does not have a WRC bit.

### Watchdog Control (WDTCTL)

<table>
<thead>
<tr>
<th>WDT0 base: 0x4000.0000</th>
<th>WDT1 base: 0x4000.1000</th>
<th>Offset 0x008</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RW, reset 0x0000.0000 (WDT0) and 0x8000.0000 (WDT1)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>WRC</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>1</td>
<td>Write Complete</td>
</tr>
</tbody>
</table>

The WRC values are defined as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>A write access to one of the WDT1 registers is in progress.</td>
</tr>
<tr>
<td>1</td>
<td>A write access is not in progress, and WDT1 registers can be read or written.</td>
</tr>
</tbody>
</table>

**Note:** This bit is reserved for WDT0 and has a reset value of 0.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>30:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>------</td>
<td>-------</td>
<td>------------------------------------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>INTTYPE</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Interrupt Type</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <strong>INTTYPE</strong> values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong>  <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Watchdog interrupt is a standard interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Watchdog interrupt is a non-maskable interrupt.</td>
</tr>
<tr>
<td>1</td>
<td>RESEN</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Reset Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <strong>RESEN</strong> values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong>  <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enable the Watchdog module reset output.</td>
</tr>
<tr>
<td>0</td>
<td>INTEN</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <strong>INTEN</strong> values are defined as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong>  <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Interrupt event disabled. Once this bit is set, it can only be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>cleared by a hardware reset or a software reset initiated by</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>setting the appropriate bit in the **Watchdog Timer Software</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reset (SRWD) register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Interrupt event enabled. Once enabled, all writes are ignored.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Setting this bit enables the Watchdog Timer.</td>
</tr>
</tbody>
</table>
Register 4: Watchdog Interrupt Clear (WDTICR), offset 0x00C

This register is the interrupt clear register. A write of any value to this register clears the Watchdog interrupt and reloads the 32-bit counter from the WDTLOAD register. Write to this register when a watchdog time-out interrupt has occurred to properly service the Watchdog. Value for a read or reset is indeterminate.

**Note:** Locking the watchdog registers by using the WDTLOCK register does not affect the WDTICR register and allows interrupts to always be serviced. Thus, a write at any time of the WDTICR register clears the WDTMIS register and reloads the 32-bit counter from the WDTLOAD register. The WDTICR register should only be written when interrupts have triggered and need to be serviced.

Watchdog Interrupt Clear (WDTICR)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00C</td>
<td>WO, reset</td>
<td>A write of any value to this register clears the Watchdog interrupt and reloads the 32-bit counter from the WDTLOAD register. Write to this register when a watchdog time-out interrupt has occurred to properly service the Watchdog. Value for a read or reset is indeterminate.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WDTINTCLR</td>
<td>WO</td>
<td>-</td>
<td>Watchdog Interrupt Clear</td>
</tr>
</tbody>
</table>
Register 5: Watchdog Raw Interrupt Status (WDTRIS), offset 0x010

This register is the raw interrupt status register. Watchdog interrupt events can be monitored via this register if the controller interrupt is masked.

Watchdog Raw Interrupt Status (WDTRIS)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>WDTRIS</td>
<td>RO</td>
<td>0</td>
<td>Watchdog Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The watchdog has not timed out.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A watchdog time-out event has occurred.</td>
</tr>
</tbody>
</table>
Register 6: Watchdog Masked Interrupt Status (WDTMIS), offset 0x014

This register is the masked interrupt status register. The value of this register is the logical AND of the raw interrupt bit and the Watchdog interrupt enable bit.

Watchdog Masked Interrupt Status (WDTMIS)

<table>
<thead>
<tr>
<th>Offset 0x014</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RO, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>WDTMIS</td>
<td>RO</td>
<td>0</td>
<td>Watchdog Masked Interrupt Status</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The watchdog has not timed out or the watchdog timer interrupt is masked.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A watchdog time-out event has been signalled to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Register 7: Watchdog Test (WDTTEST), offset 0x418**

This register provides user-enabled stalling when the microcontroller asserts the CPU halt flag during debug.

**Watchdog Test (WDTTEST)**
- WDT0 base: 0x4000.0000
- WDT1 base: 0x4000.1000
- Offset 0x418
- Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:9</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>STALL</td>
<td>RW</td>
<td>0</td>
<td>Watchdog Stall Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The watchdog timer continues counting if the microcontroller is stopped with a debugger.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>If the microcontroller is stopped with a debugger, the watchdog timer stops counting. Once the microcontroller is restarted, the watchdog timer resumes counting.</td>
</tr>
<tr>
<td>7:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 8: Watchdog Lock (WDTLOCK), offset 0xC00

Writing 0x1ACC.E551 to the WDTLOCK register enables write access to all other registers. Writing any other value to the WDTLOCK register re-enables the locked state for register writes to all the other registers, except for the Watchdog Test (WDTTEST) register. The locked state will be enabled after 2 clock cycles. Reading the WDTLOCK register returns the lock status rather than the 32-bit value written. Therefore, when write accesses are disabled, reading the WDTLOCK register returns 0x0000.0001 (when locked; otherwise, the returned value is 0x0000.0000 (unlocked)).

Watchdog Lock (WDTLOCK)
WDT0 base: 0x4000.0000
WDT1 base: 0x4000.1000
Offset 0xC00
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>WDTLOCK</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Watchdog Lock</td>
</tr>
</tbody>
</table>

A write of the value 0x1ACC.E551 unlocks the watchdog registers for write access. A write of any other value re-applies the lock, preventing any register updates, except for the WDTTEST register. Avoid writes to the WDTTEST register when the watchdog registers are locked.

A read of this register returns the following values:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000.0001</td>
<td>Locked</td>
</tr>
<tr>
<td>0x0000.0000</td>
<td>Unlocked</td>
</tr>
</tbody>
</table>
Register 9: Watchdog Peripheral Identification 4 (WDTPeriphID4), offset 0xFD0

The **WDTPeriphIDn** registers are hard-coded and the fields within the register determine the reset value.

Watchdog Peripheral Identification 4 (WDTPeriphID4)

- **WDT0 base:** 0x4000.0000
- **WDT1 base:** 0x4000.1000
- **Offset 0xFD0**
- **Type RO, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID4</td>
<td>RO</td>
<td>0x00</td>
<td>WDT Peripheral ID Register [7:0]</td>
</tr>
</tbody>
</table>
Register 10: Watchdog Peripheral Identification 5 (WDTPeriphID5), offset 0xFD4

The WDTPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog Peripheral Identification 5 (WDTPeriphID5)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Base Address</th>
<th>Offset</th>
<th>Type</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Watchdog Peripheral Identification 5 (WDTPeriphID5)</td>
<td>0x4000.0000</td>
<td>0xFD4</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Description: Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 11: Watchdog Peripheral Identification 6 (WDTPeriphID6), offset 0xFD8

The WDTPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog Peripheral Identification 6 (WDTPeriphID6)
WDT0 base: 0x4000.0000
WDT1 base: 0x4000.1000
Offset 0xFD8
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7-0</td>
<td>PID6</td>
<td>RO</td>
<td>0x00</td>
<td>WDT Peripheral ID Register [23:16]</td>
</tr>
</tbody>
</table>
Register 12: Watchdog Peripheral Identification 7 (WDTPeriphID7), offset 0xFDC

The WDTPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog Peripheral Identification 7 (WDTPeriphID7)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID7</td>
<td>RO</td>
<td>0x00</td>
<td>WDT Peripheral ID Register [31:24]</td>
</tr>
</tbody>
</table>
Register 13: Watchdog Peripheral Identification 0 (WDTPeriphID0), offset 0xFE0

The WDTPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

**Watchdog Peripheral Identification 0 (WDTPeriphID0)**

WDT0 base: 0x4000.0000  
WDT1 base: 0x4000.1000  
Offset 0xFE0  
Type RO, reset 0x0000.0005

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID0</td>
<td>RO</td>
<td>0x05</td>
<td>Watchdog Peripheral ID Register [7:0]</td>
</tr>
</tbody>
</table>
Register 14: Watchdog Peripheral Identification 1 (WDTPeriphID1), offset 0xFE4

The WDTPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog Peripheral Identification 1 (WDTPeriphID1)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000.00</td>
<td>31:8</td>
<td>reserved</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>0x18</td>
<td>7:0</td>
<td>PID1</td>
<td>Watchdog Peripheral ID Register [15:8]</td>
</tr>
</tbody>
</table>
Register 15: Watchdog Peripheral Identification 2 (WDTPeriphID2), offset 0xFE8

The WDTPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog Peripheral Identification 2 (WDTPeriphID2)

<table>
<thead>
<tr>
<th>Offset 0xFE8</th>
</tr>
</thead>
</table>

**Type RO, reset 0x0000.0018**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID2</td>
<td>RO</td>
<td>0x18</td>
<td>Watchdog Peripheral ID Register [23:16]</td>
</tr>
</tbody>
</table>
Register 16: Watchdog Peripheral Identification 3 (WDTPeriphID3), offset 0xFEC

The WDTPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog Peripheral Identification 3 (WDTPeriphID3)
WDT0 base: 0x4000.0000
WDT1 base: 0x4000.1000
Offset 0xFEC
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7-0</td>
<td>PID3</td>
<td>RO</td>
<td>0x01</td>
<td>Watchdog Peripheral ID Register [31:24]</td>
</tr>
</tbody>
</table>
Register 17: Watchdog PrimeCell Identification 0 (WDTPCellID0), offset 0xFF0

The WDTPCellIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog PrimeCell Identification 0 (WDTPCellID0)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID0</td>
<td>RO</td>
<td>0x0D</td>
<td>Watchdog PrimeCell ID Register [7:0]</td>
</tr>
</tbody>
</table>
Register 18: Watchdog PrimeCell Identification 1 (WDTPCellID1), offset 0xFF4

The WDTPCellIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog PrimeCell Identification 1 (WDTPCellID1)

WDT0 base: 0x4000.0000
WDT1 base: 0x4000.1000
Offset 0xFF4
Type RO, reset 0x0000.00F0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID1</td>
<td>RO</td>
<td>0xF0</td>
<td>Watchdog PrimeCell ID Register [15:8]</td>
</tr>
</tbody>
</table>
Register 19: Watchdog PrimeCell Identification 2 (WDTPCellID2), offset 0xFF8

The **WDTPCellIDn** registers are hard-coded and the fields within the register determine the reset value.

**Watchdog PrimeCell Identification 2 (WDTPCellID2)**

WDT0 base: 0x4000.0000  
WDT1 base: 0x4000.1000  
Offset 0xFF8

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID2</td>
<td>RO</td>
<td>0x06</td>
<td>Watchdog PrimeCell ID Register [23:16]</td>
</tr>
</tbody>
</table>
Register 20: Watchdog PrimeCell Identification 3 (WDTPCellID3), offset 0xFFC

The WDTPCellIDn registers are hard-coded and the fields within the register determine the reset value.

Watchdog PrimeCell Identification 3 (WDTPCellID3)

- WDT0 base: 0x4000.0000
- WDT1 base: 0x4000.1000
- Offset 0xFFF
- Type RO, reset 0x0000.00B1

---

<table>
<thead>
<tr>
<th>Description</th>
<th>Reset</th>
<th>Type</th>
<th>Bit/Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>0x0000.00</td>
<td>RO</td>
<td>31:8</td>
</tr>
<tr>
<td>Watchdog PrimeCell ID Register [31:24]</td>
<td>0xB1</td>
<td>RO</td>
<td>7:0</td>
</tr>
</tbody>
</table>

---
13 Analog-to-Digital Converter (ADC)

An analog-to-digital converter (ADC) is a peripheral that converts a continuous analog voltage to a discrete digital number. Two identical converter modules are included, which share 22 input channels.

The TM4C123GH6PZ ADC module features 12-bit conversion resolution and supports 22 input channels, plus an internal temperature sensor. Each ADC module contains four programmable sequencers allowing the sampling of multiple analog input sources without controller intervention. Each sample sequencer provides flexible programming with fully configurable input source, trigger events, interrupt generation, and sequencer priority. In addition, the conversion value can optionally be diverted to a digital comparator module. Each ADC module provides eight digital comparators. Each digital comparator evaluates the ADC conversion value against its two user-defined values to determine the operational range of the signal. The trigger source for ADC0 and ADC1 may be independent or the two ADC modules may operate from the same trigger source and operate on the same or different inputs. A phase shifter can delay the start of sampling by a specified phase angle. When using both ADC modules, it is possible to configure the converters to start the conversions coincidentally or within a relative phase from each other, see “Sample Phase Control” on page 819.

The TM4C123GH6PZ microcontroller provides two ADC modules with each having the following features:

- 22 shared analog input channels
- 12-bit precision ADC
- Single-ended and differential-input configurations
- On-chip internal temperature sensor
- Maximum sample rate of one million samples/second
- Optional phase shift in sample time programmable from 22.5º to 337.5º
- Four programmable sample conversion sequencers from one to eight entries long, with corresponding conversion result FIFOs

- Flexible trigger control
  - Controller (software)
  - Timers
  - Analog Comparators
  - PWM
  - GPIO

- Hardware averaging of up to 64 samples

- Eight digital comparators

- Converter uses two external reference signals (VREFA+ and VREFA−) or VDDA and GND as the voltage reference
Power and ground for the analog circuitry is separate from the digital power and ground

- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Dedicated channel for each sample sequencer
  - ADC module uses burst requests for DMA

## 13.1 Block Diagram

The TM4C123GH6PZ microcontroller contains two identical Analog-to-Digital Converter modules. These two modules, ADC0 and ADC1, share the same 22 analog input channels. Each ADC module operates independently and can therefore execute different sample sequences, sample any of the analog input channels at any time, and generate different interrupts and triggers. Figure 13-1 on page 814 shows how the two modules are connected to analog inputs and the system bus.

**Figure 13-1. Implementation of Two ADC Blocks**

![Diagram of two ADC blocks connected to input channels and system bus](image-url)

Figure 13-2 on page 815 provides details on the internal configuration of the ADC controls and data registers.
Figure 13-2. ADC Module Block Diagram

13.2 Signal Description

The following table lists the external signals of the ADC module and describes the function of each. The AINx signals are analog functions for some GPIO signals. The column in the table below titled “Pin Mux/Pin Assignment” lists the GPIO pin placement for the ADC signals. These signals are configured by clearing the corresponding DEN bit in the GPIO Digital Enable (GPIODEN) register and setting the corresponding AMSEL bit in the GPIO Analog Mode Select (GPIOAMSEL) register. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659. The VREFA+ and VREFA− signals (with the word “fixed” in the Pin Mux/Pin Assignment column) have a fixed pin assignment and function and are not 5-V tolerant.

Table 13-1. ADC Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type^2</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIN0</td>
<td>12</td>
<td>PE3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 0.</td>
</tr>
<tr>
<td>AIN1</td>
<td>13</td>
<td>PE2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 1.</td>
</tr>
<tr>
<td>AIN2</td>
<td>14</td>
<td>PE1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 2.</td>
</tr>
<tr>
<td>AIN3</td>
<td>15</td>
<td>PE0</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 3.</td>
</tr>
<tr>
<td>AIN4</td>
<td>100</td>
<td>PD7</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 4.</td>
</tr>
<tr>
<td>AIN5</td>
<td>99</td>
<td>PD6</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 5.</td>
</tr>
<tr>
<td>AIN6</td>
<td>98</td>
<td>PD5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 6.</td>
</tr>
</tbody>
</table>
Table 13-1. ADC Signals (100LQFP) (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Typea</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIN8</td>
<td>96</td>
<td>PE5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 8.</td>
</tr>
<tr>
<td>AIN11</td>
<td>91</td>
<td>PB5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 11.</td>
</tr>
<tr>
<td>AIN12</td>
<td>4</td>
<td>PD3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 12.</td>
</tr>
<tr>
<td>AIN13</td>
<td>3</td>
<td>PD2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 13.</td>
</tr>
<tr>
<td>AIN14</td>
<td>2</td>
<td>PD1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 14.</td>
</tr>
<tr>
<td>AIN15</td>
<td>1</td>
<td>PD0</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 15.</td>
</tr>
<tr>
<td>AIN16</td>
<td>16</td>
<td>PH0</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 16.</td>
</tr>
<tr>
<td>AIN17</td>
<td>17</td>
<td>PH1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 17.</td>
</tr>
<tr>
<td>AIN18</td>
<td>18</td>
<td>PH2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 18.</td>
</tr>
<tr>
<td>AIN19</td>
<td>19</td>
<td>PH3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 19.</td>
</tr>
<tr>
<td>AIN20</td>
<td>90</td>
<td>PE7</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 20.</td>
</tr>
<tr>
<td>AIN21</td>
<td>89</td>
<td>PE6</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 21.</td>
</tr>
<tr>
<td>VREFA+</td>
<td>8</td>
<td>fixed</td>
<td>-</td>
<td>Analog</td>
<td>A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with VREFA–, which specifies the minimum value. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in Table 24-33 on page 1426.</td>
</tr>
<tr>
<td>VREFA–</td>
<td>9</td>
<td>fixed</td>
<td>-</td>
<td>Analog</td>
<td>A reference voltage used to specify the input voltage at which the ADC converts to a minimum value. This pin is used in conjunction with VREFA–, which specifies the maximum value. In other words, the voltage that is applied to VREFA– is the voltage with which an AINn signal is converted to 0, while the voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA– voltage is limited to the range specified in Table 24-33 on page 1426.</td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

13.3 Functional Description

The TM4C123GH6PZ ADC collects sample data by using a programmable sequence-based approach instead of the traditional single or double-sampling approaches found on many ADC modules. Each sample sequence is a fully programmed series of consecutive (back-to-back) samples, allowing the ADC to collect data from multiple input sources without having to be re-configured or serviced by the processor. The programming of each sample in the sample sequence includes parameters such as the input source and mode (differential versus single-ended input), interrupt generation on sample completion, and the indicator for the last sample in the sequence. In addition, the μDMA can be used to more efficiently move data from the sample sequencers without CPU intervention.

13.3.1 Sample Sequencers

The sampling control and data capture is handled by the sample sequencers. All of the sequencers are identical in implementation except for the number of samples that can be captured and the depth
of the FIFO. Table 13-2 on page 817 shows the maximum number of samples that each sequencer can capture and its corresponding FIFO depth. Each sample that is captured is stored in the FIFO. In this implementation, each FIFO entry is a 32-bit word, with the lower 12 bits containing the conversion result.

Table 13-2. Samples and FIFO Depth of Sequencers

<table>
<thead>
<tr>
<th>Sequecer</th>
<th>Number of Samples</th>
<th>Depth of FIFO</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS3</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SS2</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>SS1</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>SS0</td>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

For a given sample sequence, each sample is defined by bit fields in the ADC Sample Sequence Input Multiplexer Select (ADCSSMUXn), ADC Sample Sequence Extended Input Multiplexer Select (ADCSSEMUXn) and ADC Sample Sequence Control (ADCSSCTLn) registers, where "n" corresponds to the sequence number. The ADCSSMUXn and ADCSSEMUXn fields select the input pin, while the ADCSSCTLn fields contain the sample control bits corresponding to parameters such as temperature sensor selection, interrupt enable, end of sequence, and differential input mode. Sample sequencers are enabled by setting the respective ASEn bit in the ADC Active Sample Sequencer (ADCACTSS) register and should be configured before being enabled. Sampling is then initiated by setting the SSn bit in the ADC Processor Sample Sequence Initiate (ADCPSSI) register. In addition, sample sequences may be initiated on multiple ADC modules simultaneously using the GSNC and SYNCWAIT bits in the ADCPSSI register during the configuration of each ADC module. For more information on using these bits, refer to page 859.

When configuring a sample sequence, multiple uses of the same input pin within the same sequence are allowed. In the ADCSSCTLn register, the IEn bits can be set for any combination of samples, allowing interrupts to be generated after every sample in the sequence if necessary. Also, the END bit can be set at any point within a sample sequence. For example, if Sequencer 0 is used, the END bit can be set in the nibble associated with the fifth sample, allowing Sequencer 0 to complete execution of the sample sequence after the fifth sample.

After a sample sequence completes execution, the result data can be retrieved from the ADC Sample Sequence Result FIFO (ADCSSFIFOn) registers. The FIFOs are simple circular buffers that read a single address to "pop" result data. For software debug purposes, the positions of the FIFO head and tail pointers are visible in the ADC Sample Sequence FIFO Status (ADCSSFSTATn) registers along with FULL and EMPTY status flags. If a write is attempted when the FIFO is full, the write does not occur and an overflow condition is indicated. Overflow and underflow conditions are monitored using the ADCOSTAT and ADCUSTAT registers.

13.3.2 Module Control

Outside of the sample sequencers, the remainder of the control logic is responsible for tasks such as:

- Interrupt generation
- DMA operation
- Sequence prioritization
- Trigger configuration
Comparator configuration

■ External voltage reference

■ Sample phase control

■ Module clocking

Most of the ADC control logic runs at the ADC clock rate of 16 MHz. The internal ADC divider is configured for 16-MHz operation automatically by hardware when the system XTAL is selected with the PLL.

13.3.2.1 Interrupts

The register configurations of the sample sequencers and digital comparators dictate which events generate raw interrupts, but do not have control over whether the interrupt is actually sent to the interrupt controller. The ADC module's interrupt signals are controlled by the state of the MASK bits in the ADC Interrupt Mask (ADCIM) register. Interrupt status can be viewed at two locations: the ADC Raw Interrupt Status (ADCRIS) register, which shows the raw status of the various interrupt signals; and the ADC Interrupt Status and Clear (ADCISC) register, which shows active interrupts that are enabled by the ADCIM register. Sequencer interrupts are cleared by writing a 1 to the corresponding IN bit in ADCISC. Digital comparator interrupts are cleared by writing a 1 to the ADC Digital Comparator Interrupt Status and Clear (ADCDCISC) register.

13.3.2.2 DMA Operation

DMA may be used to increase efficiency by allowing each sample sequencer to operate independently and transfer data without processor intervention or reconfiguration. The ADC module provides a request signal from each sample sequencer to the associated dedicated channel of the μDMA controller. The ADC does not support single transfer requests. A burst transfer request is asserted when the interrupt bit for the sample sequence is set (IE bit in the ADCSSCTLn register is set).

The arbitration size of the μDMA transfer must be a power of 2, and the associated IE bits in the ADCSSCTLn register must be set. For example, if the μDMA channel of SS0 has an arbitration size of four, the IE3 bit (4th sample) and the IE7 bit (8th sample) must be set. Thus the μDMA request occurs every time 4 samples have been acquired. No other special steps are needed to enable the ADC module for μDMA operation.

Refer to the "Micro Direct Memory Access (μDMA)" on page 595 for more details about programming the μDMA controller.

13.3.2.3 Prioritization

When sampling events (triggers) happen concurrently, they are prioritized for processing by the values in the ADC Sample Sequencer Priority (ADCSSPRI) register. Valid priority values are in the range of 0-3, with 0 being the highest priority and 3 being the lowest. Multiple active sample sequencer units with the same priority do not provide consistent results, so software must ensure that all active sample sequencer units have a unique priority value.

13.3.2.4 Sampling Events

Sample triggering for each sample sequencer is defined in the ADC Event Multiplexer Select (ADCEMUX) register. Trigger sources include processor (default), analog comparators, an external signal on a GPIO specified by the GPIO ADC Control (GPIOADCCTL) register, a GP Timer, a PWM generator, and continuous sampling. The processor triggers sampling by setting the SSx bits in the ADC Processor Sample Sequence Initiate (ADCPSSI) register.
Care must be taken when using the continuous sampling trigger. If a sequencer's priority is too high, it is possible to starve other lower priority sequencers. Generally, a sample sequencer using continuous sampling should be set to the lowest priority. Continuous sampling can be used with a digital comparator to cause an interrupt when a particular voltage is seen on an input.

13.3.2.5 Sample Phase Control

The trigger source for ADC0 and ADC1 may be independent or the two ADC modules may operate from the same trigger source and operate on the same or different inputs. If the converters are running at the same sample rate, they may be configured to start the conversions coincidently or with one of 15 different discrete phases relative to each other. The sample time can be delayed from the standard sampling time in 22.5° increments up to 337.5° using the ADC Sample Phase Control (ADCSPC) register. Figure 13-3 on page 819 shows an example of various phase relationships at a 1 Mps rate.

Figure 13-3. ADC Sample Phases

This feature can be used to double the sampling rate of an input. Both ADC module 0 and ADC module 1 can be programmed to sample the same input. ADC module 0 could sample at the standard position (the PHASE field in the ADCSPC register is 0x0). ADC module 1 can be configured to sample at 180 (PHASE = 0x8). The two modules can be be synchronized using the GSYNC and SYNCWAIT bits in the ADC Processor Sample Sequence Initiate (ADCPSSI) register. Software could then combine the results from the two modules to create a sample rate of one million samples/second at 16 MHz as shown in Figure 13-4 on page 819.

Figure 13-4. Doubling the ADC Sample Rate

Using the ADCSPC register, ADC0 and ADC1 may provide a number of interesting applications:

- Coincident continuous sampling of different signals. The sample sequence steps run coincidently in both converters.
  - ADC Module 0, ADCSPC = 0x0, sampling AIN0
  - ADC Module 1, ADCSPC = 0x0, sampling AIN1
Note: If two ADCs are configured to sample the same signal, a skew (phase lag) must be added to one of the ADC modules to prevent coincident sampling. Phase lag can be added by programming the PHASE field in the ADCSPC register.

■ Skewed sampling of the same signal. The sample sequence steps are 0.5 µs out of phase with each other for 1 Msps. This configuration doubles the conversion bandwidth of a single input when software combines the results as shown in Figure 13-5 on page 820.

- ADC Module 0, ADCSPC = 0x0, sampling AIN0
- ADC Module 1, ADCSPC = 0x8, sampling AIN0

Figure 13-5. Skewed Sampling

13.3.2.6 Module Clocking
The module is clocked by a 16-MHz clock which can be sourced by a divided version of the PLL output, the PIOSC or an external source connected to MOSC (with the PLL in bypass mode). When the PLL is operating, the ADC clock is derived from the PLL ÷ 25 by default. However, the PIOSC can be used for the module clock using the ADC Clock Configuration (ADCCC) register. To use the PIOSC to clock the ADC, first power up the PLL and then enable the PIOSC in the CS bit field in the ADCCC register, then disable the PLL. When the PLL is bypassed, the module clock source clock attached to the MOSC must be 16 MHz unless the PIOSC is used for the clock source. To use the MOSC to clock the ADC, first power up the PLL and then enable the clock to the ADC module, then disable the PLL and switch to the MOSC for the system clock. The ADC module can continue to operate in Deep-Sleep mode if the PIOSC is the ADC module clock source.

The system clock must be at the same frequency or higher than the ADC clock. All ADC modules share the same clock source to facilitate the synchronization of data samples between conversion units, the selection and programming of which is provided by ADC0's ADCCC register. The ADC modules do not run at different conversion rates.

13.3.2.7 Busy Status
The BUSY bit of the ADCACTSS register is used to indicate when the ADC is busy with a current conversion. When there are no triggers pending which may start a new conversion in the immediate
cycle or next few cycles, the BUSY bit reads as 0. Software must read the status of the BUSY bit as clear before disabling the ADC clock by writing to the Analog-to-Digital Converter Run Mode Clock Gating Control (RCGCADC) register.

13.3.2.8 Dither Enable

The DITHER bit in the ADCCTL register is used to reduce random noise in ADC sampling and keep the ADC operation within the specified performance limits defined in Table 24-33 on page 1426. When taking multiple consecutive samples with the ADC Module, the DITHER bit should be enabled in the ADCCTL register along with hardware averaging in the ADC Sample Averaging Control (ADCSAC) register. The DITHER bit is disabled by default at reset.

13.3.3 Hardware Sample Averaging Circuit

Higher precision results can be generated using the hardware averaging circuit, however, the improved results are at the cost of throughput. Up to 64 samples can be accumulated and averaged to form a single data entry in the sequencer FIFO. Throughput is decreased proportionally to the number of samples in the averaging calculation. For example, if the averaging circuit is configured to average 16 samples, the throughput is decreased by a factor of 16.

By default the averaging circuit is off, and all data from the converter passes through to the sequencer FIFO. The averaging hardware is controlled by the ADC Sample Averaging Control (ADCSAC) register (see page 861). A single averaging circuit has been implemented, thus all input channels receive the same amount of averaging whether they are single-ended or differential.

Figure 13-6 shows an example in which the ADCSAC register is set to 0x2 for 4x hardware oversampling and the IE1 bit is set for the sample sequence, resulting in an interrupt after the second averaged value is stored in the FIFO.

Figure 13-6. Sample Averaging Example
13.3.4 Analog-to-Digital Converter

The Analog-to-Digital Converter (ADC) module uses a Successive Approximation Register (SAR) architecture to deliver a 12-bit, low-power, high-precision conversion value. The successive approximation uses a switched capacitor array to perform the dual functions of sampling and holding the signal as well as providing the 12-bit DAC operation.

Figure 13-7 shows the ADC input equivalency diagram; for parameter values, see “Analog-to-Digital Converter (ADC)” on page 1426.

Figure 13-7. ADC Input Equivalency

The ADC operates from both the 3.3-V analog and 1.2-V digital power supplies. The ADC clock can be configured to reduce power consumption when ADC conversions are not required (see “System Control” on page 227). The analog inputs are connected to the ADC through specially balanced input paths to minimize the distortion and cross-talk on the inputs. Detailed information on the ADC power supplies and analog inputs can be found in “Analog-to-Digital Converter (ADC)” on page 1426.

13.3.4.1 Voltage Reference

The ADC uses internal signals VREFP and VREFN as references to produce a conversion value from the selected analog input. VREFP can be connected to either VREFA+ or VDDA and VREFN can be connected to either VREFA− or GNDA as configured by the VREF bit in the ADC Control (ADCCTL) register, as shown in Figure 13-8.
The range of this conversion value is from 0x000 to 0xFFF. In single-ended-input mode, the 0x000 value corresponds to the voltage level on VREFN; the 0xFFF value corresponds to the voltage level on VREFP. This configuration results in a resolution that can be calculated using the following equation:

\[
mV \text{ per ADC code} = \frac{(V_{REFP} - V_{REFN})}{4096}
\]

While the analog input pads can handle voltages beyond this range, the analog input voltages must remain within the limits prescribed by Table 24-33 on page 1426 to produce accurate results. The \(V_{REFA+}\) and \(V_{REFA-}\) specifications define the useful range for the external voltage references on \(V_{REFA+}\) and \(V_{REFA-}\), see Table 24-33 on page 1426. Care must be taken to supply a reference voltage of acceptable quality. Figure 13-9 on page 824 shows the ADC conversion function of the analog inputs.
13.3.5 Differential Sampling

In addition to traditional single-ended sampling, the ADC module supports differential sampling of two analog input channels. To enable differential sampling, software must set the \( D_n \) bit in the \( \text{ADCSSCTL0n} \) register in a step’s configuration nibble.

When a sequence step is configured for differential sampling, the input pair to sample must be configured in the \( \text{ADCSSMUXn} \) register. Differential pair 0 samples analog inputs 0 and 1; differential pair 1 samples analog inputs 2 and 3; and so on (see Table 13-3 on page 824). The ADC does not support other differential pairings such as analog input 0 with analog input 3.

Table 13-3. Differential Sampling Pairs

<table>
<thead>
<tr>
<th>Differential Pair</th>
<th>Analog Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 and 1</td>
</tr>
<tr>
<td>1</td>
<td>2 and 3</td>
</tr>
<tr>
<td>2</td>
<td>4 and 5</td>
</tr>
<tr>
<td>3</td>
<td>6 and 7</td>
</tr>
<tr>
<td>4</td>
<td>8 and 9</td>
</tr>
<tr>
<td>5</td>
<td>10 and 11</td>
</tr>
<tr>
<td>6</td>
<td>12 and 13</td>
</tr>
</tbody>
</table>
Table 13-3. Differential Sampling Pairs (continued)

<table>
<thead>
<tr>
<th>Differential Pair</th>
<th>Analog Inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>14 and 15</td>
</tr>
<tr>
<td>8</td>
<td>16 and 17</td>
</tr>
<tr>
<td>9</td>
<td>18 and 19</td>
</tr>
<tr>
<td>10</td>
<td>20 and 21</td>
</tr>
</tbody>
</table>

The voltage sampled in differential mode is the difference between the odd and even channels:

- Input Positive Voltage: \( V_{IN+} = V_{IN_{EVEN}} \) (even channel)
- Input Negative Voltage: \( V_{IN-} = V_{IN_{ODD}} \) (odd channel)

The input differential voltage is defined as: \( V_{IN_D} = V_{IN+} - V_{IN-} \), therefore:

- If \( V_{IN_D} = 0 \), then the conversion result = 0x800
- If \( V_{IN_D} > 0 \), then the conversion result > 0x800 (range is 0x800–0xFFF)
- If \( V_{IN_D} < 0 \), then the conversion result < 0x800 (range is 0–0x800)

When using differential sampling, the following definitions are relevant:

- Input Common Mode Voltage: \( V_{IN_{CM}} = (V_{IN+} + V_{IN-}) / 2 \)
- Reference Positive Voltage: \( V_{REFP} \)
- Reference Negative Voltage: \( V_{REFN} \)
- Reference Differential Voltage: \( V_{REF_D} = V_{REFP} - V_{REFN} \)
- Reference Common Mode Voltage: \( V_{REF_{CM}} = (V_{REFP} + V_{REFN}) / 2 \)

The following conditions provide optimal results in differential mode:

- Both \( V_{IN_{EVEN}} \) and \( V_{IN_{ODD}} \) must be in the range of \( V_{REFP} \) to \( V_{REFN} \) for a valid conversion result
- The maximum possible differential input swing, or the maximum differential range, is: \(-V_{REF_D} \) to \(+V_{REF_D}\), so the maximum peak-to-peak input differential signal is \((+V_{REF_D} - -V_{REF_D}) = 2 \times V_{REF_D} = 2 \times (V_{REFP} - V_{REFN})\)
- In order to take advantage of the maximum possible differential input swing, \( V_{IN_{CM}} \) should be very close to \( V_{REF_{CM}} \), see Table 24-33 on page 1426.

If \( V_{IN_{CM}} \) is not equal to \( V_{REF_{CM}} \), the differential input signal may clip at either maximum or minimum voltage, because either single ended input can never be larger than \( V_{REFP} \) or smaller than \( V_{REFN} \), and it is not possible to achieve full swing. Thus any difference in common mode between the input voltage and the reference voltage limits the differential dynamic range of the ADC.

Because the maximum peak-to-peak differential signal voltage is \( 2 \times (V_{REFP} - V_{REFN}) \), the ADC codes are interpreted as:

\[
mV \text{ per ADC code} = \frac{(2 \times (V_{REFP} - V_{REFN}))}{4096}
\]
Figure 13-10 shows how the differential voltage, $\Delta V$, is represented in ADC codes.

**Figure 13-10. Differential Voltage Representation**

13.3.6 **Internal Temperature Sensor**

The temperature sensor serves two primary purposes: 1) to notify the system that internal temperature is too high or low for reliable operation and 2) to provide temperature measurements for calibration of the Hibernate module RTC trim value.

The temperature sensor does not have a separate enable, because it also contains the bandgap reference and must always be enabled. The reference is supplied to other analog modules; not just the ADC. In addition, the temperature sensor has a second power-down input in the 3.3 V domain which provides control by the Hibernation module.

The internal temperature sensor converts a temperature measurement into a voltage. This voltage value, $V_{TSENS}$, is given by the following equation (where TEMP is the temperature in °C):

$$V_{TSENS} = 2.7 - \left(\frac{(TEMP + 55)}{75}\right)$$

This relation is shown in Figure 13-11 on page 827.
The temperature sensor reading can be sampled in a sample sequence by setting the TSn bit in the ADCSSCTLn register. The temperature reading from the temperature sensor can also be given as a function of the ADC value. The following formula calculates temperature (TEMP in °C) based on the ADC reading (ADC_CODE, given as an unsigned decimal number from 0 to 4095) and the maximum ADC voltage range (VREFP - VREFN):

\[ TEMP = 147.5 - \left( \frac{75 \times (VREFP - VREFN) \times ADC_{CODE}}{4096} \right) \]

### 13.3.7 Digital Comparator Unit

An ADC is commonly used to sample an external signal and to monitor its value to ensure that it remains in a given range. To automate this monitoring procedure and reduce the amount of processor overhead that is required, each module provides eight digital comparators.

Conversions from the ADC that are sent to the digital comparators are compared against the user programmable limits in the ADC Digital Comparator Range (ADCDCCMPn) registers. The ADC can be configured to generate an interrupt depending on whether the ADC is operating within the low, mid or high-band region configured in the ADCDCMPn bit fields. The digital comparators four operational modes (Once, Always, Hysteresis Once, Hysteresis Always) can be additionally applied to the interrupt configuration.

#### 13.3.7.1 Output Functions

ADC conversions can either be stored in the ADC Sample Sequence FIFOs or compared using the digital comparator resources as defined by the SnDCOP bits in the ADC Sample Sequence n Operation (ADCSSOPn) register. These selected ADC conversions are used by their respective digital comparator to monitor the external signal. Each comparator has two possible output functions: processor interrupts and triggers.

Each function has its own state machine to track the monitored signal. Even though the interrupt and trigger functions can be enabled individually or both at the same time, the same conversion
data is used by each function to determine if the right conditions have been met to assert the associated output.

**Interrupts**

The digital comparator interrupt function is enabled by setting the CIE bit in the ADC Digital Comparator Control (ADCDCTL<n>) register. This bit enables the interrupt function state machine to start monitoring the incoming ADC conversions. When the appropriate set of conditions is met, and the DCONSSx bit is set in the ADCIM register, an interrupt is sent to the interrupt controller.

**Note:** Only a single DCONSSn bit should be set at any given time. Setting more than one of these bits results in the INRDC bit from the ADCRIS register being masked, and no interrupt is generated on any of the sample sequencer interrupt lines. It is recommended that when interrupts are used, they are enabled on alternating samples or at the end of the sample sequence.

**Triggers**

The digital comparator trigger function is enabled by setting the CTE bit in the ADCDCCTL<n> register. This bit enables the trigger function state machine to start monitoring the incoming ADC conversions. When the appropriate set of conditions is met, the corresponding digital comparator trigger to the PWM module is asserted.

### 13.3.7.2 Operational Modes

Four operational modes are provided to support a broad range of applications and multiple possible signaling requirements: Always, Once, Hysteresis Always, and Hysteresis Once. The operational mode is selected using the CIM or CTM field in the ADCDCCTL<n> register.

**Always Mode**

In the Always operational mode, the associated interrupt or trigger is asserted whenever the ADC conversion value meets its comparison criteria. The result is a string of assertions on the interrupt or trigger while the conversions are within the appropriate range.

**Once Mode**

In the Once operational mode, the associated interrupt or trigger is asserted whenever the ADC conversion value meets its comparison criteria, and the previous ADC conversion value did not. The result is a single assertion of the interrupt or trigger when the conversions are within the appropriate range.

**Hysteresis-Always Mode**

The Hysteresis-Always operational mode can only be used in conjunction with the low-band or high-band regions because the mid-band region must be crossed and the opposite region entered to clear the hysteresis condition. In the Hysteresis-Always mode, the associated interrupt or trigger is asserted in the following cases: 1) the ADC conversion value meets its comparison criteria or 2) a previous ADC conversion value has met the comparison criteria, and the hysteresis condition has not been cleared by entering the opposite region. The result is a string of assertions on the interrupt or trigger that continue until the opposite region is entered.

**Hysteresis-Once Mode**

The Hysteresis-Once operational mode can only be used in conjunction with the low-band or high-band regions because the mid-band region must be crossed and the opposite region entered to clear the hysteresis condition. In the Hysteresis-Once mode, the associated interrupt or trigger
is asserted only when the ADC conversion value meets its comparison criteria, the hysteresis condition is clear, and the previous ADC conversion did not meet the comparison criteria. The result is a single assertion on the interrupt or trigger.

### 13.3.7.3 Function Ranges

The two comparison values, COMP0 and COMP1, in the ADC Digital Comparator Range (ADCDCCMPn) register effectively break the conversion area into three distinct regions. These regions are referred to as the low-band (less than COMP0), mid-band (greater than COMP0 but less than or equal to COMP1), and high-band (greater than or equal to COMP1) regions. COMP0 and COMP1 may be programmed to the same value, effectively creating two regions, but COMP1 must always be greater than or equal to the value of COMP0. A COMP1 value that is less than COMP0 generates unpredictable results.

#### Low-Band Operation

To operate in the low-band region, the CIC field or the CTC field in the ADCDCCTLn register must be programmed to 0x0. This setting causes interrupts or triggers to be generated in the low-band region as defined by the programmed operational mode. An example of the state of the interrupt/trigger signal in the low-band region for each of the operational modes is shown in Figure 13-12 on page 829. Note that a “0” in a column following the operational mode name (Always, Once, Hysteresis Always, and Hysteresis Once) indicates that the interrupt or trigger signal is deasserted and a “1” indicates that the signal is asserted.

#### Figure 13-12. Low-Band Operation (CIC=0x0 and/or CTC=0x0)

![Diagram](image)

#### Mid-Band Operation

To operate in the mid-band region, the CIC field or the CTC field in the ADCDCCTLn register must be programmed to 0x1. This setting causes interrupts or triggers to be generated in the mid-band region according the operation mode. Only the Always and Once operational modes are available in the mid-band region. An example of the state of the interrupt/trigger signal in the mid-band region
for each of the allowed operational modes is shown in Figure 13-13 on page 830. Note that a "0" in a column following the operational mode name (Always or Once) indicates that the interrupt or trigger signal is deasserted and a "1" indicates that the signal is asserted.

**Figure 13-13. Mid-Band Operation (CIC=0x1 and/or CTC=0x1)**

![Graph showing mid-band operation](image)

**High-Band Operation**

To operate in the high-band region, the CIC field or the CTC field in the ADCDCCTLn register must be programmed to 0x3. This setting causes interrupts or triggers to be generated in the high-band region according the operation mode. An example of the state of the interrupt/trigger signal in the high-band region for each of the allowed operational modes is shown in Figure 13-14 on page 831. Note that a "0" in a column following the operational mode name (Always, Once, Hysteresis Always, and Hysteresis Once) indicates that the interrupt or trigger signal is deasserted and a "1" indicates that the signal is asserted.
13.4 Initialization and Configuration

In order for the ADC module to be used, the PLL must be enabled and programmed to a supported crystal frequency in the RCC register (see page 254). Using unsupported frequencies can cause faulty operation in the ADC module.

13.4.1 Module Initialization

Initialization of the ADC module is a simple process with very few steps: enabling the clock to the ADC, disabling the analog isolation circuit associated with all inputs that are to be used, and reconfiguring the sample sequencer priorities (if needed).

The initialization sequence for the ADC is as follows:

1. Enable the ADC clock using the RCGCADC register (see page 355).

2. Enable the clock to the appropriate GPIO modules via the RCGCGPIO register (see page 342). To find out which GPIO ports to enable, refer to “Signal Description” on page 815.

3. Set the GPIO AFSEL bits for the ADC input pins (see page 684). To determine which GPIOs to configure, see Table 23-4 on page 1377.

4. Configure the AINx signals to be analog inputs by clearing the corresponding DEN bit in the GPIO Digital Enable (GPIODEN) register (see page 695).

5. Disable the analog isolation circuit for all ADC input pins that are to be used by writing a 1 to the appropriate bits of the GPIOAMSEL register (see page 700) in the associated GPIO block.
If required by the application, reconfigure the sample sequencer priorities in the ADCSSPRI register. The default configuration has Sample Sequencer 0 with the highest priority and Sample Sequencer 3 as the lowest priority.

13.4.2 Sample Sequencer Configuration

Configuration of the sample sequencers is slightly more complex than the module initialization because each sample sequencer is completely programmable.

The configuration for each sample sequencer should be as follows:

1. Ensure that the sample sequencer is disabled by clearing the corresponding ASEn bit in the ADCACTSS register. Programming of the sample sequencers is allowed without having them enabled. Disabling the sequencer during programming prevents erroneous execution if a trigger event were to occur during the configuration process.

2. Configure the trigger event for the sample sequencer in the ADCEMUX register.

3. When using a PWM generator as the trigger source, use the ADC Trigger Source Select (ADCTSSEL) register to specify in which PWM module the generator is located. The default register reset selects PWM module 0 for all generators.

4. For each sample in the sample sequence, configure the corresponding input source in the ADCSSMUXn and ADCSSEMUXn registers.

5. For each sample in the sample sequence, configure the sample control bits in the corresponding nibble in the ADCSSCTLn register. When programming the last nibble, ensure that the END bit is set. Failure to set the END bit causes unpredictable behavior.

6. If interrupts are to be used, set the corresponding MASK bit in the ADCIM register.

7. Enable the sample sequencer logic by setting the corresponding ASEn bit in the ADCACTSS register.

13.5 Register Map

Table 13-4 on page 832 lists the ADC registers. The offset listed is a hexadecimal increment to the register's address, relative to that ADC module's base address of:

- ADC0: 0x4003.8000
- ADC1: 0x4003.9000

Note that the ADC module clock must be enabled before the registers can be programmed (see page 355). There must be a delay of 3 system clocks after the ADC module clock is enabled before any ADC module registers are accessed.

Table 13-4. ADC Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>ADCACTSS</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Active Sample Sequencer</td>
<td>835</td>
</tr>
<tr>
<td>0x004</td>
<td>ADRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>ADC Raw Interrupt Status</td>
<td>837</td>
</tr>
<tr>
<td>0x008</td>
<td>ADCIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Interrupt Mask</td>
<td>839</td>
</tr>
</tbody>
</table>
Table 13-4. ADC Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00C</td>
<td>ADCISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>ADC Interrupt Status and Clear</td>
<td>842</td>
</tr>
<tr>
<td>0x010</td>
<td>ADCCOSTAT</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>ADC Overflow Status</td>
<td>845</td>
</tr>
<tr>
<td>0x014</td>
<td>ADCEMUX</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Event Multiplexer Select</td>
<td>847</td>
</tr>
<tr>
<td>0x018</td>
<td>ADCUSTAT</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>ADC Underflow Status</td>
<td>852</td>
</tr>
<tr>
<td>0x01C</td>
<td>ADCTSSEL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Trigger Source Select</td>
<td>853</td>
</tr>
<tr>
<td>0x020</td>
<td>ADCSSPRI</td>
<td>RW</td>
<td>0x0000.3210</td>
<td>ADC Sample Sequencer Priority</td>
<td>855</td>
</tr>
<tr>
<td>0x024</td>
<td>ADCSPC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Phase Control</td>
<td>857</td>
</tr>
<tr>
<td>0x028</td>
<td>ADCPSSI</td>
<td>RW</td>
<td>-</td>
<td>ADC Processor Sample Sequence Initiate</td>
<td>859</td>
</tr>
<tr>
<td>0x030</td>
<td>ADCSAC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Averaging Control</td>
<td>861</td>
</tr>
<tr>
<td>0x034</td>
<td>ADCDCISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Interrupt Status and Clear</td>
<td>862</td>
</tr>
<tr>
<td>0x038</td>
<td>ADCCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Control</td>
<td>864</td>
</tr>
<tr>
<td>0x040</td>
<td>ADCSSMUX0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Input Multiplexer Select 0</td>
<td>865</td>
</tr>
<tr>
<td>0x044</td>
<td>ADCSSCTRL0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Control 0</td>
<td>867</td>
</tr>
<tr>
<td>0x048</td>
<td>ADCSSFIFO0</td>
<td>RO</td>
<td>-</td>
<td>ADC Sample Sequence Result FIFO 0</td>
<td>874</td>
</tr>
<tr>
<td>0x04C</td>
<td>ADCSSFSTAT0</td>
<td>RO</td>
<td>0x0000.0100</td>
<td>ADC Sample Sequence FIFO 0 Status</td>
<td>875</td>
</tr>
<tr>
<td>0x050</td>
<td>ADCSSOP0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence 0 Operation</td>
<td>877</td>
</tr>
<tr>
<td>0x054</td>
<td>ADCSSDC0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence 0 Digital Comparator Select</td>
<td>879</td>
</tr>
<tr>
<td>0x058</td>
<td>ADCSSEMUX0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Extended Input Multiplexer Select 0</td>
<td>881</td>
</tr>
<tr>
<td>0x060</td>
<td>ADCSSMUX1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Input Multiplexer Select 1</td>
<td>883</td>
</tr>
<tr>
<td>0x064</td>
<td>ADCSSCTRL1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Control 1</td>
<td>884</td>
</tr>
<tr>
<td>0x068</td>
<td>ADCSSFIFO1</td>
<td>RO</td>
<td>-</td>
<td>ADC Sample Sequence Result FIFO 1</td>
<td>874</td>
</tr>
<tr>
<td>0x06C</td>
<td>ADCSSFSTAT1</td>
<td>RO</td>
<td>0x0000.0100</td>
<td>ADC Sample Sequence FIFO 1 Status</td>
<td>875</td>
</tr>
<tr>
<td>0x070</td>
<td>ADCSSOP1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence 1 Operation</td>
<td>888</td>
</tr>
<tr>
<td>0x074</td>
<td>ADCSSDC1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence 1 Digital Comparator Select</td>
<td>889</td>
</tr>
<tr>
<td>0x078</td>
<td>ADCSSEMUX1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Extended Input Multiplexer Select 1</td>
<td>891</td>
</tr>
<tr>
<td>0x080</td>
<td>ADCSSMUX2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Input Multiplexer Select 2</td>
<td>883</td>
</tr>
<tr>
<td>0x084</td>
<td>ADCSSCTRL2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Control 2</td>
<td>884</td>
</tr>
<tr>
<td>0x088</td>
<td>ADCSSFIFO2</td>
<td>RO</td>
<td>-</td>
<td>ADC Sample Sequence Result FIFO 2</td>
<td>874</td>
</tr>
<tr>
<td>0x08C</td>
<td>ADCSSFSTAT2</td>
<td>RO</td>
<td>0x0000.0100</td>
<td>ADC Sample Sequence FIFO 2 Status</td>
<td>875</td>
</tr>
<tr>
<td>0x090</td>
<td>ADCSSOP2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence 2 Operation</td>
<td>888</td>
</tr>
<tr>
<td>0x094</td>
<td>ADCSSDC2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence 2 Digital Comparator Select</td>
<td>889</td>
</tr>
</tbody>
</table>
### Table 13-4. ADC Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x098</td>
<td>ADCSSEMUX2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Extended Input Multiplexer Select 2</td>
<td>891</td>
</tr>
<tr>
<td>0x0A0</td>
<td>ADCSSMUX3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Input Multiplexer Select 3</td>
<td>893</td>
</tr>
<tr>
<td>0x0A4</td>
<td>ADCSSCTL3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Control 3</td>
<td>894</td>
</tr>
<tr>
<td>0x0A8</td>
<td>ADCSSFIFO3</td>
<td>RO</td>
<td>-</td>
<td>ADC Sample Sequence Result FIFO 3</td>
<td>874</td>
</tr>
<tr>
<td>0x0AC</td>
<td>ADCSSFSTAT3</td>
<td>RO</td>
<td>0x0000.0100</td>
<td>ADC Sample Sequence FIFO 3 Status</td>
<td>875</td>
</tr>
<tr>
<td>0x0B0</td>
<td>ADCSSOP3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence 3 Operation</td>
<td>896</td>
</tr>
<tr>
<td>0x0B4</td>
<td>ADCSSDC3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence 3 Digital Comparator Select</td>
<td>897</td>
</tr>
<tr>
<td>0x0B8</td>
<td>ADCSSEMUX3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Sample Sequence Extended Input Multiplexer Select 3</td>
<td>898</td>
</tr>
<tr>
<td>0xD00</td>
<td>ADCDCRIC</td>
<td>WO</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Reset Initial Conditions</td>
<td>899</td>
</tr>
<tr>
<td>0x0E00</td>
<td>ADCDCCTL0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Control 0</td>
<td>904</td>
</tr>
<tr>
<td>0x0E04</td>
<td>ADCDCCTL1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Control 1</td>
<td>904</td>
</tr>
<tr>
<td>0x0E08</td>
<td>ADCDCCTL2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Control 2</td>
<td>904</td>
</tr>
<tr>
<td>0x0E0C</td>
<td>ADCDCCTL3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Control 3</td>
<td>904</td>
</tr>
<tr>
<td>0x0E10</td>
<td>ADCDCCTL4</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Control 4</td>
<td>904</td>
</tr>
<tr>
<td>0x0E14</td>
<td>ADCDCCTL5</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Control 5</td>
<td>904</td>
</tr>
<tr>
<td>0x0E18</td>
<td>ADCDCCTL6</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Control 6</td>
<td>904</td>
</tr>
<tr>
<td>0x0E1C</td>
<td>ADCDCCTL7</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Control 7</td>
<td>904</td>
</tr>
<tr>
<td>0x0E40</td>
<td>ADCDCCMP0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Range 0</td>
<td>907</td>
</tr>
<tr>
<td>0x0E44</td>
<td>ADCDCMP1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Range 1</td>
<td>907</td>
</tr>
<tr>
<td>0x0E48</td>
<td>ADCDCMP2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Range 2</td>
<td>907</td>
</tr>
<tr>
<td>0x0E4C</td>
<td>ADCDCMP3</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Range 3</td>
<td>907</td>
</tr>
<tr>
<td>0x0E50</td>
<td>ADCDCMP4</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Range 4</td>
<td>907</td>
</tr>
<tr>
<td>0x0E54</td>
<td>ADCDCMP5</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Range 5</td>
<td>907</td>
</tr>
<tr>
<td>0x0E58</td>
<td>ADCDCMP6</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Range 6</td>
<td>907</td>
</tr>
<tr>
<td>0x0E5C</td>
<td>ADCDCMP7</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Digital Comparator Range 7</td>
<td>907</td>
</tr>
<tr>
<td>0xFC0</td>
<td>ADCPP</td>
<td>RO</td>
<td>0x00B0.2167</td>
<td>ADC Peripheral Properties</td>
<td>908</td>
</tr>
<tr>
<td>0xFC4</td>
<td>ADCPC</td>
<td>RW</td>
<td>0x0000.0007</td>
<td>ADC Peripheral Configuration</td>
<td>910</td>
</tr>
<tr>
<td>0xFC8</td>
<td>ADCCC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>ADC Clock Configuration</td>
<td>911</td>
</tr>
</tbody>
</table>

### 13.6 Register Descriptions

The remainder of this section lists and describes the ADC registers, in numerical order by address offset.
Register 1: ADC Active Sample Sequencer (ADCACTSS), offset 0x000

This register controls the activation of the sample sequencers. Each sample sequencer can be enabled or disabled independently.

ADC Active Sample Sequencer (ADCACTSS)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>0</td>
<td>ADC Busy</td>
<td>1</td>
</tr>
<tr>
<td>Sample Sequencer 3 is disabled.</td>
<td>0</td>
<td>Sample Sequencer 3 is enabled.</td>
<td>1</td>
</tr>
<tr>
<td>Sample Sequencer 2 is disabled.</td>
<td>0</td>
<td>Sample Sequencer 2 is enabled.</td>
<td>1</td>
</tr>
<tr>
<td>Sample Sequencer 1 is disabled.</td>
<td>0</td>
<td>Sample Sequencer 1 is enabled.</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>BUSY</td>
<td>RO</td>
<td>0</td>
<td>ADC Busy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 ADC is idle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 ADC is busy</td>
</tr>
<tr>
<td>15:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>ASEN3</td>
<td>RW</td>
<td>0</td>
<td>ADC SS3 Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Sample Sequencer 3 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Sample Sequencer 3 is enabled.</td>
</tr>
<tr>
<td>2</td>
<td>ASEN2</td>
<td>RW</td>
<td>0</td>
<td>ADC SS2 Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Sample Sequencer 2 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Sample Sequencer 2 is enabled.</td>
</tr>
<tr>
<td>1</td>
<td>ASEN1</td>
<td>RW</td>
<td>0</td>
<td>ADC SS1 Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Sample Sequencer 1 is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Sample Sequencer 1 is enabled.</td>
</tr>
</tbody>
</table>
### Analog-to-Digital Converter (ADC)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ASEN0</td>
<td>RW</td>
<td>0</td>
<td>ADC SS0 Enable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Sample Sequencer 0 is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>Sample Sequencer 0 is enabled.</td>
</tr>
</tbody>
</table>
Register 2: ADC Raw Interrupt Status (ADCRIS), offset 0x004

This register shows the status of the raw interrupt signal of each sample sequencer. These bits may be polled by software to look for interrupt conditions without sending the interrupts to the interrupt controller.

ADC Raw Interrupt Status (ADCRIS)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x004
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:17</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>16</td>
<td>INRDC</td>
<td>RO</td>
<td>0</td>
<td>Digital Comparator Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>All bits in the ADCDCISC register are clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>At least one bit in the ADCDCISC register is set, meaning that a digital comparator interrupt has occurred.</td>
</tr>
<tr>
<td>15:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>INR3</td>
<td>RO</td>
<td>0</td>
<td>SS3 Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A sample has completed conversion and the respective ADCSSCTL3 IEn bit is set, enabling a raw interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the IN3 bit in the ADCISC register.</td>
</tr>
<tr>
<td>2</td>
<td>INR2</td>
<td>RO</td>
<td>0</td>
<td>SS2 Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A sample has completed conversion and the respective ADCSSCTL2 IEn bit is set, enabling a raw interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the IN2 bit in the ADCISC register.</td>
</tr>
</tbody>
</table>
### SS1 Raw Interrupt Status

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>INR1</td>
<td>RO</td>
<td>0</td>
<td>SS1 Raw Interrupt Status</td>
</tr>
</tbody>
</table>

**Value** | **Description**
--- | ---
0 | An interrupt has not occurred.
1 | A sample has completed conversion and the respective ADCSSCTL1 EEn bit is set, enabling a raw interrupt.

This bit is cleared by writing a 1 to the IN1 bit in the ADCISC register.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>INR0</td>
<td>RO</td>
<td>0</td>
<td>SS0 Raw Interrupt Status</td>
</tr>
</tbody>
</table>

**Value** | **Description**
--- | ---
0 | An interrupt has not occurred.
1 | A sample has completed conversion and the respective ADCSSCTL0 EEn bit is set, enabling a raw interrupt.

This bit is cleared by writing a 1 to the IN0 bit in the ADCISC register.
Register 3: ADC Interrupt Mask (ADCIM), offset 0x008

This register controls whether the sample sequencer and digital comparator raw interrupt signals are sent to the interrupt controller. Each raw interrupt signal can be masked independently.

**Note:** Only a single DCONSSn bit should be set at any given time. Setting more than one of these bits results in the INRDC bit from the ADCRIS register being masked, and no interrupt is generated on any of the sample sequencer interrupt lines. It is recommended that when interrupts are used, they are enabled on alternating samples or at the end of the sample sequence.

ADC Interrupt Mask (ADCIM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19</td>
<td>DCONSS3</td>
<td>RW</td>
<td>0</td>
<td>Digital Comparator Interrupt on SS3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>18</td>
<td>DCONSS2</td>
<td>RW</td>
<td>0</td>
<td>Digital Comparator Interrupt on SS2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
### Digital Comparator Interrupt on SS1

**Description**

The status of the digital comparators does not affect the SS1 interrupt status.

**Value**

0  The status of the digital comparators does not affect the SS1 interrupt status.

1  The raw interrupt signal from the digital comparators (INRDC bit in the ADCRIS register) is sent to the interrupt controller on the SS1 interrupt line.

### Digital Comparator Interrupt on SS0

**Description**

The status of the digital comparators does not affect the SS0 interrupt status.

**Value**

0  The status of the digital comparators does not affect the SS0 interrupt status.

1  The raw interrupt signal from the digital comparators (INRDC bit in the ADCRIS register) is sent to the interrupt controller on the SS0 interrupt line.

### Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

**Value**

0  Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

### SS3 Interrupt Mask

**Description**

The status of Sample Sequencer 3 does not affect the SS3 interrupt status.

**Value**

0  The status of Sample Sequencer 3 does not affect the SS3 interrupt status.

1  The raw interrupt signal from Sample Sequencer 3 (ADCRIS register INR3 bit) is sent to the interrupt controller.

### SS2 Interrupt Mask

**Description**

The status of Sample Sequencer 2 does not affect the SS2 interrupt status.

**Value**

0  The status of Sample Sequencer 2 does not affect the SS2 interrupt status.

1  The raw interrupt signal from Sample Sequencer 2 (ADCRIS register INR2 bit) is sent to the interrupt controller.

### SS1 Interrupt Mask

**Description**

The status of Sample Sequencer 1 does not affect the SS1 interrupt status.

**Value**

0  The status of Sample Sequencer 1 does not affect the SS1 interrupt status.

1  The raw interrupt signal from Sample Sequencer 1 (ADCRIS register INR1 bit) is sent to the interrupt controller.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>MASK0</td>
<td>RW</td>
<td>0</td>
<td>SS0 Interrupt Mask</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The status of Sample Sequencer 0 does not affect the SS0 interrupt status.</td>
</tr>
<tr>
<td>1</td>
<td>The raw interrupt signal from Sample Sequencer 0 (ADCRIS register INR0 bit) is sent to the interrupt controller.</td>
</tr>
</tbody>
</table>
Register 4: ADC Interrupt Status and Clear (ADCISC), offset 0x00C

This register provides the mechanism for clearing sample sequencer interrupt conditions and shows the status of interrupts generated by the sample sequencers and the digital comparators which have been sent to the interrupt controller. When read, each bit field is the logical AND of the respective INR and MASK bits. Sample sequencer interrupts are cleared by writing a 1 to the corresponding bit position. Digital comparator interrupts are cleared by writing a 1 to the appropriate bits in the ADCDCISC register. If software is polling the ADCRIS instead of generating interrupts, the sample sequence INRn bits are still cleared via the ADCISC register, even if the INn bit is not set.

ADC Interrupt Status and Clear (ADCISC)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x00C
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19</td>
<td>DCINSS3</td>
<td>RO</td>
<td>0</td>
<td>Digital Comparator Interrupt Status on SS3</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No interrupt has occurred or the interrupt is masked.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Both the INRDC bit in the ADCRIS register and the DCINSS3 bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to it. Clearing this bit also clears the INRDC bit in the ADCRIS register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>DCINSS2</td>
<td>RO</td>
<td>0</td>
<td>Digital Comparator Interrupt Status on SS2</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No interrupt has occurred or the interrupt is masked.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Both the INRDC bit in the ADCRIS register and the DCINSS2 bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to it. Clearing this bit also clears the INRDC bit in the ADCRIS register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>17</td>
<td>DCINSS1</td>
<td>RO</td>
<td>0</td>
<td>Digital Comparator Interrupt Status on SS1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to it. Clearing this bit also clears the INRDC bit in the ADCRIS register.</td>
</tr>
<tr>
<td>16</td>
<td>DCINSS0</td>
<td>RO</td>
<td>0</td>
<td>Digital Comparator Interrupt Status on SS0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to it. Clearing this bit also clears the INRDC bit in the ADCRIS register.</td>
</tr>
<tr>
<td>15:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>IN3</td>
<td>RW1C</td>
<td>0</td>
<td>SS3 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1. Clearing this bit also clears the INR3 bit in the ADCRIS register.</td>
</tr>
<tr>
<td>2</td>
<td>IN2</td>
<td>RW1C</td>
<td>0</td>
<td>SS2 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1. Clearing this bit also clears the INR2 bit in the ADCRIS register.</td>
</tr>
</tbody>
</table>
### SS1 Interrupt Status and Clear

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>IN1</td>
<td>RW1C</td>
<td>0</td>
<td>SS1 Interrupt Status and Clear</td>
</tr>
</tbody>
</table>

**Value**  
0  
1  Both the INR1 bit in the ADCRIS register and the MASK1 bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller.  

This bit is cleared by writing a 1. Clearing this bit also clears the INR1 bit in the ADCRIS register.

### SS0 Interrupt Status and Clear

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>IN0</td>
<td>RW1C</td>
<td>0</td>
<td>SS0 Interrupt Status and Clear</td>
</tr>
</tbody>
</table>

**Value**  
0  
1  Both the INR0 bit in the ADCRIS register and the MASK0 bit in the ADCIM register are set, providing a level-based interrupt to the interrupt controller.  

This bit is cleared by writing a 1. Clearing this bit also clears the INR0 bit in the ADCRIS register.
Register 5: ADC Overflow Status (ADCOSTAT), offset 0x010

This register indicates overflow conditions in the sample sequencer FIFOs. Once the overflow condition has been handled by software, the condition can be cleared by writing a 1 to the corresponding bit position.

ADC Overflow Status (ADCOSTAT)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x010
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>OV3</td>
<td>RW1C</td>
<td>0</td>
<td>SS3 FIFO Overflow</td>
</tr>
<tr>
<td>2</td>
<td>OV2</td>
<td>RW1C</td>
<td>0</td>
<td>SS2 FIFO Overflow</td>
</tr>
<tr>
<td>1</td>
<td>OV1</td>
<td>RW1C</td>
<td>0</td>
<td>SS1 FIFO Overflow</td>
</tr>
</tbody>
</table>

Value  Description
0  The FIFO has not overflowed.
1  The FIFO for Sample Sequencer 3 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped.

This bit is cleared by writing a 1.

Value  Description
0  The FIFO has not overflowed.
1  The FIFO for Sample Sequencer 2 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped.

This bit is cleared by writing a 1.

Value  Description
0  The FIFO has not overflowed.
1  The FIFO for Sample Sequencer 1 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped.

This bit is cleared by writing a 1.
The FIFO for Sample Sequencer 0 has hit an overflow condition, meaning that the FIFO is full and a write was requested. When an overflow is detected, the most recent write is dropped.

This bit is cleared by writing a 1.
Register 6: ADC Event Multiplexer Select (ADCEMUX), offset 0x014

The ADCEMUX selects the event (trigger) that initiates sampling for each sample sequencer. Each sample sequencer can be configured with a unique trigger source. When using a PWM generator as the trigger source, the ADCEMUX register selects which generator within a PWM module is used as a trigger and the PSn field in the ADC Trigger Source Select (ADCTSSEL) register specifies the PWM module instance in which the generator is located.

ADC Event Multiplexer Select (ADCEMUX)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x014
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
### SS3 Trigger Select

This field selects the trigger source for Sample Sequencer 3. The valid configurations for this field are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Event</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Processor (default)</td>
<td>The trigger is initiated by setting the <code>SSn</code> bit in the <code>ADCPSSI</code> register.</td>
</tr>
<tr>
<td>0x1</td>
<td>Analog Comparator 0</td>
<td>This trigger is configured by the <code>Analog Comparator Control 0 (ACCTL0)</code> register (page 1248).</td>
</tr>
<tr>
<td>0x2</td>
<td>Analog Comparator 1</td>
<td>This trigger is configured by the <code>Analog Comparator Control 1 (ACCTL1)</code> register (page 1248).</td>
</tr>
<tr>
<td>0x3</td>
<td>Analog Comparator 2</td>
<td>This trigger is configured by the <code>Analog Comparator Control 2 (ACCTL2)</code> register (page 1248).</td>
</tr>
<tr>
<td>0x4</td>
<td>External (GPIO Pins)</td>
<td>This trigger is connected to the GPIO interrupt for the corresponding GPIO (see “ADC Trigger Source” on page 666).</td>
</tr>
<tr>
<td>0x5</td>
<td>Timer</td>
<td>In addition, the trigger must be enabled with the <code>TnOTE</code> bit in the <code>GPTMCTL</code> register (page 751).</td>
</tr>
<tr>
<td>0x6</td>
<td>PWM generator 0</td>
<td>The PWM generator 0 trigger can be configured with the <code>PWM0 Interrupt and Trigger Enable (PWM0INTEN)</code> register (page 1296).</td>
</tr>
<tr>
<td>0x7</td>
<td>PWM generator 1</td>
<td>The PWM generator 1 trigger can be configured with the <code>PWM1INTEN</code> register (page 1296).</td>
</tr>
<tr>
<td>0x8</td>
<td>PWM generator 2</td>
<td>The PWM generator 2 trigger can be configured with the <code>PWM2INTEN</code> register (page 1296).</td>
</tr>
<tr>
<td>0x9</td>
<td>PWM generator 3</td>
<td>The PWM generator 3 trigger can be configured with the <code>PWM3INTEN</code> register (page 1296).</td>
</tr>
<tr>
<td>0xA-0xE</td>
<td>reserved</td>
<td></td>
</tr>
<tr>
<td>0xF</td>
<td>Always (continuously sample)</td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
</tr>
<tr>
<td>11:8</td>
<td>EM2</td>
<td>RW</td>
</tr>
</tbody>
</table>

This field selects the trigger source for Sample Sequencer 2. The valid configurations for this field are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Processor (default)</td>
</tr>
<tr>
<td></td>
<td>The trigger is initiated by setting the \texttt{SSn} bit in the \texttt{ADCPSSI} register.</td>
</tr>
<tr>
<td>0x1</td>
<td>Analog Comparator 0</td>
</tr>
<tr>
<td></td>
<td>This trigger is configured by the \texttt{Analog Comparator Control 0 (ACCTL0)} register (page 1248).</td>
</tr>
<tr>
<td>0x2</td>
<td>Analog Comparator 1</td>
</tr>
<tr>
<td></td>
<td>This trigger is configured by the \texttt{Analog Comparator Control 1 (ACCTL1)} register (page 1248).</td>
</tr>
<tr>
<td>0x3</td>
<td>Analog Comparator 2</td>
</tr>
<tr>
<td></td>
<td>This trigger is configured by the \texttt{Analog Comparator Control 2 (ACCTL2)} register (page 1248).</td>
</tr>
<tr>
<td>0x4</td>
<td>External (GPIO Pins)</td>
</tr>
<tr>
<td></td>
<td>This trigger is connected to the GPIO interrupt for the corresponding GPIO (see “ADC Trigger Source” on page 666).</td>
</tr>
<tr>
<td>0x5</td>
<td>Timer</td>
</tr>
<tr>
<td></td>
<td>In addition, the trigger must be enabled with the \texttt{TnOTE} bit in the \texttt{GPTMCTL} register (page 751).</td>
</tr>
<tr>
<td>0x6</td>
<td>PWM generator 0</td>
</tr>
<tr>
<td></td>
<td>The PWM generator 0 trigger can be configured with the \texttt{PWM0 Interrupt and Trigger Enable (PWM0INTEN)} register (page 1296).</td>
</tr>
<tr>
<td>0x7</td>
<td>PWM generator 1</td>
</tr>
<tr>
<td></td>
<td>The PWM generator 1 trigger can be configured with the \texttt{PWM1INTEN} register (page 1296).</td>
</tr>
<tr>
<td>0x8</td>
<td>PWM generator 2</td>
</tr>
<tr>
<td></td>
<td>The PWM generator 2 trigger can be configured with the \texttt{PWM2INTEN} register (page 1296).</td>
</tr>
<tr>
<td>0x9</td>
<td>PWM generator 3</td>
</tr>
<tr>
<td></td>
<td>The PWM generator 3 trigger can be configured with the \texttt{PWM3INTEN} register (page 1296).</td>
</tr>
<tr>
<td>0xA-0xE</td>
<td>reserved</td>
</tr>
<tr>
<td>0xF</td>
<td>Always (continuously sample)</td>
</tr>
</tbody>
</table>
SS1 Trigger Select
This field selects the trigger source for Sample Sequencer 1.
The valid configurations for this field are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Processor (default) The trigger is initiated by setting the SSn bit in the ADCPSSI register.</td>
</tr>
<tr>
<td>0x1</td>
<td>Analog Comparator 0 This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1248).</td>
</tr>
<tr>
<td>0x2</td>
<td>Analog Comparator 1 This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1248).</td>
</tr>
<tr>
<td>0x3</td>
<td>Analog Comparator 2 This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1248).</td>
</tr>
<tr>
<td>0x4</td>
<td>External (GPIO Pins) This trigger is connected to the GPIO interrupt for the corresponding GPIO (see “ADC Trigger Source” on page 666).</td>
</tr>
<tr>
<td>0x5</td>
<td>Timer In addition, the trigger must be enabled with the TnOTE bit in the GPTMCTL register (page 751).</td>
</tr>
<tr>
<td>0x6</td>
<td>PWM generator 0 The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1296).</td>
</tr>
<tr>
<td>0x7</td>
<td>PWM generator 1 The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1296).</td>
</tr>
<tr>
<td>0x8</td>
<td>PWM generator 2 The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1296).</td>
</tr>
<tr>
<td>0x9</td>
<td>PWM generator 3 The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1296).</td>
</tr>
<tr>
<td>0xA-0xE</td>
<td>reserved</td>
</tr>
<tr>
<td>0xF</td>
<td>Always (continuously sample)</td>
</tr>
</tbody>
</table>
SS0 Trigger Select

This field selects the trigger source for Sample Sequencer 0. The valid configurations for this field are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Event</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Processor (default)</td>
<td>The trigger is initiated by setting the SSn bit in the ADCPSSI register.</td>
</tr>
<tr>
<td>0x1</td>
<td>Analog Comparator 0</td>
<td>This trigger is configured by the Analog Comparator Control 0 (ACCTL0) register (page 1248).</td>
</tr>
<tr>
<td>0x2</td>
<td>Analog Comparator 1</td>
<td>This trigger is configured by the Analog Comparator Control 1 (ACCTL1) register (page 1248).</td>
</tr>
<tr>
<td>0x3</td>
<td>Analog Comparator 2</td>
<td>This trigger is configured by the Analog Comparator Control 2 (ACCTL2) register (page 1248).</td>
</tr>
<tr>
<td>0x4</td>
<td>External (GPIO Pins)</td>
<td>This trigger is connected to the GPIO interrupt for the corresponding GPIO (see “ADC Trigger Source” on page 666).</td>
</tr>
<tr>
<td>0x5</td>
<td>Timer</td>
<td>In addition, the trigger must be enabled with the TnOTE bit in the GPTMCTL register (page 751).</td>
</tr>
<tr>
<td>0x6</td>
<td>PWM generator 0</td>
<td>The PWM generator 0 trigger can be configured with the PWM0 Interrupt and Trigger Enable (PWM0INTEN) register (page 1296).</td>
</tr>
<tr>
<td>0x7</td>
<td>PWM generator 1</td>
<td>The PWM generator 1 trigger can be configured with the PWM1INTEN register (page 1296).</td>
</tr>
<tr>
<td>0x8</td>
<td>PWM generator 2</td>
<td>The PWM generator 2 trigger can be configured with the PWM2INTEN register (page 1296).</td>
</tr>
<tr>
<td>0x9</td>
<td>PWM generator 3</td>
<td>The PWM generator 3 trigger can be configured with the PWM3INTEN register (page 1296).</td>
</tr>
<tr>
<td>0xA-0xE</td>
<td>reserved</td>
<td></td>
</tr>
<tr>
<td>0xF</td>
<td>Always (continuously sample)</td>
<td></td>
</tr>
</tbody>
</table>
Register 7: ADC Underflow Status (ADCUSTAT), offset 0x018

This register indicates underflow conditions in the sample sequencer FIFOs. The corresponding underflow condition is cleared by writing a 1 to the relevant bit position.

ADC Underflow Status (ADCUSTAT)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x018
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>UV3</td>
<td>RW1C</td>
<td>0</td>
<td>SS3 FIFO Underflow&lt;br&gt;The valid configurations for this field are shown below. This bit is cleared by writing a 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>UV2</td>
<td>RW1C</td>
<td>0</td>
<td>SS2 FIFO Underflow&lt;br&gt;The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.</td>
</tr>
<tr>
<td>1</td>
<td>UV1</td>
<td>RW1C</td>
<td>0</td>
<td>SS1 FIFO Underflow&lt;br&gt;The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.</td>
</tr>
<tr>
<td>0</td>
<td>UV0</td>
<td>RW1C</td>
<td>0</td>
<td>SS0 FIFO Underflow&lt;br&gt;The valid configurations are the same as those for the UV3 field. This bit is cleared by writing a 1.</td>
</tr>
</tbody>
</table>
Register 8: ADC Trigger Source Select (ADCTSSEL), offset 0x01C

If a PWM Generator n is selected as a trigger source through the EMn bit field in the ADC Event Multiplexer Select (ADCEMUX) register, the ADCTSSEL register is programmed to identify in which PWM module instance the generator creating the trigger is located. The register resets to 0x0000.0000, which selects PWM module 0 for all generators. Note that field PS3 selects the PWM module that maps to Generator 3; PS2 selects the PWM module that maps to Generator 2, and so on.

ADC Trigger Source Select (ADCTSSEL)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x01C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:30</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>29:28</td>
<td>PS3</td>
<td>RW</td>
<td>0x0</td>
<td>Generator 3 PWM Module Trigger Select This field selects in which PWM module the generator 3 trigger is located.</td>
</tr>
<tr>
<td>27:22</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>21:20</td>
<td>PS2</td>
<td>RW</td>
<td>0x0</td>
<td>Generator 2 PWM Module Trigger Select This field selects in which PWM module the Generator 2 trigger is located.</td>
</tr>
<tr>
<td>19:14</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>13:12</td>
<td>PS1</td>
<td>RW</td>
<td>0x0</td>
<td>Generator 1 PWM Module Trigger Select&lt;br&gt;This field selects in which PWM module the Generator 1 trigger is located.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 - 0x3</td>
</tr>
<tr>
<td>11:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5:4</td>
<td>PS0</td>
<td>RW</td>
<td>0x0</td>
<td>Generator 0 PWM Module Trigger Select&lt;br&gt;This field selects in which PWM module the Generator 0 trigger is located.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 - 0x3</td>
</tr>
<tr>
<td>3:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 9: ADC Sample Sequencer Priority (ADCSSPRI), offset 0x020

This register sets the priority for each of the sample sequencers. Out of reset, Sequencer 0 has the highest priority, and Sequencer 3 has the lowest priority. When reconfiguring sequence priorities, each sequence must have a unique priority for the ADC to operate properly.

ADC Sample Sequencer Priority (ADCSSPRI)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x020
Type RW, reset 0x0000.3210

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13:12</td>
<td>SS3</td>
<td>RW</td>
<td>0x3</td>
<td>SS3 Priority</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 3. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.</td>
</tr>
<tr>
<td>11:10</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9:8</td>
<td>SS2</td>
<td>RW</td>
<td>0x2</td>
<td>SS2 Priority</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 2. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.</td>
</tr>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5:4</td>
<td>SS1</td>
<td>RW</td>
<td>0x1</td>
<td>SS1 Priority</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 1. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.</td>
</tr>
<tr>
<td>3:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
### Bit/Field | Name | Type | Reset | Description
---|---|---|---|---
1:0 | SS0 | RW | 0x0 | **SS0 Priority**

This field contains a binary-encoded value that specifies the priority encoding of Sample Sequencer 0. A priority encoding of 0x0 is highest and 0x3 is lowest. The priorities assigned to the sequencers must be uniquely mapped. The ADC may not operate properly if two or more fields are equal.
Register 10: ADC Sample Phase Control (ADCSPC), offset 0x024

This register allows the ADC module to sample at one of 16 different discrete phases from 0.0° through 337.5°. For example, the sample rate could be effectively doubled by sampling a signal using one ADC module configured with the standard sample time and the second ADC module configured with a 180.0° phase lag.

**Note:** Care should be taken when the PHASE field is non-zero, as the resulting delay in sampling the AINx input may result in undesirable system consequences. The time from ADC trigger to sample is increased and could make the response time longer than anticipated. The added latency could have ramifications in the system design. Designers should carefully consider the impact of this delay.

ADC Sample Phase Control (ADCSPC)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x024
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>3:0</td>
<td>PHASE</td>
<td>RW</td>
<td>0x0</td>
<td>Phase Difference</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field selects the sample phase difference from the standard sample</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>time.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>0x0</td>
<td>ADC sample lags by 0.0°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>ADC sample lags by 22.5°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2</td>
<td>ADC sample lags by 45.0°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x3</td>
<td>ADC sample lags by 67.5°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x4</td>
<td>ADC sample lags by 90.0°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x5</td>
<td>ADC sample lags by 112.5°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x6</td>
<td>ADC sample lags by 135.0°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x7</td>
<td>ADC sample lags by 157.5°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x8</td>
<td>ADC sample lags by 180.0°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x9</td>
<td>ADC sample lags by 202.5°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xA</td>
<td>ADC sample lags by 225.0°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xB</td>
<td>ADC sample lags by 247.5°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xC</td>
<td>ADC sample lags by 270.0°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xD</td>
<td>ADC sample lags by 292.5°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xE</td>
<td>ADC sample lags by 315.0°</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0xF</td>
<td>ADC sample lags by 337.5°</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 11: ADC Processor Sample Sequence Initiate (ADCPSSI), offset 0x028

This register provides a mechanism for application software to initiate sampling in the sample sequencers. Sample sequences can be initiated individually or in any combination. When multiple sequences are triggered simultaneously, the priority encodings in ADCSSPRI dictate execution order.

This register also provides a means to configure and then initiate concurrent sampling on all ADC modules. To do this, the first ADC module should be configured. The ADCPSSI register for that module should then be written. The appropriate SS bits should be set along with the SYNCWAIT bit. Additional ADC modules should then be configured following the same procedure. Once the final ADC module is configured, its ADCPSSI register should be written with the appropriate SS bits set along with the GSYNC bit. All of the ADC modules then begin concurrent sampling according to their configuration.

ADC Processor Sample Sequence Initiate (ADCPSSI)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x028
Type RW, reset -

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>GSYNC</td>
<td>RW</td>
<td>0</td>
<td>Global Synchronize</td>
</tr>
<tr>
<td>RO</td>
<td>SYNCWAIT</td>
<td>RO</td>
<td>0</td>
<td>Synchronize Wait</td>
</tr>
<tr>
<td>RO</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>SS3</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>SS2</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>SS1</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>SS0</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
### Analog-to-Digital Converter (ADC)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>SS3</td>
<td>WO</td>
<td>-</td>
<td>SS3 Initiate</td>
</tr>
</tbody>
</table>

  **Value**  **Description**
  0  No effect.
  1  Begin sampling on Sample Sequencer 3, if the sequencer is enabled in the *ADCACTSS* register.

Only a write by software is valid; a read of this register returns no meaningful data.

| 2         | SS2  | WO   | -     | SS2 Initiate |

  **Value**  **Description**
  0  No effect.
  1  Begin sampling on Sample Sequencer 2, if the sequencer is enabled in the *ADCACTSS* register.

Only a write by software is valid; a read of this register returns no meaningful data.

| 1         | SS1  | WO   | -     | SS1 Initiate |

  **Value**  **Description**
  0  No effect.
  1  Begin sampling on Sample Sequencer 1, if the sequencer is enabled in the *ADCACTSS* register.

Only a write by software is valid; a read of this register returns no meaningful data.

| 0         | SS0  | WO   | -     | SS0 Initiate |

  **Value**  **Description**
  0  No effect.
  1  Begin sampling on Sample Sequencer 0, if the sequencer is enabled in the *ADCACTSS* register.

Only a write by software is valid; a read of this register returns no meaningful data.
Register 12: ADC Sample Averaging Control (ADCSAC), offset 0x030

This register controls the amount of hardware averaging applied to conversion results. The final conversion result stored in the FIFO is averaged from $2^{AVG}$ consecutive ADC samples at the specified ADC speed. If AVG is 0, the sample is passed directly through without any averaging. If AVG=6, then 64 consecutive ADC samples are averaged to generate one result in the sequencer FIFO. An AVG=7 provides unpredictable results.

ADC Sample Averaging Control (ADCSAC)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x030
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 2:0       | AVG      | RW   | 0x0       | Hardware Averaging Control
Specifies the amount of hardware averaging that will be applied to ADC samples. The AVG field can be any value between 0 and 6. Entering a value of 7 creates unpredictable results. |

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>No hardware oversampling</td>
</tr>
<tr>
<td>0x1</td>
<td>2x hardware oversampling</td>
</tr>
<tr>
<td>0x2</td>
<td>4x hardware oversampling</td>
</tr>
<tr>
<td>0x3</td>
<td>8x hardware oversampling</td>
</tr>
<tr>
<td>0x4</td>
<td>16x hardware oversampling</td>
</tr>
<tr>
<td>0x5</td>
<td>32x hardware oversampling</td>
</tr>
<tr>
<td>0x6</td>
<td>64x hardware oversampling</td>
</tr>
<tr>
<td>0x7</td>
<td>reserved</td>
</tr>
</tbody>
</table>
Register 13: ADC Digital Comparator Interrupt Status and Clear (ADCDCISC), offset 0x034

This register provides status and acknowledgement of digital comparator interrupts. One bit is provided for each comparator.

ADC Digital Comparator Interrupt Status and Clear (ADCDCISC)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x034
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>DCINT7</td>
<td>RW1C</td>
<td>0</td>
<td>Digital Comparator 7 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td>No interrupt.</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>Digital Comparator 7 has generated an interrupt.</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>DCINT6</td>
<td>RW1C</td>
<td>0</td>
<td>Digital Comparator 6 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td>No interrupt.</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>Digital Comparator 6 has generated an interrupt.</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DCINT5</td>
<td>RW1C</td>
<td>0</td>
<td>Digital Comparator 5 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td>No interrupt.</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>Digital Comparator 5 has generated an interrupt.</td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>--------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td>DCINT4</td>
<td>RW1C</td>
<td>0</td>
<td>Digital Comparator 4 Interrupt Status and Clear</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1.</td>
</tr>
<tr>
<td>3</td>
<td>DCINT3</td>
<td>RW1C</td>
<td>0</td>
<td>Digital Comparator 3 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1.</td>
</tr>
<tr>
<td>2</td>
<td>DCINT2</td>
<td>RW1C</td>
<td>0</td>
<td>Digital Comparator 2 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1.</td>
</tr>
<tr>
<td>1</td>
<td>DCINT1</td>
<td>RW1C</td>
<td>0</td>
<td>Digital Comparator 1 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1.</td>
</tr>
<tr>
<td>0</td>
<td>DCINT0</td>
<td>RW1C</td>
<td>0</td>
<td>Digital Comparator 0 Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1.</td>
</tr>
</tbody>
</table>
Register 14: ADC Control (ADCCTL), offset 0x038

This register configures the voltage reference. The voltage references for the conversion can be \( \text{VREF} + \) and \( \text{VREF} - \) or \( \text{VDD} \) and \( \text{GND} \). Note that values set in this register apply to all ADC modules, it is not possible to set one module to use internal references and another to use external references.

ADC Control (ADCCTL)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x038
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:7</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6</td>
<td>DITHER</td>
<td>RW</td>
<td>0</td>
<td>Dither Mode Enable</td>
</tr>
<tr>
<td>5:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>VREF</td>
<td>RW</td>
<td>0x0</td>
<td>Voltage Reference Select</td>
</tr>
</tbody>
</table>

Value Description

- 0  Dither mode disabled
- 1  Dither mode enabled

\( \text{VDD} \) and \( \text{GND} \) are the voltage references for all ADC modules.

The external \( \text{VREF} + \) and \( \text{VREF} - \) inputs are the voltage references for all ADC modules.
Register 15: ADC Sample Sequence Input Multiplexer Select 0 (ADCSSMUX0), offset 0x040

This register, along with the ADCSSEMUX0 register, defines the analog input configuration for each sample in a sequence executed with Sample Sequencer 0. If the corresponding EMUXn bit in the ADCSSEMUX0 register is set, the MUXn field in this register selects from $\text{AIN}[21:16]$. When the corresponding EMUXn bit is clear, the MUXn field selects from $\text{AIN}[15:0]$. This register is 32 bits wide and contains information for eight possible samples.

**Note:** Channels $\text{AIN}[31:22]$ do not exist on this microcontroller. Configuring MUXn to be 0xA-0xF when the corresponding EMUXn bit is set results in undefined behavior.

ADC Sample Sequence Input Multiplexer Select 0 (ADCSSMUX0)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x040
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:28     | MUX7      | RW   | 0x0   | 8th Sample Input Select
The MUX7 field is used during the eighth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion. The value set here indicates the corresponding pin, for example, a value of 0x1 when EMUX7 is clear indicates the input is $\text{AIN1}$. A value of 0x1 when EMUX7 is set indicates the input is $\text{AIN17}$.

If differential sampling is enabled (the $D7$ bit in the ADCSSCTL0 register is set), this field must be set to the pair number "i", where the paired inputs are "2i and 2i+1".

| 27:24     | MUX6      | RW   | 0x0   | 7th Sample Input Select
The MUX6 field is used during the seventh sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.

| 23:20     | MUX5      | RW   | 0x0   | 6th Sample Input Select
The MUX5 field is used during the sixth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.

| 19:16     | MUX4      | RW   | 0x0   | 5th Sample Input Select
The MUX4 field is used during the fifth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion. |
### Analog-to-Digital Converter (ADC)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:12</td>
<td>MUX3</td>
<td>RW</td>
<td>0x0</td>
<td>4th Sample Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The MUX3 field is used during the fourth sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</td>
</tr>
<tr>
<td>11:8</td>
<td>MUX2</td>
<td>RW</td>
<td>0x0</td>
<td>3rd Sample Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The MUX2 field is used during the third sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</td>
</tr>
<tr>
<td>7:4</td>
<td>MUX1</td>
<td>RW</td>
<td>0x0</td>
<td>2nd Sample Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The MUX1 field is used during the second sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</td>
</tr>
<tr>
<td>3:0</td>
<td>MUX0</td>
<td>RW</td>
<td>0x0</td>
<td>1st Sample Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The MUX0 field is used during the first sample of a sequence executed with the sample sequencer. It specifies which of the analog inputs is sampled for the analog-to-digital conversion.</td>
</tr>
</tbody>
</table>
Register 16: ADC Sample Sequence Control 0 (ADCSSCTL0), offset 0x044

This register contains the configuration information for each sample for a sequence executed with a sample sequencer. When configuring a sample sequence, the END bit must be set for the final sample, whether it be after the first sample, eighth sample, or any sample in between. This register is 32 bits wide and contains information for eight possible samples.

ADC Sample Sequence Control 0 (ADCSSCTL0)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>TS7</td>
<td>RW</td>
<td>0</td>
<td>8th Sample Temp Sensor Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The input pin specified by the ADCSSMUXn register is read during the eighth sample of the sample sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The temperature sensor is read during the eighth sample of the sample sequence.</td>
</tr>
<tr>
<td>30</td>
<td>IE7</td>
<td>RW</td>
<td>0</td>
<td>8th Sample Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The raw interrupt is not asserted to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The raw interrupt signal (INR0 bit) is asserted at the end of the eighth sample's conversion. If the MASK0 bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.</td>
</tr>
<tr>
<td>29</td>
<td>END7</td>
<td>RW</td>
<td>0</td>
<td>8th Sample is End of Sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Another sample in the sequence is the final sample.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The eighth sample is the last sample of the sequence.</td>
</tr>
</tbody>
</table>

It is possible to end the sequence on any sample position. Software must set an ENDn bit somewhere within the sequence. Samples defined after the sample containing a set ENDn bit are not requested for conversion even though the fields may be non-zero.
### Analog-to-Digital Converter (ADC)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>D7</td>
<td>RW</td>
<td>0</td>
<td>8th Sample Differential Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The analog inputs are not differentially sampled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The analog input is differentially sampled. The corresponding ADCSSMUXn nibble must be set to the pair number &quot;i&quot;, where the paired inputs are &quot;2i and 2i+1&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the temperature sensor does not have a differential option, this bit must not be set when the TS7 bit is set.</td>
</tr>
<tr>
<td>27</td>
<td>TS6</td>
<td>RW</td>
<td>0</td>
<td>7th Sample Temp Sensor Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The input pin specified by the ADCSSMUXn register is read during the seventh sample of the sample sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The temperature sensor is read during the seventh sample of the sample sequence.</td>
</tr>
<tr>
<td>26</td>
<td>IE6</td>
<td>RW</td>
<td>0</td>
<td>7th Sample Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The raw interrupt is not asserted to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The raw interrupt signal (INR0 bit) is asserted at the end of the seventh sample’s conversion. If the MASK0 bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>It is legal to have multiple samples within a sequence generate interrupts.</td>
</tr>
<tr>
<td>25</td>
<td>END6</td>
<td>RW</td>
<td>0</td>
<td>7th Sample is End of Sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Another sample in the sequence is the final sample.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The seventh sample is the last sample of the sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>It is possible to end the sequence on any sample position. Software must set an ENDn bit somewhere within the sequence. Samples defined after the sample containing a set ENDn bit are not requested for conversion even though the fields may be non-zero.</td>
</tr>
<tr>
<td>24</td>
<td>D6</td>
<td>RW</td>
<td>0</td>
<td>7th Sample Differential Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The analog inputs are not differentially sampled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The analog input is differentially sampled. The corresponding ADCSSMUXn nibble must be set to the pair number &quot;i&quot;, where the paired inputs are &quot;2i and 2i+1&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the temperature sensor does not have a differential option, this bit must not be set when the TS6 bit is set.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>23</td>
<td>TS5</td>
<td>RW</td>
<td>0</td>
<td>6th Sample Temp Sensor Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>22</td>
<td>IE5</td>
<td>RW</td>
<td>0</td>
<td>6th Sample Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>21</td>
<td>END5</td>
<td>RW</td>
<td>0</td>
<td>6th Sample is End of Sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>20</td>
<td>D5</td>
<td>RW</td>
<td>0</td>
<td>6th Sample Differential Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>19</td>
<td>TS4</td>
<td>RW</td>
<td>0</td>
<td>5th Sample Temp Sensor Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
### Bit/Field Name Type Reset Description

<table>
<thead>
<tr>
<th>18</th>
<th>IE4</th>
<th>RW</th>
<th>0</th>
<th>5th Sample Interrupt Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The raw interrupt is not asserted to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The raw interrupt signal (INR0 bit) is asserted at the end of the fifth sample's conversion. If the MASK0 bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.</td>
</tr>
</tbody>
</table>

It is legal to have multiple samples within a sequence generate interrupts.

<table>
<thead>
<tr>
<th>17</th>
<th>END4</th>
<th>RW</th>
<th>0</th>
<th>5th Sample is End of Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Another sample in the sequence is the final sample.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The fifth sample is the last sample of the sequence.</td>
</tr>
</tbody>
</table>

It is possible to end the sequence on any sample position. Software must set an ENDr bit somewhere within the sequence. Samples defined after the sample containing a set ENDr bit are not requested for conversion even though the fields may be non-zero.

<table>
<thead>
<tr>
<th>16</th>
<th>D4</th>
<th>RW</th>
<th>0</th>
<th>5th Sample Differential Input Select</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The analog inputs are not differentially sampled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The analog input is differentially sampled. The corresponding ADCSSMUXn nibble must be set to the pair number &quot;i&quot;, where the paired inputs are &quot;2i and 2i+1&quot;.</td>
</tr>
</tbody>
</table>

Because the temperature sensor does not have a differential option, this bit must not be set when the TS4 bit is set.

<table>
<thead>
<tr>
<th>15</th>
<th>TS3</th>
<th>RW</th>
<th>0</th>
<th>4th Sample Temp Sensor Select</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The input pin specified by the ADCSSMUXn register is read during the fourth sample of the sample sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The temperature sensor is read during the fourth sample of the sample sequence.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>14</th>
<th>IE3</th>
<th>RW</th>
<th>0</th>
<th>4th Sample Interrupt Enable</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The raw interrupt is not asserted to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The raw interrupt signal (INR0 bit) is asserted at the end of the fourth sample's conversion. If the MASK0 bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.</td>
</tr>
</tbody>
</table>

It is legal to have multiple samples within a sequence generate interrupts.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>END3</td>
<td>RW</td>
<td>0</td>
<td>4th Sample is End of Sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Another sample in the sequence is the final sample.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The fourth sample is the last sample of the sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>It is possible to end the sequence on any sample position.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must set an ENDn bit somewhere within the sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Samples defined after the sample containing a set ENDn bit are</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>not requested for conversion even though the fields may be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>non-zero.</td>
</tr>
<tr>
<td>12</td>
<td>D3</td>
<td>RW</td>
<td>0</td>
<td>4th Sample Differential Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The analog inputs are not differentially sampled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The analog input is differentially sampled. The corresponding</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ADCSSMUXn nibble must be set to the pair number &quot;i&quot;, where</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the paired inputs are &quot;2i and 2i+1&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the temperature sensor does not have a differential</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>option, this bit must not be set when the TS2 bit is set.</td>
</tr>
<tr>
<td>11</td>
<td>TS2</td>
<td>RW</td>
<td>0</td>
<td>3rd Sample Temp Sensor Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The input pin specified by the ADCSSMUXn register is read</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>during the third sample of the sample sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The temperature sensor is read during the third sample of</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the sample sequence.</td>
</tr>
<tr>
<td>10</td>
<td>IE2</td>
<td>RW</td>
<td>0</td>
<td>3rd Sample Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The raw interrupt is not asserted to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The raw interrupt signal (INRO bit) is asserted at the end</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>of the third sample's conversion. If the MASK0 bit in the ADCIM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is set, the interrupt is promoted to the interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>It is legal to have multiple samples within a sequence generate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>interrupts.</td>
</tr>
<tr>
<td>9</td>
<td>END2</td>
<td>RW</td>
<td>0</td>
<td>3rd Sample is End of Sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: Another sample in the sequence is the final sample.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The third sample is the last sample of the sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>It is possible to end the sequence on any sample position.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must set an ENDn bit somewhere within the sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Samples defined after the sample containing a set ENDn bit are</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>not requested for conversion even though the fields may be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>non-zero.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>8</td>
<td>D2</td>
<td>RW</td>
<td>0</td>
<td>3rd Sample Differential Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The analog inputs are not differentially sampled.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>The analog input is differentially sampled. The corresponding ADCSSMUX&lt;sub&gt;n&lt;/sub&gt; nibble must be set to the pair number &quot;i&quot;, where the paired inputs are &quot;2i and 2i+1&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the temperature sensor does not have a differential option, this bit must not be set when the TS&lt;sub&gt;2&lt;/sub&gt; bit is set.</td>
</tr>
<tr>
<td>7</td>
<td>TS1</td>
<td>RW</td>
<td>0</td>
<td>2nd Sample Temp Sensor Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The input pin specified by the ADCSSMUX&lt;sub&gt;n&lt;/sub&gt; register is read during the second sample of the sample sequence.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>The temperature sensor is read during the second sample of the sample sequence.</td>
</tr>
<tr>
<td>6</td>
<td>IE1</td>
<td>RW</td>
<td>0</td>
<td>2nd Sample Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The raw interrupt is not asserted to the interrupt controller.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>The raw interrupt signal (INR&lt;sub&gt;0&lt;/sub&gt; bit) is asserted at the end of the second sample's conversion. If the MASK&lt;sub&gt;0&lt;/sub&gt; bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>It is legal to have multiple samples within a sequence generate interrupts.</td>
</tr>
<tr>
<td>5</td>
<td>END1</td>
<td>RW</td>
<td>0</td>
<td>2nd Sample is End of Sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>Another sample in the sequence is the final sample.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>The second sample is the last sample of the sequence.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>It is possible to end the sequence on any sample position. Software must set an END&lt;sub&gt;n&lt;/sub&gt; bit somewhere within the sequence. Samples defined after the sample containing a set END&lt;sub&gt;n&lt;/sub&gt; bit are not requested for conversion even though the fields may be non-zero.</td>
</tr>
<tr>
<td>4</td>
<td>D1</td>
<td>RW</td>
<td>0</td>
<td>2nd Sample Differential Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The analog inputs are not differentially sampled.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>The analog input is differentially sampled. The corresponding ADCSSMUX&lt;sub&gt;n&lt;/sub&gt; nibble must be set to the pair number &quot;i&quot;, where the paired inputs are &quot;2i and 2i+1&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the temperature sensor does not have a differential option, this bit must not be set when the TS&lt;sub&gt;1&lt;/sub&gt; bit is set.</td>
</tr>
</tbody>
</table>
### Bit/Field Name Type Reset Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>TS0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample Temp Sensor Select</td>
</tr>
<tr>
<td>2</td>
<td>IE0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample Interrupt Enable</td>
</tr>
<tr>
<td>1</td>
<td>END0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample is End of Sequence</td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample Differential Input Select</td>
</tr>
</tbody>
</table>

#### Description

**Value Description**

- **0**: The input pin specified by the ADCSSMUX[n] register is read during the first sample of the sample sequence.
- **1**: The temperature sensor is read during the first sample of the sample sequence.

**Value Description**

- **0**: The raw interrupt is not asserted to the interrupt controller.
- **1**: The raw interrupt signal (INR0 bit) is asserted at the end of the first sample's conversion. If the MASK0 bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.

It is legal to have multiple samples within a sequence generate interrupts.

**Value Description**

- **0**: Another sample in the sequence is the final sample.
- **1**: The first sample is the last sample of the sequence.

It is possible to end the sequence on any sample position. Software must set an ENDn bit somewhere within the sequence. Samples defined after the sample containing a set ENDn bit are not requested for conversion even though the fields may be non-zero.

**Value Description**

- **0**: The analog inputs are not differentially sampled.
- **1**: The analog input is differentially sampled. The corresponding ADCSSMUX[n] nibble must be set to the pair number "i", where the paired inputs are "2i and 2i+1".

Because the temperature sensor does not have a differential option, this bit must not be set when the TS0 bit is set.
Register 17: ADC Sample Sequence Result FIFO 0 (ADCSSFIFO0), offset 0x048
Register 18: ADC Sample Sequence Result FIFO 1 (ADCSSFIFO1), offset 0x068
Register 19: ADC Sample Sequence Result FIFO 2 (ADCSSFIFO2), offset 0x088
Register 20: ADC Sample Sequence Result FIFO 3 (ADCSSFIFO3), offset 0x0A8

Important: This register is read-sensitive. See the register description for details.

This register contains the conversion results for samples collected with the sample sequencer (the ADCSSFIFO0 register is used for Sample Sequencer 0, ADCSSFIFO1 for Sequencer 1, ADCSSFIFO2 for Sequencer 2, and ADCSSFIFO3 for Sequencer 3). Reads of this register return conversion result data in the order sample 0, sample 1, and so on, until the FIFO is empty. If the FIFO is not properly handled by software, overflow and underflow conditions are registered in the ADCOSTAT and ADCUSTAT registers.

ADC Sample Sequence Result FIFO n (ADCSSFIFOOn)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x048
Type RO, reset -

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11:0</td>
<td>DATA</td>
<td>RO</td>
<td>-</td>
<td>Conversion Result Data</td>
</tr>
</tbody>
</table>
Register 21: ADC Sample Sequence FIFO 0 Status (ADCSSFSTAT0), offset 0x04C

Register 22: ADC Sample Sequence FIFO 1 Status (ADCSSFSTAT1), offset 0x06C

Register 23: ADC Sample Sequence FIFO 2 Status (ADCSSFSTAT2), offset 0x08C

Register 24: ADC Sample Sequence FIFO 3 Status (ADCSSFSTAT3), offset 0x0AC

This register provides a window into the sample sequencer, providing full/empty status information as well as the positions of the head and tail pointers. The reset value of 0x100 indicates an empty FIFO with the head and tail pointers both pointing to index 0. The ADCSSFSTAT0 register provides status on FIFO0, which has 8 entries; ADCSSFSTAT1 on FIFO1, which has 4 entries; ADCSSFSTAT2 on FIFO2, which has 4 entries; and ADCSSFSTAT3 on FIFO3 which has a single entry.

ADC Sample Sequence FIFO n Status (ADCSSFSTATn)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x04C
Type RO, reset 0x0000.0100

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12</td>
<td>FULL</td>
<td>RO</td>
<td>0</td>
<td>FIFO Full</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The FIFO is not currently full.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The FIFO is currently full.</td>
</tr>
<tr>
<td>11:9</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>EMPTY</td>
<td>RO</td>
<td>1</td>
<td>FIFO Empty</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The FIFO is not currently empty.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The FIFO is currently empty.</td>
</tr>
</tbody>
</table>
FIFO Head Pointer
This field contains the current "head" pointer index for the FIFO, that is, the next entry to be written.
Valid values are 0x0-0x7 for FIFO0; 0x0-0x3 for FIFO1 and FIFO2; and 0x0 for FIFO3.

FIFO Tail Pointer
This field contains the current "tail" pointer index for the FIFO, that is, the next entry to be read.
Valid values are 0x0-0x7 for FIFO0; 0x0-0x3 for FIFO1 and FIFO2; and 0x0 for FIFO3.
Register 25: ADC Sample Sequence 0 Operation (ADCSSOP0), offset 0x050

This register determines whether the sample from the given conversion on Sample Sequence 0 is saved in the Sample Sequence FIFO0 or sent to the digital comparator unit.

ADC Sample Sequence 0 Operation (ADCSSOP0)

- ADC0 base: 0x4003.8000
- ADC1 base: 0x4003.9000
- Offset 0x050
- Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>31:29</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>28</td>
<td>S7DCOP</td>
<td>RW</td>
<td>0</td>
<td>Sample 7 Digital Comparator Operation</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>27:25</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Sample 6 Digital Comparator Operation</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>24</td>
<td>S6DCOP</td>
<td>RW</td>
<td>0</td>
<td>Sample 5 Digital Comparator Operation</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>23:21</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Sample 4 Digital Comparator Operation</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>20</td>
<td>S5DCOP</td>
<td>RW</td>
<td>0</td>
<td>Sample 3 Digital Comparator Operation</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>19:17</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Sample 2 Digital Comparator Operation</td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>16</td>
<td>S4DCOP</td>
<td>RW</td>
<td>0</td>
<td>Sample 1 Digital Comparator Operation</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 12       | S3DCOP | RW   | 0     | Sample 3 Digital Comparator Operation  
|          |        |      |       | Same definition as S7DCOP but used during the fourth sample. |
| 11:9     | reserved | RO | 0x0  | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 8        | S2DCOP | RW   | 0     | Sample 2 Digital Comparator Operation  
|          |        |      |       | Same definition as S7DCOP but used during the third sample. |
| 7:5      | reserved | RO | 0x0  | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 4        | S1DCOP | RW   | 0     | Sample 1 Digital Comparator Operation  
|          |        |      |       | Same definition as S7DCOP but used during the second sample. |
| 3:1      | reserved | RO | 0x0  | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
| 0        | S0DCOP | RW   | 0     | Sample 0 Digital Comparator Operation  
|          |        |      |       | Same definition as S7DCOP but used during the first sample. |
Register 26: ADC Sample Sequence 0 Digital Comparator Select (ADCSSDC0), offset 0x054

This register determines which digital comparator receives the sample from the given conversion on Sample Sequence 0, if the corresponding $S_{n}DCOP$ bit in the $ADCSSOP0$ register is set.

**ADC Sample Sequence 0 Digital Comparator Select (ADCSSDC0)**

<table>
<thead>
<tr>
<th>Offset</th>
<th>0x054</th>
</tr>
</thead>
</table>

**Type**: RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>S7DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 7 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the $S_{7}DCOP$ bit in the $ADCSSOP0$ register is set, this field</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>indicates which digital comparator unit (and its associated set of control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>registers) receives the eighth sample from Sample Sequencer 0.</td>
</tr>
<tr>
<td>27:24</td>
<td>S6DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 6 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as $S7DCSEL$ but is used during the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>seventh sample.</td>
</tr>
<tr>
<td>23:20</td>
<td>S5DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 5 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as $S7DCSEL$ but is used during the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>sixth sample.</td>
</tr>
<tr>
<td>19:16</td>
<td>S4DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 4 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as $S7DCSEL$ but is used during the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>fifth sample.</td>
</tr>
<tr>
<td>15:12</td>
<td>S3DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 3 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as $S7DCSEL$ but is used during the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>fourth sample.</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11:8</td>
<td>S2DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 2 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as $S7DCSEL$ but is used during the third sample.</td>
</tr>
<tr>
<td>7:4</td>
<td>S1DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 1 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as $S7DCSEL$ but is used during the second sample.</td>
</tr>
<tr>
<td>3:0</td>
<td>S0DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 0 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as $S7DCSEL$ but is used during the first sample.</td>
</tr>
</tbody>
</table>
Register 27: ADC Sample Sequence Extended Input Multiplexer Select 0 (ADCSSEMUX0), offset 0x058

This register, along with the ADCSSMUX0 register, defines the analog input configuration for each sample in a sequence executed with Sample Sequencer 0. If a bit in this register is set, the corresponding MUXn field in the ADCSSMUX0 register selects from AIN[21:16]. When a bit in this register is clear, the corresponding MUXn field selects from AIN[15:0]. This register is 32 bits wide and contains information for eight possible samples.

Note that this register is not used when the differential channel designation is used (the Dn bit is set in the ADCSSCTL0 register) because the ADCSSMUX0 register can select all the available pairs.

ADC Sample Sequence Extended Input Multiplexer Select 0 (ADCSSEMUX0)

| ADC0 base: 0x4003.8000 |
| ADC1 base: 0x4003.9000 |
| Offset 0x058 |
| Type RW, reset 0x0000.0000 |

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
</tr>
<tr>
<td>8th Sample Input Select (Upper Bit)</td>
<td></td>
</tr>
<tr>
<td>The EMUX7 field is used during the eighth sample of a sequence executed with the sample sequencer.</td>
<td>0: The eighth sample input is selected from AIN[15:0] using the ADCSSMUX0 register. For example, if the MUX7 field is 0x0, AIN0 is selected.</td>
</tr>
<tr>
<td></td>
<td>1: The eighth sample input is selected from AIN[21:16] using the ADCSSMUX0 register. For example, if the MUX7 field is 0x0, AIN16 is selected.</td>
</tr>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
</tr>
<tr>
<td>7th Sample Input Select (Upper Bit)</td>
<td></td>
</tr>
<tr>
<td>The EMUX6 field is used during the seventh sample of a sequence executed with the sample sequencer. This bit has the same description as EMUX7.</td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
</tr>
<tr>
<td>20</td>
<td>EMUX5</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>19:17</td>
<td>reserved</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>EMUX4</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>15:13</td>
<td>reserved</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>EMUX3</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>11:9</td>
<td>reserved</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>EMUX2</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>7:5</td>
<td>reserved</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>EMUX1</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>3:1</td>
<td>reserved</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>EMUX0</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 28: ADC Sample Sequence Input Multiplexer Select 1 (ADCSSMUX1), offset 0x060

Register 29: ADC Sample Sequence Input Multiplexer Select 2 (ADCSSMUX2), offset 0x080

This register, along with the ADCSSMUX1 or ADCSSMUX2 register, defines the analog input configuration for each sample in a sequence executed with Sample Sequencer 1 or 2. If the corresponding EMUXn bit in the ADCSSMUX1 or ADCSSMUX2 register is set, the MUXn field in this register selects from AIN[21:16]. When the corresponding EMUXn bit is clear, the MUXn field selects from AIN[15:0]. These registers are 16 bits wide and contain information for four possible samples. See the ADCSSMUX0 register on page 865 for detailed bit descriptions. The ADCSSMUX1 register affects Sample Sequencer 1 and the ADCSSMUX2 register affects Sample Sequencer 2.

**Note:** Channels AIN[31:22] do not exist on this microcontroller. Configuring MUXn to be 0xA-0xF when the corresponding EMUXn bit is set results in undefined behavior.

### ADC Sample Sequence Input Multiplexer Select n (ADCSSMUXn)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:12</td>
<td>MUX3</td>
<td>RW</td>
<td>0x0</td>
<td>4th Sample Input Select</td>
</tr>
<tr>
<td>11:8</td>
<td>MUX2</td>
<td>RW</td>
<td>0x0</td>
<td>3rd Sample Input Select</td>
</tr>
<tr>
<td>7:4</td>
<td>MUX1</td>
<td>RW</td>
<td>0x0</td>
<td>2nd Sample Input Select</td>
</tr>
<tr>
<td>3:0</td>
<td>MUX0</td>
<td>RW</td>
<td>0x0</td>
<td>1st Sample Input Select</td>
</tr>
</tbody>
</table>
Register 30: ADC Sample Sequence Control 1 (ADCSSCTL1), offset 0x064

Register 31: ADC Sample Sequence Control 2 (ADCSSCTL2), offset 0x084

These registers contain the configuration information for each sample for a sequence executed with Sample Sequencer 1 or 2. When configuring a sample sequence, the END bit must be set for the final sample, whether it be after the first sample, fourth sample, or any sample in between. These registers are 16-bits wide and contain information for four possible samples. See the ADCSSCTL0 register on page 867 for detailed bit descriptions. The ADCSSCTL1 register configures Sample Sequencer 1 and the ADCSSCTL2 register configures Sample Sequencer 2.

ADC Sample Sequence Control n (ADCSSCTLn)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x064
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15</td>
<td>TS3</td>
<td>RW</td>
<td>0</td>
<td>4th Sample Temp Sensor Select</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The input pin specified by the ADCSSMUXn register is read during the fourth sample of the sample sequence.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The temperature sensor is read during the fourth sample of the sample sequence.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>IE3</td>
<td>RW</td>
<td>0</td>
<td>4th Sample Interrupt Enable</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The raw interrupt is not asserted to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The raw interrupt signal (INR0 bit) is asserted at the end of the fourth sample's conversion. If the MASK0 bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

It is legal to have multiple samples within a sequence generate interrupts.
### Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>END3</td>
<td>RW</td>
<td>0</td>
<td>4th Sample is End of Sequence</td>
</tr>
<tr>
<td>12</td>
<td>D3</td>
<td>RW</td>
<td>0</td>
<td>4th Sample Differential Input Select</td>
</tr>
<tr>
<td>11</td>
<td>TS2</td>
<td>RW</td>
<td>0</td>
<td>3rd Sample Temp Sensor Select</td>
</tr>
<tr>
<td>10</td>
<td>IE2</td>
<td>RW</td>
<td>0</td>
<td>3rd Sample Interrupt Enable</td>
</tr>
<tr>
<td>9</td>
<td>END2</td>
<td>RW</td>
<td>0</td>
<td>3rd Sample is End of Sequence</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: Another sample in the sequence is the final sample.
- **1**: The fourth sample is the last sample of the sequence.

It is possible to end the sequence on any sample position. Software must set an `ENDn` bit somewhere within the sequence. Samples defined after the sample containing a set `ENDn` bit are not requested for conversion even though the fields may be non-zero.

**D3**

- **0**: The analog inputs are not differentially sampled.
- **1**: The analog input is differentially sampled. The corresponding `ADCSSMUXn` nibble must be set to the pair number "i", where the paired inputs are "2i and 2i+1".

Because the temperature sensor does not have a differential option, this bit must not be set when the `TS3` bit is set.

**TS2**

- **0**: The input pin specified by the `ADCSSMUXn` register is read during the third sample of the sample sequence.
- **1**: The temperature sensor is read during the third sample of the sample sequence.

**IE2**

- **0**: The raw interrupt is not asserted to the interrupt controller.
- **1**: The raw interrupt signal (`INR0` bit) is asserted at the end of the third sample's conversion. If the `MASK0` bit in the `ADCIM` register is set, the interrupt is promoted to the interrupt controller.

It is legal to have multiple samples within a sequence generate interrupts.

**END2**

- **0**: Another sample in the sequence is the final sample.
- **1**: The third sample is the last sample of the sequence.

It is possible to end the sequence on any sample position. Software must set an `ENDn` bit somewhere within the sequence. Samples defined after the sample containing a set `ENDn` bit are not requested for conversion even though the fields may be non-zero.
### 3rd Sample Differential Input Select

**Description:**

- Value: 0 The analog inputs are not differentially sampled.
- Value: 1 The analog input is differentially sampled. The corresponding ADCSSMUXn nibble must be set to the pair number “i”, where the paired inputs are “2i and 2i+1.”

Because the temperature sensor does not have a differential option, this bit must not be set when the TS2 bit is set.

### 2nd Sample Temp Sensor Select

**Description:**

- Value: 0 The input pin specified by the ADCSSMUXn register is read during the second sample of the sample sequence.
- Value: 1 The temperature sensor is read during the second sample of the sample sequence.

### 2nd Sample Interrupt Enable

**Description:**

- Value: 0 The raw interrupt is not asserted to the interrupt controller.
- Value: 1 The raw interrupt signal (INR0 bit) is asserted at the end of the second sample’s conversion. If the MASK0 bit in the ADCIM register is set, the interrupt is promoted to the interrupt controller.

It is legal to have multiple samples within a sequence generate interrupts.

### 2nd Sample is End of Sequence

**Description:**

- Value: 0 Another sample in the sequence is the final sample.
- Value: 1 The second sample is the last sample of the sequence.

It is possible to end the sequence on any sample position. Software must set an ENDn bit somewhere within the sequence. Samples defined after the sample containing a set ENDn bit are not requested for conversion even though the fields may be non-zero.

### 2nd Sample Differential Input Select

**Description:**

- Value: 0 The analog inputs are not differentially sampled.
- Value: 1 The analog input is differentially sampled. The corresponding ADCSSMUXn nibble must be set to the pair number “i”, where the paired inputs are “2i and 2i+1.”

Because the temperature sensor does not have a differential option, this bit must not be set when the TS1 bit is set.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>TS0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample Temp Sensor Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>IE0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>It is legal to have multiple samples within a sequence generate interrupts.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>END0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample is End of Sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>It is possible to end the sequence on any sample position. Software must set an ENDe bit somewhere within the sequence. Samples defined after the sample containing a set ENDe bit are not requested for conversion even though the fields may be non-zero.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample Differential Input Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Because the temperature sensor does not have a differential option, this bit must not be set when the TS0 bit is set.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 32: ADC Sample Sequence 1 Operation (ADCSSOP1), offset 0x070

Register 33: ADC Sample Sequence 2 Operation (ADCSSOP2), offset 0x090

This register determines whether the sample from the given conversion on Sample Sequence n is saved in the Sample Sequence n FIFO or sent to the digital comparator unit. The ADCSSOP1 register controls Sample Sequencer 1 and the ADCSSOP2 register controls Sample Sequencer 2.

ADC Sample Sequence n Operation (ADCSSOPn)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x070
Type RW, reset 0x0000.0000

Bit/Field | Name          | Type | Reset | Description
----------|---------------|------|-------|--------------------------------------------------------
31:13      | reserved      | RO   | 0x0000.0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
12         | S3DCOP        | RW   | 0     | Sample 3 Digital Comparator Operation
11:9       | reserved      | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
8          | S2DCOP        | RW   | 0     | Sample 2 Digital Comparator Operation
            |               |      |       | Same definition as S3DCOP but used during the third sample.
7:5        | reserved      | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
4          | S1DCOP        | RW   | 0     | Sample 1 Digital Comparator Operation
            |               |      |       | Same definition as S3DCOP but used during the second sample.
3:1        | reserved      | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0          | S0DCOP        | RW   | 0     | Sample 0 Digital Comparator Operation
            |               |      |       | Same definition as S3DCOP but used during the first sample.
Register 34: ADC Sample Sequence 1 Digital Comparator Select (ADCSSDC1), offset 0x074

Register 35: ADC Sample Sequence 2 Digital Comparator Select (ADCSSDC2), offset 0x094

These registers determine which digital comparator receives the sample from the given conversion on Sample Sequence n if the corresponding SnDCOP bit in the ADCSSOPn register is set. The ADCSSDC1 register controls the selection for Sample Sequencer 1 and the ADCSSDC2 register controls the selection for Sample Sequencer 2.

ADC Sample Sequence n Digital Comparator Select (ADCSSDCn)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x074
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:12</td>
<td>S3DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 3 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the S3DCOP bit in the ADCSSOPn register is set, this field indicates which digital comparator unit (and its associated set of control registers) receives the eighth sample from Sample Sequencer n.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> Values not listed are reserved.</td>
</tr>
</tbody>
</table>

### Value Description

- **0x0** Digital Comparator Unit 0 (ADCDCCMP0 and ADCCCTL0)
- **0x1** Digital Comparator Unit 1 (ADCDCCMP1 and ADCCCTL1)
- **0x2** Digital Comparator Unit 2 (ADCDCCMP2 and ADCCCTL2)
- **0x3** Digital Comparator Unit 3 (ADCDCCMP3 and ADCCCTL3)
- **0x4** Digital Comparator Unit 4 (ADCDCCMP4 and ADCCCTL4)
- **0x5** Digital Comparator Unit 5 (ADCDCCMP5 and ADCCCTL5)
- **0x6** Digital Comparator Unit 6 (ADCDCCMP6 and ADCCCTL6)
- **0x7** Digital Comparator Unit 7 (ADCDCCMP7 and ADCCCTL7)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11:8</td>
<td>S2DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 2 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as S3DCSEL but is used during the third sample.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>7:4</td>
<td>S1DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 1 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as S3DCSEL but is used during the second sample.</td>
</tr>
<tr>
<td>3:0</td>
<td>S0DCSEL</td>
<td>RW</td>
<td>0x0</td>
<td>Sample 0 Digital Comparator Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field has the same encodings as S3DCSEL but is used during the first sample.</td>
</tr>
</tbody>
</table>
Register 36: ADC Sample Sequence Extended Input Multiplexer Select 1 (ADCSSEMUX1), offset 0x078

Register 37: ADC Sample Sequence Extended Input Multiplexer Select 2 (ADCSSEMUX2), offset 0x098

This register, along with the ADCSSMUX1 or ADCSSMUX2 register, defines the analog input configuration for each sample in a sequence executed with either Sample Sequencer 1 or 2. If a bit in this register is set, the corresponding MUXn field in the ADCSSMUX1 or ADCSSMUX2 register selects from AIN[21:16]. When a bit in this register is clear, the corresponding MUXn field selects from AIN[15:0]. This register is 16 bits wide and contains information for four possible samples. The ADCSSMUX1 register controls Sample Sequencer 1 and the ADCSSMUX2 register controls Sample Sequencer 2.

Note that this register is not used when the differential channel designation is used (the Dn bit is set in the ADCSSCTL1 or ADCSSCTL2 register) because the ADCSSMUX1 or ADCSSMUX2 register can select all the available pairs.

### ADCSSMUXn Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12</td>
<td>EMUX3</td>
<td>RW</td>
<td>0x0</td>
<td>4th Sample Input Select (Upper Bit)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The EMUX3 field is used during the fourth sample of a sequence executed with the sample sequencer.</td>
</tr>
</tbody>
</table>

#### Description

- **0**: The fourth sample input is selected from AIN[15:0] using the ADCSSMUX1 or ADCSSMUX2 register. For example, if the MUX3 field is 0x0, AIN0 is selected.
- **1**: The fourth sample input is selected from AIN[21:16] using the ADCSSMUX1 or ADCSSMUX2 register. For example, if the MUX3 field is 0x0, AIN16 is selected.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11:9</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>8</td>
<td>EMUX2</td>
<td>RW</td>
<td>0x0</td>
<td>3rd Sample Input Select (Upper Bit)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The EMUX2 field is used during the third sample of a sequence executed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>with the sample sequencer. This bit has the same description as EMUX3.</td>
</tr>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>EMUX1</td>
<td>RW</td>
<td>0x0</td>
<td>2th Sample Input Select (Upper Bit)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The EMUX1 field is used during the second sample of a sequence executed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>with the sample sequencer. This bit has the same description as EMUX3.</td>
</tr>
<tr>
<td>3:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>EMUX0</td>
<td>RW</td>
<td>0x0</td>
<td>1st Sample Input Select (Upper Bit)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The EMUX0 field is used during the first sample of a sequence executed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>with the sample sequencer. This bit has the same description as EMUX3.</td>
</tr>
</tbody>
</table>
Register 38: ADC Sample Sequence Input Multiplexer Select 3 (ADCSSMUX3), offset 0x0A0

This register, along with the ADCSSEMUX3 register, defines the analog input configuration for the sample in a sequence executed with Sample Sequencer 3. If the EMUX0 bit in the ADCSSEMUX3 register is set, the MUX0 field in this register selects from AIN[21:16]. When the EMUX0 bit is clear, the MUX0 field selects from AIN[15:0]. This register is four bits wide and contains information for one possible sample. See the ADCSSMUX0 register on page 865 for detailed bit descriptions.
Register 39: ADC Sample Sequence Control 3 (ADCSSCTL3), offset 0x0A4

This register contains the configuration information for a sample executed with Sample Sequencer 3. This register is 4 bits wide and contains information for one possible sample. See the ADCSSCTL0 register on page 867 for detailed bit descriptions.

**Note:** When configuring a sample sequence in this register, the END0 bit must be set.

ADC Sample Sequence Control 3 (ADCSSCTL3)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x0A4
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>TS0</td>
<td>RW</td>
<td>0</td>
<td>1st Sample Temp Sensor Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>IE0</td>
<td>RW</td>
<td>0</td>
<td>Sample Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>It is legal to have multiple samples within a sequence generate interrupts.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>END0</td>
<td>RW</td>
<td>0</td>
<td>End of Sequence</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>D0</td>
<td>RW</td>
<td>0</td>
<td>Sample Differential Input Select</td>
</tr>
</tbody>
</table>

**Value** | **Description**
--- | ---
0 | The analog inputs are not differentially sampled.
1 | The analog input is differentially sampled. The corresponding ADCSSMUXn nibble must be set to the pair number “i”, where the paired inputs are “2i and 2i+1”.

Because the temperature sensor does not have a differential option, this bit must not be set when the TS0 bit is set.
Register 40: ADC Sample Sequence 3 Operation (ADCSSOP3), offset 0x0B0

This register determines whether the sample from the given conversion on Sample Sequence 3 is saved in the Sample Sequence 3 FIFO or sent to the digital comparator unit.

ADC Sample Sequence 3 Operation (ADCSSOP3)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x0B0
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>S0DCOP</td>
<td>RW</td>
<td>0</td>
<td>Sample 0 Digital Comparator Operation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The sample is saved in Sample Sequence FIFO.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The sample is sent to the digital comparator unit specified by the S0DCSEL bit in the ADCSSDC03 register, and the value is not written to the FIFO.</td>
</tr>
</tbody>
</table>
Register 41: ADC Sample Sequence 3 Digital Comparator Select (ADCSSDC3), offset 0x0B4

This register determines which digital comparator receives the sample from the given conversion on Sample Sequence 3 if the corresponding SnDCOP bit in the ADCSSOP3 register is set.

ADC Sample Sequence 3 Digital Comparator Select (ADCSSDC3)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x0B4
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
</tr>
<tr>
<td>3:0</td>
<td>S0DCSEL</td>
<td>RW</td>
</tr>
</tbody>
</table>

### Bit/Field: reserved

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

### Bit/Field: S0DCSEL

Sample 0 Digital Comparator Select

When the S0DCSEL bit in the ADCSSOP3 register is set, this field indicates which digital comparator unit (and its associated set of control registers) receives the sample from Sample Sequencer 3.

**Note:** Values not listed are reserved.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Digital Comparator Unit 0 (ADCDCCMP0 and ADCCCTL0)</td>
</tr>
<tr>
<td>0x1</td>
<td>Digital Comparator Unit 1 (ADCDCCMP1 and ADCCCTL1)</td>
</tr>
<tr>
<td>0x2</td>
<td>Digital Comparator Unit 2 (ADCDCCMP2 and ADCCCTL2)</td>
</tr>
<tr>
<td>0x3</td>
<td>Digital Comparator Unit 3 (ADCDCCMP3 and ADCCCTL3)</td>
</tr>
<tr>
<td>0x4</td>
<td>Digital Comparator Unit 4 (ADCDCCMP4 and ADCCCTL4)</td>
</tr>
<tr>
<td>0x5</td>
<td>Digital Comparator Unit 5 (ADCDCCMP5 and ADCCCTL5)</td>
</tr>
<tr>
<td>0x6</td>
<td>Digital Comparator Unit 6 (ADCDCCMP6 and ADCCCTL6)</td>
</tr>
<tr>
<td>0x7</td>
<td>Digital Comparator Unit 7 (ADCDCCMP7 and ADCCCTL7)</td>
</tr>
</tbody>
</table>
Register 42: ADC Sample Sequence Extended Input Multiplexer Select 3 (ADCSSEMUX3), offset 0x0B8

This register, along with the ADCSSMUX3 register, defines the analog input configuration for the sample in a sequence executed with Sample Sequencer 3. If EMUX0 is set, the MUX0 field in the ADCSSMUX3 register selects from AIN[21:16]. When EMUX0 is clear, the MUX0 field selects from AIN[15:0]. This register is 1 bit wide and contains information for one possible sample.

Note that this register is not used when the differential channel designation is used (the Dn bit is set in the ADCSSCTL3 register) because the ADCSSMUX3 register can select all the available pairs.

ADC Sample Sequence Extended Input Multiplexer Select 3 (ADCSSEMUX3)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0x0B8
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>EMUX0</td>
<td>RW</td>
<td>0x0</td>
<td>1st Sample Input Select (Upper Bit)</td>
</tr>
</tbody>
</table>

The EMUX0 field is used during the only sample of a sequence executed with the sample sequencer.

Value Description

0 The sample input is selected from AIN[15:0] using the ADCSSMUX3 register. For example, if the MUX0 field is 0x0, AIN0 is selected.

1 The sample input is selected from AIN[21:16] using the ADCSSMUX3 register. For example, if the MUX0 field is 0x0, AIN16 is selected.
Register 43: ADC Digital Comparator Reset Initial Conditions (ADCDCRIC), offset 0xD00

This register provides the ability to reset any of the digital comparator interrupt or trigger functions back to their initial conditions. Resetting these functions ensures that the data that is being used by the interrupt and trigger functions in the digital comparator unit is not stale.

ADC Digital Comparator Reset Initial Conditions (ADCDCRIC)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0xD00
Type WO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23</td>
<td>DCTRIG7</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Trigger 7</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>22</td>
<td>DCTRIG6</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Trigger 6</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

When the trigger has been cleared, this bit is automatically cleared. Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used. After setting this bit, software should wait until the bit clears before continuing.
### Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>21</td>
<td>DCTRIG5</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Trigger 5</td>
</tr>
</tbody>
</table>

#### Value Description

- 0: No effect.
- 1: Resets the Digital Comparator 5 trigger unit to its initial conditions.

When the trigger has been cleared, this bit is automatically cleared.

Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>DCTRIG4</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Trigger 4</td>
</tr>
</tbody>
</table>

#### Value Description

- 0: No effect.
- 1: Resets the Digital Comparator 4 trigger unit to its initial conditions.

When the trigger has been cleared, this bit is automatically cleared.

Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19</td>
<td>DCTRIG3</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Trigger 3</td>
</tr>
</tbody>
</table>

#### Value Description

- 0: No effect.
- 1: Resets the Digital Comparator 3 trigger unit to its initial conditions.

When the trigger has been cleared, this bit is automatically cleared.

Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>DCTRIG2</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Trigger 2</td>
</tr>
</tbody>
</table>

#### Value Description

- 0: No effect.
- 1: Resets the Digital Comparator 2 trigger unit to its initial conditions.

When the trigger has been cleared, this bit is automatically cleared.

Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>17</td>
<td>DCTRI17</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Trigger 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 1 trigger unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the trigger has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>16</td>
<td>DCTRI16</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Trigger 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 0 trigger unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the trigger has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the trigger, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>DCINT7</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Interrupt 7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 7 interrupt unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the interrupt has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>6</td>
<td>DCINT6</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Interrupt 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 6 interrupt unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the interrupt has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>5</td>
<td>DCINT5</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Interrupt 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 5 interrupt unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the interrupt has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>4</td>
<td>DCINT4</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Interrupt 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 4 interrupt unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the interrupt has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>3</td>
<td>DCINT3</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Interrupt 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 3 interrupt unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the interrupt has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>2</td>
<td>DCINT2</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Interrupt 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 2 interrupt unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the interrupt has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>1</td>
<td>DCINT1</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Interrupt 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 1 interrupt unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the interrupt has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
<tr>
<td>0</td>
<td>DCINT0</td>
<td>WO</td>
<td>0</td>
<td>Digital Comparator Interrupt 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Resets the Digital Comparator 0 interrupt unit to its initial conditions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the interrupt has been cleared, this bit is automatically cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Because the digital comparators use the current and previous ADC conversion values to determine when to assert the interrupt, it is important to reset the digital comparator to initial conditions when starting a new sequence so that stale data is not used.</td>
</tr>
</tbody>
</table>
Register 44: ADC Digital Comparator Control 0 (ADCDCCTL0), offset 0xE0
Register 45: ADC Digital Comparator Control 1 (ADCDCCTL1), offset 0xE04
Register 46: ADC Digital Comparator Control 2 (ADCDCCTL2), offset 0xE08
Register 47: ADC Digital Comparator Control 3 (ADCDCCTL3), offset 0xE0C
Register 48: ADC Digital Comparator Control 4 (ADCDCCTL4), offset 0xE10
Register 49: ADC Digital Comparator Control 5 (ADCDCCTL5), offset 0xE14
Register 50: ADC Digital Comparator Control 6 (ADCDCCTL6), offset 0xE18
Register 51: ADC Digital Comparator Control 7 (ADCDCCTL7), offset 0xE1C

This register provides the comparison encodings that generate an interrupt and/or PWM trigger. See “Interrupt/ADC-Trigger Selector” on page 1259 for more information on using the ADC digital comparators to trigger a PWM generator.

ADC Digital Comparator Control n (ADCDCCTLn)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0xE00
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>RO</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12</td>
<td>CTE</td>
<td>RW</td>
<td>0</td>
<td>Comparison Trigger Enable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Disables the trigger function state machine. ADC conversion data is ignored by the trigger function.</td>
</tr>
<tr>
<td>1</td>
<td>Enables the trigger function state machine. The ADC conversion data is used to determine if a trigger should be generated according to the programming of the CTC and CTM fields.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
</tr>
<tr>
<td>11:10</td>
<td>CTC</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Low Band</td>
</tr>
<tr>
<td></td>
<td>ADC Data &lt; COMP0 ≤ COMP1</td>
</tr>
<tr>
<td>0x1</td>
<td>Mid Band</td>
</tr>
<tr>
<td></td>
<td>COMP0 &lt; ADC Data ≤ COMP1</td>
</tr>
<tr>
<td>0x2</td>
<td>reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>High Band</td>
</tr>
<tr>
<td></td>
<td>COMP0 ≤ COMP1 ≤ ADC Data</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>9:8</th>
<th>CTM</th>
<th>RW</th>
<th>0x0</th>
<th>Comparison Trigger Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field specifies the mode by which the trigger comparison is made.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Always</td>
</tr>
<tr>
<td></td>
<td>This mode generates a trigger every time the ADC conversion data falls within the selected operational region.</td>
</tr>
<tr>
<td>0x1</td>
<td>Once</td>
</tr>
<tr>
<td></td>
<td>This mode generates a trigger the first time that the ADC conversion data enters the selected operational region.</td>
</tr>
<tr>
<td>0x2</td>
<td>Hysteresis Always</td>
</tr>
<tr>
<td></td>
<td>This mode generates a trigger when the ADC conversion data falls within the selected operational region and continues to generate the trigger until the hysteresis condition is cleared by entering the opposite operational region.</td>
</tr>
<tr>
<td></td>
<td>Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.</td>
</tr>
<tr>
<td>0x3</td>
<td>Hysteresis Once</td>
</tr>
<tr>
<td></td>
<td>This mode generates a trigger the first time that the ADC conversion data falls within the selected operational region. No additional triggers are generated until the hysteresis condition is cleared by entering the opposite operational region.</td>
</tr>
<tr>
<td></td>
<td>Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.</td>
</tr>
</tbody>
</table>

| 7:5     | reserved | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
### Comparison Interrupt Enable

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>CIE</td>
<td>RW</td>
<td>0</td>
<td>Comparison Interrupt Enable</td>
</tr>
</tbody>
</table>

- **Value**
- **Description**
  - 0: Disables the comparison interrupt. ADC conversion data has no effect on interrupt generation.
  - 1: Enables the comparison interrupt. The ADC conversion data is used to determine if an interrupt should be generated according to the programming of the CIC and CIM fields.

### Comparison Interrupt Condition

This field specifies the operational region in which an interrupt is generated when the ADC conversion data is compared against the values of COMP0 and COMP1. The COMP0 and COMP1 fields are defined in the ADCDCMPx registers.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Low Band</td>
</tr>
<tr>
<td></td>
<td>ADC Data &lt; COMP0 ≤ COMP1</td>
</tr>
<tr>
<td>0x1</td>
<td>Mid Band</td>
</tr>
<tr>
<td></td>
<td>COMP0 ≤ ADC Data &lt; COMP1</td>
</tr>
<tr>
<td>0x2</td>
<td>reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>High Band</td>
</tr>
<tr>
<td></td>
<td>COMP0 &lt; COMP1 ≤ ADC Data</td>
</tr>
</tbody>
</table>

### Comparison Interrupt Mode

This field specifies the mode by which the interrupt comparison is made.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Always</td>
</tr>
<tr>
<td></td>
<td>This mode generates an interrupt every time the ADC conversion data falls within the selected operational region.</td>
</tr>
<tr>
<td>0x1</td>
<td>Once</td>
</tr>
<tr>
<td></td>
<td>This mode generates an interrupt the first time that the ADC conversion data enters the selected operational region.</td>
</tr>
<tr>
<td>0x2</td>
<td>Hysteresis Always</td>
</tr>
<tr>
<td></td>
<td>This mode generates an interrupt when the ADC conversion data falls within the selected operational region and continues to generate the interrupt until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.</td>
</tr>
<tr>
<td>0x3</td>
<td>Hysteresis Once</td>
</tr>
<tr>
<td></td>
<td>This mode generates an interrupt the first time that the ADC conversion data falls within the selected operational region. No additional interrupts are generated until the hysteresis condition is cleared by entering the opposite operational region. Note that the hysteresis modes are only defined for CTC encodings of 0x0 and 0x3.</td>
</tr>
</tbody>
</table>
Register 52: ADC Digital Comparator Range 0 (ADCDCCMP0), offset 0xE40
Register 53: ADC Digital Comparator Range 1 (ADCDCCMP1), offset 0xE44
Register 54: ADC Digital Comparator Range 2 (ADCDCCMP2), offset 0xE48
Register 55: ADC Digital Comparator Range 3 (ADCDCCMP3), offset 0xE4C
Register 56: ADC Digital Comparator Range 4 (ADCDCCMP4), offset 0xE50
Register 57: ADC Digital Comparator Range 5 (ADCDCCMP5), offset 0xE54
Register 58: ADC Digital Comparator Range 6 (ADCDCCMP6), offset 0xE58
Register 59: ADC Digital Comparator Range 7 (ADCDCCMP7), offset 0xE5C

This register defines the comparison values that are used to determine if the ADC conversion data falls in the appropriate operating region.

**Note:** The value in the COMP1 field must be greater than or equal to the value in the COMP0 field or unexpected results can occur.

### ADC Digital Comparator Range n (ADCDCCMPn)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>27:16</td>
<td>COMP1</td>
<td>RW</td>
<td>0x000</td>
<td>Compare 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value in this field is compared against the ADC conversion data.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The result of the comparison is used to determine if the data lies within the high-band region.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note that the value of COMP1 must be greater than or equal to the value of COMP0.</td>
</tr>
<tr>
<td>15:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11:0</td>
<td>COMP0</td>
<td>RW</td>
<td>0x000</td>
<td>Compare 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value in this field is compared against the ADC conversion data.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The result of the comparison is used to determine if the data lies within the low-band region.</td>
</tr>
</tbody>
</table>
Register 60: ADC Peripheral Properties (ADCPP), offset 0xFC0

The **ADCPP** register provides information regarding the properties of the ADC module.

ADC Peripheral Properties (ADCPP)

ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset (0xFC0)
Type RO, reset 0x00B0.2167

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23</td>
<td>TS</td>
<td>RO</td>
<td>0x1</td>
<td>Temperature Sensor</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td>The ADC module does not have a temperature sensor.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The ADC module has a temperature sensor.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This field provides the similar information as the legacy DC1 register TEMPSNS bit.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22:18</td>
<td>RSL</td>
<td>RO</td>
<td>0xC</td>
<td>Resolution</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0x0</td>
<td>SAR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1 - 0x3</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17:16</td>
<td>TYPE</td>
<td>RO</td>
<td>0x0</td>
<td>ADC Architecture</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0x0</td>
<td>SAR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Digital Comparator Count</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:10</td>
<td>DC</td>
<td>RO</td>
<td>0x8</td>
<td>This field specifies the number of ADC digital comparators available to</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>the converter. The field is encoded as a binary value, in the range of 0</td>
</tr>
<tr>
<td>0x0</td>
<td>SAR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>to 63. This field provides similar information to the legacy DC9 register ADCnDCn bits.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### ADC Channel Count

This field specifies the number of ADC input channels available to the converter. This field is encoded as a binary value, in the range of 0 to 63. This field provides similar information to the legacy DC3 and DC8 register ADCnAINn bits.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:4</td>
<td>CH</td>
<td>RO</td>
<td>0x16</td>
<td>ADC Channel Count</td>
</tr>
</tbody>
</table>

### Maximum ADC Sample Rate

This field specifies the maximum number of ADC conversions per second. The MSR field is encoded as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x1</td>
<td>125 ksp</td>
</tr>
<tr>
<td>0x2</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>250 ksp</td>
</tr>
<tr>
<td>0x4</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x5</td>
<td>500 ksp</td>
</tr>
<tr>
<td>0x6</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x7</td>
<td>1 Msps</td>
</tr>
<tr>
<td>0x8 - 0xF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register 61: ADC Peripheral Configuration (ADCPC), offset 0xFC4

The ADCPC register provides information regarding the configuration of the peripheral.

ADC Peripheral Configuration (ADCPC)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0xFC4
Type RW, reset 0x0000.0007

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Bit/Field</th>
<th>Type</th>
<th>Reset</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on</td>
<td>0x0000.0000</td>
<td>31:4</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>reserved</td>
<td>the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>ADC Sample Rate</td>
<td>0x7</td>
<td>3:0</td>
<td>RW</td>
<td>0x7</td>
<td>SR</td>
<td>This field specifies the number of ADC conversions per second and is used in Run, Sleep, and Deep-Sleep modes. The field encoding is based on the legacy RCGC0 register encoding. The programmed sample rate cannot exceed the maximum sample rate specified by the MSR field in the ADCPP register. The SR field is encoded as follows:</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x1</td>
<td>125 kbps</td>
</tr>
<tr>
<td>0x2</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x3</td>
<td>250 kbps</td>
</tr>
<tr>
<td>0x4</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x5</td>
<td>500 kbps</td>
</tr>
<tr>
<td>0x6</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x7</td>
<td>1 Msps</td>
</tr>
<tr>
<td>0x8 - 0xF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register 62: ADC Clock Configuration (ADCCC), offset 0xFC8

The ADCCC register controls the clock source for the ADC module.

To use the PIOSC to clock the ADC, first power up the PLL and then enable the PIOSC in the CS bit field, then disable the PLL.

To use the MOSC to clock the ADC, first power up the PLL and then enable the clock to the ADC module, then disable the PLL and switch to the MOSC for the system clock.

ADC Clock Configuration (ADCCC)
ADC0 base: 0x4003.8000
ADC1 base: 0x4003.9000
Offset 0xFC8
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3:0</td>
<td>CS</td>
<td>RW</td>
<td>0</td>
<td>ADC Clock Source</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The following table specifies the clock source that generates the ADC clock input, see Figure 5-5 on page 222.</td>
</tr>
</tbody>
</table>

Value | Description
--- | ---
0x0 | Either the 16-MHz system clock (if the PLL bypass is in effect) or the 16 MHz clock derived from PLL ÷ 25 (default). Note that when the PLL is bypassed, the system clock must be at least 16 MHz.
0x1 | PIOSC
The PIOSC provides a 16-MHz clock source for the ADC.
If the PIOSC is used as the clock source, the ADC module can continue to operate in Deep-Sleep mode.
0x2 - 0xF | Reserved
Universal Asynchronous Receivers/Transmitters (UARTs)

The TM4C123GH6PZ controller includes eight Universal Asynchronous Receiver/Transmitter (UART) with the following features:

- Programmable baud-rate generator allowing speeds up to 5 Mbps for regular speed (divide by 16) and 10 Mbps for high speed (divide by 8)
- Separate 16x8 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte deep operation providing conventional double-buffered interface
- FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no-parity bit generation/detection
  - 1 or 2 stop bit generation
- IrDA serial-IR (SIR) encoder/decoder providing
  - Programmable use of IrDA Serial Infrared (SIR) or UART input/output
  - Support of IrDA SIR encoder/decoder functions for data rates up to 115.2 Kbps half-duplex
  - Support of normal 3/16 and low-power (1.41-2.23 μs) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power mode bit duration
- Support for communication with ISO 7816 smart cards
- Modem flow control and status (on UART1)
- EIA-485 9-bit support
- Standard FIFO-level and End-of-Transmission interrupts
- Efficient transfers using Micro Direct Memory Access Controller (μDMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted at programmed FIFO level
- Transmit single request asserted when there is space in the FIFO; burst request asserted at programmed FIFO level

### 14.1 Block Diagram

**Figure 14-1. UART Module Block Diagram**

![Block Diagram](image)

#### 14.2 Signal Description

The following table lists the external signals of the UART module and describes the function of each. The UART signals are alternate functions for some GPIO signals and default to be GPIO signals at reset, with the exception of the `U0Rx` and `U0Tx` pins which default to the UART function. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for these UART signals. The `AFSEL` bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the UART function. The number in parentheses is the encoding that must be programmed into the `PMCn` field in the GPIO Port Control (GPIOPCTL) register (page 702) to assign the UART signal to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659.
### Table 14-1. UART Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Typeᵃ</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>U0Rx</td>
<td>26</td>
<td>PA0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 0 receive.</td>
</tr>
<tr>
<td>U0Tx</td>
<td>27</td>
<td>PA1 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 0 transmit.</td>
</tr>
<tr>
<td>U1CTS</td>
<td>24</td>
<td>PC5 (8) PF1 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Clear To Send modem flow control input signal.</td>
</tr>
<tr>
<td>U1DCD</td>
<td>42</td>
<td>PF2 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Data Carrier Detect modem status input signal.</td>
</tr>
<tr>
<td>U1DSR</td>
<td>43</td>
<td>PF3 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Data Set Ready modem output control line.</td>
</tr>
<tr>
<td>U1DTR</td>
<td>39</td>
<td>PF4 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Data Terminal Ready modem status input signal.</td>
</tr>
<tr>
<td>U1RI</td>
<td>90</td>
<td>PE7 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Ring Indicator modem status input signal.</td>
</tr>
<tr>
<td>U1RTS</td>
<td>25 40</td>
<td>PC4 (8) PF0 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Request to Send modem flow control output line.</td>
</tr>
<tr>
<td>U1Rx</td>
<td>25 70</td>
<td>PC4 (2) PB0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 receive.</td>
</tr>
<tr>
<td>U1Tx</td>
<td>24 71</td>
<td>PC5 (2) PB1 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 transmit.</td>
</tr>
<tr>
<td>U2Rx</td>
<td>74 99</td>
<td>PG4 (1) PD6 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 2 receive.</td>
</tr>
<tr>
<td>U2Tx</td>
<td>75 100</td>
<td>PG5 (1) PD7 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 2 transmit.</td>
</tr>
<tr>
<td>U3Rx</td>
<td>23</td>
<td>PC6 (1) PD7 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 3 receive.</td>
</tr>
<tr>
<td>U3Tx</td>
<td>22</td>
<td>PC7 (1) PD6 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 3 transmit.</td>
</tr>
<tr>
<td>U4Rx</td>
<td>25 68</td>
<td>PC4 (1) PJ0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 4 receive.</td>
</tr>
<tr>
<td>U4Tx</td>
<td>24 69</td>
<td>PC5 (1) PJ1 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 4 transmit.</td>
</tr>
<tr>
<td>U5Rx</td>
<td>11 95</td>
<td>PJ2 (1) PE4 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 5 receive.</td>
</tr>
<tr>
<td>U5Tx</td>
<td>96</td>
<td>PE5 (1) PD4 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 5 transmit.</td>
</tr>
<tr>
<td>U6Rx</td>
<td>97</td>
<td>PD4 (1) PD0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 6 receive.</td>
</tr>
<tr>
<td>U6Tx</td>
<td>98</td>
<td>PD5 (1) PD0 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 6 transmit.</td>
</tr>
<tr>
<td>U7Rx</td>
<td>15</td>
<td>PE0 (1) PD0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 7 receive.</td>
</tr>
<tr>
<td>U7Tx</td>
<td>14</td>
<td>PE1 (1) PD0 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 7 transmit.</td>
</tr>
</tbody>
</table>

ᵃ. The TTL designation indicates the pin has TTL-compatible voltage levels.

### 14.3 Functional Description

Each TM4C123GH6PZ UART performs the functions of parallel-to-serial and serial-to-parallel conversions. It is similar in functionality to a 16C550 UART, but is not register compatible.

The UART is configured for transmit and/or receive via the $\text{TXE}$ and $\text{RXE}$ bits of the UART Control (UARTCTL) register (see page 939). Transmit and receive are both enabled out of reset. Before any control registers are programmed, the UART must be disabled by clearing the $\text{UARTEN}$ bit in UARTCTL. If the UART is disabled during a TX or RX operation, the current transaction is completed prior to the UART stopping.
The UART module also includes a serial IR (SIR) encoder/decoder block that can be connected to an infrared transceiver to implement an IrDA SIR physical layer. The SIR function is programmed using the UARTCTL register.

### 14.3.1 Transmit/Receive Logic

The transmit logic performs parallel-to-serial conversion on the data read from the transmit FIFO. The control logic outputs the serial bit stream beginning with a start bit and followed by the data bits (LSB first), parity bit, and the stop bits according to the programmed configuration in the control registers. See Figure 14-2 on page 915 for details.

The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse has been detected. Overrun, parity, frame error checking, and line-break detection are also performed, and their status accompanies the data that is written to the receive FIFO.

#### Figure 14-2. UART Character Frame

![UART Character Frame](image)

### 14.3.2 Baud-Rate Generation

The baud-rate divisor is a 22-bit number consisting of a 16-bit integer and a 6-bit fractional part. The number formed by these two values is used by the baud-rate generator to determine the bit period. Having a fractional baud-rate divisor allows the UART to generate all the standard baud rates.

The 16-bit integer is loaded through the UART Integer Baud-Rate Divisor (UARTIBRD) register (see page 935) and the 6-bit fractional part is loaded with the UART Fractional Baud-Rate Divisor (UARTFBRD) register (see page 936). The baud-rate divisor (BRD) has the following relationship to the system clock (where BRDI is the integer part of the BRD and BRDF is the fractional part, separated by a decimal place.)

\[
BRD = BRDI + BRDF = UARTSysClk / (ClkDiv \times Baud\ Rate)
\]

where UARTSysClk is the system clock connected to the UART, and ClkDiv is either 16 (if HSE in UARTCTL is clear) or 8 (if HSE is set). By default, this will be the main system clock described in “Clock Control” on page 219. Alternatively, the UART may be clocked from the internal precision oscillator (PIOSC), independent of the system clock selection. This will allow the UART clock to be programmed independently of the system clock PLL settings. See the UARTCC register for more details.

The 6-bit fractional number (that is to be loaded into the DIVFRAC bit field in the UARTFBRD register) can be calculated by taking the fractional part of the baud-rate divisor, multiplying it by 64, and adding 0.5 to account for rounding errors:

\[
UARTFBRD[DIVFRAC] = \text{integer}(BRDF \times 64 + 0.5)
\]

The UART generates an internal baud-rate reference clock at 8x or 16x the baud-rate (referred to as Baud8 and Baud16, depending on the setting of the HSE bit (bit 5) in UARTCTL). This reference clock is divided by 8 or 16 to generate the transmit clock, and is used for error detection during receive operations. Note that the state of the HSE bit has no effect on clock generation in ISO 7816 smart card mode (when the SMART bit in the UARTCTL register is set).
Along with the UART Line Control, High Byte (UARTLCRH) register (see page 937), the UARTIBRD and UARTFBRD registers form an internal 30-bit register. This internal register is only updated when a write operation to UARTLCRH is performed, so any changes to the baud-rate divisor must be followed by a write to the UARTLCRH register for the changes to take effect.

To update the baud-rate registers, there are four possible sequences:

- UARTIBRD write, UARTFBRD write, and UARTLCRH write
- UARTFBRD write, UARTIBRD write, and UARTLCRH write
- UARTIBRD write and UARTLCRH write
- UARTFBRD write and UARTLCRH write

### 14.3.3 Data Transmission

Data received or transmitted is stored in two 16-byte FIFOs, though the receive FIFO has an extra four bits per character for status information. For transmission, data is written into the transmit FIFO. If the UART is enabled, it causes a data frame to start transmitting with the parameters indicated in the UARTLCRH register. Data continues to be transmitted until there is no data left in the transmit FIFO. The BUSY bit in the UART Flag (UARTFR) register (see page 931) is asserted as soon as data is written to the transmit FIFO (that is, if the FIFO is non-empty) and remains asserted while data is being transmitted. The BUSY bit is negated only when the transmit FIFO is empty, and the last character has been transmitted from the shift register, including the stop bits. The UART can indicate that it is busy even though the UART may no longer be enabled.

When the receiver is idle (the UnRx signal is continuously 1), and the data input goes Low (a start bit has been received), the receive counter begins running and data is sampled on the eighth cycle of Baud16 or fourth cycle of Baud8 depending on the setting of the HSE bit (bit 5) in UARTCTL (described in “Transmit/Receive Logic” on page 915).

The start bit is valid and recognized if the UnRx signal is still low on the eighth cycle of Baud16 (HSE clear) or the fourth cycle of Baud 8 (HSE set), otherwise it is ignored. After a valid start bit is detected, successive data bits are sampled on every 16th cycle of Baud16 or 8th cycle of Baud8 (that is, one bit period later) according to the programmed length of the data characters and value of the HSE bit in UARTCTL. The parity bit is then checked if parity mode is enabled. Data length and parity are defined in the UARTLCRH register.

Lastly, a valid stop bit is confirmed if the UnRx signal is High, otherwise a framing error has occurred. When a full word is received, the data is stored in the receive FIFO along with any error bits associated with that word.

### 14.3.4 Serial IR (SIR)

The UART peripheral includes an IrDA serial-IR (SIR) encoder/decoder block. The IrDA SIR block provides functionality that converts between an asynchronous UART data stream and a half-duplex serial SIR interface. No analog processing is performed on-chip. The role of the SIR block is to provide a digital encoded output and decoded input to the UART. When enabled, the SIR block uses the UnTx and UnRx pins for the SIR protocol. These signals should be connected to an infrared transceiver to implement an IrDA SIR physical layer link. The SIR block can receive and transmit, but it is only half-duplex so it cannot do both at the same time. Transmission must be stopped before data can be received. The IrDA SIR physical layer specifies a minimum 10-ms delay between transmission and reception. The SIR block has two modes of operation:
In normal IrDA mode, a zero logic level is transmitted as a high pulse of 3/16th duration of the selected baud rate bit period on the output pin, while logic one levels are transmitted as a static LOW signal. These levels control the driver of an infrared transmitter, sending a pulse of light for each zero. On the reception side, the incoming light pulses energize the photo transistor base of the receiver, pulling its output LOW and driving the UART input pin LOW.

In low-power IrDA mode, the width of the transmitted infrared pulse is set to three times the period of the internally generated IrLPBaud16 signal (1.63 μs, assuming a nominal 1.8432 MHz frequency) by changing the appropriate bit in the UARTCTL register (see page 939).

Whether the device is in normal or low-power IrDA mode, a start bit is deemed valid if the decoder is still Low, one period of IrLPBaud16 after the Low was first detected. This enables a normal-mode UART to receive data from a low-power mode UART that can transmit pulses as small as 1.41 μs. Thus, for both low-power and normal mode operation, the ILPDVSR field in the UARTILPR register must be programmed such that 1.42 MHz < \( F_{IrLPBaud16} \) < 2.12 MHz, resulting in a low-power pulse duration of 1.41–2.11 μs (three times the period of IrLPBaud16). The minimum frequency of IrLPBaud16 ensures that pulses less than one period of IrLPBaud16 are rejected, but pulses greater than 1.4 μs are accepted as valid pulses.

Figure 14-3 on page 917 shows the UART transmit and receive signals, with and without IrDA modulation.

![Figure 14-3. IrDA Data Modulation](image)

In both normal and low-power IrDA modes:

- During transmission, the UART data bit is used as the base for encoding.
- During reception, the decoded bits are transferred to the UART receive logic.

The IrDA SIR physical layer specifies a half-duplex communication link, with a minimum 10-ms delay between transmission and reception. This delay must be generated by software because it is not automatically supported by the UART. The delay is required because the infrared receiver electronics might become biased or even saturated from the optical power coupled from the adjacent transmitter LED. This delay is known as latency or receiver setup time.

### 14.3.5 ISO 7816 Support

The UART offers basic support to allow communication with an ISO 7816 smartcard. When bit 3 (SMART) of the UARTCTL register is set, the UnTx signal is used as a bit clock, and the UnRx signal...
is used as the half-duplex communication line connected to the smartcard. A GPIO signal can be used to generate the reset signal to the smartcard. The remaining smartcard signals should be provided by the system design. The maximum clock rate in this mode is system clock / 16.

When using ISO 7816 mode, the UARTLCRH register must be set to transmit 8-bit words (WLEN bits 6:5 configured to 0x3) with EVEN parity (PEN set and EPS set). In this mode, the UART automatically uses 2 stop bits, and the STP2 bit of the UARTLCRH register is ignored.

If a parity error is detected during transmission, UnRx is pulled Low during the second stop bit. In this case, the UART aborts the transmission, flushes the transmit FIFO and discards any data it contains, and raises a parity error interrupt, allowing software to detect the problem and initiate retransmission of the affected data. Note that the UART does not support automatic retransmission in this case.

### 14.3.6 Modem Handshake Support

This section describes how to configure and use the modem flow control and status signals for UART1 when connected as a DTE (data terminal equipment) or as a DCE (data communications equipment). In general, a modem is a DCE and a computing device that connects to a modem is the DTE.

#### 14.3.6.1 Signaling

The status signals provided by UART1 differ based on whether the UART is used as a DTE or DCE. When used as a DTE, the modem flow control and status signals are defined as:

- U1CTS is Clear To Send
- U1DSR is Data Set Ready
- U1DCD is Data Carrier Detect
- U1RI is Ring Indicator
- U1RTS is Request To Send
- U1DTR is Data Terminal Ready

When used as a DCE, the modem flow control and status signals are defined as:

- U1CTS is Request To Send
- U1DSR is Data Terminal Ready
- U1RTS is Clear To Send
- U1DTR is Data Set Ready

Note that the support for DCE functions Data Carrier Detect and Ring Indicator are not provided. If these signals are required, their function can be emulated by using a general-purpose I/O signal and providing software support.

#### 14.3.6.2 Flow Control

Flow control can be accomplished by either hardware or software. The following sections describe the different methods.
Hardware Flow Control (RTS/CTS)

Hardware flow control between two devices is accomplished by connecting the U1RTS output to the Clear-To-Send input on the receiving device, and connecting the Request-To-Send output on the receiving device to the U1CTS input.

The U1CTS input controls the transmitter. The transmitter may only transmit data when the U1CTS input is asserted. The U1RTS output signal indicates the state of the receive FIFO. U1CTS remains asserted until the preprogrammed watermark level is reached, indicating that the Receive FIFO has no space to store additional characters.

The UARTCTL register bits 15 (CTSEN) and 14 (RTSEN) specify the flow control mode as shown in Table 14-2 on page 919.

Table 14-2. Flow Control Mode

<table>
<thead>
<tr>
<th>CTSEN</th>
<th>RTSEN</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>RTS and CTS flow control enabled</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Only CTS flow control enabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Only RTS flow control enabled</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>Both RTS and CTS flow control disabled</td>
</tr>
</tbody>
</table>

Note that when RTSEN is 1, software cannot modify the U1RTS output value through the UARTCTL register Request to Send (RTS) bit, and the status of the RTS bit should be ignored.

Software Flow Control (Modem Status Interrupts)

Software flow control between two devices is accomplished by using interrupts to indicate the status of the UART. Interrupts may be generated for the U1DSR, U1DCD, U1CTS, and U1RI signals using bits 3:0 of the UARTIM register, respectively. The raw and masked interrupt status may be checked using the UARTRIS and UARTMIS register. These interrupts may be cleared using the UARTICR register.

14.3.7 9-Bit UART Mode

The UART provides a 9-bit mode that is enabled with the 9BITEN bit in the UART9BITADDR register. This feature is useful in a multi-drop configuration of the UART where a single master connected to multiple slaves can communicate with a particular slave through its address or set of addresses along with a qualifier for an address byte. All the slaves check for the address qualifier in the place of the parity bit and, if set, then compare the byte received with the preprogrammed address. If the address matches, then it receives or sends further data. If the address does not match, it drops the address byte and any subsequent data bytes. If the UART is in 9-bit mode, then the receiver operates with no parity mode. The address can be predefined to match with the received byte and it can be configured with the UART9BITADDR register. The matching can be extended to a set of addresses using the address mask in the UART9BITAMASK register. By default, the UART9BITAMASK is 0xFF, meaning that only the specified address is matched.

When not finding a match, the rest of the data bytes with the 9th bit cleared are dropped. If a match is found, then an interrupt is generated to the NVIC for further action. The subsequent data bytes with the cleared 9th bit are stored in the FIFO. Software can mask this interrupt in case μDMA and/or FIFO operations are enabled for this instance and processor intervention is not required. All the send transactions with 9-bit mode are data bytes and the 9th bit is cleared. Software can override the 9th bit to be set (to indicate address) by overriding the parity settings to sticky parity with odd parity enabled for a particular byte. To match the transmission time with correct parity settings, the
14.3.8 FIFO Operation

The UART has two 16x8 FIFOs; one for transmit and one for receive. Both FIFOs are accessed via the UART Data (UARTDR) register (see page 926). Read operations of the UARTDR register return a 12-bit value consisting of 8 data bits and 4 error flags while write operations place 8-bit data in the transmit FIFO.

Out of reset, both FIFOs are disabled and act as 1-byte-deep holding registers. The FIFOs are enabled by setting the FEN bit in UARTLCRH (page 937).

FIFO status can be monitored via the UART Flag (UARTFR) register (see page 931) and the UART Receive Status (UARTRSR) register. Hardware monitors empty, full and overrun conditions. The UARTFR register contains empty and full flags (TXFE, TXFF, RXFE, and RXFF bits), and the UARTRSR register shows overrun status via the OE bit. If the FIFOs are disabled, the empty and full flags are set according to the status of the 1-byte-deep holding registers.

The trigger points at which the FIFOs generate interrupts is controlled via the UART Interrupt FIFO Level Select (UARTIFLS) register (see page 943). Both FIFOs can be individually configured to trigger interrupts at different levels. Available configurations include ⅛, ¼, ½, ¾, and ⅞. For example, if the ¼ option is selected for the receive FIFO, the UART generates a receive interrupt after 4 data bytes are received. Out of reset, both FIFOs are configured to trigger an interrupt at the ½ mark.

14.3.9 Interrupts

The UART can generate interrupts when the following conditions are observed:

- Overrun Error
- Break Error
- Parity Error
- Framing Error
- Receive Timeout
- Transmit (when condition defined in the TXIFLSEL bit in the UARTIFLS register is met, or if the EOT bit in UARTCTL is set, when the last bit of all transmitted data leaves the serializer)
- Receive (when condition defined in the RXIFLSEL bit in the UARTIFLS register is met)

All of the interrupt events are ORed together before being sent to the interrupt controller, so the UART can only generate a single interrupt request to the controller at any given time. Software can service multiple interrupt events in a single interrupt service routine by reading the UART Masked Interrupt Status (UARTMIS) register (see page 951).

The interrupt events that can trigger a controller-level interrupt are defined in the UART Interrupt Mask (UARTIM) register (see page 945) by setting the corresponding IM bits. If interrupts are not used, the raw interrupt status is visible via the UART Raw Interrupt Status (UARTRIS) register (see page 948).

**Note:** For receive timeout, the RTIM bit in the UARTIM register must be set to see the RTMIS and RTRIS status in the UARTMIS and UARTRIS registers.
Interrupts are always cleared (for both the UARTMIS and UARTRIS registers) by writing a 1 to the corresponding bit in the UART Interrupt Clear (UARTICR) register (see page 954).

The receive timeout interrupt is asserted when the receive FIFO is not empty, and no further data is received over a 32-bit period when the HSE bit is clear or over a 64-bit period when the HSE bit is set. The receive timeout interrupt is cleared either when the FIFO becomes empty through reading all the data (or by reading the holding register), or when a 1 is written to the corresponding bit in the UARTICR register.

The receive interrupt changes state when one of the following events occurs:

- If the FIFOs are enabled and the receive FIFO reaches the programmed trigger level, the RXRIS bit is set. The receive interrupt is cleared by reading data from the receive FIFO until it becomes less than the trigger level, or by clearing the interrupt by writing a 1 to the RXIC bit.

- If the FIFOs are disabled (have a depth of one location) and data is received thereby filling the location, the RXRIS bit is set. The receive interrupt is cleared by performing a single read of the receive FIFO, or by clearing the interrupt by writing a 1 to the RXIC bit.

The transmit interrupt changes state when one of the following events occurs:

- If the FIFOs are enabled and the transmit FIFO progresses through the programmed trigger level, the TXRIS bit is set. The transmit interrupt is based on a transition through level, therefore the FIFO must be written past the programmed trigger level otherwise no further transmit interrupts will be generated. The transmit interrupt is cleared by writing data to the transmit FIFO until it becomes greater than the trigger level, or by clearing the interrupt by writing a 1 to the TXIC bit.

- If the FIFOs are disabled (have a depth of one location) and there is no data present in the transmitters single location, the TXRIS bit is set. It is cleared by performing a single write to the transmit FIFO, or by clearing the interrupt by writing a 1 to the TXIC bit.

14.3.10 Loopback Operation

The UART can be placed into an internal loopback mode for diagnostic or debug work by setting the LBE bit in the UARTCTL register (see page 939). In loopback mode, data transmitted on the UnTx output is received on the UnRx input. Note that the LBE bit should be set before the UART is enabled.

14.3.11 DMA Operation

The UART provides an interface to the µDMA controller with separate channels for transmit and receive. The DMA operation of the UART is enabled through the UART DMA Control (UARTDMACTL) register. When DMA operation is enabled, the UART asserts a DMA request on the receive or transmit channel when the associated FIFO can transfer data. For the receive channel, a single transfer request is asserted whenever any data is in the receive FIFO. A burst transfer request is asserted whenever the amount of data in the receive FIFO is at or above the FIFO trigger level configured in the UARTIFLS register. For the transmit channel, a single transfer request is asserted whenever there is at least one empty location in the transmit FIFO. The burst request is asserted whenever the transmit FIFO contains fewer characters than the FIFO trigger level. The single and burst DMA transfer requests are handled automatically by the µDMA controller depending on how the DMA channel is configured.

To enable DMA operation for the receive channel, set the RXDMAE bit of the DMA Control (UARTDMACTL) register. To enable DMA operation for the transmit channel, set the TXDMAE bit of the UARTDMACTL register. The UART can also be configured to stop using DMA for the receive
channel if a receive error occurs. If the DMAERR bit of the UARTDMACR register is set and a receive error occurs, the DMA receive requests are automatically disabled. This error condition can be cleared by clearing the appropriate UART error interrupt.

If the µDMA is enabled, then the controller triggers an interrupt when the TX FIFO or RX FIFO has reached a trigger point as programmed in the UARTIFLS register. The interrupt occurs on the UART interrupt vector. Therefore, if interrupts are used for UART operation and DMA is enabled, the UART interrupt handler must be designed to handle the µDMA completion interrupt.

**Note:** To trigger an interrupt on transmit completion from the UART's serializer, the EOT bit must be set in the UARTCTL register. In this configuration, the transmit interrupt is generated once the FIFO is completely empty and all data including the stop bits have left the transmit serializer. In this case, setting the TXIFLSEL bit in the UARTIFLS register is ignored.

When transfers are performed from a FIFO of the UART using the µDMA, and any interrupt is generated from the UART, the UART module's status bit in the DMA Channel Interrupt Status (DMACHIS) register must be checked at the end of the interrupt service routine. If the status bit is set, clear the interrupt by writing a 1 to it.

See “Micro Direct Memory Access (µDMA)” on page 595 for more details about programming the µDMA controller.

### 14.4 Initialization and Configuration

To enable and initialize the UART, the following steps are necessary:

1. Enable the UART module using the RCGCUART register (see page 347).

2. Enable the clock to the appropriate GPIO module via the RCGCGPIO register (see page 342). To find out which GPIO port to enable, refer to Table 23-5 on page 1386.

3. Set the GPIO AFSEL bits for the appropriate pins (see page 684). To determine which GPIOs to configure, see Table 23-4 on page 1377.

4. Configure the GPIO current level and/or slew rate as specified for the mode selected (see page 686 and page 694).

5. Configure the PMCn fields in the GPIOPCTL register to assign the UART signals to the appropriate pins (see page 702 and Table 23-5 on page 1386).

To use the UART, the peripheral clock must be enabled by setting the appropriate bit in the RCGCUART register (page 347). In addition, the clock to the appropriate GPIO module must be enabled via the RCGCGPIO register (page 342) in the System Control module. To find out which GPIO port to enable, refer to Table 23-5 on page 1386.

This section discusses the steps that are required to use a UART module. For this example, the UART clock is assumed to be 20 MHz, and the desired UART configuration is:

- 115200 baud rate
- Data length of 8 bits
- One stop bit
- No parity
- FIFOs disabled
The first thing to consider when programming the UART is the baud-rate divisor (BRD), because the UARTIBRD and UARTFBRD registers must be written before the UARTLCRH register. Using the equation described in “Baud-Rate Generation” on page 915, the BRD can be calculated:

\[ \text{BRD} = \frac{20,000,000}{16 \times 115,200} = 10.8507 \]

which means that the DIVINT field of the UARTIBRD register (see page 935) should be set to 10 decimal or 0xA. The value to be loaded into the UARTFBRD register (see page 936) is calculated by the equation:

\[ \text{UARTFBRD}[\text{DIVFRAC}] = \text{integer}(0.8507 \times 64 + 0.5) = 54 \]

With the BRD values in hand, the UART configuration is written to the module in the following order:

1. Disable the UART by clearing the UARTEN bit in the UARTCTL register.
2. Write the integer portion of the BRD to the UARTIBRD register.
3. Write the fractional portion of the BRD to the UARTFBRD register.
4. Write the desired serial parameters to the UARTLCRH register (in this case, a value of 0x0000.0060).
5. Configure the UART clock source by writing to the UARTCC register.
6. Optionally, configure the μDMA channel (see “Micro Direct Memory Access (μDMA)” on page 595) and enable the DMA option(s) in the UARTDMACTL register.
7. Enable the UART by setting the UARTEN bit in the UARTCTL register.

### 14.5 Register Map

Table 14-3 on page 924 lists the UART registers. The offset listed is a hexadecimal increment to the register's address, relative to that UART's base address:

- UART0: 0x4000.C000
- UART1: 0x4000.D000
- UART2: 0x4000.E000
- UART3: 0x4000.F000
- UART4: 0x4001.0000
- UART5: 0x4001.1000
- UART6: 0x4001.2000
- UART7: 0x4001.3000

The UART module clock must be enabled before the registers can be programmed (see page 347). There must be a delay of 3 system clocks after the UART module clock is enabled before any UART module registers are accessed.

The UART must be disabled (see the UARTEN bit in the UARTCTL register on page 939) before any of the control registers are reprogrammed. When the UART is disabled during a TX or RX operation, the current transaction is completed prior to the UART stopping.
## Table 14-3. UART Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>UARTDR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART Data</td>
<td>926</td>
</tr>
<tr>
<td>0x004</td>
<td>UARTRSR/UARTECR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART Receive Status/Error Clear</td>
<td>928</td>
</tr>
<tr>
<td>0x018</td>
<td>UARTFR</td>
<td>RO</td>
<td>0x0000.0090</td>
<td>UART Flag</td>
<td>931</td>
</tr>
<tr>
<td>0x020</td>
<td>UARTILPR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART IrDA Low-Power Register</td>
<td>934</td>
</tr>
<tr>
<td>0x024</td>
<td>UARTIBRD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART Integer Baud-Rate Divisor</td>
<td>935</td>
</tr>
<tr>
<td>0x028</td>
<td>UARTFBRD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART Fractional Baud-Rate Divisor</td>
<td>936</td>
</tr>
<tr>
<td>0x02C</td>
<td>UARTLCRH</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART Line Control</td>
<td>937</td>
</tr>
<tr>
<td>0x030</td>
<td>UARTCTL</td>
<td>RW</td>
<td>0x0000.0300</td>
<td>UART Control</td>
<td>939</td>
</tr>
<tr>
<td>0x034</td>
<td>UARTIFLS</td>
<td>RW</td>
<td>0x0000.0012</td>
<td>UART Interrupt FIFO Level Select</td>
<td>943</td>
</tr>
<tr>
<td>0x038</td>
<td>UARTIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART Interrupt Mask</td>
<td>945</td>
</tr>
<tr>
<td>0x03C</td>
<td>UARTRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>UART Raw Interrupt Status</td>
<td>948</td>
</tr>
<tr>
<td>0x040</td>
<td>UARTMIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>UART Masked Interrupt Status</td>
<td>951</td>
</tr>
<tr>
<td>0x044</td>
<td>UARTICR</td>
<td>W1C</td>
<td>0x0000.0000</td>
<td>UART Interrupt Clear</td>
<td>954</td>
</tr>
<tr>
<td>0x048</td>
<td>UARTDMACCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART DMA Control</td>
<td>956</td>
</tr>
<tr>
<td>0x0A4</td>
<td>UART9BITADDR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART 9-Bit Self Address</td>
<td>957</td>
</tr>
<tr>
<td>0x0A8</td>
<td>UART9BITAMASK</td>
<td>RW</td>
<td>0x0000.00FF</td>
<td>UART 9-Bit Self Address Mask</td>
<td>958</td>
</tr>
<tr>
<td>0xFC0</td>
<td>UARTPP</td>
<td>RO</td>
<td>0x0000.0003</td>
<td>UART Peripheral Properties</td>
<td>959</td>
</tr>
<tr>
<td>0xFC8</td>
<td>UARTCC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>UART Clock Configuration</td>
<td>960</td>
</tr>
<tr>
<td>0xFD0</td>
<td>UARTPeriphID4</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>UART Peripheral Identification 4</td>
<td>961</td>
</tr>
<tr>
<td>0xFD4</td>
<td>UARTPeriphID5</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>UART Peripheral Identification 5</td>
<td>962</td>
</tr>
<tr>
<td>0xFD8</td>
<td>UARTPeriphID6</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>UART Peripheral Identification 6</td>
<td>963</td>
</tr>
<tr>
<td>0xFD0</td>
<td>UARTPeriphID7</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>UART Peripheral Identification 7</td>
<td>964</td>
</tr>
<tr>
<td>0xFE0</td>
<td>UARTPeriphID0</td>
<td>RO</td>
<td>0x0000.0060</td>
<td>UART Peripheral Identification 0</td>
<td>965</td>
</tr>
<tr>
<td>0xFE4</td>
<td>UARTPeriphID1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>UART Peripheral Identification 1</td>
<td>966</td>
</tr>
<tr>
<td>0xFE8</td>
<td>UARTPeriphID2</td>
<td>RO</td>
<td>0x0000.0018</td>
<td>UART Peripheral Identification 2</td>
<td>967</td>
</tr>
<tr>
<td>0xFE0</td>
<td>UARTPeriphID3</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>UART Peripheral Identification 3</td>
<td>968</td>
</tr>
<tr>
<td>0xFF0</td>
<td>UARTCellID0</td>
<td>RO</td>
<td>0x0000.000D</td>
<td>UART PrimeCell Identification 0</td>
<td>969</td>
</tr>
<tr>
<td>0xFF4</td>
<td>UARTCellID1</td>
<td>RO</td>
<td>0x0000.00F0</td>
<td>UART PrimeCell Identification 1</td>
<td>970</td>
</tr>
<tr>
<td>0xFF8</td>
<td>UARTCellID2</td>
<td>RO</td>
<td>0x0000.0005</td>
<td>UART PrimeCell Identification 2</td>
<td>971</td>
</tr>
<tr>
<td>0xFFC</td>
<td>UARTCellID3</td>
<td>RO</td>
<td>0x0000.00B1</td>
<td>UART PrimeCell Identification 3</td>
<td>972</td>
</tr>
</tbody>
</table>
14.6 Register Descriptions

The remainder of this section lists and describes the UART registers, in numerical order by address offset.
Register 1: UART Data (UARTDR), offset 0x000

**Important:** This register is read-sensitive. See the register description for details.

This register is the data register (the interface to the FIFOs).

For transmitted data, if the FIFO is enabled, data written to this location is pushed onto the transmit FIFO. If the FIFO is disabled, data is stored in the transmitter holding register (the bottom word of the transmit FIFO). A write to this register initiates a transmission from the UART.

For received data, if the FIFO is enabled, the data byte and the 4-bit status (break, frame, parity, and overrun) is pushed onto the 12-bit wide receive FIFO. If the FIFO is disabled, the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO). The received data can be retrieved by reading this register.

**UART Data (UARTDR)**

UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0x000
Type RW, reset 0x0000.0000

- **Bit 31:** Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
- **Bit 11:** UART Overrun Error
  - Value Description
    - 0: No data has been lost due to a FIFO overrun.
    - 1: New data was received when the FIFO was full, resulting in data loss.
### UART Break Error

**Description**

No break condition has occurred

**Value**

- 0: No break condition has occurred
- 1: A break condition has been detected, indicating that the receive data input was held Low for longer than a full-word transmission time (defined as start, data, parity, and stop bits).

In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the received data input goes to a 1 (marking state), and the next valid start bit is received.

### UART Parity Error

**Description**

The parity of the received data character does not match the parity defined by bits 2 and 7 of the UARTLCRH register.

**Value**

- 0: No parity error has occurred
- 1: The parity of the received data character does not match the parity defined by bits 2 and 7 of the UARTLCRH register.

In FIFO mode, this error is associated with the character at the top of the FIFO.

### UART Framing Error

**Description**

The received character does not have a valid stop bit (a valid stop bit is 1).

**Value**

- 0: No framing error has occurred
- 1: The received character does not have a valid stop bit (a valid stop bit is 1).

### Data Transmitted or Received

Data that is to be transmitted via the UART is written to this field. When read, this field contains the data that was received by the UART.

---

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>BE</td>
<td>RO</td>
<td>0</td>
<td>UART Break Error</td>
</tr>
<tr>
<td>9</td>
<td>PE</td>
<td>RO</td>
<td>0</td>
<td>UART Parity Error</td>
</tr>
<tr>
<td>8</td>
<td>FE</td>
<td>RO</td>
<td>0</td>
<td>UART Framing Error</td>
</tr>
<tr>
<td>7:0</td>
<td>DATA</td>
<td>RW</td>
<td>0x00</td>
<td>Data Transmitted or Received</td>
</tr>
</tbody>
</table>

**Texas Instruments-Production Data**

June 12, 2014
Register 2: UART Receive Status/Error Clear (UARTRSR/UARTECR), offset 0x004

The **UARTRSR/UARTECR** register is the receive status register/error clear register.

In addition to the **UARTDR** register, receive status can also be read from the **UARTRSR** register. If the status is read from this register, then the status information corresponds to the entry read from **UARTDR** prior to reading **UARTRSR**. The status information for overrun is set immediately when an overrun condition occurs.

The **UARTRSR** register cannot be written.

A write of any value to the **UARTECR** register clears the framing, parity, break, and overrun errors. All the bits are cleared on reset.

### Read-Only Status Register

**UART Receive Status/Error Clear (UARTRSR/UARTECR)**

<table>
<thead>
<tr>
<th>UART0 base: 0x4000.C000</th>
<th>UART1 base: 0x4000.D000</th>
<th>UART2 base: 0x4000.E000</th>
<th>UART3 base: 0x4000.F000</th>
<th>UART4 base: 0x4001.0000</th>
<th>UART5 base: 0x4001.1000</th>
<th>UART6 base: 0x4001.2000</th>
<th>UART7 base: 0x4001.3000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset 0x004 Type RO, reset 0x0000.0000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>OE</td>
<td>RO</td>
<td>0</td>
<td>UART Overrun Error</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

This bit is cleared by a write to **UARTECR**. The FIFO contents remain valid because no further data is written when the FIFO is full, only the contents of the shift register are overwritten. The CPU must read the data in order to empty the FIFO.
### UART Receive Status/Error Clear (UARTRSR/UARTECR)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>BE</td>
<td>RO</td>
<td>0</td>
<td>UART Break Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No break condition has occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  A break condition has been detected, indicating that the receive data input was held Low for longer than a full-word transmission time (defined as start, data, parity, and stop bits).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared to 0 by a write to UARTCR.</td>
</tr>
<tr>
<td>1</td>
<td>PE</td>
<td>RO</td>
<td>0</td>
<td>UART Parity Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No parity error has occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The parity of the received data character does not match the parity defined by bits 2 and 7 of the UARTLCRH register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared to 0 by a write to UARTCR.</td>
</tr>
<tr>
<td>0</td>
<td>FE</td>
<td>RO</td>
<td>0</td>
<td>UART Framing Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No framing error has occurred</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The received character does not have a valid stop bit (a valid stop bit is 1).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared to 0 by a write to UARTCR.</td>
</tr>
</tbody>
</table>

**Write-Only Error Clear Register**

UART Receive Status/Error Clear (UARTRSR/UARTECR)
### Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

### Error Clear
A write to this register of any data clears the framing, parity, break, and overrun flags.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>WO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>DATA</td>
<td>WO</td>
<td>0x00</td>
<td>Error Clear</td>
</tr>
</tbody>
</table>

A write to this register of any data clears the framing, parity, break, and overrun flags.
Register 3: UART Flag (UARTFR), offset 0x018

The UARTFR register is the flag register. After reset, the TXFF, RXFF, and BUSY bits are 0, and TXFE and RXFE bits are 1. The RI, DCD, DSR and CTS bits indicate the modem flow control and status. Note that the modem bits are only implemented on UART1 and are reserved on UART0 and UART2.

UART Flag (UARTFR)

| UART0 base: 0x4000.C000 |
| UART1 base: 0x4000.D000 |
| UART2 base: 0x4000.E000 |
| UART3 base: 0x4000.F000 |
| UART4 base: 0x4001.0000 |
| UART5 base: 0x4001.1000 |
| UART6 base: 0x4001.2000 |
| UART7 base: 0x4001.3000 |
| Offset 0x018 |
| Type RO, reset 0x0000.0090 |

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0000 0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:9</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8</td>
<td>RI</td>
<td>RO</td>
<td>0</td>
<td>Ring Indicator</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>7</td>
<td>TXFE</td>
<td>RO</td>
<td>1</td>
<td>UART Transmit FIFO Empty</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Universal Asynchronous Receivers/Transmitters (UARTs)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>RXFF</td>
<td>RO</td>
<td>0</td>
<td>UART Receive FIFO Full</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The meaning of this bit depends on the state of the FEN bit in the UARTLCRH register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The receiver can receive data.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>If the FIFO is disabled (FEN is 0), the receive holding register is full.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the FIFO is enabled (FEN is 1), the receive FIFO is full.</td>
</tr>
<tr>
<td>5</td>
<td>TXFF</td>
<td>RO</td>
<td>0</td>
<td>UART Transmit FIFO Full</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The meaning of this bit depends on the state of the FEN bit in the UARTLCRH register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The transmitter is not full.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>If the FIFO is disabled (FEN is 0), the transmit holding register is full.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the FIFO is enabled (FEN is 1), the transmit FIFO is full.</td>
</tr>
<tr>
<td>4</td>
<td>RXFE</td>
<td>RO</td>
<td>1</td>
<td>UART Receive FIFO Empty</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The meaning of this bit depends on the state of the FEN bit in the UARTLCRH register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The receiver is not empty.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>If the FIFO is disabled (FEN is 0), the receive holding register is empty.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the FIFO is enabled (FEN is 1), the receive FIFO is empty.</td>
</tr>
<tr>
<td>3</td>
<td>BUSY</td>
<td>RO</td>
<td>0</td>
<td>UART Busy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The UART is not busy.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>The UART is busy transmitting data. This bit remains set until the complete byte, including all stop bits, has been sent from the shift register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is set as soon as the transmit FIFO becomes non-empty (regardless of whether UART is enabled).</td>
</tr>
<tr>
<td>2</td>
<td>DCD</td>
<td>RO</td>
<td>0</td>
<td>Data Carrier Detect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>The U1DCD signal is not asserted.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td>The U1DCD signal is asserted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>----------------------------</td>
</tr>
<tr>
<td>1</td>
<td>DSR</td>
<td>RO</td>
<td>0</td>
<td>Data Set Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>CTS</td>
<td>RO</td>
<td>0</td>
<td>Clear To Send</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

This bit is implemented only on UART1 and is reserved for UART0 and UART2.
Register 4: UART IrDA Low-Power Register (UARTILPR), offset 0x020

The UARTILPR register stores the 8-bit low-power counter divisor value used to derive the low-power SIR pulse width clock by dividing down the system clock (SysClk). All the bits are cleared when reset.

The internal IrLPBaud16 clock is generated by dividing down SysClk according to the low-power divisor value written to UARTILPR. The duration of SIR pulses generated when low-power mode is enabled is three times the period of the IrLPBaud16 clock. The low-power divisor value is calculated as follows:

$$\text{ILPDVSR} = \frac{\text{SysClk}}{F_{\text{IrLPBaud16}}}$$

where $F_{\text{IrLPBaud16}}$ is nominally 1.8432 MHz.

Because the IrLPBaud16 clock is used to sample transmitted data irrespective of mode, the ILPDVSR field must be programmed in both low power and normal mode, such that $1.42 \text{ MHz} < F_{\text{IrLPBaud16}} < 2.12 \text{ MHz}$, resulting in a low-power pulse duration of 1.41–2.11 μs (three times the period of IrLPBaud16). The minimum frequency of IrLPBaud16 ensures that pulses less than one period of IrLPBaud16 are rejected, but pulses greater than 1.4 μs are accepted as valid pulses.

**Note:** Zero is an illegal value. Programming a zero value results in no IrLPBaud16 pulses being generated.

UART IrDA Low-Power Register (UARTILPR)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x020</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td></td>
<td>RW</td>
<td>0x00</td>
<td>IrDA Low-Power Divisor</td>
</tr>
</tbody>
</table>

This field contains the 8-bit low-power divisor value.
Register 5: UART Integer Baud-Rate Divisor (UARTIBRD), offset 0x024

The UARTIBRD register is the integer part of the baud-rate divisor value. All the bits are cleared on reset. The minimum possible divide ratio is 1 (when UARTIBRD=0), in which case the UARTFBRD register is ignored. When changing the UARTIBRD register, the new value does not take effect until transmission/reception of the current character is complete. Any changes to the baud-rate divisor must be followed by a write to the UARTLCRH register. See “Baud-Rate Generation” on page 915 for configuration details.

UART Integer Baud-Rate Divisor (UARTIBRD)
UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0x024
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>DIVINT</td>
<td>RW</td>
<td>0x0000</td>
<td>Integer Baud-Rate Divisor</td>
</tr>
</tbody>
</table>
Register 6: UART Fractional Baud-Rate Divisor (UARTFBRD), offset 0x028

The UARTFBRD register is the fractional part of the baud-rate divisor value. All the bits are cleared on reset. When changing the UARTFBRD register, the new value does not take effect until transmission/reception of the current character is complete. Any changes to the baud-rate divisor must be followed by a write to the UARTLCRH register. See “Baud-Rate Generation” on page 915 for configuration details.

UART Fractional Baud-Rate Divisor (UARTFBRD)
UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0x028
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5:0</td>
<td>DIVFRAC</td>
<td>RW</td>
<td>0x0</td>
<td>Fractional Baud-Rate Divisor</td>
</tr>
</tbody>
</table>
Register 7: UART Line Control (UARTLCRH), offset 0x02C

The UARTLCRH register is the line control register. Serial parameters such as data length, parity, and stop bit selection are implemented in this register.

When updating the baud-rate divisor (UARTIBRD and/or UARTIFRD), the UARTLCRH register must also be written. The write strobe for the baud-rate divisor registers is tied to the UARTLCRH register.

UART Line Control (UARTLCRH)

| UART0 base: 0x4000.C000 |
| UART1 base: 0x4000.D000 |
| UART2 base: 0x4000.E000 |
| UART3 base: 0x4000.F000 |
| UART4 base: 0x4001.0000 |
| UART5 base: 0x4001.1000 |
| UART6 base: 0x4001.2000 |
| UART7 base: 0x4001.3000 |

Offset 0x02C
Type RW, reset 0x0000.0000
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>FEN</td>
<td>RW</td>
<td>0</td>
<td>UART Enable FIFOs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The FIFOs are disabled (Character mode). The FIFOs become 1-byte-deep holding registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The transmit and receive FIFO buffers are enabled (FIFO mode).</td>
</tr>
<tr>
<td>3</td>
<td>STP2</td>
<td>RW</td>
<td>0</td>
<td>UART Two Stop Bits Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>One stop bit is transmitted at the end of a frame.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Two stop bits are transmitted at the end of a frame. The receive logic does not check for two stop bits being received. When in 7816 smartcard mode (the SMART bit is set in the UARTCTL register), the number of stop bits is forced to 2.</td>
</tr>
<tr>
<td>2</td>
<td>EPS</td>
<td>RW</td>
<td>0</td>
<td>UART Even Parity Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Odd parity is performed, which checks for an odd number of 1s.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Even parity generation and checking is performed during transmission and reception, which checks for an even number of 1s in data and parity bits. This bit has no effect when parity is disabled by the PEN bit.</td>
</tr>
<tr>
<td>1</td>
<td>PEN</td>
<td>RW</td>
<td>0</td>
<td>UART Parity Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Parity is disabled and no parity bit is added to the data frame.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Parity checking and generation is enabled.</td>
</tr>
<tr>
<td>0</td>
<td>BRK</td>
<td>RW</td>
<td>0</td>
<td>UART Send Break</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Normal use.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A Low level is continually output on the UnTx signal, after completing transmission of the current character. For the proper execution of the break command, software must set this bit for at least two frames (character periods).</td>
</tr>
</tbody>
</table>
Register 8: UART Control (UARTCTL), offset 0x030

The UARTCTL register is the control register. All the bits are cleared on reset except for the Transmit Enable (TXE) and Receive Enable (RXE) bits, which are set.

To enable the UART module, the UARTEN bit must be set. If software requires a configuration change in the module, the UARTEN bit must be cleared before the configuration changes are written. If the UART is disabled during a transmit or receive operation, the current transaction is completed prior to the UART stopping.

Note that bits [15:14, 11:10] are only implemented on UART1. These bits are reserved on UART0 and UART2.

Note: The UARTCTL register should not be changed while the UART is enabled or else the results are unpredictable. The following sequence is recommended for making changes to the UARTCTL register.

1. Disable the UART.
2. Wait for the end of transmission or reception of the current character.
3. Flush the transmit FIFO by clearing bit 4 (FEN) in the line control register (UARTLCRH).
4. Reprogram the control register.
5. Enable the UART.

UART Control (UARTCTL)

| UART0 base: 0x4000.C000 |
| UART1 base: 0x4000.D000 |
| UART2 base: 0x4000.E000 |
| UART3 base: 0x4000.F000 |
| UART4 base: 0x4001.0000 |
| UART5 base: 0x4001.1000 |
| UART6 base: 0x4001.2000 |
| UART7 base: 0x4001.3000 |
Offset 0x030
Type RW, reset 0x0000.0300

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
## Universal Asynchronous Receivers/Transmitters (UARTs)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>CTSEN</td>
<td>RW</td>
<td>0</td>
<td>Enable Clear To Send</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  CTS hardware flow control is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  CTS hardware flow control is enabled. Data is only transmitted when the U1CTS signal is asserted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>14</td>
<td>RTSEN</td>
<td>RW</td>
<td>0</td>
<td>Enable Request to Send</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  RTS hardware flow control is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  RTS hardware flow control is enabled. Data is only requested (by asserting U1RTS) when the receive FIFO has available entries.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>13:12</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>RTS</td>
<td>RW</td>
<td>0</td>
<td>Request to Send</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When RTSEN is clear, the status of this bit is reflected on the U1RTS signal. If RTSEN is set, this bit is ignored on a write and should be ignored on read.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>10</td>
<td>DTR</td>
<td>RW</td>
<td>0</td>
<td>Data Terminal Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit sets the state of the U1DTR output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>9</td>
<td>RXE</td>
<td>RW</td>
<td>1</td>
<td>UART Receive Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The receive section of the UART is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The receive section of the UART is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the UART is disabled in the middle of a receive, it completes the current character before stopping.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> To enable reception, the UARTEN bit must also be set.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>8</td>
<td>TXE</td>
<td>RW</td>
<td>1</td>
<td>UART Transmit Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The transmit section of the UART is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The transmit section of the UART is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the UART is disabled in the middle of a transmission, it completes the current character before stopping.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> To enable transmission, the UARTEN bit must also be set.</td>
</tr>
<tr>
<td>7</td>
<td>LBE</td>
<td>RW</td>
<td>0</td>
<td>UART Loop Back Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The UnTx path is fed through the UnRx path.</td>
</tr>
<tr>
<td>6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>HSE</td>
<td>RW</td>
<td>0</td>
<td>High-Speed Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The UART is clocked using the system clock divided by 16.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The UART is clocked using the system clock divided by 8.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> System clock used is also dependent on the baud-rate divisor configuration (see page 935) and page 936).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The state of this bit has no effect on clock generation in ISO 7816 smart card mode (the SMART bit is set).</td>
</tr>
<tr>
<td>4</td>
<td>EOT</td>
<td>RW</td>
<td>0</td>
<td>End of Transmission</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit determines the behavior of the TXRIS bit in the UARTRIS register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The TXRIS bit is set when the transmit FIFO condition specified in UARTIFLS is met.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The TXRIS bit is set only after all transmitted data, including stop bits, have cleared the serializer.</td>
</tr>
</tbody>
</table>
### ISO 7816 Smart Card Support

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>SMART</td>
<td>RW</td>
<td>0</td>
<td>ISO 7816 Smart Card Support</td>
</tr>
</tbody>
</table>

**Value**  
0 Normal operation.  
1 The UART operates in Smart Card mode.

The application must ensure that it sets 8-bit word length (WLEN set to 0x3) and even parity (PEN set to 1, EPS set to 1, SPS set to 0) in UARTLCRH when using ISO 7816 mode.

In this mode, the value of the STP2 bit in UARTLCRH is ignored and the number of stop bits is forced to 2. Note that the UART does not support automatic retransmission on parity errors. If a parity error is detected on transmission, all further transmit operations are aborted and software must handle retransmission of the affected byte or message.

### UART SIR Low-Power Mode

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>SIRLP</td>
<td>RW</td>
<td>0</td>
<td>UART SIR Low-Power Mode</td>
</tr>
</tbody>
</table>

This bit selects the IrDA encoding mode.

**Value**  
0 Low-level bits are transmitted as an active High pulse with a width of 3/16th of the bit period.  
1 The UART operates in SIR Low-Power mode. Low-level bits are transmitted with a pulse width which is 3 times the period of the IrLPBaud16 input signal, regardless of the selected bit rate.

Setting this bit uses less power, but might reduce transmission distances. See page 934 for more information.

### UART SIR Enable

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SIREN</td>
<td>RW</td>
<td>0</td>
<td>UART SIR Enable</td>
</tr>
</tbody>
</table>

**Value**  
0 Normal operation.  
1 The IrDA SIR block is enabled, and the UART will transmit and receive data using SIR protocol.

### UART Enable

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>UARTEN</td>
<td>RW</td>
<td>0</td>
<td>UART Enable</td>
</tr>
</tbody>
</table>

**Value**  
0 The UART is disabled.  
1 The UART is enabled.

If the UART is disabled in the middle of transmission or reception, it completes the current character before stopping.
Register 9: UART Interrupt FIFO Level Select (UARTIFLS), offset 0x034

The UARTIFLS register is the interrupt FIFO level select register. You can use this register to define the FIFO level at which the TXRIS and RXRIS bits in the UARTRIS register are triggered.

The interrupts are generated based on a transition through a level rather than being based on the level. That is, the interrupts are generated when the fill level progresses through the trigger level. For example, if the receive trigger level is set to the half-way mark, the interrupt is triggered as the module is receiving the 9th character.

Out of reset, the TXIFLSEL and RXIFLSEL bits are configured so that the FIFOs trigger an interrupt at the half-way mark.

UART Interrupt FIFO Level Select (UARTIFLS)

| UART0 base: 0x4000.C000 |
| UART1 base: 0x4000.D000 |
| UART2 base: 0x4000.E000 |
| UART3 base: 0x4000.F000 |
| UART4 base: 0x4001.0000 |
| UART5 base: 0x4001.1000 |
| UART6 base: 0x4001.2000 |
| UART7 base: 0x4001.3000 |
| Offset 0x034 |
Type RW, reset 0x0000.0012

| 31:6 | reserved |
Type RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |
Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

| 5:3 | RXIFLSEL |
Type RW | 0x2 |
Reset 0x0000.00 |

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

UART Receive Interrupt FIFO Level Select
The trigger points for the receive interrupt are as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>RX FIFO ≥ ¼ full</td>
</tr>
<tr>
<td>0x1</td>
<td>RX FIFO ≥ ¼ full</td>
</tr>
<tr>
<td>0x2</td>
<td>RX FIFO ≥ ½ full (default)</td>
</tr>
<tr>
<td>0x3</td>
<td>RX FIFO ≥ ¾ full</td>
</tr>
<tr>
<td>0x4</td>
<td>RX FIFO ≥ ¾ full</td>
</tr>
<tr>
<td>0x5-0x7</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### UART Transmit Interrupt FIFO Level Select

The trigger points for the transmit interrupt are as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>TX FIFO ≤ ⅛ empty</td>
</tr>
<tr>
<td>0x1</td>
<td>TX FIFO ≤ ¼ empty</td>
</tr>
<tr>
<td>0x2</td>
<td>TX FIFO ≤ ½ empty (default)</td>
</tr>
<tr>
<td>0x3</td>
<td>TX FIFO ≤ ¼ empty</td>
</tr>
<tr>
<td>0x4</td>
<td>TX FIFO ≤ ⅛ empty</td>
</tr>
<tr>
<td>0x5-0x7</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Note:** If the EOT bit in UARTCTL is set (see page 939), the transmit interrupt is generated once the FIFO is completely empty and all data including stop bits have left the transmit serializer. In this case, the setting of TXIFLSEL is ignored.
Register 10: UART Interrupt Mask (UARTIM), offset 0x038

The UARTIM register is the interrupt mask set/clear register.

On a read, this register gives the current value of the mask on the relevant interrupt. Setting a bit allows the corresponding raw interrupt signal to be routed to the interrupt controller. Clearing a bit prevents the raw interrupt signal from being sent to the interrupt controller.

Note that bits [3:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

UART Interrupt Mask (UARTIM)

UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0x038
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12</td>
<td>9BITIM</td>
<td>RW</td>
<td>0</td>
<td>9-Bit Mode Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The 9BITRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the 9BITRIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td>11</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10</td>
<td>OEIM</td>
<td>RW</td>
<td>0</td>
<td>UART Overrun Error Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The OERIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the OERIS bit in the UARTRIS register is set.</td>
</tr>
</tbody>
</table>
### Universal Asynchronous Receivers/Transmitters (UARTs)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>BEIM</td>
<td>RW</td>
<td>0</td>
<td>UART Break Error Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The BERIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the BERIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td>8</td>
<td>PEIM</td>
<td>RW</td>
<td>0</td>
<td>UART Parity Error Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The PERIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the PERIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td>7</td>
<td>FEIM</td>
<td>RW</td>
<td>0</td>
<td>UART Framing Error Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The FERIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the FERIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td>6</td>
<td>RTIM</td>
<td>RW</td>
<td>0</td>
<td>UART Receive Time-Out Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The RTRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the RTRIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td>5</td>
<td>TXIM</td>
<td>RW</td>
<td>0</td>
<td>UART Transmit Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The TXRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the TXRIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td>4</td>
<td>RXIM</td>
<td>RW</td>
<td>0</td>
<td>UART Receive Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The RXRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the RXRIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>----------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>3</td>
<td>DSRIM</td>
<td>RW</td>
<td>0</td>
<td>UART Data Set Ready Modem Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   The DSRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An interrupt is sent to the interrupt controller when the DSRIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>2</td>
<td>DCDIM</td>
<td>RW</td>
<td>0</td>
<td>UART Data Carrier Detect Modem Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   The DCDRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An interrupt is sent to the interrupt controller when the DCDRIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>1</td>
<td>CTSIM</td>
<td>RW</td>
<td>0</td>
<td>UART Clear to Send Modem Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   The CTSRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An interrupt is sent to the interrupt controller when the CTSRIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>0</td>
<td>RIIM</td>
<td>RW</td>
<td>0</td>
<td>UART Ring Indicator Modem Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   The RIRIS interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   An interrupt is sent to the interrupt controller when the RIRIS bit in the UARTRIS register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
</tbody>
</table>
Register 11: UART Raw Interrupt Status (UARTRIS), offset 0x03C

The UARTRIS register is the raw interrupt status register. On a read, this register gives the current raw status value of the corresponding interrupt. A write has no effect.

Note that bits [3:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

UART Raw Interrupt Status (UARTRIS)
UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0x03C
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12</td>
<td>9BITRIS</td>
<td>RO</td>
<td>0</td>
<td>9-Bit Mode Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A receive address match has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the 9BITIC bit in the UARTICR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>11</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10</td>
<td>OERIS</td>
<td>RO</td>
<td>0</td>
<td>UART Overrun Error Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An overrun error has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the OERIC bit in the UARTICR register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>9</td>
<td>BERIS</td>
<td>RO</td>
<td>0</td>
<td>UART Break Error Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A break error has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the BEIC bit in the UARTICR register.</td>
</tr>
<tr>
<td>8</td>
<td>PERIS</td>
<td>RO</td>
<td>0</td>
<td>UART Parity Error Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A parity error has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the PEIC bit in the UARTICR register.</td>
</tr>
<tr>
<td>7</td>
<td>FERIS</td>
<td>RO</td>
<td>0</td>
<td>UART Framing Error Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A framing error has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the FEIC bit in the UARTICR register.</td>
</tr>
<tr>
<td>6</td>
<td>RTRIS</td>
<td>RO</td>
<td>0</td>
<td>UART Receive Time-Out Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A receive time out has occurred.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the RTIC bit in the UARTICR register. For receive timeout, the RTIM bit in the UARTIM register must be set to see the RTRIS status.</td>
</tr>
<tr>
<td>5</td>
<td>TXRIS</td>
<td>RO</td>
<td>0</td>
<td>UART Transmit Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 If the EOT bit in the UARTCTL register is clear, the transmit FIFO level has passed through the condition defined in the UARTIFLS register. If the EOT bit is set, the last bit of all transmitted data and flags has left the serializer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the TXIC bit in the UARTICR register or by writing data to the transmit FIFO until it becomes greater than the trigger level, if the FIFO is enabled, or by writing a single byte if the FIFO is disabled.</td>
</tr>
</tbody>
</table>
**Universal Asynchronous Receivers/Transmitters (UARTs)**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>RXRIS</td>
<td>RO</td>
<td>0</td>
<td>UART Receive Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The receive FIFO level has passed through the condition defined in the UARTIFLS register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the RXIC bit in the UARTICR register or by reading data from the receive FIFO until it becomes less than the trigger level, if the FIFO is enabled, or by reading a single byte if the FIFO is disabled.</td>
</tr>
<tr>
<td>3</td>
<td>DSRRIS</td>
<td>RO</td>
<td>0</td>
<td>UART Data Set Ready Modem Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Data Set Ready used for software flow control.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the DSRIC bit in the UARTICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>2</td>
<td>DCDRIS</td>
<td>RO</td>
<td>0</td>
<td>UART Data Carrier Detect Modem Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Data Carrier Detect used for software flow control.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the DCDIC bit in the UARTICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>1</td>
<td>CTSRIS</td>
<td>RO</td>
<td>0</td>
<td>UART Clear to Send Modem Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Clear to Send used for software flow control.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CTSIC bit in the UARTICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>0</td>
<td>RIRIS</td>
<td>RO</td>
<td>0</td>
<td>UART Ring Indicator Modem Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Ring Indicator used for software flow control.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the RIIC bit in the UARTICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
</tbody>
</table>
The **UARTMIS** register is the masked interrupt status register. On a read, this register gives the current masked status value of the corresponding interrupt. A write has no effect.

Note that bits [3:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

### UART Masked Interrupt Status (UARTMIS)

UART0 base: 0x4000.C000  
UART1 base: 0x4000.D000  
UART2 base: 0x4000.E000  
UART3 base: 0x4000.F000  
UART4 base: 0x4001.0000  
UART5 base: 0x4001.1000  
UART6 base: 0x4001.2000  
UART7 base: 0x4001.3000  
Offset 0x040  
Type RO, reset 0x0000.0000

![Register 12: UART Masked Interrupt Status (UARTMIS), offset 0x040](image)

### Description

**Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.**

#### 9-Bit Mode Masked Interrupt Status

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12</td>
<td>9BITMIS</td>
<td>RO</td>
<td>0</td>
<td>9-Bit Mode Masked Interrupt Status</td>
</tr>
<tr>
<td>11</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10</td>
<td>OEMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Overrun Error Masked Interrupt Status</td>
</tr>
</tbody>
</table>

**Value Description**

0  
An interrupt has not occurred or is masked.

1  
An unmasked interrupt was signaled due to a receive address match.

This bit is cleared by writing a 1 to the OEIC bit in the UARTCR register.

#### UART Overrun Error Masked Interrupt Status

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10</td>
<td>OEMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Overrun Error Masked Interrupt Status</td>
</tr>
</tbody>
</table>

**Value Description**

0  
An interrupt has not occurred or is masked.

1  
An unmasked interrupt was signaled due to an overrun error.

This bit is cleared by writing a 1 to the OEIC bit in the UARTCR register.
### UART Break Error Masked Interrupt Status

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>BEMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Break Error Masked Interrupt Status</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: An interrupt has not occurred or is masked.
- **1**: An unmasked interrupt was signaled due to a break error.

This bit is cleared by writing a **1** to the **BEIC** bit in the **UARTCR** register.

### UART Parity Error Masked Interrupt Status

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>PEMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Parity Error Masked Interrupt Status</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: An interrupt has not occurred or is masked.
- **1**: An unmasked interrupt was signaled due to a parity error.

This bit is cleared by writing a **1** to the **PEIC** bit in the **UARTCR** register.

### UART Framing Error Masked Interrupt Status

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>FEMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Framing Error Masked Interrupt Status</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: An interrupt has not occurred or is masked.
- **1**: An unmasked interrupt was signaled due to a framing error.

This bit is cleared by writing a **1** to the **FEIC** bit in the **UARTCR** register.

### UART Receive Time-Out Masked Interrupt Status

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>RTMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Receive Time-Out Masked Interrupt Status</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: An interrupt has not occurred or is masked.
- **1**: An unmasked interrupt was signaled due to a receive time out.

This bit is cleared by writing a **1** to the **RTIC** bit in the **UARTCR** register. For receive timeout, the **RTIM** bit in the **UARTIM** register must be set to see the **RTMIS** status.

### UART Transmit Masked Interrupt Status

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>TXMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Transmit Masked Interrupt Status</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: An interrupt has not occurred or is masked.
- **1**: An unmasked interrupt was signaled due to passing through the specified transmit FIFO level (if the **EOT** bit is clear) or due to the transmission of the last data bit (if the **EOT** bit is set).

This bit is cleared by writing a **1** to the **TXIC** bit in the **UARTCR** register or by writing data to the transmit FIFO until it becomes greater than the trigger level, if the FIFO is enabled, or by writing a single byte if the FIFO is disabled.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RXMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Receive Masked Interrupt Status</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked interrupt was signaled due to passing through the specified receive FIFO level.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the RXIC bit in the UARTICR register or by reading data from the receive FIFO until it becomes less than the trigger level, if the FIFO is enabled, or by reading a single byte if the FIFO is disabled.</td>
</tr>
<tr>
<td>3</td>
<td>DSRMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Data Set Ready Modem Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked interrupt was signaled due to Data Set Ready.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the DSRIC bit in the UARTICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>2</td>
<td>DCDMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Data Carrier Detect Modem Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked interrupt was signaled due to Data Carrier Detect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the DCDIC bit in the UARTICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>1</td>
<td>CTSMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Clear to Send Modem Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked interrupt was signaled due to Clear to Send.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CTSIC bit in the UARTICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>0</td>
<td>RIMIS</td>
<td>RO</td>
<td>0</td>
<td>UART Ring Indicator Modem Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked interrupt was signaled due to Ring Indicator.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the RIIC bit in the UARTICR register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
</tbody>
</table>
Register 13: UART Interrupt Clear (UARTICR), offset 0x044

The UARTICR register is the interrupt clear register. On a write of 1, the corresponding interrupt (both raw interrupt and masked interrupt, if enabled) is cleared. A write of 0 has no effect.

Note that bits [3:0] are only implemented on UART1. These bits are reserved on UART0 and UART2.

UART Interrupt Clear (UARTICR)
UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000

Offset 0x044
Type W1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:13</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>12</td>
<td>9BITIC</td>
<td>RW</td>
<td>0</td>
<td>9-Bit Mode Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the 9BITRIS bit in the UARTRIS register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and the 9BITMIS bit in the UARTMIS register.</td>
</tr>
<tr>
<td>11</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10</td>
<td>OEIC</td>
<td>W1C</td>
<td>0</td>
<td>Overrun Error Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the OERIS bit in the UARTRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the OEMIS bit in the UARTMIS register.</td>
</tr>
<tr>
<td>9</td>
<td>BEIC</td>
<td>W1C</td>
<td>0</td>
<td>Break Error Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the BERIS bit in the UARTRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the BEMIS bit in the UARTMIS register.</td>
</tr>
<tr>
<td>8</td>
<td>PEIC</td>
<td>W1C</td>
<td>0</td>
<td>Parity Error Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the PERIS bit in the UARTRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the PEMIS bit in the UARTMIS register.</td>
</tr>
<tr>
<td>7</td>
<td>FEIC</td>
<td>W1C</td>
<td>0</td>
<td>Framing Error Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the FERIS bit in the UARTRIS register and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the FEMIS bit in the UARTMIS register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>6</td>
<td>RTIC</td>
<td>W1C</td>
<td>0</td>
<td>Receive Time-Out Interrupt Clear Writing a 1 to this bit clears the RTRIS bit in the UARTRIS register and the RTMIS bit in the UARTMIS register.</td>
</tr>
<tr>
<td>5</td>
<td>TXIC</td>
<td>W1C</td>
<td>0</td>
<td>Transmit Interrupt Clear Writing a 1 to this bit clears the TXRIS bit in the UARTRIS register and the TXMIS bit in the UARTMIS register.</td>
</tr>
<tr>
<td>4</td>
<td>RXIC</td>
<td>W1C</td>
<td>0</td>
<td>Receive Interrupt Clear Writing a 1 to this bit clears the RXRIS bit in the UARTRIS register and the RXMIS bit in the UARTMIS register.</td>
</tr>
<tr>
<td>3</td>
<td>DSRMIC</td>
<td>W1C</td>
<td>0</td>
<td>UART Data Set Ready Modem Interrupt Clear Writing a 1 to this bit clears the DSRRIS bit in the UARTRIS register and the DSRMIS bit in the UARTMIS register. This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>2</td>
<td>DCDMIC</td>
<td>W1C</td>
<td>0</td>
<td>UART Data Carrier Detect Modem Interrupt Clear Writing a 1 to this bit clears the DCDRIS bit in the UARTRIS register and the DCDMIS bit in the UARTMIS register. This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>1</td>
<td>CTSMIC</td>
<td>W1C</td>
<td>0</td>
<td>UART Clear to Send Modem Interrupt Clear Writing a 1 to this bit clears the CTSRIS bit in the UARTRIS register and the CTSMIS bit in the UARTMIS register. This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
<tr>
<td>0</td>
<td>RIMIC</td>
<td>W1C</td>
<td>0</td>
<td>UART Ring Indicator Modem Interrupt Clear Writing a 1 to this bit clears the RI RIS bit in the UARTRIS register and the RIMIS bit in the UARTMIS register. This bit is implemented only on UART1 and is reserved for UART0 and UART2.</td>
</tr>
</tbody>
</table>
Register 14: UART DMA Control (UARTDMACTL), offset 0x048

The **UARTDMACTL** register is the DMA control register.

### UART DMA Control (UARTDMACTL)

| UART0 base: 0x4000.C000 |
| UART1 base: 0x4000.D000 |
| UART2 base: 0x4000.E000 |
| UART3 base: 0x4000.F000 |
| UART4 base: 0x4001.0000 |
| UART5 base: 0x4001.1000 |
| UART6 base: 0x4001.2000 |
| UART7 base: 0x4001.3000 |
| Offset 0x048 |
| Type RW, reset 0x0000.0000 |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x00000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>DMAERR</td>
<td>RW</td>
<td>0</td>
<td>DMA on Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>µDMA receive requests are unaffected when a receive error occurs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>µDMA receive requests are automatically disabled when a receive error occurs.</td>
</tr>
<tr>
<td>1</td>
<td>TXDMAE</td>
<td>RW</td>
<td>0</td>
<td>Transmit DMA Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>µDMA for the transmit FIFO is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>µDMA for the transmit FIFO is enabled.</td>
</tr>
<tr>
<td>0</td>
<td>RXDMAE</td>
<td>RW</td>
<td>0</td>
<td>Receive DMA Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>µDMA for the receive FIFO is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>µDMA for the receive FIFO is enabled.</td>
</tr>
</tbody>
</table>
Register 15: UART 9-Bit Self Address (UART9BITADDR), offset 0x0A4

The UART9BITADDR register is used to write the specific address that should be matched with the receiving byte when the 9-bit Address Mask (UART9BITAMASK) is set to 0xFF. This register is used in conjunction with UART9BITAMASK to form a match for address-byte received.

UART 9-Bit Self Address (UART9BITADDR)

<table>
<thead>
<tr>
<th>UART0 base: 0x4000.C000</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART1 base: 0x4000.D000</td>
</tr>
<tr>
<td>UART2 base: 0x4000.E000</td>
</tr>
<tr>
<td>UART3 base: 0x4000.F000</td>
</tr>
<tr>
<td>UART4 base: 0x4001.0000</td>
</tr>
<tr>
<td>UART5 base: 0x4001.1000</td>
</tr>
<tr>
<td>UART6 base: 0x4001.2000</td>
</tr>
<tr>
<td>UART7 base: 0x4001.3000</td>
</tr>
</tbody>
</table>

Offset 0x0A4
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15</td>
<td>9BITEN</td>
<td>RW</td>
<td>0</td>
<td>Enable 9-Bit Mode</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td>9-bit mode is disabled.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>9-bit mode is enabled.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>ADDR</td>
<td>RW</td>
<td>0x00</td>
<td>Self Address for 9-Bit Mode</td>
</tr>
<tr>
<td>This field contains the address that should be matched when UART9BITAMASK is 0xFF.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 16: UART 9-Bit Self Address Mask (UART9BITAMASK), offset 0x0A8

The UART9BITAMASK register is used to enable the address mask for 9-bit mode. The address bits are masked to create a set of addresses to be matched with the received address byte.

UART 9-Bit Self Address Mask (UART9BITAMASK)

<table>
<thead>
<tr>
<th>UART base</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART0</td>
<td>0x4000.C000</td>
</tr>
<tr>
<td>UART1</td>
<td>0x4000.D000</td>
</tr>
<tr>
<td>UART2</td>
<td>0x4000.E000</td>
</tr>
<tr>
<td>UART3</td>
<td>0x4000.F000</td>
</tr>
<tr>
<td>UART4</td>
<td>0x4001.0000</td>
</tr>
<tr>
<td>UART5</td>
<td>0x4001.1000</td>
</tr>
<tr>
<td>UART6</td>
<td>0x4001.2000</td>
</tr>
<tr>
<td>UART7</td>
<td>0x4001.3000</td>
</tr>
</tbody>
</table>

| Offset | 0x0A8 |

<table>
<thead>
<tr>
<th>Type</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>0x0000.00FF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 7:0       | MASK      | RW   | 0xFF  | Self Address Mask for 9-Bit Mode
This field contains the address mask that creates a set of addresses that should be matched. |
Register 17: UART Peripheral Properties (UARTPP), offset 0xFC0

The UARTPP register provides information regarding the properties of the UART module.

### UART Peripheral Properties (UARTPP)

<table>
<thead>
<tr>
<th>UART0 base: 0x4000.C000</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART1 base: 0x4000.D000</td>
</tr>
<tr>
<td>UART2 base: 0x4000.E000</td>
</tr>
<tr>
<td>UART3 base: 0x4000.F000</td>
</tr>
<tr>
<td>UART4 base: 0x4001.0000</td>
</tr>
<tr>
<td>UART5 base: 0x4001.1000</td>
</tr>
<tr>
<td>UART6 base: 0x4001.2000</td>
</tr>
<tr>
<td>UART7 base: 0x4001.3000</td>
</tr>
</tbody>
</table>

Offset 0xFC0

| Type RO, reset 0x0000.0003 |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>NB</td>
<td>RO</td>
<td>0x1</td>
<td>9-Bit Support</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The UART module does not provide support for the transmission of 9-bit data for RS-485 support.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The UART module provides support for the transmission of 9-bit data for RS-485 support.</td>
</tr>
<tr>
<td>0</td>
<td>SC</td>
<td>RO</td>
<td>0x1</td>
<td>Smart Card Support</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The UART module does not provide smart card support.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The UART module provides smart card support.</td>
</tr>
</tbody>
</table>
Register 18: UART Clock Configuration (UARTCC), offset 0xFC8

The UARTCC register controls the baud clock source for the UART module. For more information, see the section called “Communication Clock Sources” on page 222.

**Note:** If the PIOSC is used for the UART baud clock, the system clock frequency must be at least 9 MHz in Run mode.

UART Clock Configuration (UARTCC)

<table>
<thead>
<tr>
<th>UART0 base: 0x4000.C000</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART1 base: 0x4000.D000</td>
</tr>
<tr>
<td>UART2 base: 0x4000.E000</td>
</tr>
<tr>
<td>UART3 base: 0x4000.F000</td>
</tr>
<tr>
<td>UART4 base: 0x4001.0000</td>
</tr>
<tr>
<td>UART5 base: 0x4001.1000</td>
</tr>
<tr>
<td>UART6 base: 0x4001.2000</td>
</tr>
<tr>
<td>UART7 base: 0x4001.3000</td>
</tr>
<tr>
<td>Offset 0xFC8</td>
</tr>
<tr>
<td>Type RW, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

**Description**

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

**Description**

UART Baud Clock Source

The following table specifies the source that generates for the UART baud clock:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>System clock (based on clock source and divisor factor)</td>
</tr>
<tr>
<td>0x1-0x4</td>
<td>reserved</td>
</tr>
<tr>
<td>0x5</td>
<td>PIOSC</td>
</tr>
<tr>
<td>0x5-0xF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3:0</td>
<td>CS</td>
<td>RW</td>
<td>0</td>
<td>UART Baud Clock Source</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>The following table specifies the source that generates for the UART baud clock:</td>
</tr>
<tr>
<td>Value</td>
</tr>
<tr>
<td>-------</td>
</tr>
<tr>
<td>0x0</td>
</tr>
<tr>
<td>0x1-0x4</td>
</tr>
<tr>
<td>0x5</td>
</tr>
<tr>
<td>0x5-0xF</td>
</tr>
</tbody>
</table>
Register 19: UART Peripheral Identification 4 (UARTPeriphID4), offset 0xFD0

The UARTPeriphIDn registers are hard-coded and the fields within the registers determine the reset values.

UART Peripheral Identification 4 (UARTPeriphID4)

UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0xFD0
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID4</td>
<td>RO</td>
<td>0x00</td>
<td>UART Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 20: UART Peripheral Identification 5 (UARTPeriphID5), offset 0xFD4

The UARTPeriphIDn registers are hard-coded and the fields within the registers determine the reset values.

**UART Peripheral Identification 5 (UARTPeriphID5)**

UART0 base: 0x4000.C000  
UART1 base: 0x4000.D000  
UART2 base: 0x4000.E000  
UART3 base: 0x4000.F000  
UART4 base: 0x4001.0000  
UART5 base: 0x4001.1000  
UART6 base: 0x4001.2000  
UART7 base: 0x4001.3000  
Offset 0xFD4  
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID5</td>
<td>RO</td>
<td>0x00</td>
<td>UART Peripheral ID Register [15:8] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 21: UART Peripheral Identification 6 (UARTPeriphID6), offset 0xFD8

The UARTPeriphIDn registers are hard-coded and the fields within the registers determine the reset values.

UART Peripheral Identification 6 (UARTPeriphID6)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID6</td>
<td>RO</td>
<td>0x00</td>
<td>UART Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 22: UART Peripheral Identification 7 (UARTPeriphID7), offset 0xFDC

The UARTPeriphIDn registers are hard-coded and the fields within the registers determine the reset values.

UART Peripheral Identification 7 (UARTPeriphID7)

| UART0 base: 0x4000.C000 |
| UART1 base: 0x4000.D000 |
| UART2 base: 0x4000.E000 |
| UART3 base: 0x4000.F000 |
| UART4 base: 0x4001.0000 |
| UART5 base: 0x4001.1000 |
| UART6 base: 0x4001.2000 |
| UART7 base: 0x4001.3000 |
| Offset 0xFDC |

Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID7</td>
<td>RO</td>
<td>0x00</td>
<td>UART Peripheral ID Register [31:24] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 23: UART Peripheral Identification 0 (UARTPeriphID0), offset 0xFE0

The UARTPeriphIDn registers are hard-coded and the fields within the registers determine the reset values.

UART Peripheral Identification 0 (UARTPeriphID0)
UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0xFE0
Type RO, reset 0x0000.0060

```
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>000000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID0</td>
<td>RO</td>
<td>0x60</td>
<td>UART Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
```
Register 24: UART Peripheral Identification 1 (UARTPeriphID1), offset 0xFE4

The UARTPeriphIDn registers are hard-coded and the fields within the registers determine the reset values.

UART Peripheral Identification 1 (UARTPeriphID1)
UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0xFE4
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID1</td>
<td>RO</td>
<td>0x00</td>
<td>UART Peripheral ID Register [15:8] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 25: UART Peripheral Identification 2 (UARTPeriphID2), offset 0xFE8

The UARTPeriphIDn registers are hard-coded and the fields within the registers determine the reset values.

UART Peripheral Identification 2 (UARTPeriphID2)

UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0xFE8
Type RO, reset 0x0000.0018

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID2</td>
<td>RO</td>
<td>0x18</td>
<td>UART Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 26: UART Peripheral Identification 3 (UARTPeriphID3), offset 0xFEC

The UARTPeriphIDn registers are hard-coded and the fields within the registers determine the reset values.

UART Peripheral Identification 3 (UARTPeriphID3)

| UART0 base: 0x4000.C000 |
| UART1 base: 0x4000.D000 |
| UART2 base: 0x4000.E000 |
| UART3 base: 0x4000.F000 |
| UART4 base: 0x4001.0000 |
| UART5 base: 0x4001.1000 |
| UART6 base: 0x4001.2000 |
| UART7 base: 0x4001.3000 |

Offset 0xFEC
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID3</td>
<td>RO</td>
<td>0x01</td>
<td>UART Peripheral ID Register [31:24] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 27: UART PrimeCell Identification 0 (UARTPCellID0), offset 0xFF0

The UARTPCellIDn registers are hard-coded and the fields within the registers determine the reset values.

UART PrimeCell Identification 0 (UARTPCellID0)

UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0xFF0
Type RO, reset 0x0000.000D

Bit/Field   Name       Type    Reset   Description
           31:8       reserved   RO    0x0000.00 Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
           7:0        CID0      RO    0x0D    UART PrimeCell ID Register [7:0]

Provides software a standard cross-peripheral identification system.
Register 28: UART PrimeCell Identification 1 (UARTPCellID1), offset 0xFF4

The UARTPCellIDn registers are hard-coded and the fields within the registers determine the reset values.

UART PrimeCell Identification 1 (UARTPCellID1)
UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0xFF4
Type RO, reset 0x0000.00F0

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID1</td>
<td>RO</td>
<td>0xF0</td>
<td>UART PrimeCell ID Register [15:8]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 29: UART PrimeCell Identification 2 (UARTPCellID2), offset 0xFF8

The UARTPCellIDn registers are hard-coded and the fields within the registers determine the reset values.

UART PrimeCell Identification 2 (UARTPCellID2)

| UART0 base: 0x4000.C000 |
| UART1 base: 0x4000.D000 |
| UART2 base: 0x4000.E000 |
| UART3 base: 0x4000.F000 |
| UART4 base: 0x4001.0000 |
| UART5 base: 0x4001.1000 |
| UART6 base: 0x4001.2000 |
| UART7 base: 0x4001.3000 |

Offset 0xFF8
Type RO, reset 0x0000.0005

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID2</td>
<td>RO</td>
<td>0x05</td>
<td>UART PrimeCell ID Register [23:16] Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 30: UART PrimeCell Identification 3 (UARTPCellID3), offset 0xFFC

The UARTPCellIDn registers are hard-coded and the fields within the registers determine the reset values.

UART PrimeCell Identification 3 (UARTPCellID3)
UART0 base: 0x4000.C000
UART1 base: 0x4000.D000
UART2 base: 0x4000.E000
UART3 base: 0x4000.F000
UART4 base: 0x4001.0000
UART5 base: 0x4001.1000
UART6 base: 0x4001.2000
UART7 base: 0x4001.3000
Offset 0xFFC
Type RO, reset 0x0000.00B1

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID3</td>
<td>RO</td>
<td>0xB1</td>
<td>UART PrimeCell ID Register [31:24]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
15 Synchronous Serial Interface (SSI)

The TM4C123GH6PZ microcontroller includes four Synchronous Serial Interface (SSI) modules. Each SSI module is a master or slave interface for synchronous serial communication with peripheral devices that have either Freescale SPI, MICROWIRE, or Texas Instruments synchronous serial interfaces.

The TM4C123GH6PZ SSI modules have the following features:

- Programmable interface operation for Freescale SPI, MICROWIRE, or Texas Instruments synchronous serial interfaces
- Master or slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive FIFOs, each 16 bits wide and 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Internal loopback test mode for diagnostic/debug testing
- Standard FIFO-based interrupts and End-of-Transmission interrupt
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive
  - Receive single request asserted when data is in the FIFO; burst request asserted when FIFO contains 4 entries
  - Transmit single request asserted when there is space in the FIFO; burst request asserted when four or more entries are available to be written in the FIFO
15.1 Block Diagram

Figure 15-1. SSI Module Block Diagram

15.2 Signal Description

The following table lists the external signals of the SSI module and describes the function of each. Most SSI signals are alternate functions for some GPIO signals and default to be GPIO signals at
reset. The exceptions to this rule are the SSI0Clk, SSI0Fss, SSI0Rx, and SSI0Tx pins, which default to the SSI function. The "Pin Mux/Pin Assignment" column in the following table lists the possible GPIO pin placements for the SSI signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the SSI function. The number in parentheses is the encoding that must be programmed into the PMCn field in the GPIO Port Control (GPIOPCTL) register (page 702) to assign the SSI signal to the specified GPIO port pin. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 659.

![Table 15-1. SSI Signals (100LQFP)]

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSI0Clk</td>
<td>28</td>
<td>PA2 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 0 clock</td>
</tr>
<tr>
<td>SSI0Fss</td>
<td>29</td>
<td>PA3 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 0 frame signal</td>
</tr>
<tr>
<td>SSI0Rx</td>
<td>30</td>
<td>PA4 (2)</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 0 receive</td>
</tr>
<tr>
<td>SSI0Tx</td>
<td>31</td>
<td>PA5 (2)</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 0 transmit</td>
</tr>
<tr>
<td>SSI1Clk</td>
<td>1</td>
<td>PD0 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 clock</td>
</tr>
<tr>
<td>SSI1Fss</td>
<td>2</td>
<td>PD1 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 frame signal</td>
</tr>
<tr>
<td>SSI1Rx</td>
<td>3</td>
<td>PD2 (2)</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 1 receive</td>
</tr>
<tr>
<td>SSI1Tx</td>
<td>4</td>
<td>PD3 (2)</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 1 transmit</td>
</tr>
<tr>
<td>SSI2Clk</td>
<td>79</td>
<td>PH4 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 clock</td>
</tr>
<tr>
<td>SSI2Fss</td>
<td>78</td>
<td>PH5 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 frame signal</td>
</tr>
<tr>
<td>SSI2Rx</td>
<td>77</td>
<td>PH6 (2)</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 2 receive</td>
</tr>
<tr>
<td>SSI2Tx</td>
<td>76</td>
<td>PH7 (2)</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 2 transmit</td>
</tr>
<tr>
<td>SSI3Clk</td>
<td>1</td>
<td>PD0 (1)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 clock</td>
</tr>
<tr>
<td>SSI3Fss</td>
<td>2</td>
<td>PD1 (1)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 frame signal</td>
</tr>
<tr>
<td>SSI3Rx</td>
<td>3</td>
<td>PD2 (1)</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 3 receive</td>
</tr>
<tr>
<td>SSI3Tx</td>
<td>4</td>
<td>PD3 (1)</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 3 transmit</td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

15.3 Functional Description

The SSI performs serial-to-parallel conversion on data received from a peripheral device. The CPU accesses data, control, and status information. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes. The SSI also supports the µDMA interface. The transmit and receive FIFOs can be programmed as destination/source addresses in the µDMA module. µDMA operation is enabled by setting the appropriate bit(s) in the SSIDMACTL register (see page 1004).

June 12, 2014

Texas Instruments-Production Data
### 15.3.1 Bit Rate Generation

The SSI includes a programmable bit rate clock divider and prescaler to generate the serial output clock. Bit rates are supported to 2 MHz and higher, although maximum bit rate is determined by peripheral devices.

The serial bit rate is derived by dividing down the input clock (SysClk). The clock is first divided by an even prescale value \( CPSDVSR \) from 2 to 254, which is programmed in the **SSI Clock Prescale (SSICPSR)** register (see page 997). The clock is further divided by a value from 1 to 256, which is \( 1 + SCR \), where \( SCR \) is the value programmed in the **SSI Control 0 (SSICR0)** register (see page 990).

The frequency of the output clock **SSInClk** is defined by:

\[
SSInClk = \frac{SysClk}{(CPSDVSR \times (1 + SCR))}
\]

**Note:** The System Clock or the PIOUSC can be used as the source for the **SSInClk**. When the **CS** field in the **SSI Clock Configuration (SSICC)** register is configured to 0x5, PIOUSC is selected as the source. For master mode, the system clock or the PIOUSC must be at least two times faster than the **SSInClk**, with the restriction that **SSInClk** cannot be faster than 25 MHz. For slave mode, the system clock or the PIOUSC must be at least 12 times faster than the **SSInClk**, with the restriction that **SSInClk** cannot be faster than 6.67 MHz.

See “Synchronous Serial Interface (SSI)” on page 1430 to view SSI timing parameters.

### 15.3.2 FIFO Operation

#### 15.3.2.1 Transmit FIFO

The common transmit FIFO is a 16-bit wide, 8-locations deep, first-in, first-out memory buffer. The CPU writes data to the FIFO by writing the **SSI Data (SSIDR)** register (see page 994), and data is stored in the FIFO until it is read out by the transmission logic.

When configured as a master or a slave, parallel data is written into the transmit FIFO prior to serial conversion and transmission to the attached slave or master, respectively, through the **SSInTx** pin.

In slave mode, the SSI transmits data each time the master initiates a transaction. If the transmit FIFO is empty and the master initiates, the slave transmits the 8th most recent value in the transmit FIFO. If less than 8 values have been written to the transmit FIFO since the SSI module clock was enabled using the **Rn** bit in the **RCGCSSI** register, then 0 is transmitted. Care should be taken to ensure that valid data is in the FIFO as needed. The SSI can be configured to generate an interrupt or a µDMA request when the FIFO is empty.

#### 15.3.2.2 Receive FIFO

The common receive FIFO is a 16-bit wide, 8-locations deep, first-in, first-out memory buffer. Received data from the serial interface is stored in the buffer until read out by the CPU, which accesses the read FIFO by reading the **SSIDR** register.

When configured as a master or slave, serial data received through the **SSInRx** pin is registered prior to parallel loading into the attached slave or master receive FIFO, respectively.

### 15.3.3 Interrupts

The SSI can generate interrupts when the following conditions are observed:

- Transmit FIFO service (when the transmit FIFO is half full or less)
- Receive FIFO service (when the receive FIFO is half full or more)
Receive FIFO time-out
Receive FIFO overrun
End of transmission
Receive DMA transfer complete
Transmit DMA transfer complete

All of the interrupt events are ORed together before being sent to the interrupt controller, so the SSI generates a single interrupt request to the controller regardless of the number of active interrupts. Each of the four individual maskable interrupts can be masked by clearing the appropriate bit in the SSI Interrupt Mask (SSIIM) register (see page 998). Setting the appropriate mask bit enables the interrupt.

The individual outputs, along with a combined interrupt output, allow use of either a global interrupt service routine or modular device drivers to handle interrupts. The transmit and receive dynamic dataflow interrupts have been separated from the status interrupts so that data can be read or written in response to the FIFO trigger levels. The status of the individual interrupt sources can be read from the SSI Raw Interrupt Status (SSIRIS) and SSI Masked Interrupt Status (SSIMIS) registers (see page 999 and page 1001, respectively).

The receive FIFO has a time-out period that is 32 periods at the rate of SSInClk (whether or not SSInClk is currently active) and is started when the RX FIFO goes from EMPTY to not-EMPTY. If the RX FIFO is emptied before 32 clocks have passed, the time-out period is reset. As a result, the ISR should clear the Receive FIFO Time-out Interrupt just after reading out the RX FIFO by writing a 1 to the RTIC bit in the SSI Interrupt Clear (SSIICR) register. The interrupt should not be cleared so late that the ISR returns before the interrupt is actually cleared, or the ISR may be re-activated unnecessarily.

The End-of-Transmission (EOT) interrupt indicates that the data has been transmitted completely and is only valid for Master mode devices/operations. This interrupt can be used to indicate when it is safe to turn off the SSI module clock or enter sleep mode. In addition, because transmitted data and received data complete at exactly the same time, the interrupt can also indicate that read data is ready immediately, without waiting for the receive FIFO time-out period to complete.

Note: In Freescale SPI mode only, a condition can be created where an EOT interrupt is generated for every byte transferred even if the FIFO is full. If the EOT bit has been set to 0 in an integrated slave SSI and the μDMA has been configured to transfer data from this SSI to a Master SSI on the device using external loopback, an EOT interrupt is generated by the SSI slave for every byte even if the FIFO is full.

15.3.4 Frame Formats

Each data frame is between 4 and 16 bits long depending on the size of data programmed and is transmitted starting with the MSB. There are three basic frame types that can be selected by programming the FRF bit in the SSICR0 register:

- Texas Instruments synchronous serial
- Freescale SPI
- MICROWIRE
For all three formats, the serial clock (SSInClk) is held inactive while the SSI is idle, and SSInClk transitions at the programmed frequency only during active transmission or reception of data. The idle state of SSInClk is utilized to provide a receive timeout indication that occurs when the receive FIFO still contains data after a timeout period.

For Freescale SPI and MICROWIRE frame formats, the serial frame (SSInFss) pin is active Low, and is asserted (pulled down) during the entire transmission of the frame.

For Texas Instruments synchronous serial frame format, the SSInFss pin is pulsed for one serial clock period starting at its rising edge, prior to the transmission of each frame. For this frame format, both the SSI and the off-chip slave device drive their output data on the rising edge of SSInClk and latch data from the other device on the falling edge.

Unlike the full-duplex transmission of the other two frame formats, the MICROWIRE format uses a special master-slave messaging technique which operates at half-duplex. In this mode, when a frame begins, an 8-bit control message is transmitted to the off-chip slave. During this transmit, no incoming data is received by the SSI. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the requested data. The returned data can be 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

15.3.4.1 Texas Instruments Synchronous Serial Frame Format

Figure 15-2 on page 978 shows the Texas Instruments synchronous serial frame format for a single transmitted frame.

Figure 15-2. TI Synchronous Serial Frame Format (Single Transfer)

In this mode, SSInClk and SSInFss are forced Low, and the transmit data line SSInTx is tristated whenever the SSI is idle. Once the bottom entry of the transmit FIFO contains data, SSInFss is pulsed High for one SSInClk period. The value to be transmitted is also transferred from the transmit FIFO to the serial shift register of the transmit logic. On the next rising edge of SSInClk, the MSB of the 4 to 16-bit data frame is shifted out on the SSInTx pin. Likewise, the MSB of the received data is shifted onto the SSInRx pin by the off-chip serial slave device.

Both the SSI and the off-chip serial slave device then clock each data bit into their serial shifter on each falling edge of SSInClk. The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of SSInClk after the LSB has been latched.

Figure 15-3 on page 979 shows the Texas Instruments synchronous serial frame format when back-to-back frames are transmitted.
15.3.4.2 Freescale SPI Frame Format

The Freescale SPI interface is a four-wire interface where the SSInFss signal behaves as a slave select. The main feature of the Freescale SPI format is that the inactive state and phase of the SSInClk signal are programmable through the SPO and SPH bits in the SSICR0 control register.

**SPO Clock Polarity Bit**

When the SPO clock polarity control bit is clear, it produces a steady state Low value on the SSInClk pin. If the SPO bit is set, a steady state High value is placed on the SSInClk pin when data is not being transferred.

**SPH Phase Control Bit**

The SPH phase control bit selects the clock edge that captures data and allows it to change state. The state of this bit has the most impact on the first bit transmitted by either allowing or not allowing a clock transition before the first data capture edge. When the SPH phase control bit is clear, data is captured on the first clock edge transition. If the SPH bit is set, data is captured on the second clock edge transition.

15.3.4.3 Freescale SPI Frame Format with SPO=0 and SPH=0

Single and continuous transmission signal sequences for Freescale SPI format with SPO=0 and SPH=0 are shown in Figure 15-4 on page 980 and Figure 15-5 on page 980.
In this configuration, during idle periods:

- **SSInClk** is forced Low
- **SSInFss** is forced High
- The transmit data line **SSInTx** is tristated
- When the SSI is configured as a master, it enables the **SSInClk** pad
- When the SSI is configured as a slave, it disables the **SSInClk** pad

If the SSI is enabled and valid data is in the transmit FIFO, the start of transmission is signified by the **SSInFss** master signal being driven Low, causing slave data to be enabled onto the **SSInRx** input line of the master. The master **SSInTx** output pad is enabled.

One half **SSInClk** period later, valid master data is transferred to the **SSInTx** pin. Once both the master and slave data have been set, the **SSInClk** master clock pin goes High after one additional half **SSInClk** period.

The data is now captured on the rising and propagated on the falling edges of the **SSInClk** signal.
In the case of a single word transmission, after all bits of the data word have been transferred, the SSInFss line is returned to its idle High state one SSInClk period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSInFss signal must be pulsed High between each data word transfer because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the SPH bit is clear. Therefore, the master device must raise the SSInFss pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSInFss pin is returned to its idle state one SSInClk period after the last bit has been captured.

15.3.4.4 Freescale SPI Frame Format with SPO=0 and SPH=1

The transfer signal sequence for Freescale SPI format with SPO=0 and SPH=1 is shown in Figure 15-6 on page 981, which covers both single and continuous transfers.

**Figure 15-6. Freescale SPI Frame Format with SPO=0 and SPH=1**

In this configuration, during idle periods:

- SSInClk is forced Low
- SSInFss is forced High
- The transmit data line SSInTx is tristated
- When the SSI is configured as a master, it enables the SSInClk pad
- When the SSI is configured as a slave, it disables the SSInClk pad

If the SSI is enabled and valid data is in the transmit FIFO, the start of transmission is signified by the SSInFss master signal being driven Low. The master SSInTx output is enabled. After an additional one-half SSInClk period, both master and slave valid data are enabled onto their respective transmission lines. At the same time, the SSInClk is enabled with a rising edge transition.

Data is then captured on the falling edges and propagated on the rising edges of the SSInClk signal.

In the case of a single word transfer, after all bits have been transferred, the SSInFss line is returned to its idle High state one SSInClk period after the last bit has been captured.
For continuous back-to-back transfers, the SSInFss pin is held Low between successive data words, and termination is the same as that of the single word transfer.

15.3.4.5 Freescale SPI Frame Format with SPO=1 and SPH=0

Single and continuous transmission signal sequences for Freescale SPI format with SPO=1 and SPH=0 are shown in Figure 15-7 on page 982 and Figure 15-8 on page 982.

Figure 15-7. Freescale SPI Frame Format (Single Transfer) with SPO=1 and SPH=0

![Freescale SPI Frame Format (Single Transfer) with SPO=1 and SPH=0](image)

Note: Q is undefined.

Figure 15-8. Freescale SPI Frame Format (Continuous Transfer) with SPO=1 and SPH=0

![Freescale SPI Frame Format (Continuous Transfer) with SPO=1 and SPH=0](image)

In this configuration, during idle periods:

- SSInClk is forced High
- SSInFss is forced High
- The transmit data line SSInTx is tristated
- When the SSI is configured as a master, it enables the SSInClk pad
- When the SSI is configured as a slave, it disables the SSInClk pad

If the SSI is enabled and valid data is in the transmit FIFO, the start of transmission is signified by the SSInFss master signal being driven Low, causing slave data to be immediately transferred onto the SSInRx line of the master. The master SSInTx output pad is enabled. One-half period later, valid master data is transferred to the SSInTx line. Once both the master and slave data have been set, the SSInClk master clock pin becomes Low after one additional half
SSInClk period, meaning that data is captured on the falling edges and propagated on the rising edges of the SSInClk signal.

In the case of a single word transmission, after all bits of the data word are transferred, the SSInFss line is returned to its idle High state one SSInClk period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSInFss signal must be pulsed High between each data word transfer because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the SPH bit is clear. Therefore, the master device must raise the SSInFss pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSInFss pin is returned to its idle state one SSInClk period after the last bit has been captured.

15.3.4.6 Freescale SPI Frame Format with SPO=1 and SPH=1

The transfer signal sequence for Freescale SPI format with SPO=1 and SPH=1 is shown in Figure 15-9 on page 983, which covers both single and continuous transfers.

Figure 15-9. Freescale SPI Frame Format with SPO=1 and SPH=1

---

**Note:** Q is undefined.

In this configuration, during idle periods:

- SSInClk is forced High
- SSInFss is forced High
- The transmit data line SSInTx is tristated
- When the SSI is configured as a master, it enables the SSInClk pad
- When the SSI is configured as a slave, it disables the SSInClk pad

If the SSI is enabled and valid data is in the transmit FIFO, the start of transmission is signified by the SSInFss master signal being driven Low. The master SSInTx output pad is enabled. After an additional one-half SSInClk period, both master and slave data are enabled onto their respective transmission lines. At the same time, SSInClk is enabled with a falling edge transition. Data is then captured on the rising edges and propagated on the falling edges of the SSInClk signal.

After all bits have been transferred, in the case of a single word transmission, the SSInFss line is returned to its idle high state one SSInClk period after the last bit has been captured.
For continuous back-to-back transmissions, the SSInFss pin remains in its active Low state until the final bit of the last word has been captured and then returns to its idle state as described above.

For continuous back-to-back transfers, the SSInFss pin is held Low between successive data words and termination is the same as that of the single word transfer.

15.3.4.7 MICROWIRE Frame Format

Figure 15-10 on page 984 shows the MICROWIRE frame format for a single frame. Figure 15-11 on page 985 shows the same format when back-to-back frames are transmitted.

Figure 15-10. MICROWIRE Frame Format (Single Frame)

MICROWIRE format is very similar to SPI format, except that transmission is half-duplex instead of full-duplex and uses a master-slave message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the SSI to the off-chip slave device. During this transmission, no incoming data is received by the SSI. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the required data. The returned data is 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

In this configuration, during idle periods:

- SSInClk is forced Low
- SSInFss is forced High
- The transmit data line SSInTx is tristated

A transmission is triggered by writing a control byte to the transmit FIFO. The falling edge of SSInFss causes the value contained in the bottom entry of the transmit FIFO to be transferred to the serial shift register of the transmit logic and the MSB of the 8-bit control frame to be shifted out onto the SSInTx pin. SSInFss remains Low for the duration of the frame transmission. The SSInRx pin remains tristated during this transmission.

The off-chip serial slave device latches each control bit into its serial shifter on each rising edge of SSInClk. After the last bit is latched by the slave device, the control byte is decoded during a one clock wait-state, and the slave responds by transmitting data back to the SSI. Each bit is driven onto the SSInRx line on the falling edge of SSInClk. The SSI in turn latches each bit on the rising edge of SSInClk. At the end of the frame, for single transfers, the SSInFss signal is pulled High one clock period after the last bit has been latched in the receive serial shifter, causing the data to be transferred to the receive FIFO.
Note: The off-chip slave device can tristate the receive line either on the falling edge of SSInClk after the LSB has been latched by the receive shifter or when the SSInFss pin goes High.

For continuous transfers, data transmission begins and ends in the same manner as a single transfer. However, the SSInFss line is continuously asserted (held Low) and transmission of data occurs back-to-back. The control byte of the next frame follows directly after the LSB of the received data from the current frame. Each of the received values is transferred from the receive shifter on the falling edge of SSInClk, after the LSB of the frame has been latched into the SSI.

Figure 15-11. MICROWIRE Frame Format (Continuous Transfer)

In the MICROWIRE mode, the SSI slave samples the first bit of receive data on the rising edge of SSInClk after SSInFss has gone Low. Masters that drive a free-running SSInClk must ensure that the SSInFss signal has sufficient setup and hold margins with respect to the rising edge of SSInClk.

Figure 15-12 on page 985 illustrates these setup and hold time requirements. With respect to the SSInClk rising edge on which the first bit of receive data is to be sampled by the SSI slave, SSInFss must have a setup of at least two times the period of SSInClk on which the SSI operates. With respect to the SSInClk rising edge previous to this edge, SSInFss must have a hold of at least one SSInClk period.

Figure 15-12. MICROWIRE Frame Format, SSInFss Input Setup and Hold Requirements

15.3.5 DMA Operation

The SSI peripheral provides an interface to the μDMA controller with separate channels for transmit and receive. The μDMA operation of the SSI is enabled through the SSI DMA Control (SSIDMACCTL) register. When μDMA operation is enabled, the SSI asserts a μDMA request on the receive or transmit channel when the associated FIFO can transfer data.
For the receive channel, a single transfer request is asserted whenever any data is in the receive FIFO. A burst transfer request is asserted whenever the amount of data in the receive FIFO is 4 or more items. For the transmit channel, a single transfer request is asserted whenever at least one empty location is in the transmit FIFO. The burst request is asserted whenever the transmit FIFO has 4 or more empty slots. The single and burst µDMA transfer requests are handled automatically by the µDMA controller depending how the µDMA channel is configured.

To enable µDMA operation for the receive channel, the RXDMAE bit of the DMA Control (SSIDMACTL) register should be set after configuring the µDMA. To enable µDMA operation for the transmit channel, the TXDMAE bit of SSIDMACTL should be set after configuring the µDMA. If µDMA is enabled, then the µDMA controller triggers an interrupt when a transfer is complete. The interrupt occurs on the SSI interrupt vector. Therefore, if interrupts are used for SSI operation and µDMA is enabled, the SSI interrupt handler must be designed to handle the µDMA completion interrupt.

When transfers are performed from a FIFO of the SSI using the µDMA, and any interrupt is generated from the SSI, the SSI module’s status bit in the DMA Channel Interrupt Status (DMACHIS) register must be checked at the end of the interrupt service routine. If the status bit is set, clear the interrupt by writing a 1 to it.

See “Micro Direct Memory Access (µDMA)” on page 595 for more details about programming the µDMA controller.

15.4 Initialization and Configuration

To enable and initialize the SSI, the following steps are necessary:

1. Enable the SSI module using the RCGCSSI register (see page 349).

2. Enable the clock to the appropriate GPIO module via the RCGCGPIO register (see page 342). To find out which GPIO port to enable, refer to Table 23-5 on page 1386.

3. Set the GPIO AFSEL bits for the appropriate pins (see page 684). To determine which GPIOs to configure, see Table 23-4 on page 1377.

4. Configure the PMCn fields in the GPIOPCTL register to assign the SSI signals to the appropriate pins. See page 702 and Table 23-5 on page 1386.

5. Program the GPIODEN register to enable the pin's digital function. In addition, the drive strength, drain select and pull-up/pull-down functions must be configured. Refer to “General-Purpose Input/Outputs (GPIOs)” on page 659 for more information.

   Note: Pull-ups can be used to avoid unnecessary toggles on the SSI pins, which can take the slave to a wrong state. In addition, if the SSIClk signal is programmed to steady state High through the SPO bit in the SSICR0 register, then software must also configure the GPIO port pin corresponding to the SSInClk signal as a pull-up in the GPIO Pull-Up Select (GPIOPUR) register.

For each of the frame formats, the SSI is configured using the following steps:

1. Ensure that the SSE bit in the SSICR1 register is clear before making any configuration changes.

2. Select whether the SSI is a master or slave:

   a. For master operations, set the SSICR1 register to 0x0000.0000.
b. For slave mode (output enabled), set the SSICR1 register to 0x0000.0004.

c. For slave mode (output disabled), set the SSICR1 register to 0x0000.000C.

3. Configure the SSI clock source by writing to the SSI CC register.

4. Configure the clock prescale divisor by writing the SSICPSR register.

5. Write the SSICR0 register with the following configuration:
   - Serial clock rate (SCR)
   - Desired clock phase/polarity, if using Freescale SPI mode (SPH and SPO)
   - The protocol mode: Freescale SPI, TI SSF, MICROWIRE (FRF)
   - The data size (DSS)

6. Optionally, configure the SSI module for μDMA use with the following steps:
   a. Configure a μDMA for SSI use. See "Micro Direct Memory Access (μDMA)" on page 595 for more information.
   b. Enable the SSI Module’s TX FIFO or RX FIFO by setting the TXDMAE or RXDMAE bit in the SSSIDMACTL register.

7. Enable the SSI by setting the SSE bit in the SSICR1 register.

As an example, assume the SSI must be configured to operate with the following parameters:

- Master operation
- Freescale SPI mode (SPO=1, SPH=1)
- 1 Mbps bit rate
- 8 data bits

Assuming the system clock is 20 MHz, the bit rate calculation would be:

\[
\text{SSIncClk} = \frac{\text{SysClk}}{(\text{CPSDVSR} \times (1 + \text{SCR}))}
\]

\[
1 \times 10^6 = \frac{20 \times 10^6}{(\text{CPSDVSR} \times (1 + \text{SCR}))}
\]

In this case, if CPSDVSR=0x2, SCR must be 0x9.

The configuration sequence would be as follows:

1. Ensure that the SSE bit in the SSICR1 register is clear.

2. Write the SSICR1 register with a value of 0x0000.0000.

3. Write the SSICPSR register with a value of 0x0000.0002.

4. Write the SSICR0 register with a value of 0x0000.09C7.

5. The SSI is then enabled by setting the SSE bit in the SSICR1 register.
15.5 Register Map

Table 15-2 on page 988 lists the SSI registers. The offset listed is a hexadecimal increment to the register’s address, relative to that SSI module’s base address:

- SSI0: 0x4000.8000
- SSI1: 0x4000.9000
- SSI2: 0x4000.A000
- SSI3: 0x4000.B000

Note that the SSI module clock must be enabled before the registers can be programmed (see page 349). The \( Rn \) bit of the PRSSI register must be read as 0x1 before any SSI module registers are accessed.

Note: The SSI must be disabled (see the \( SSE \) bit in the SSICR1 register) before any of the control registers are reprogrammed.

### Table 15-2. SSI Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>SSICR0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>SSI Control 0</td>
<td>990</td>
</tr>
<tr>
<td>0x004</td>
<td>SSICR1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>SSI Control 1</td>
<td>992</td>
</tr>
<tr>
<td>0x008</td>
<td>SSIDR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>SSI Data</td>
<td>994</td>
</tr>
<tr>
<td>0x00C</td>
<td>SSISR</td>
<td>RO</td>
<td>0x0000.0003</td>
<td>SSI Status</td>
<td>995</td>
</tr>
<tr>
<td>0x010</td>
<td>SSICPSR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>SSI Clock Prescale</td>
<td>997</td>
</tr>
<tr>
<td>0x014</td>
<td>SSIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>SSI Interrupt Mask</td>
<td>998</td>
</tr>
<tr>
<td>0x018</td>
<td>SSIRIS</td>
<td>RO</td>
<td>0x0000.0008</td>
<td>SSI Raw Interrupt Status</td>
<td>999</td>
</tr>
<tr>
<td>0x01C</td>
<td>SSIMIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>SSI Masked Interrupt Status</td>
<td>1001</td>
</tr>
<tr>
<td>0x020</td>
<td>SSICR</td>
<td>W1C</td>
<td>0x0000.0000</td>
<td>SSI Interrupt Clear</td>
<td>1003</td>
</tr>
<tr>
<td>0x024</td>
<td>SSIDMACTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>SSI DMA Control</td>
<td>1004</td>
</tr>
<tr>
<td>0x0C8</td>
<td>SSICC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>SSI Clock Configuration</td>
<td>1005</td>
</tr>
<tr>
<td>0xFD0</td>
<td>SSIPeripheralID4</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>SSI Peripheral Identification 4</td>
<td>1006</td>
</tr>
<tr>
<td>0xFD4</td>
<td>SSIPeripheralID5</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>SSI Peripheral Identification 5</td>
<td>1007</td>
</tr>
<tr>
<td>0xFD8</td>
<td>SSIPeripheralID6</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>SSI Peripheral Identification 6</td>
<td>1008</td>
</tr>
<tr>
<td>0xFD9</td>
<td>SSIPeripheralID7</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>SSI Peripheral Identification 7</td>
<td>1009</td>
</tr>
<tr>
<td>0xFE0</td>
<td>SSIPeripheralID0</td>
<td>RO</td>
<td>0x0000.0022</td>
<td>SSI Peripheral Identification 0</td>
<td>1010</td>
</tr>
<tr>
<td>0xFE4</td>
<td>SSIPeripheralID1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>SSI Peripheral Identification 1</td>
<td>1011</td>
</tr>
<tr>
<td>0xFE8</td>
<td>SSIPeripheralID2</td>
<td>RO</td>
<td>0x0000.0018</td>
<td>SSI Peripheral Identification 2</td>
<td>1012</td>
</tr>
<tr>
<td>0xFE6</td>
<td>SSIPeripheralID3</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>SSI Peripheral Identification 3</td>
<td>1013</td>
</tr>
<tr>
<td>0xFF0</td>
<td>SSIPCellID0</td>
<td>RO</td>
<td>0x0000.000D</td>
<td>SSI PrimeCell Identification 0</td>
<td>1014</td>
</tr>
<tr>
<td>0xFF4</td>
<td>SSIPCellID1</td>
<td>RO</td>
<td>0x0000.00F0</td>
<td>SSI PrimeCell Identification 1</td>
<td>1015</td>
</tr>
</tbody>
</table>
Table 15-2. SSI Register Map *(continued)*

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFF8</td>
<td>SSIPCellID2</td>
<td>RO</td>
<td>0x0000.0005</td>
<td>SSI PrimeCell Identification 2</td>
<td>1016</td>
</tr>
<tr>
<td>0xFFC</td>
<td>SSIPCellID3</td>
<td>RO</td>
<td>0x0000.00B1</td>
<td>SSI PrimeCell Identification 3</td>
<td>1017</td>
</tr>
</tbody>
</table>

15.6 Register Descriptions

The remainder of this section lists and describes the SSI registers, in numerical order by address offset.
Register 1: SSI Control 0 (SSICR0), offset 0x000

The SSICR0 register contains bit fields that control various functions within the SSI module. Functionality such as protocol mode, clock rate, and data size are configured in this register.

SSI Control 0 (SSICR0)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>0x00000000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>This bit field is used to generate the transmit and receive bit rate of the SSI. The bit rate is: BR=SysClk/(CPSDVSR * (1 + SCR))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>where CPSDVSR is an even value from 2-254 programmed in the SSICPSR register, and SCR is a value from 0-255.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>This bit is only applicable to the Freescale SPI Format.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>The SPH control bit selects the clock edge that captures data and allows it to change state. This bit has the most impact on the first bit transmitted by either allowing or not allowing a clock transition before the first data capture edge.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Data is captured on the first clock edge transition.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Data is captured on the second clock edge transition.</td>
<td></td>
</tr>
<tr>
<td>This bit is set, then software must also configure the GPIO port pin corresponding to the SSInClk signal as a pull-up in the GPIO Pull-Up Select (GPIOPUR) register.</td>
<td></td>
<td>Note:</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>5:4</td>
<td>FRF</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3:0</td>
<td>DSS</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 2: SSI Control 1 (SSICR1), offset 0x004

The SSICR1 register contains bit fields that control various functions within the SSI module. Master and slave mode functionality is controlled by this register.

### SSI Control 1 (SSICR1)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| RW     | 0     | End of Transmission \( (MS = 0x0) \). \n\n\begin{itemize}
  \item Value Description
  \begin{itemize}
    \item 0: The TXRIS interrupt indicates that the transmit FIFO is half full or less.
    \item 1: The End of Transmit interrupt mode for the TXRIS interrupt is enabled.
  \end{itemize}
\end{itemize} |

\textbf{Note:} In Freescale SPI mode only, a condition can be created where an EOT interrupt is generated for every byte transferred even if the FIFO is full. If the EOT bit has been set to 0 in an integrated slave SSI and the µDMA has been configured to transfer data from this SSI to a Master SSI on the device using external loopback, an EOT interrupt is generated by the SSI slave for every byte even if the FIFO is full.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 4         | EOT      | RW   | 0     | End of Transmission \( (MS = 0x0) \). \n\n\begin{itemize}
  \item Value Description
  \begin{itemize}
    \item 0: The TXRIS interrupt indicates that the transmit FIFO is half full or less.
    \item 1: The End of Transmit interrupt mode for the TXRIS interrupt is enabled.
  \end{itemize}
\end{itemize} |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 2         | MS       | RW   | 0     | SSI Master/Slave Select \( (SSE=0) \). \n\n\begin{itemize}
  \item Value Description
  \begin{itemize}
    \item 0: The SSI is configured as a master.
    \item 1: The SSI is configured as a slave.
  \end{itemize}
\end{itemize} |
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1</strong></td>
<td>SSE</td>
<td>RW</td>
<td>0</td>
<td>SSI Synchronous Serial Port Enable</td>
</tr>
</tbody>
</table>

**Value** | **Description**                  
0          | SSI operation is disabled.       
1          | SSI operation is enabled.        

**Note:** This bit must be cleared before any control registers are reprogrammed.

| **0**     | LBM  | RW   | 0     | SSI Loopback Mode                               |

**Value** | **Description**                  
0          | Normal serial port operation enabled.       
1          | Output of the transmit serial shift register is connected internally to the input of the receive serial shift register. |
Register 3: SSI Data (SSIDR), offset 0x008

**Important:** This register is read-sensitive. See the register description for details.

The **SSIDR** register is 16-bits wide. When the **SSIDR** register is read, the entry in the receive FIFO that is pointed to by the current FIFO read pointer is accessed. When a data value is removed by the SSI receive logic from the incoming data frame, it is placed into the entry in the receive FIFO pointed to by the current FIFO write pointer.

When the **SSIDR** register is written to, the entry in the transmit FIFO that is pointed to by the write pointer is written to. Data values are removed from the transmit FIFO one value at a time by the transmit logic. Each data value is loaded into the transmit serial shifter, then serially shifted out onto the **SSInTx** pin at the programmed bit rate.

When a data size of less than 16 bits is selected, the user must right-justify data written to the transmit FIFO. The transmit logic ignores the unused bits. Received data less than 16 bits is automatically right-justified in the receive buffer.

When the SSI is programmed for MICROWIRE frame format, the default size for transmit data is eight bits (the most significant byte is ignored). The receive data size is controlled by the programmer. The transmit FIFO and the receive FIFO are not cleared even when the **SSE** bit in the **SSICR1** register is cleared, allowing the software to fill the transmit FIFO before enabling the SSI.

SSI Data (SSIDR)

<table>
<thead>
<tr>
<th>SSI0 base: 0x4000.8000</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSI1 base: 0x4000.9000</td>
</tr>
<tr>
<td>SSI2 base: 0x4000.A000</td>
</tr>
<tr>
<td>SSI3 base: 0x4000.B000</td>
</tr>
<tr>
<td>Offset 0x008</td>
</tr>
<tr>
<td>Type RW, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

### SSI Data (SSIDR) Register

```
<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>DATA</td>
<td>RW</td>
<td>0x0000</td>
<td>SSI Receive/Transmit Data</td>
</tr>
</tbody>
</table>
```

A read operation reads the receive FIFO. A write operation writes the transmit FIFO.

Software must right-justify data when the SSI is programmed for a data size that is less than 16 bits. Unused bits at the top are ignored by the transmit logic. The receive logic automatically right-justifies the data.
Register 4: SSI Status (SSISR), offset 0x00C

The SSISR register contains bits that indicate the FIFO fill status and the SSI busy status.

SSI Status (SSISR)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0x00C
Type RO, reset 0x0000.0003

<table>
<thead>
<tr>
<th>Bit/Field (31:5)</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>BSY</td>
<td>RO</td>
<td>0</td>
<td>SSI Busy Bit</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The SSI is idle.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The SSI is currently transmitting and/or receiving a frame, or the transmit FIFO is not empty.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>RFF</td>
<td>RO</td>
<td>0</td>
<td>SSI Receive FIFO Full</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The receive FIFO is not full.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The receive FIFO is full.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RNE</td>
<td>RO</td>
<td>0</td>
<td>SSI Receive FIFO Not Empty</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The receive FIFO is empty.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The receive FIFO is not empty.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>TNF</td>
<td>RO</td>
<td>1</td>
<td>SSI Transmit FIFO Not Full</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The transmit FIFO is full.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The transmit FIFO is not full.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Synchronous Serial Interface (SSI)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>TFE</td>
<td>RO</td>
<td>1</td>
<td>SSI Transmit FIFO Empty</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The transmit FIFO is not empty.</td>
</tr>
<tr>
<td>1</td>
<td>The transmit FIFO is empty.</td>
</tr>
</tbody>
</table>
Register 5: SSI Clock Prescale (SSICPSR), offset 0x010

The SSICPSR register specifies the division factor which is used to derive the SSInClk from the system clock. The clock is further divided by a value from 1 to 256, which is 1 + SCR. SCR is programmed in the SSICR0 register. The frequency of the SSInClk is defined by:

SSInClk = SysClk / (CPSDVSR * (1 + SCR))

The value programmed into this register must be an even number between 2 and 254. The least-significant bit of the programmed number is hard-coded to zero. If an odd number is written to this register, data read back from this register has the least-significant bit as zero.

SSI Clock Prescale (SSICPSR)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0x010
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CPSDVSR</td>
<td>RW</td>
<td>0x00</td>
<td>SSI Clock Prescale Divisor This value must be an even number from 2 to 254, depending on the frequency of SSInClk. The LSB always returns 0 on reads.</td>
</tr>
</tbody>
</table>
Register 6: SSI Interrupt Mask (SSIIM), offset 0x014

The SSIIM register is the interrupt mask set or clear register. It is a read/write register and all bits are cleared on reset.

On a read, this register gives the current value of the mask on the corresponding interrupt. Setting a bit clears the mask, enabling the interrupt to be sent to the interrupt controller. Clearing a bit sets the corresponding mask, preventing the interrupt from being signaled to the controller.

**SSI Interrupt Mask (SSIIM)**

SSI0 base: 0x4000.8000  
SSI1 base: 0x4000.9000  
SSI2 base: 0x4000.A000  
SSI3 base: 0x4000.B000  
Offset 0x014  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>TXIM</td>
<td>RW</td>
<td>0</td>
<td>SSI Transmit FIFO Interrupt Mask</td>
</tr>
<tr>
<td>2</td>
<td>RXIM</td>
<td>RW</td>
<td>0</td>
<td>SSI Receive FIFO Interrupt Mask</td>
</tr>
<tr>
<td>1</td>
<td>RTIM</td>
<td>RW</td>
<td>0</td>
<td>SSI Receive Time-Out Interrupt Mask</td>
</tr>
<tr>
<td>0</td>
<td>RORIM</td>
<td>RW</td>
<td>0</td>
<td>SSI Receive Overrun Interrupt Mask</td>
</tr>
</tbody>
</table>
Register 7: SSI Raw Interrupt Status (SSIRIS), offset 0x018

The **SSIRIS** register is the raw interrupt status register. On a read, this register gives the current raw status value of the corresponding interrupt prior to masking. A write has no effect.

SSI Raw Interrupt Status (SSIRIS)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>0</td>
<td>No interrupt.</td>
</tr>
<tr>
<td>Value Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No interrupt.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>If the EOT bit in the SSICR1 register is clear, the transmit FIFO is half empty or less. If the EOT bit is set, the transmit FIFO is empty, and the last bit has been transmitted out of the serializer.</td>
<td></td>
</tr>
<tr>
<td>This bit is cleared when the transmit FIFO is more than half full (if the EOT bit is clear) or when it has any data in it (if the EOT bit is set).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>SSI Receive FIFO Raw Interrupt Status</td>
<td>Value Description</td>
</tr>
<tr>
<td>3</td>
<td>TXRIS</td>
<td>RO 1 SSI Transmit FIFO Raw Interrupt Status</td>
</tr>
<tr>
<td>0</td>
<td>No interrupt.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The receive FIFO is half full or more.</td>
<td></td>
</tr>
<tr>
<td>This bit is cleared when the receive FIFO is less than half full.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RTRIS</td>
<td>RO 0 SSI Receive Time-Out Raw Interrupt Status</td>
</tr>
<tr>
<td>0</td>
<td>No interrupt.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The receive time-out has occurred.</td>
<td></td>
</tr>
<tr>
<td>This bit is cleared when a 1 is written to the RTIC bit in the SSI Interrupt Clear (SSIICR) register.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Synchronous Serial Interface (SSI)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RORRIS</td>
<td>RO</td>
<td>0</td>
<td>SSI Receive Overrun Raw Interrupt Status</td>
</tr>
</tbody>
</table>

Value  Description

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt.</td>
</tr>
<tr>
<td>1</td>
<td>The receive FIFO has overflowed</td>
</tr>
</tbody>
</table>

This bit is cleared when a 1 is written to the **RORC** bit in the **SSI Interrupt Clear (SSIICR)** register.
Register 8: SSI Masked Interrupt Status (SSIMIS), offset 0x01C

The SSIMIS register is the masked interrupt status register. On a read, this register gives the current masked status value of the corresponding interrupt. A write has no effect.

SSI Masked Interrupt Status (SSIMIS)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>TXMIS</td>
<td>RO</td>
<td>0</td>
<td>SSI Transmit FIFO Masked Interrupt Status</td>
</tr>
<tr>
<td>2</td>
<td>RXMIS</td>
<td>RO</td>
<td>0</td>
<td>SSI Receive FIFO Masked Interrupt Status</td>
</tr>
<tr>
<td>1</td>
<td>RTMIS</td>
<td>RO</td>
<td>0</td>
<td>SSI Receive Time-Out Masked Interrupt Status</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

An interrupt has not occurred or is masked.

An unmasked interrupt was signaled due to the transmit FIFO being half empty or less (if the EOT bit is clear) or due to the transmission of the last data bit (if the EOT bit is set).

This bit is cleared when the transmit FIFO is more than half empty (if the EOT bit is clear) or when it has any data in it (if the EOT bit is set).

An unmasked interrupt was signaled due to the receive FIFO being half full or more.

This bit is cleared when the receive FIFO is less than half full.

An unmasked interrupt was signaled due to the receive time out.

This bit is cleared when a 1 is written to the RTIC bit in the SSI Interrupt Clear (SSIICR) register.
### Synchronous Serial Interface (SSI)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RORMIS</td>
<td>RO</td>
<td>0</td>
<td>SSI Receive Overrun Masked Interrupt Status</td>
</tr>
</tbody>
</table>

Value  Description

0  An interrupt has not occurred or is masked.

1  An unmasked interrupt was signaled due to the receive FIFO overflowing.

This bit is cleared when a 1 is written to the RORIC bit in the SSI Interrupt Clear (SSICR) register.
Register 9: SSI Interrupt Clear (SSIICR), offset 0x020

The **SSIICR** register is the interrupt clear register. On a write of 1, the corresponding interrupt is cleared. A write of 0 has no effect.

SSI Interrupt Clear (SSIICR)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0x020
Type W1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>RTIC</td>
<td>W1C</td>
<td>0</td>
<td>SSI Receive Time-Out Interrupt Clear Writing a 1 to this bit clears the RTRIS bit in the SSIRIS register and the RTMIS bit in the SSIMIS register.</td>
</tr>
<tr>
<td>0</td>
<td>RORIC</td>
<td>W1C</td>
<td>0</td>
<td>SSI Receive Overrun Interrupt Clear Writing a 1 to this bit clears the RORRIS bit in the SSIRIS register and the RORMIS bit in the SSIMIS register.</td>
</tr>
</tbody>
</table>
Register 10: SSI DMA Control (SSIDMACTL), offset 0x024

The **SSIDMACTL** register is the µDMA control register.

SSI DMA Control (SSIDMACTL)

SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0x024
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>TXDMAE</td>
<td>RW</td>
<td>0</td>
<td>Transmit DMA Enable</td>
</tr>
<tr>
<td>0</td>
<td>RXDMAE</td>
<td>RW</td>
<td>0</td>
<td>Receive DMA Enable</td>
</tr>
</tbody>
</table>

Value Description

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>µDMA for the transmit FIFO is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>µDMA for the transmit FIFO is enabled.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>µDMA for the receive FIFO is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>µDMA for the receive FIFO is enabled.</td>
</tr>
</tbody>
</table>
Register 11: SSI Clock Configuration (SSICC), offset 0xFC8

The SSICC register controls the baud clock source for the SSI module.

**Note:** If the PIOSC is used for the SSI baud clock, the system clock frequency must be at least 16 MHz in Run mode.

SSI Clock Configuration (SSICC)

SSI0 base: 0x4000.8000  
SSI1 base: 0x4000.9000  
SSI2 base: 0x4000.A000  
SSI3 base: 0x4000.B000  
Offset 0xFC8  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 3:0       | CS         | RW   | 0       | SSI Baud Clock Source  

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>System clock (based on clock source and divisor factor)</td>
</tr>
<tr>
<td>0x1-0x4</td>
<td>reserved</td>
</tr>
<tr>
<td>0x5</td>
<td>PIOSC</td>
</tr>
<tr>
<td>0x6 - 0xFF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>
Register 12: SSI Peripheral Identification 4 (SSIPeriphID4), offset 0xFD0

The SSSIPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

### SSI Peripheral Identification 4 (SSIPeriphID4)

SSI0 base: 0x4000.8000  
SSI1 base: 0x4000.9000  
SSI2 base: 0x4000.A000  
SSI3 base: 0x4000.B000  
Offset 0xFD0  
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 7:0       | PID4       | RO   | 0x00        | SSI Peripheral ID Register [7:0]  
Can be used by software to identify the presence of this peripheral. |
Register 13: SSI Peripheral Identification 5 (SSIPeriphID5), offset 0xFD4

The SSIPeriphID registers are hard-coded and the fields within the register determine the reset value.

SSI Peripheral Identification 5 (SSIPeriphID5)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFD4
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>.00</td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID5</td>
<td>RO</td>
<td>0x00</td>
<td>SSI Peripheral ID Register [15:8]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 14: SSI Peripheral Identification 6 (SSIPeriphID6), offset 0xFD8

The SSSIPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

SSI Peripheral Identification 6 (SSIPeriphID6)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFD8
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 7:0       | PID6       | RO   | 0x00      | SSI Peripheral ID Register [23:16]
Can be used by software to identify the presence of this peripheral.
Register 15: SSI Peripheral Identification 7 (SSIPeriphID7), offset 0xFDC

The SSSIPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

SSI Peripheral Identification 7 (SSIPeriphID7)

<table>
<thead>
<tr>
<th>Description</th>
<th>Reset Type</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>0x0000.00</td>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
</tr>
<tr>
<td>Can be used by software to identify the presence of this peripheral.</td>
<td>0x00</td>
<td>7:0</td>
<td>PID7</td>
<td>RO</td>
<td>0x00</td>
</tr>
</tbody>
</table>
Register 16: SSI Peripheral Identification 0 (SSIPeriphID0), offset 0xFE0

The SSSIPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

SSI Peripheral Identification 0 (SSIPeriphID0)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFE0
Type RO, reset 0x0000.0022

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID0</td>
<td>RO</td>
<td>0x22</td>
<td>SSI Peripheral ID Register [7:0] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 17: SSI Peripheral Identification 1 (SSIPeriphID1), offset 0xFE4

The SSIPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

SSI Peripheral Identification 1 (SSIPeriphID1)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFE4
Type RO, reset 0x0000.0000

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

SSI Peripheral ID Register [15:8]
Can be used by software to identify the presence of this peripheral.
Register 18: SSI Peripheral Identification 2 (SSIPeriphID2), offset 0xFE8

The SSSIPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

SSI Peripheral Identification 2 (SSIPeriphID2)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFE8
Type RO, reset 0x0000.0018

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID2</td>
<td>RO</td>
<td>0x18</td>
<td>SSI Peripheral ID Register [23:16] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 19: SSI Peripheral Identification 3 (SSIPeriphID3), offset 0xFEC

The SSSIPeriphIDn registers are hard-coded and the fields within the register determine the reset value.

SSI Peripheral Identification 3 (SSIPeriphID3)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFEC
Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>PID3</td>
<td>RO</td>
<td>0x01</td>
<td>SSI Peripheral ID Register [31:24] Can be used by software to identify the presence of this peripheral.</td>
</tr>
</tbody>
</table>
Register 20: SSI PrimeCell Identification 0 (SSIPCellID0), offset 0xFF0

The **SSIPCellIDn** registers are hard-coded, and the fields within the register determine the reset value.

SSI PrimeCell Identification 0 (SSIPCellID0)

SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFF0
Type RO, reset 0x0000.000D

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID0</td>
<td>RO</td>
<td>0x0D</td>
<td>SSI PrimeCell ID Register [7:0]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 21: SSI PrimeCell Identification 1 (SSIPCellID1), offset 0xFF4

The **SSIPCellIDn** registers are hard-coded, and the fields within the register determine the reset value.

SSI PrimeCell Identification 1 (SSIPCellID1)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID1</td>
<td>RO</td>
<td>0xF0</td>
<td>SSI PrimeCell ID Register [15:8]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 22: SSI PrimeCell Identification 2 (SSIPCellID2), offset 0xFF8

The SSIPCellIDn registers are hard-coded, and the fields within the register determine the reset value.

SSI PrimeCell Identification 2 (SSIPCellID2)

SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFF8
Type RO, reset 0x0000.0005

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID2</td>
<td>RO</td>
<td>0x05</td>
<td>SSI PrimeCell ID Register [23:16]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
Register 23: SSI PrimeCell Identification 3 (SSIPCellID3), offset 0xFFC

The SSI PrimeCell ID registers are hard-coded, and the fields within the register determine the reset value.

SSI PrimeCell Identification 3 (SSIPCellID3)
SSI0 base: 0x4000.8000
SSI1 base: 0x4000.9000
SSI2 base: 0x4000.A000
SSI3 base: 0x4000.B000
Offset 0xFFC
Type RO, reset 0x0000.00B1

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CID3</td>
<td>RO</td>
<td>0xB1</td>
<td>SSI PrimeCell ID Register [31:24]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Provides software a standard cross-peripheral identification system.</td>
</tr>
</tbody>
</table>
16 Inter-Integrated Circuit (I\(^2\)C) Interface

The Inter-Integrated Circuit (I\(^2\)C) bus provides bi-directional data transfer through a two-wire design (a serial data line SDA and a serial clock line SCL), and interfaces to external I\(^2\)C devices such as serial memory (RAMs and ROMs), networking devices, LCDs, tone generators, and so on. The I\(^2\)C bus may also be used for system testing and diagnostic purposes in product development and manufacturing. The TM4C123GH6PZ microcontroller includes providing the ability to communicate (both transmit and receive) with other I\(^2\)C devices on the bus.

The TM4C123GH6PZ controller includes I\(^2\)C modules with the following features:

- Devices on the I\(^2\)C bus can be designated as either a master or a slave
  - Supports both transmitting and receiving data as either a master or a slave
  - Supports simultaneous master and slave operation
- Four I\(^2\)C modes
  - Master transmit
  - Master receive
  - Slave transmit
  - Slave receive
- Four transmission speeds:
  - Standard (100 Kbps)
  - Fast-mode (400 Kbps)
  - Fast-mode plus (1 Mbps)
  - High-speed mode (3.33 Mbps)
- Clock low timeout interrupt
- Dual slave address capability
- Glitch suppression
- Master and slave interrupt generation
  - Master generates interrupts when a transmit or receive operation completes (or aborts due to an error)
  - Slave generates interrupts when data has been transferred or requested by a master or when a START or STOP condition is detected
- Master with arbitration and clock synchronization, multimaster support, and 7-bit addressing mode
16.1 Block Diagram

Figure 16-1. I²C Block Diagram

16.2 Signal Description

The following table lists the external signals of the I²C interface and describes the function of each. The I²C interface signals are alternate functions for some GPIO signals and default to be GPIO signals at reset, with the exception of the I2C0SCL and I2C0SDA pins which default to the I²C function. The column in the table below titled “Pin Mux/Pin Assignment” lists the possible GPIO pin placements for the I²C signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the I²C function. The number in parentheses is the encoding that must be programmed into the PMCn field in the GPIOPortControl(GPIOPCTL) register (page 702) to assign the I²C signal to the specified GPIO port pin. Note that the I2CSDA pin should be set to open drain using the GPIO Open Drain Select (GPIOODR) register. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659.

Table 16-1. I²C Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C0SCL</td>
<td>72</td>
<td>PB2 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C0SDA</td>
<td>73</td>
<td>PB3 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 0 data.</td>
</tr>
<tr>
<td>I2C1SCL</td>
<td>34</td>
<td>PA6 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>74</td>
<td>PG4 (3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I2C1SDA</td>
<td>35</td>
<td>PA7 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 1 data.</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>PG5 (3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I2C2SCL</td>
<td>36</td>
<td>PF6 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>95</td>
<td>PE4 (3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I2C2SDA</td>
<td>58</td>
<td>PF7 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 2 data.</td>
</tr>
<tr>
<td></td>
<td>96</td>
<td>PE5 (3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I2C3SCL</td>
<td>1</td>
<td>PD0 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>62</td>
<td>PG0 (3)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 16-1. I\(^2\)C Signals (100LQFP) (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type\textsuperscript{a}</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C3SDA</td>
<td>2</td>
<td>PD1 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I(^2)C module 3 data.</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>PG1 (3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I2C4SCL</td>
<td>60</td>
<td>PG2 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I(^2)C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C4SDA</td>
<td>59</td>
<td>PG3 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I(^2)C module 4 data.</td>
</tr>
<tr>
<td>I2C5SCL</td>
<td>87</td>
<td>PG6 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I(^2)C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C5SDA</td>
<td>88</td>
<td>PG7 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I(^2)C module 5 data.</td>
</tr>
</tbody>
</table>

\textsuperscript{a} The TTL designation indicates the pin has TTL-compatible voltage levels.

16.3 Functional Description

Each I\(^2\)C module is comprised of both master and slave functions and is identified by a unique address. A master-initiated communication generates the clock signal, SCL. For proper operation, the SDA pin must be configured as an open-drain signal. Due to the internal circuitry that supports high-speed operation, the SCL pin must not be configured as an open-drain signal, although the internal circuitry causes it to act as if it were an open drain signal. Both SDA and SCL signals must be connected to a positive supply voltage using a pull-up resistor. A typical I\(^2\)C bus configuration is shown in Figure 16-2. Refer to the I\(^2\)C-bus specification and user manual to determine the size of the pull-ups needed for proper operation.

See “Inter-Integrated Circuit (I\(^2\)C) Interface” on page 1433 for I\(^2\)C timing diagrams.

Figure 16-2. I\(^2\)C Bus Configuration

16.3.1 I\(^2\)C Bus Functional Overview

The I\(^2\)C bus uses only two signals: SDA and SCL, named I2CSDA and I2CSCL on TM4C123GH6PZ microcontrollers. SDA is the bi-directional serial data line and SCL is the bi-directional serial clock line. The bus is considered idle when both lines are High.

Every transaction on the I\(^2\)C bus is nine bits long, consisting of eight data bits and a single acknowledge bit. The number of bytes per transfer (defined as the time between a valid START and STOP condition, described in “START and STOP Conditions” on page 1021) is unrestricted, but each data byte has to be followed by an acknowledge bit, and data must be transferred MSB first. When a receiver cannot receive another complete byte, it can hold the clock line SCL Low and force the transmitter into a wait state. The data transfer continues when the receiver releases the clock SCL.
16.3.1.1 START and STOP Conditions

The protocol of the I²C bus defines two states to begin and end a transaction: START and STOP. A High-to-Low transition on the SDA line while the SCL is High is defined as a START condition, and a Low-to-High transition on the SDA line while SCL is High is defined as a STOP condition. The bus is considered busy after a START condition and free after a STOP condition. See Figure 16-3.

![Figure 16-3. START and STOP Conditions](image)

The STOP bit determines if the cycle stops at the end of the data cycle or continues on to a repeated START condition. To generate a single transmit cycle, the I²C Master Slave Address (I2CMSA) register is written with the desired address, the R/S bit is cleared, and the Control register is written with ACK=X (0 or 1), STOP=1, START=1, and RUN=1 to perform the operation and stop. When the operation is completed (or aborted due an error), the interrupt pin becomes active and the data may be read from the I²C Master Data (I2CMDR) register. When the I²C module operates in Master receiver mode, the ACK bit is normally set causing the I²C bus controller to transmit an acknowledge automatically after each byte. This bit must be cleared when the I²C bus controller requires no further data to be transmitted from the slave transmitter.

When operating in slave mode, the STARTRIS and STOPRIS bits in the I²C Slave Raw Interrupt Status (I2CSRIS) register indicate detection of start and stop conditions on the bus and the I²C Slave Masked Interrupt Status (I2CSMIS) register can be configured to allow STARTRIS and STOPRIS to be promoted to controller interrupts (when interrupts are enabled).

16.3.1.2 Data Format with 7-Bit Address

Data transfers follow the format shown in Figure 16-4. After the START condition, a slave address is transmitted. This address is 7-bits long followed by an eighth bit, which is a data direction bit (R/S bit in the I2CMSA register). If the R/S bit is clear, it indicates a transmit operation (send), and if it is set, it indicates a request for data (receive). A data transfer is always terminated by a STOP condition generated by the master, however, a master can initiate communications with another device on the bus by generating a repeated START condition and addressing another slave without first generating a STOP condition. Various combinations of receive/transmit formats are then possible within a single transfer.

![Figure 16-4. Complete Data Transfer with a 7-Bit Address](image)

The first seven bits of the first byte make up the slave address (see Figure 16-5). The eighth bit determines the direction of the message. A zero in the R/S position of the first byte means that the
master transmits (sends) data to the selected slave, and a one in this position means that the master receives data from the slave.

**Figure 16-5. R/S Bit in First Byte**

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/S</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Slave address</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**16.3.1.3 Data Validity**

The data on the SDA line must be stable during the high period of the clock, and the data line can only change when SCL is Low (see Figure 16-6).

**Figure 16-6. Data Validity During Bit Transfer on the I2C Bus**

**16.3.1.4 Acknowledge**

All bus transactions have a required acknowledge clock cycle that is generated by the master. During the acknowledge cycle, the transmitter (which can be the master or slave) releases the SDA line. To acknowledge the transaction, the receiver must pull down SDA during the acknowledge clock cycle. The data transmitted out by the receiver during the acknowledge cycle must comply with the data validity requirements described in “Data Validity” on page 1022.

When a slave receiver does not acknowledge the slave address, SDA must be left High by the slave so that the master can generate a STOP condition and abort the current transfer. If the master device is acting as a receiver during a transfer, it is responsible for acknowledging each transfer made by the slave. Because the master controls the number of bytes in the transfer, it signals the end of data to the slave transmitter by not generating an acknowledge on the last data byte. The slave transmitter must then release SDA to allow the master to generate the STOP or a repeated START condition.

If the slave is required to provide a manual ACK or NACK, the I2C Slave ACK Control (I2CSACKCTL) register allows the slave to NACK for invalid data or command or ACK for valid data or command. When this operation is enabled, the MCU slave module I2C clock is pulled low after the last data bit until this register is written with the indicated response.

**16.3.1.5 Repeated Start**

The I2C master module has the capability of executing a repeated START (transmit or receive) after an initial transfer has occurred.

A repeated start sequence for a Master transmit is as follows:

1. When the device is in the idle state, the Master writes the slave address to the I2CMSA register and configures the R/S bit for the desired transfer type.
2. Data is written to the I2CMDR register.

3. When the BUSY bit in the I2CMCS register is 0, the Master writes 0x3 to the I2CMCS register to initiate a transfer.

4. The Master does not generate a STOP condition but instead writes another slave address to the I2CMSA register and then writes 0x3 to initiate the repeated START.

A repeated start sequence for a Master receive is similar:

1. When the device is in idle, the Master writes the slave address to the I2CMSA register and configures the R/S bit for the desired transfer type.

2. The master reads data from the I2CMDR register.

3. When the BUSY bit in the I2CMCS register is 0, the Master writes 0x3 to the I2CMCS register to initiate a transfer.

4. The Master does not generate a STOP condition but instead writes another slave address to the I2CMSA register and then writes 0x3 to initiate the repeated START.

For more information on repeated START, refer to Figure 16-12 on page 1033 and Figure 16-13 on page 1034.

16.3.1.6 Clock Low Timeout (CLTO)

The \( \text{I}^2\text{C} \) slave can extend the transaction by pulling the clock low periodically to create a slow bit transfer rate. The \( \text{I}^2\text{C} \) module has a 12-bit programmable counter that is used to track how long the clock has been held low. The upper 8 bits of the count value are software programmable through the I2C Master Clock Low Timeout Count (I2CMCLKOCNT) register. The lower four bits are not user visible and are 0x0. The CNTL value programmed in the I2CMCLKOCNT register has to be greater than 0x01. The application can program the eight most significant bits of the counter to reflect the acceptable cumulative low period in transaction. The count is loaded at the START condition and counts down on each falling edge of the internal bus clock of the Master. Note that the internal bus clock generated for this counter keeps running at the programmed \( \text{I}^2\text{C} \) speed even if SCL is held low on the bus. Upon reaching terminal count, the master state machine forces ABORT on the bus by issuing a STOP condition at the instance of SCL and SDA release.

As an example, if an \( \text{I}^2\text{C} \) module was operating at 100 kHz speed, programming the I2CMCLKOCNT register to 0xDA would translate to the value 0xDA0 since the lower four bits are set to 0x0. This would translate to a decimal value of 3488 clocks or a cumulative clock low period of 34.88 ms at 100 kHz.

The CLKRIS bit in the I2C Master Raw Interrupt Status (I2CMRIS) register is set when the clock timeout period is reached, allowing the master to start corrective action to resolve the remote slave state. In addition, the CLKTO bit in the I2C Master Control/Status (I2CMCS) register is set; this bit is cleared when a STOP condition is sent or during the I2C master reset. The status of the raw SDA and SCL signals are readable by software through the SDA and SCL bits in the I2C Master Bus Monitor (I2CMBMON) register to help determine the state of the remote slave.

In the event of a CLTO condition, application software must choose how it intends to attempt bus recovery. Most applications may attempt to manually toggle the \( \text{I}^2\text{C} \) pins to force the slave to let go of the clock signal (a common solution is to attempt to force a STOP on the bus). If a CLTO is detected before the end of a burst transfer, and the bus is successfully recovered by the master, the master hardware attempts to finish the pending burst operation. Depending on the state of the
slave after bus recovery, the actual behavior on the bus varies. If the slave resumes in a state where it can acknowledge the master (essentially, where it was before the bus hang), it continues where it left off. However, if the slave resumes in a reset state (or if a forced STOP by the master causes the slave to enter the idle state), it may ignore the master's attempt to complete the burst operation and NAK the first data byte that the master sends or requests.

Since the behavior of slaves cannot always be predicted, it is suggested that the application software always write the STOP bit in the I²C Master Configuration (I2CMCR) register during the CLTO interrupt service routine. This limits the amount of data the master attempts to send or receive upon bus recovery to a single byte, and after the single byte is on the wire, the master issues a STOP.

An alternative solution is to have the application software reset the I²C peripheral before attempting to manually recover the bus. This solution allows the I²C master hardware to be returned to a known good (and idle) state before attempting to recover a stuck bus and prevents any unwanted data from appearing on the wire.

Note: The Master Clock Low Timeout counter counts for the entire time SCL is held Low continuously. If SCL is deasserted at any point, the Master Clock Low Timeout Counter is reloaded with the value in the I2CMCLKOCNT register and begins counting down from this value.

16.3.1.7 Dual Address

The I²C interface supports dual address capability for the slave. The additional programmable address is provided and can be matched if enabled. In legacy mode with dual address disabled, the I²C slave provides an ACK on the bus if the address matches the OAR field in the I2CSOAR register. In dual address mode, the I²C slave provides an ACK on the bus if either the OAR field in the I2CSOAR register or the OAR2 field in the I2CSOAR2 register is matched. The enable for dual address is programmable through the OAR2EN bit in the I2CSOAR2 register and there is no disable on the legacy address.

The OAR2SEL bit in the I2CSCSR register indicates if the address that was ACKed is the alternate address or not. When this bit is clear, it indicates either legacy operation or no address match.

16.3.1.8 Arbitration

A master may start a transfer only if the bus is idle. It's possible for two or more masters to generate a START condition within minimum hold time of the START condition. In these situations, an arbitration scheme takes place on the SDA line, while SCL is High. During arbitration, the first of the competing master devices to place a 1 (High) on SDA, while another master transmits a 0 (Low), switches off its data output stage and retires until the bus is idle again.

Arbitration can take place over several bits. Its first stage is a comparison of address bits, and if both masters are trying to address the same device, arbitration continues on to the comparison of data bits.

16.3.1.9 Glitch Suppression in Multi-Master Configuration

When a multi-master configuration is being used, the GFE bit in the I²C Master Configuration (I2CMCR) register can be set to enable glitch suppression on the SCL and SDA lines and assure proper signal values. The filter can be programmed to different filter widths using the GFPW bit in the I²C Master Configuration 2 (I2CMCR2) register. The glitch suppression value is in terms of buffered system clocks. Note that all signals will be delayed internally when glitch suppression is nonzero. For example, if GFPW is set to 0x7, 31 clocks should be added onto the calculation for the expected transaction time.
16.3.2 Available Speed Modes

The I²C bus can run in Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) or High-Speed mode (3.33 Mbps). The selected mode should match the speed of the other I²C devices on the bus.

16.3.2.1 Standard, Fast, and Fast Plus Modes

Standard, Fast, and Fast Plus modes are selected using a value in the I²C Master Timer Period (I²CMTPR) register that results in an SCL frequency of 100 kbps for Standard mode, 400 kbps for Fast mode, or 1 Mbps for Fast mode plus.

The I²C clock rate is determined by the parameters $CLK_{PRD}$, $TIMER_{PRD}$, $SCL_{LP}$, and $SCL_{HP}$ where:

- $CLK_{PRD}$ is the system clock period
- $SCL_{LP}$ is the low phase of SCL (fixed at 6)
- $SCL_{HP}$ is the high phase of SCL (fixed at 4)
- $TIMER_{PRD}$ is the programmed value in the I²CMTPR register (see page 1047). This value is determined by replacing the known variables in the equation below and solving for $TIMER_{PRD}$.

The I²C clock period is calculated as follows:

$$SCL\_PERIOD = 2 \times (1 + TIMER_{PRD}) \times (SCL_{LP} + SCL_{HP}) \times CLK_{PRD}$$

For example:

- $CLK_{PRD} = 50$ ns
- $TIMER_{PRD} = 2$
- $SCL_{LP} = 6$
- $SCL_{HP} = 4$

yields a SCL frequency of:

$$1/SCL\_PERIOD = 333 \text{ KHz}$$

Table 16-2 gives examples of the timer periods that should be used to generate Standard, Fast mode, and Fast mode plus SCL frequencies based on various system clock frequencies.

Table 16-2. Examples of I²C Master Timer Period Versus Speed Mode

<table>
<thead>
<tr>
<th>System Clock</th>
<th>Timer Period</th>
<th>Standard Mode</th>
<th>Timer Period</th>
<th>Fast Mode</th>
<th>Timer Period</th>
<th>Fast Mode Plus</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 MHz</td>
<td>0x01</td>
<td>100 Kbps</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>6 MHz</td>
<td>0x02</td>
<td>100 Kbps</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>12.5 MHz</td>
<td>0x06</td>
<td>89 Kbps</td>
<td>0x01</td>
<td>312 Kbps</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>16.7 MHz</td>
<td>0x08</td>
<td>93 Kbps</td>
<td>0x02</td>
<td>278 Kbps</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>20 MHz</td>
<td>0x09</td>
<td>100 Kbps</td>
<td>0x02</td>
<td>333 Kbps</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>25 MHz</td>
<td>0x0C</td>
<td>96.2 Kbps</td>
<td>0x03</td>
<td>312 Kbps</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>33 MHz</td>
<td>0x10</td>
<td>97.1 Kbps</td>
<td>0x04</td>
<td>330 Kbps</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>40 MHz</td>
<td>0x13</td>
<td>100 Kbps</td>
<td>0x04</td>
<td>400 Kbps</td>
<td>0x01</td>
<td>1000 Kbps</td>
</tr>
<tr>
<td>50 MHz</td>
<td>0x18</td>
<td>100 Kbps</td>
<td>0x06</td>
<td>357 Kbps</td>
<td>0x02</td>
<td>833 Kbps</td>
</tr>
<tr>
<td>80 MHz</td>
<td>0x27</td>
<td>100 Kbps</td>
<td>0x09</td>
<td>400 Kbps</td>
<td>0x03</td>
<td>1000 Kbps</td>
</tr>
</tbody>
</table>
16.3.2.2 High-Speed Mode

The TM4C123GH6PZ \( \text{I}^2\text{C} \) peripheral has support for High-speed operation as both a master and slave. High-Speed mode is configured by setting the HS bit in the \( \text{I}^2\text{C} \) Master Control/Status (I2CMCS) register. High-Speed mode transmits data at a high bit rate with a 66.6%/33.3% duty cycle, but communication and arbitration are done at Standard, Fast mode, or Fast-mode plus speed, depending on which is selected by the user. When the HS bit in the I2CMCS register is set, current mode pull-ups are enabled.

The clock period can be selected using the equation below, but in this case, SCL_LP=2 and SCL_HP=1.

\[
SCL\_PERIOD = 2 \times (1 + \text{TIMER\_PRD}) \times (SCL\_LP + SCL\_HP) \times \text{CLK\_PRD}
\]

So for example:

- \( \text{CLK\_PRD} = 25 \text{ ns} \)
- \( \text{TIMER\_PRD} = 1 \)
- \( \text{SCL\_LP}=2 \)
- \( \text{SCL\_HP}=1 \)

yields a SCL frequency of:

\[
1/T = 3.33 \text{ Mhz}
\]

Table 16-3 on page 1026 gives examples of timer period and system clock in High-Speed mode. Note that the HS bit in the I2CMTPR register needs to be set for the TPR value to be used in High-Speed mode.

### Table 16-3. Examples of \( \text{I}^2\text{C} \) Master Timer Period in High-Speed Mode

<table>
<thead>
<tr>
<th>System Clock</th>
<th>Timer Period</th>
<th>Transmission Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>40 MHz</td>
<td>0x01</td>
<td>3.33 Mbps</td>
</tr>
<tr>
<td>50 MHz</td>
<td>0x02</td>
<td>2.77 Mbps</td>
</tr>
<tr>
<td>80 MHz</td>
<td>0x03</td>
<td>3.33 Mbps</td>
</tr>
</tbody>
</table>

When operating as a master, the protocol is shown in Figure 16-7. The master is responsible for sending a master code byte in either Standard (100 Kbps) or Fast-mode (400 Kbps) before it begins transferring in High-speed mode. The master code byte must contain data in the form of 0000.1XXX and is used to tell the slave devices to prepare for a High-speed transfer. The master code byte should never be acknowledged by a slave since it is only used to indicate that the upcoming data is going to be transferred at a higher data rate. To send the master code byte, software should place the value of the master code byte into the I2CMSA register and write the I2CMCS register with a value of 0x13. This places the \( \text{I}^2\text{C} \) master peripheral in High-speed mode, and all subsequent transfers (until STOP) are carried out at High-speed data rate using the normal I2CMCS command bits, without setting the HS bit in the I2CMCS register. Again, setting the HS bit in the I2CMCS register is only necessary during the master code byte.

When operating as a High-speed slave, there is no additional software required.
16.3.3 Interrupts

The I²C can generate interrupts when the following conditions are observed:

- Master transaction completed
- Master arbitration lost
- Master transaction error
- Master bus timeout
- Slave transaction received
- Slave transaction requested
- Stop condition on bus detected
- Start condition on bus detected

The I²C master and I²C slave modules have separate interrupt signals. While both modules can generate interrupts for multiple conditions, only a single interrupt signal is sent to the interrupt controller.

16.3.3.1 I²C Master Interrupts

The I²C master module generates an interrupt when a transaction completes (either transmit or receive), when arbitration is lost, or when an error occurs during a transaction. To enable the I²C master interrupt, software must set the IM bit in the I²C Master Interrupt Mask (I2CMIMR) register. When an interrupt condition is met, software must check the ERROR and ARBLST bits in the I²C Master Control/Status (I2CMCS) register to verify that an error didn't occur during the last transaction and to ensure that arbitration has not been lost. An error condition is asserted if the last transaction wasn't acknowledged by the slave. If an error is not detected and the master has not lost arbitration, the application can proceed with the transfer. The interrupt is cleared by writing a 1 to the IC bit in the I²C Master Interrupt Clear (I2CMICR) register.

If the application doesn't require the use of interrupts, the raw interrupt status is always visible via the I²C Master Raw Interrupt Status (I2CMRIS) register.

16.3.3.2 I²C Slave Interrupts

The slave module can generate an interrupt when data has been received or requested. This interrupt is enabled by setting the DATAIM bit in the I²C Slave Interrupt Mask (I2CSIMR) register. Software
determines whether the module should write (transmit) or read (receive) data from the \textit{I}^2C \textit{Slave Data (I2CSDR)} register, by checking the \texttt{RREQ} and \texttt{TREQ} bits of the \textit{I}^2C \textit{Slave Control/Status (I2CSCSR)} register. If the slave module is in receive mode and the first byte of a transfer is received, the \texttt{FBR} bit is set along with the \texttt{RREQ} bit. The interrupt is cleared by setting the \texttt{DATAIC} bit in the \textit{I}^2C \textit{Slave Interrupt Clear (I2CSICR)} register.

In addition, the slave module can generate an interrupt when a start and stop condition is detected. These interrupts are enabled by setting the \texttt{STARTIM} and \texttt{STOPIM} bits of the \textit{I}^2C \textit{Slave Interrupt Mask (I2CSIMR)} register and cleared by writing a 1 to the \texttt{STOPIC} and \texttt{STARTIC} bits of the \textit{I}^2C \textit{Slave Interrupt Clear (I2CSICR)} register.

If the application doesn't require the use of interrupts, the raw interrupt status is always visible via the \textit{I}^2C \textit{Slave Raw Interrupt Status (I2CSRIS)} register.

16.3.4 Loopback Operation

The \textit{I}^2C modules can be placed into an internal loopback mode for diagnostic or debug work by setting the \texttt{LPBK} bit in the \textit{I}^2C \textit{Master Configuration (I2CMCR)} register. In loopback mode, the SDA and SCL signals from the master and are tied to the SDA and SCL signals of the slave module to allow internal testing of the device without having to go through I/O.

16.3.5 Command Sequence Flow Charts

This section details the steps required to perform the various \textit{I}^2C transfer types in both master and slave mode.

16.3.5.1 \textit{I}^2C Master Command Sequences

The figures that follow show the command sequences available for the \textit{I}^2C master.
Figure 16-8. Master Single TRANSMIT

Idle

Write Slave Address to I2CMSA

Write data to I2CMDR

Read I2CMCS

BUSBSY bit=0?

YES

Write ---0-111 to I2CMCS

Read I2CMCS

BUSY bit=0?

YES

Error Service

ERROR bit=0?

YES

Idle

Sequence may be omitted in a Single Master system
Figure 16-9. Master Single RECEIVE

Idle

Write Slave Address to I2CMSA

Read I2CMCS

BUSBSY bit=0? NO

YES

Write 00111 to I2CMCS

Read I2CMCS

BUSY bit=0? NO

YES

Error Service

Error bit=0? NO

YES

Read data from I2CMDR

Idle
Figure 16-10. Master TRANSMIT of Multiple Data Bytes

```
Idle
Write Slave Address to I2CMSA
Write data to I2CMDR
Read I2CMCS
BUSY bit=0?  
YES
ERROR bit=0?  
YES
Write ---0-011 to I2CMCS

Sequence may be omitted in a Single Master system

Read I2CMCS
BUSY bit=0?  
NO
ERROR bit=0?  
NO
Write data to I2CMDR
Index=n?  
YES
Write ---0-101 to I2CMCS

Write ---0-001 to I2CMCS

Read I2CMCS
BUSY bit=0?  
YES
Error Service

Write ---0-100 to I2CMCS

Error Service

Idle
```
Figure 16-11. Master RECEIVE of Multiple Data Bytes
Figure 16-12. Master RECEIVE with Repeated START after Master TRANSMIT

1. Idle

2. Master operates in Master Transmit mode
   STOP condition is not generated

3. Write Slave Address to I2CMSA

4. Write ---01011 to I2CMCS

5. Repeated START condition is generated with changing data direction

6. Master operates in Master Receive mode

7. Idle
Figure 16-13. Master TRANSMIT with Repeated START after Master RECEIVE

1. **Idle**
   - Master operates in Master Receive mode
   - STOP condition is not generated

2. **Write Slave Address to I2CMSA**
   - Write **---0-011** to I2CMCS

3. **Repeated START condition is generated with changing data direction**

4. **Repeat**
   - Master operates in Master Transmit mode

5. **Idle**
Figure 16-14. Standard High Speed Mode Master Transmit

- IDLE
- Write slave address to I2CMSA register
- Write "---1001 1" to I2CMCS register
- Read I2CMCS register
  - Busy='0'
  - Error='0'
- IDLE
- Yes
  - Normal sequence starts here. The sequence below covers SINGLE send
  - Write Slave Address to I2MISA register
  - Write Data to I2CMDR register
  - Write "---0-111" to I2CMCS register
  - Read I2CMCS register
  - Busy='0'
  - Error='0'
- IDLE
  - Error service
  - IDLE
16.3.5.2  \(\text{I}^2\text{C} \) Slave Command Sequences

Figure 16-15 on page 1036 presents the command sequence available for the \(\text{I}^2\text{C} \) slave.

Figure 16-15. Slave Command Sequence

```
Idle

Write OWN Slave Address to I2CSOAR

Write ------- 1 to I2CSCSR

Read I2CSCSR

RREQ bit=1?

TREQ bit=1?

YES

NO

YES

NO

Write data to I2CSDR

Read data from I2CSDR

FBR is also valid
```

16.4 Initialization and Configuration

16.4.1 Configure the \(\text{I}^2\text{C} \) Module to Transmit a Single Byte as a Master

The following example shows how to configure the \(\text{I}^2\text{C} \) module to transmit a single byte as a master. This assumes the system clock is 20 MHz.

1. Enable the \(\text{I}^2\text{C} \) clock using the RCGCI2C register in the System Control module (see page 351).

2. Enable the clock to the appropriate GPIO module via the RCGCGPIO register in the System Control module (see page 342). To find out which GPIO port to enable, refer to Table 23-5 on page 1386.

3. In the GPIO module, enable the appropriate pins for their alternate function using the GPIOAFSEL register (see page 684). To determine which GPIOs to configure, see Table 23-4 on page 1377.
4. Enable the I2CSDA pin for open-drain operation. See page 689.

5. Configure the PMCn fields in the GPIOPCTL register to assign the I2C signals to the appropriate pins. See page 702 and Table 23-5 on page 1386.

6. Initialize the I2C Master by writing the I2CMCR register with a value of 0x0000.0010.

7. Set the desired SCL clock speed of 100 Kbps by writing the I2CMTPR register with the correct value. The value written to the I2CMTPR register represents the number of system clock periods in one SCL clock period. The TPR value is determined by the following equation:

\[
TPR = \left( \frac{\text{System Clock}}{2 \times (\text{SCL_LP} + \text{SCL_HP}) \times \text{SCL_CLK}} \right) - 1;
\]

\[
TPR = \left( \frac{20\text{MHz}}{2 \times (6+4) \times 100000} \right) - 1;
\]

TPR = 9

Write the I2CMTPR register with the value of 0x0000.0009.

8. Specify the slave address of the master and that the next operation is a Transmit by writing the I2CMSA register with a value of 0x0000.0076. This sets the slave address to 0x3B.

9. Place data (byte) to be transmitted in the data register by writing the I2CMDR register with the desired data.

10. Initiate a single byte transmit of the data from Master to Slave by writing the I2CMCS register with a value of 0x0000.0007 (STOP, START, RUN).

11. Wait until the transmission completes by polling the I2CMCS register's BUSBSY bit until it has been cleared.

12. Check the ERROR bit in the I2CMCS register to confirm the transmit was acknowledged.

16.4.2 Configure the I2C Master to High Speed Mode

To configure the I2C master to High Speed mode:

1. Enable the I2C clock using the RCGCI2C register in the System Control module (see page 351).

2. Enable the clock to the appropriate GPIO module via the RCGCGPIO register in the System Control module (see page 342). To find out which GPIO port to enable, refer to Table 23-5 on page 1386.

3. In the GPIO module, enable the appropriate pins for their alternate function using the GPIOAFSEL register (see page 684). To determine which GPIOs to configure, see Table 23-4 on page 1377.

4. Enable the I2CSDA pin for open-drain operation. See page 689.

5. Configure the PMCn fields in the GPIOPCTL register to assign the I2C signals to the appropriate pins. See page 702 and Table 23-5 on page 1386.

6. Initialize the I2C Master by writing the I2CMCR register with a value of 0x0000.0010.

7. Set the desired SCL clock speed of 3.33 Mbps by writing the I2CMTPR register with the correct value. The value written to the I2CMTPR register represents the number of system clock periods in one SCL clock period. The TPR value is determined by the following equation:
TPR = (System Clock/(2*(SCL_LP + SCL_HP)*SCL_CLK))-1;
TPR = (80 MHz/(2*(2+1)*3330000))-1;
TPR = 3

Write the \texttt{I2CMTPR} register with the value of 0x0000.0003.

8. To send the master code byte, software should place the value of the master code byte into the \texttt{I2CMSA} register and write the \texttt{I2CMCS} register with a value of 0x13.

9. This places the I2C master peripheral in High-speed mode, and all subsequent transfers (until STOP) are carried out at High-speed data rate using the normal \texttt{I2CMCS} command bits, without setting the \texttt{HS} bit in the \texttt{I2CMCS} register.

10. The transaction is ended by setting the \texttt{STOP} bit in the \texttt{I2CMCS} register.

11. Wait until the transmission completes by polling the \texttt{I2CMCS} register’s \texttt{BUSBSY} bit until it has been cleared.

12. Check the \texttt{ERROR} bit in the \texttt{I2CMCS} register to confirm the transmit was acknowledged.

16.5 Register Map

Table 16-4 on page 1038 lists the I2C registers. All addresses given are relative to the I2C base address:

- I:\textsuperscript{2}C 0: 0x4002.0000
- I:\textsuperscript{2}C 1: 0x4002.1000
- I:\textsuperscript{2}C 2: 0x4002.2000
- I:\textsuperscript{2}C 3: 0x4002.3000
- I:\textsuperscript{2}C 4: 0x400C.0000
- I:\textsuperscript{2}C 5: 0x400C.1000

Note that the I2C module clock must be enabled before the registers can be programmed (see page 351). There must be a delay of 3 system clocks after the I2C module clock is enabled before any I2C module registers are accessed.

The \texttt{hw_i2c.h} file in the TivaWare™ Driver Library uses a base address of 0x800 for the I2C slave registers. Be aware when using registers with offsets between 0x800 and 0x818 that TivaWare™ for C Series uses an offset between 0x000 and 0x018 with the slave base address.

Table 16-4. Inter-Integrated Circuit (I2C) Interface Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>I2CMSA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Master Slave Address</td>
<td>1040</td>
</tr>
<tr>
<td>0x004</td>
<td>I2CMCS</td>
<td>RW</td>
<td>0x0000.0020</td>
<td>I2C Master Control/Status</td>
<td>1041</td>
</tr>
<tr>
<td>0x008</td>
<td>I2CMDR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Master Data</td>
<td>1046</td>
</tr>
<tr>
<td>0x00C</td>
<td>I2CMTPR</td>
<td>RW</td>
<td>0x0000.0001</td>
<td>I2C Master Timer Period</td>
<td>1047</td>
</tr>
<tr>
<td>0x010</td>
<td>I2CMIMR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Master Interrupt Mask</td>
<td>1048</td>
</tr>
<tr>
<td>0x014</td>
<td>I2CMRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>I2C Master Raw Interrupt Status</td>
<td>1049</td>
</tr>
</tbody>
</table>
Table 16-4. Inter-Integrated Circuit (I²C) Interface Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x018</td>
<td>I2CMMIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>I2C Master Masked Interrupt Status</td>
<td>1050</td>
</tr>
<tr>
<td>0x01C</td>
<td>I2CMICR</td>
<td>WO</td>
<td>0x0000.0000</td>
<td>I2C Master Interrupt Clear</td>
<td>1051</td>
</tr>
<tr>
<td>0x020</td>
<td>I2CMCR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Master Configuration</td>
<td>1052</td>
</tr>
<tr>
<td>0x024</td>
<td>I2CMCLKOCNT</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Master Clock Low Timeout Count</td>
<td>1054</td>
</tr>
<tr>
<td>0x02C</td>
<td>I2CMBMON</td>
<td>RO</td>
<td>0x0000.0003</td>
<td>I2C Master Bus Monitor</td>
<td>1055</td>
</tr>
<tr>
<td>0x038</td>
<td>I2CMCR2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Master Configuration 2</td>
<td>1056</td>
</tr>
</tbody>
</table>

I²C Slave

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x800</td>
<td>I2CSOAR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Slave Own Address</td>
<td>1057</td>
</tr>
<tr>
<td>0x804</td>
<td>I2SCCSR</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>I2C Slave Control/Status</td>
<td>1058</td>
</tr>
<tr>
<td>0x808</td>
<td>I2CSDR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Slave Data</td>
<td>1060</td>
</tr>
<tr>
<td>0x80C</td>
<td>I2CSIMR</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Slave Interrupt Mask</td>
<td>1061</td>
</tr>
<tr>
<td>0x810</td>
<td>I2CSRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>I2C Slave Raw Interrupt Status</td>
<td>1062</td>
</tr>
<tr>
<td>0x814</td>
<td>I2CSMIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>I2C Slave Masked Interrupt Status</td>
<td>1063</td>
</tr>
<tr>
<td>0x818</td>
<td>I2CSICR</td>
<td>WO</td>
<td>0x0000.0000</td>
<td>I2C Slave Interrupt Clear</td>
<td>1064</td>
</tr>
<tr>
<td>0x81C</td>
<td>I2CSOAR2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Slave Own Address 2</td>
<td>1065</td>
</tr>
<tr>
<td>0x820</td>
<td>I2CSACKCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>I2C Slave ACK Control</td>
<td>1066</td>
</tr>
</tbody>
</table>

I²C Status and Control

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xFC0</td>
<td>I2CPP</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>I2C Peripheral Properties</td>
<td>1067</td>
</tr>
<tr>
<td>0xFC4</td>
<td>I2 CPC</td>
<td>RO</td>
<td>0x0000.0001</td>
<td>I2C Peripheral Configuration</td>
<td>1068</td>
</tr>
</tbody>
</table>

16.6 Register Descriptions (I²C Master)

The remainder of this section lists and describes the I²C master registers, in numerical order by address offset.
Register 1: \(I^2C\) Master Slave Address (I2CMSA), offset 0x000

This register consists of eight bits: seven address bits (A6-A0), and a Receive/Send bit, which determines if the next operation is a Receive (High), or Transmit (Low).

I2C Master Slave Address (I2CMSA)

- \(I^2C\) 0 base: 0x4002.0000
- \(I^2C\) 1 base: 0x4002.1000
- \(I^2C\) 2 base: 0x4002.2000
- \(I^2C\) 3 base: 0x4002.3000
- \(I^2C\) 4 base: 0x400C.0000
- \(I^2C\) 5 base: 0x400C.1000

Offset 0x000
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:1</td>
<td>SA</td>
<td>RW</td>
<td>0x00</td>
<td>(I^2C) Slave Address</td>
</tr>
<tr>
<td>0</td>
<td>R/S</td>
<td>RW</td>
<td>0</td>
<td>Receive/Send</td>
</tr>
</tbody>
</table>

The \(R/S\) bit specifies if the next master operation is a Receive (High) or Transmit (Low).

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Transmit</td>
</tr>
<tr>
<td>1</td>
<td>Receive</td>
</tr>
</tbody>
</table>
Register 2: I2C Master Control/Status (I2CMCS), offset 0x004

This register accesses status bits when read and control bits when written. When read, the status register indicates the state of the I2C bus controller. When written, the control register configures the I2C controller operation.

The **START** bit generates the START or REPEATED START condition. The **STOP** bit determines if the cycle stops at the end of the data cycle or continues to the next transfer cycle, which could be a repeated START. To generate a single transmit cycle, the **I2C Master Slave Address (I2CMSA)** register is written with the desired address, the **R/S** bit is cleared, and this register is written with **ACK**=X (0 or 1), **STOP**=1, **START**=1, and **RUN**=1 to perform the operation and stop. When the operation is completed (or aborted due an error), an interrupt becomes active and the data may be read from the **I2CMDR** register. When the I2C module operates in Master receiver mode, the **ACK** bit is normally set, causing the I2C bus controller to transmit an acknowledge automatically after each byte. This bit must be cleared when the I2C bus controller requires no further data to be transmitted from the slave transmitter.

**Read-Only Status Register**

**I2C Master Control/Status (I2CMCS)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
<td>Clock Timeout Error</td>
<td>1</td>
<td>The clock timeout error has occurred.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>CLKTO</td>
<td>RO</td>
<td>0</td>
<td>Clock Timeout Error</td>
</tr>
</tbody>
</table>

**Description**

- **Reserved**: Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
- **Clock Timeout Error**: Value Description
  - 0: No clock timeout error.
  - 1: The clock timeout error has occurred.

This bit is cleared when the master sends a STOP condition or if the I2C master is reset.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>BUSBSY</td>
<td>RO</td>
<td>0</td>
<td>Bus Busy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The (^2)C bus is idle.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The (^2)C bus is busy.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The bit changes based on the START and STOP conditions.</td>
</tr>
<tr>
<td>5</td>
<td>IDLE</td>
<td>RO</td>
<td>1</td>
<td>(^2)C Idle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The (^2)C controller is not idle.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The (^2)C controller is idle.</td>
</tr>
<tr>
<td>4</td>
<td>ARBLST</td>
<td>RO</td>
<td>0</td>
<td>Arbitration Lost</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The (^2)C controller won arbitration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The (^2)C controller lost arbitration.</td>
</tr>
<tr>
<td>3</td>
<td>DATACK</td>
<td>RO</td>
<td>0</td>
<td>Acknowledge Data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The transmitted data was acknowledged</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The transmitted data was not acknowledged.</td>
</tr>
<tr>
<td>2</td>
<td>ADRACK</td>
<td>RO</td>
<td>0</td>
<td>Acknowledge Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The transmitted address was acknowledged</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The transmitted address was not acknowledged.</td>
</tr>
<tr>
<td>1</td>
<td>ERROR</td>
<td>RO</td>
<td>0</td>
<td>Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       No error was detected on the last operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       An error occurred on the last operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The error can be from the slave address not being acknowledged or the transmit data not being acknowledged.</td>
</tr>
<tr>
<td>0</td>
<td>BUSY</td>
<td>RO</td>
<td>0</td>
<td>(^2)C Busy</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The controller is idle.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The controller is busy.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When the BUSY bit is set, the other status bits are not valid.</td>
</tr>
</tbody>
</table>
## Write-Only Control Register

I2C Master Control/Status (I2CMCS)

I2C 0 base: 0x4002.0000
I2C 1 base: 0x4002.1000
I2C 2 base: 0x4002.2000
I2C 3 base: 0x4002.3000
I2C 4 base: 0x400C.0000
I2C 5 base: 0x400C.1000
Offset 0x004
Type WO, reset 0x0000.0020

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:5</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>HS</td>
<td>WO</td>
<td>0</td>
<td>High-Speed Enable</td>
</tr>
<tr>
<td>3</td>
<td>ACK</td>
<td>WO</td>
<td>0</td>
<td>Data Acknowledge Enable</td>
</tr>
<tr>
<td>2</td>
<td>STOP</td>
<td>WO</td>
<td>0</td>
<td>Generate STOP</td>
</tr>
</tbody>
</table>

### High-Speed Enable

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The master operates in Standard, Fast mode, or Fast mode plus as selected by using a value in the I2CMTPR register that results in an SCL frequency of 100 kbps for Standard mode, 400 kbps for Fast mode, or 1 Mpbs for Fast mode plus.</td>
</tr>
<tr>
<td>1</td>
<td>The master operates in High-Speed mode with transmission speeds up to 3.33 Mbps.</td>
</tr>
</tbody>
</table>

### Data Acknowledge Enable

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The received data byte is not acknowledged automatically by the master.</td>
</tr>
<tr>
<td>1</td>
<td>The received data byte is acknowledged automatically by the master. See field decoding in Table 16-5 on page 1044.</td>
</tr>
</tbody>
</table>

### Generate STOP

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The controller does not generate the STOP condition.</td>
</tr>
<tr>
<td>1</td>
<td>The controller generates the STOP condition. See field decoding in Table 16-5 on page 1044.</td>
</tr>
</tbody>
</table>
The controller does not generate the START condition.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The controller does not generate the START condition.</td>
</tr>
<tr>
<td>1</td>
<td>The controller generates the START or repeated START condition. See field decoding in Table 16-5 on page 1044.</td>
</tr>
</tbody>
</table>

The master is able to transmit or receive data.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>This encoding means the master is unable to transmit or receive data.</td>
</tr>
<tr>
<td>1</td>
<td>The master is able to transmit or receive data. See field decoding in Table 16-5 on page 1044.</td>
</tr>
</tbody>
</table>

### Table 16-5. Write Field Decoding for I2CMCS[3:0] Field

<table>
<thead>
<tr>
<th>Current State</th>
<th>I2CMCS[3:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>0, X&lt;sup&gt;0&lt;/sup&gt;, 1, 1</td>
<td>START condition followed by TRANSMIT (master goes to the Master Transmit state).</td>
</tr>
<tr>
<td></td>
<td>0, X, 1, 1</td>
<td>START condition followed by a TRANSMIT and STOP condition (master remains in Idle state).</td>
</tr>
<tr>
<td></td>
<td>1, 0, 0, 1</td>
<td>START condition followed by RECEIVE operation with negative ACK (master goes to the Master Receive state).</td>
</tr>
<tr>
<td></td>
<td>1, 0, 1, 1</td>
<td>START condition followed by RECEIVE and STOP condition (master remains in Idle state).</td>
</tr>
<tr>
<td></td>
<td>1, 1, 0, 1</td>
<td>START condition followed by RECEIVE (master goes to the Master Receive state).</td>
</tr>
<tr>
<td></td>
<td>1, 1, 1, 1</td>
<td>Illegal</td>
</tr>
</tbody>
</table>

All other combinations not listed are non-operations. NOP
### Table 16-5. Write Field Decoding for I2CMCS[3:0] Field (continued)

<table>
<thead>
<tr>
<th>Current State</th>
<th>I2CMSA[0]</th>
<th>I2CMCS[3:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R/S A K</td>
<td>STOP START</td>
<td>RUN</td>
</tr>
<tr>
<td>Master Transmit</td>
<td>X X 0 0 1</td>
<td>1</td>
<td>TRANSMIT operation (master remains in Master Transmit state).</td>
</tr>
<tr>
<td></td>
<td>X X 1 0 0</td>
<td>0</td>
<td>STOP condition (master goes to Idle state).</td>
</tr>
<tr>
<td></td>
<td>X X 1 0 1</td>
<td>1</td>
<td>TRANSMIT followed by STOP condition (master goes to Idle state).</td>
</tr>
<tr>
<td></td>
<td>0 X 0 1 1</td>
<td>1</td>
<td>Repeated START condition followed by a TRANSMIT (master remains in Master Transmit state).</td>
</tr>
<tr>
<td></td>
<td>0 X 1 1 1</td>
<td>1</td>
<td>Repeated START condition followed by a TRANSMIT and STOP condition (master goes to Idle state).</td>
</tr>
<tr>
<td></td>
<td>1 0 0 1 1</td>
<td>1</td>
<td>Repeated START condition followed by a RECEIVE operation with a negative ACK (master goes to Master Receive state).</td>
</tr>
<tr>
<td></td>
<td>1 0 1 1 1</td>
<td>1</td>
<td>Repeated START condition followed by a TRANSMIT and STOP condition (master goes to Idle state).</td>
</tr>
<tr>
<td></td>
<td>1 1 0 1 1</td>
<td>1</td>
<td>Repeated START condition followed by RECEIVE (master goes to Master Receive state).</td>
</tr>
<tr>
<td></td>
<td>1 1 1 1 1</td>
<td>1</td>
<td>Illegal.</td>
</tr>
</tbody>
</table>

All other combinations not listed are non-operations. NOP.

---

| Master Receive | X 0 0 0 1 | 1 | RECEIVE operation with negative ACK (master remains in Master Receive state). |
| X X 1 0 0 | 0 | STOP condition (master goes to Idle state). |
| X 0 1 0 1 | 1 | RECEIVE followed by STOP condition (master goes to Idle state). |
| X 1 0 0 1 | 1 | RECEIVE operation (master remains in Master Receive state). |
| X 1 1 0 1 | 1 | Illegal. |

1. An X in a table cell indicates the bit can be 0 or 1.
2. In Master Receive mode, a STOP condition should be generated only after a Data Negative Acknowledge executed by the master or an Address Negative Acknowledge executed by the slave.
Register 3: I\textsuperscript{2}C Master Data (I2CMDR), offset 0x008

Important: This register is read-sensitive. See the register description for details.

This register contains the data to be transmitted when in the Master Transmit state and the data received when in the Master Receive state.

I\textsuperscript{2}C Master Data (I2CMDR)

I\textsuperscript{2}C 0 base: 0x4002.0000
I\textsuperscript{2}C 1 base: 0x4002.1000
I\textsuperscript{2}C 2 base: 0x4002.2000
I\textsuperscript{2}C 3 base: 0x4002.3000
I\textsuperscript{2}C 4 base: 0x400C.0000
I\textsuperscript{2}C 5 base: 0x400C.1000
Offset 0x008
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>DATA</td>
<td>RW</td>
<td>0x00</td>
<td>This byte contains the data transferred during a transaction.</td>
</tr>
</tbody>
</table>
Register 4: I²C Master Timer Period (I2CMTPR), offset 0x00C

This register is programmed to set the timer period for the SCL clock and assign the SCL clock to either standard or high-speed mode.

### I²C Master Timer Period (I2CMTPR)

- **I²C 0 base:** 0x4002.0000
- **I²C 1 base:** 0x4002.1000
- **I²C 2 base:** 0x4002.2000
- **I²C 3 base:** 0x4002.3000
- **I²C 4 base:** 0x400C.0000
- **I²C 5 base:** 0x400C.1000

**Offset 0x00C**
- **Type RW, reset 0x0000.0001**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>HS</td>
<td>WO</td>
<td>0x0</td>
<td>High-Speed Enable</td>
</tr>
<tr>
<td>6:0</td>
<td>TPR</td>
<td>RW</td>
<td>0x1</td>
<td>Timer Period</td>
</tr>
</tbody>
</table>

This field is used in the equation to configure \( SCL\_PERIOD \):

\[
SCL\_PERIOD = 2 \times (1 + TPR) \times (SCL\_LP + SCL\_HP) \times CLK\_PRD
\]

where:
- \( SCL\_PRD \) is the SCL line period (I²C clock).
- \( TPR \) is the Timer Period register value (range of 1 to 127).
- \( SCL\_LP \) is the SCL Low period (fixed at 6).
- \( SCL\_HP \) is the SCL High period (fixed at 6).
- \( CLK\_PRD \) is the system clock period in ns.
Register 5: I2C Master Interrupt Mask (I2CMIMR), offset 0x010

This register controls whether a raw interrupt is promoted to a controller interrupt.

### I2C Master Interrupt Mask (I2CMIMR)

| I2C 0 base: 0x4002.0000 |
| I2C 1 base: 0x4002.1000 |
| I2C 2 base: 0x4002.2000 |
| I2C 3 base: 0x4002.3000 |
| I2C 4 base: 0x400C.0000 |
| I2C 5 base: 0x400C.1000 |

Offset 0x010
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>CLKIM</td>
<td>RW</td>
<td>0</td>
<td>Clock Timeout Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The <strong>CLKRIS</strong> interrupt is suppressed and not sent to the interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The clock timeout interrupt is sent to the interrupt controller when the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>CLKRIS</strong> bit in the <strong>I2CMRIS</strong> register is set.</td>
</tr>
<tr>
<td>0</td>
<td>IM</td>
<td>RW</td>
<td>0</td>
<td>Master Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The <strong>RIS</strong> interrupt is suppressed and not sent to the interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The master interrupt is sent to the interrupt controller when the <strong>RIS</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>bit in the <strong>I2CMRIS</strong> register is set.</td>
</tr>
</tbody>
</table>
Register 6: I²C Master Raw Interrupt Status (I2CMRIS), offset 0x014

This register specifies whether an interrupt is pending.

I²C Master Raw Interrupt Status (I2CMRIS)

| I²C 0 base: 0x4002.0000 |
| I²C 1 base: 0x4002.1000 |
| I²C 2 base: 0x4002.2000 |
| I²C 3 base: 0x4002.3000 |
| I²C 4 base: 0x400C.0000 |
| I²C 5 base: 0x400C.1000 |

Offset 0x014
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>CLKRIS</td>
<td>RO</td>
<td>0</td>
<td>Clock Timeout Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The clock timeout interrupt is pending.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the CLKIC bit in the I2CMICR register.</td>
</tr>
<tr>
<td>0</td>
<td>RIS</td>
<td>RO</td>
<td>0</td>
<td>Master Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A master interrupt is pending.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the iC bit in the I2CMICR register.</td>
</tr>
</tbody>
</table>
Register 7: I2C Master Masked Interrupt Status (I2CMMIS), offset 0x018

This register specifies whether an interrupt was signaled.

### I2C Master Masked Interrupt Status (I2CMMIS)

| I2C 0 base: 0x4002.0000 |
| I2C 1 base: 0x4002.1000 |
| I2C 2 base: 0x4002.2000 |
| I2C 3 base: 0x4002.3000 |
| I2C 4 base: 0x400C.0000 |
| I2C 5 base: 0x400C.1000 |
| Offset 0x018 |
| Type RO, reset 0x0000.0000 |

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>An unmasked clock timeout interrupt was signaled and is pending.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>This bit is cleared by writing a 1 to the CLKIC bit in the I2CMICR register.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>An unmasked master interrupt was signaled and is pending.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>This bit is cleared by writing a 1 to the IC bit in the I2CMICR register.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>CLKMIS</td>
<td>RO</td>
<td>0</td>
<td>Clock Timeout Masked Interrupt Status</td>
</tr>
<tr>
<td>0</td>
<td>MIS</td>
<td>RO</td>
<td>0</td>
<td>Masked Interrupt Status</td>
</tr>
</tbody>
</table>

**Value**

- **Description**
  - **0** No interrupt.
  - **1** An unmasked clock timeout interrupt was signaled and is pending.

**Value**

- **Description**
  - **0** An interrupt has not occurred or is masked.
  - **1** An unmasked master interrupt was signaled and is pending.

**Value**

- **Description**
  - **0** No interrupt.
  - **1** An unmasked clock timeout interrupt was signaled and is pending.

**Value**

- **Description**
  - **0** An interrupt has not occurred or is masked.
  - **1** An unmasked master interrupt was signaled and is pending.
Register 8: I²C Master Interrupt Clear (I2CMICR), offset 0x01C

This register clears the raw and masked interrupts.

I²C Master Interrupt Clear (I2CMICR)

I²C 0 base: 0x4002.0000
I²C 1 base: 0x4002.1000
I²C 2 base: 0x4002.2000
I²C 3 base: 0x4002.3000
I²C 4 base: 0x400C.0000
I²C 5 base: 0x400C.1000
Offset 0x01C
Type WO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>CLKIC</td>
<td>WO</td>
<td>0</td>
<td>Clock Timeout Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the CLKRIS bit in the I2CMRIS register and the CLKMIS bit in the I2CMMIS register. A read of this register returns no meaningful data.</td>
</tr>
<tr>
<td>0</td>
<td>IC</td>
<td>WO</td>
<td>0</td>
<td>Master Interrupt Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the RIS bit in the I2CMRIS register and the MIS bit in the I2CMMIS register. A read of this register returns no meaningful data.</td>
</tr>
</tbody>
</table>
Register 9: I²C Master Configuration (I2CMCR), offset 0x020

This register configures the mode (Master or Slave), enables the glitch filter, and sets the interface for test mode loopback.

I²C Master Configuration (I2CMCR)
I2C 0 base: 0x4002.0000
I2C 1 base: 0x4002.1000
I2C 2 base: 0x4002.2000
I2C 3 base: 0x4002.3000
I2C 4 base: 0x400C.0000
I2C 5 base: 0x400C.1000
Offset 0x020
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:7</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6</td>
<td>GFE</td>
<td>RW</td>
<td>0</td>
<td>I²C Glitch Filter Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  I²C glitch filter is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  I²C glitch filter is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Use the GFPW bit in the I²C Master Configuration 2 (I2CMCR2) register to program the pulse width.</td>
</tr>
<tr>
<td>5</td>
<td>SFE</td>
<td>RW</td>
<td>0</td>
<td>I²C Slave Function Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Slave mode is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Slave mode is enabled.</td>
</tr>
<tr>
<td>4</td>
<td>MFE</td>
<td>RW</td>
<td>0</td>
<td>I²C Master Function Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  Master mode is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Master mode is enabled.</td>
</tr>
<tr>
<td>3:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>LPBK</td>
<td>RW</td>
<td>0</td>
<td>(\text{I}^2\text{C}) Loopback</td>
</tr>
</tbody>
</table>

**Value**  **Description**

| 0 | Normal operation. |
| 1 | The controller in a test mode loopback configuration. |
**Register 10: I²C Master Clock Low Timeout Count (I2CMCLKOCNT), offset 0x024**

This register contains the upper 8 bits of a 12-bit counter that can be used to keep the timeout limit for clock stretching by a remote slave. The lower four bits of the counter are not user visible and are always 0x0.

**Note:** The Master Clock Low Timeout counter counts for the entire time SCL is held Low continuously. If SCL is deasserted at any point, the Master Clock Low Timeout Counter is reloaded with the value in the I2CMCLKOCNT register and begins counting down from this value.

I²C Master Clock Low Timeout Count (I2CMCLKOCNT)

| I²C 0 base: 0x4002.0000 |
| I²C 1 base: 0x4002.1000 |
| I²C 2 base: 0x4002.2000 |
| I²C 3 base: 0x4002.3000 |
| I²C 4 base: 0x400C.0000 |
| I²C 5 base: 0x400C.1000 |
| Offset 0x024 |
| Type RW, reset 0x0000.0000 |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>CNTL</td>
<td>RW</td>
<td>0</td>
<td>I²C Master Count&lt;br&gt;This field contains the upper 8 bits of a 12-bit counter for the clock low timeout count. <strong>Note:</strong> The value of CNTL must be greater than 0x1.</td>
</tr>
</tbody>
</table>
Register 11: I²C Master Bus Monitor (I2CMBMON), offset 0x02C

This register is used to determine the SCL and SDA signal status.

I²C Master Bus Monitor (I2CMBMON)

I²C 0 base: 0x4002.0000
I²C 1 base: 0x4002.1000
I²C 2 base: 0x4002.2000
I²C 3 base: 0x4002.3000
I²C 4 base: 0x400C.0000
I²C 5 base: 0x400C.1000
Offset 0x02C
Type RO, reset 0x0000.0003

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>SDA</td>
<td>RO</td>
<td>1</td>
<td>I²C SDA Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The I2CSDA signal is low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The I2CSDA signal is high.</td>
</tr>
<tr>
<td>0</td>
<td>SCL</td>
<td>RO</td>
<td>1</td>
<td>I²C SCL Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The I2CSCCL signal is low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The I2CSCCL signal is high.</td>
</tr>
</tbody>
</table>
Register 12: \textit{I}^{2}\textit{C} Master Configuration 2 (\textit{I}^{2}\textit{CMCR2}), offset 0x038

This register can be programmed to select the pulse width for glitch suppression, measured in system clocks.

\textbf{\textit{I}^{2}\textit{C} Master Configuration 2 (\textit{I}^{2}\textit{CMCR2})}

\begin{itemize}
  \item \textit{I}^{2}\textit{C} 0 base: 0x4002.0000
  \item \textit{I}^{2}\textit{C} 1 base: 0x4002.1000
  \item \textit{I}^{2}\textit{C} 2 base: 0x4002.2000
  \item \textit{I}^{2}\textit{C} 3 base: 0x4002.3000
  \item \textit{I}^{2}\textit{C} 4 base: 0x400C.0000
  \item \textit{I}^{2}\textit{C} 5 base: 0x400C.1000
\end{itemize}

\textbf{Offset 0x038}

Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6:4</td>
<td>GFPW</td>
<td>RW</td>
<td>0</td>
<td>\textit{I}^{2}\textit{C} Glitch Filter Pulse Width</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field controls the pulse width select for glitch suppression on the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SCL and SDA lines. Glitch suppression values can be programmed relative to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>system clocks.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Bypass</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 1 clock</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 2 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 3 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x4 4 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x5 8 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x6 16 clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x7 31 clocks</td>
</tr>
<tr>
<td>3:0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

16.7 Register Descriptions (\textit{I}^{2}\textit{C} Slave)

The remainder of this section lists and describes the \textit{I}^{2}\textit{C} slave registers, in numerical order by address offset.
Register 13: I2C Slave Own Address (I2CSOAR), offset 0x800

This register consists of seven address bits that identify the TM4C123GH6PZ I2C device on the I2C bus.

I2C Slave Own Address (I2CSOAR)
I2C 0 base: 0x4002.0000
I2C 1 base: 0x4002.1000
I2C 2 base: 0x4002.2000
I2C 3 base: 0x4002.3000
I2C 4 base: 0x400C.0000
I2C 5 base: 0x400C.1000
Offset 0x800
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:7</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6:0</td>
<td>OAR</td>
<td>RW</td>
<td>0x00</td>
<td>I2C Slave Own Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field specifies bits A6 through A0 of the slave address.</td>
</tr>
</tbody>
</table>
Register 14: I²C Slave Control/Status (I2CSCSR), offset 0x804
This register functions as a control register when written, and a status register when read.

Read-Only Status Register

I²C Slave Control/Status (I2CSCSR)
I²C 0 base: 0x4002.0000
I²C 1 base: 0x4002.1000
I²C 2 base: 0x4002.2000
I²C 3 base: 0x4002.3000
I²C 4 base: 0x400C.0000
I²C 5 base: 0x400C.1000
Offset 0x804
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>OAR2SEL</td>
<td>RO</td>
<td>0</td>
<td>OAR2 Address Matched</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Either the address is not matched or the match is in legacy mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 OAR2 address matched and ACKed by the slave.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit gets reevaluated after every address comparison.</td>
</tr>
<tr>
<td>2</td>
<td>FBR</td>
<td>RO</td>
<td>0</td>
<td>First Byte Received</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The first byte has not been received.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The first byte following the slave’s own address has been received.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is only valid when the RREQ bit is set and is automatically cleared when data has been read from the I2CSDR register.</td>
</tr>
</tbody>
</table>

Note: This bit is not used for slave transmit operations.
Transmit Request

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TREQ</td>
<td>RO</td>
<td>0</td>
<td>Transmit Request</td>
</tr>
</tbody>
</table>

Value | Description  
---|-------------|
0 | No outstanding transmit request.  
1 | The \( \text{I}^2\text{C} \) controller has been addressed as a slave transmitter and is using clock stretching to delay the master until data has been written to the I2CSDR register.

Receive Request

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RREQ</td>
<td>RO</td>
<td>0</td>
<td>Receive Request</td>
</tr>
</tbody>
</table>

Value | Description  
---|-------------|
0 | No outstanding receive data.  
1 | The \( \text{I}^2\text{C} \) controller has outstanding receive data from the \( \text{I}^2\text{C} \) master and is using clock stretching to delay the master until the data has been read from the I2CSDR register.

Write-Only Control Register

I2C Slave Control/Status (I2CSCSR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 31:1| reserved | RO   | 0x0000.0000 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.  
0 | DA | WO | 0 | Device Active |

Value | Description  
---|-------------|
0 | Disables the \( \text{I}^2\text{C} \) slave operation.  
1 | Enables the \( \text{I}^2\text{C} \) slave operation.  

Once this bit has been set, it should not be set again unless it has been cleared by writing a 0 or by a reset, otherwise transfer failures may occur.
Register 15: I²C Slave Data (I2CSDR), offset 0x808

**Important:** This register is read-sensitive. See the register description for details.

This register contains the data to be transmitted when in the Slave Transmit state, and the data received when in the Slave Receive state.

### I2C Slave Data (I2CSDR)

<table>
<thead>
<tr>
<th>Base Address</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C 0 base: 0x4002.0000</td>
<td>0x808</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>I2C 1 base: 0x4002.1000</td>
<td>0x808</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Data for Transfer</td>
</tr>
</tbody>
</table>

#### Bit/Field

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7:0</td>
<td>DATA</td>
<td>RW</td>
<td>0x0000.00</td>
<td>Data for Transfer</td>
</tr>
</tbody>
</table>

**Texas Instruments-Production Data**
Register 16: I²C Slave Interrupt Mask (I2CSIMR), offset 0x80C

This register controls whether a raw interrupt is promoted to a controller interrupt.

I²C Slave Interrupt Mask (I2CSIMR)
I²C 0 base: 0x4002.0000
I²C 1 base: 0x4002.1000
I²C 2 base: 0x4002.2000
I²C 3 base: 0x4002.3000
I²C 4 base: 0x400C.0000
I²C 5 base: 0x400C.1000
Offset 0x80C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>STOPIM</td>
<td>RW</td>
<td>0</td>
<td>Stop Condition Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>STOPRIS interrupt is suppressed and not sent to the interrupt controller.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The STOP condition interrupt is sent to the interrupt controller when the STOPRIS bit in the I2CSRIS register is set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>STARTIM</td>
<td>RW</td>
<td>0</td>
<td>Start Condition Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The STARTRIS interrupt is suppressed and not sent to the interrupt controller.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The START condition interrupt is sent to the interrupt controller when the STARTRIS bit in the I2CSRIS register is set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>DATAIM</td>
<td>RW</td>
<td>0</td>
<td>Data Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The DATARIS interrupt is suppressed and not sent to the interrupt controller.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The data received or data requested interrupt is sent to the interrupt controller when the DATARIS bit in the I2CSRIS register is set.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 17: I²C Slave Raw Interrupt Status (I2CSRIS), offset 0x810

This register specifies whether an interrupt is pending.

I²C Slave Raw Interrupt Status (I2CSRIS)

I²C 0 base: 0x4002.0000
I²C 1 base: 0x4002.1000
I²C 2 base: 0x4002.2000
I²C 3 base: 0x4002.3000
I²C 4 base: 0x400C.0000
I²C 5 base: 0x400C.1000
Offset 0x810
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>STOPRIS</td>
<td>RO</td>
<td>0</td>
<td>Stop Condition Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A STOP condition interrupt is pending.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the STOPIC bit in the I2CSICR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>1</td>
<td>STARTRIS</td>
<td>RO</td>
<td>0</td>
<td>Start Condition Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A START condition interrupt is pending.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the STARTIC bit in the I2CSICR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>0</td>
<td>DATARIS</td>
<td>RO</td>
<td>0</td>
<td>Data Raw Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A data received or data requested interrupt is pending.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the DATAIC bit in the I2CSICR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
</tbody>
</table>
Register 18: I²C Slave Masked Interrupt Status (I2CSMIS), offset 0x814

This register specifies whether an interrupt was signaled.

I²C Slave Masked Interrupt Status (I2CSMIS)

<table>
<thead>
<tr>
<th>Offset 0x814</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RO, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>STOPMIS</td>
<td>RO</td>
<td>0</td>
<td>Stop Condition Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked STOP condition interrupt was signaled is pending.</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to the STOPIC bit in the I2CSICR register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>STARTMIS</td>
<td>RO</td>
<td>0</td>
<td>Start Condition Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked START condition interrupt was signaled is pending.</td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to the STARTIC bit in the I2CSICR register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>DATAMIS</td>
<td>RO</td>
<td>0</td>
<td>Data Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td>0 An interrupt has not occurred or is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An unmasked data received or data requested interrupt was signaled is pending.</td>
</tr>
</tbody>
</table>
Register 19: I²C Slave Interrupt Clear (I2CSICR), offset 0x818

This register clears the raw interrupt. A read of this register returns no meaningful data.

I²C Slave Interrupt Clear (I2CSICR)
I²C 0 base: 0x4002.0000
I²C 1 base: 0x4002.1000
I²C 2 base: 0x4002.2000
I²C 3 base: 0x4002.3000
I²C 4 base: 0x400C.0000
I²C 5 base: 0x400C.1000
Offset 0x818
Type WO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>STOPIC</td>
<td>WO</td>
<td>0</td>
<td>Stop Condition Interrupt Clear writing a 1 to this bit clears the STOPRIS bit in the I2CSRIS register and the STOPMIS bit in the I2CSMIS register. A read of this register returns no meaningful data.</td>
</tr>
<tr>
<td>1</td>
<td>STARTIC</td>
<td>WO</td>
<td>0</td>
<td>Start Condition Interrupt Clear writing a 1 to this bit clears the STARTRIS bit in the I2CSRIS register and the STARTMIS bit in the I2CSMIS register. A read of this register returns no meaningful data.</td>
</tr>
<tr>
<td>0</td>
<td>DATAIC</td>
<td>WO</td>
<td>0</td>
<td>Data Interrupt Clear writing a 1 to this bit clears the STOPRIS bit in the I2CSRIS register and the STOPMIS bit in the I2CSMIS register. A read of this register returns no meaningful data.</td>
</tr>
</tbody>
</table>
# Register 20: I²C Slave Own Address 2 (I2CSOAR2), offset 0x81C

This register consists of seven address bits that identify the alternate address for the I²C device on the I²C bus.

## I²C Slave Own Address 2 (I2CSOAR2)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset 0x81C</th>
</tr>
</thead>
<tbody>
<tr>
<td>I²C 0</td>
<td>0x4002.0000</td>
</tr>
<tr>
<td>I²C 1</td>
<td>0x4002.1000</td>
</tr>
<tr>
<td>I²C 2</td>
<td>0x4002.2000</td>
</tr>
<tr>
<td>I²C 3</td>
<td>0x4002.3000</td>
</tr>
<tr>
<td>I²C 4</td>
<td>0x400C.0000</td>
</tr>
<tr>
<td>I²C 5</td>
<td>0x400C.1000</td>
</tr>
</tbody>
</table>

Offset 0x81C

### Bit/Field | Name | Type | Reset | Description
--- | --- | --- | --- | ---
31:0 | reserved | RO | 0x0000.00 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
7 | OAR2EN | RW | 0 | I²C Slave Own Address 2 Enable
<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The alternate address is disabled.</td>
</tr>
<tr>
<td>1</td>
<td>Enables the use of the alternate address in the OAR2 field.</td>
</tr>
</tbody>
</table>
6:0 | OAR2 | RW | 0x00 | I²C Slave Own Address 2
This field specifies the alternate OAR2 address.
Register 21: \(\text{I}^2\text{C}\) Slave ACK Control (I2CSACKCTL), offset 0x820

This register enables the \(\text{I}^2\text{C}\) slave to NACK for invalid data or command or ACK for valid data or command. The \(\text{I}^2\text{C}\) clock is pulled low after the last data bit until this register is written.

I2C Slave ACK Control (I2CSACKCTL)

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>1</td>
<td>ACKOVAL</td>
<td>RW</td>
<td>0</td>
<td>(\text{I}^2\text{C}) Slave ACK Override Value</td>
</tr>
<tr>
<td>0</td>
<td>ACKOEN</td>
<td>RW</td>
<td>0</td>
<td>(\text{I}^2\text{C}) Slave ACK Override Enable</td>
</tr>
</tbody>
</table>

16.8 Register Descriptions (\(\text{I}^2\text{C}\) Status and Control)

The remainder of this section lists and describes the \(\text{I}^2\text{C}\) status and control registers, in numerical order by address offset.
Register 22: \( \text{i}^2\text{C} \) Peripheral Properties (I2CPP), offset 0xFC0

The I2CPP register provides information regarding the properties of the \( \text{i}^2\text{C} \) module.

### I2C Peripheral Properties (I2CPP)

<table>
<thead>
<tr>
<th>Base Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C 0 base: 0x4002.0000</td>
</tr>
<tr>
<td>I2C 1 base: 0x4002.1000</td>
</tr>
<tr>
<td>I2C 2 base: 0x4002.2000</td>
</tr>
<tr>
<td>I2C 3 base: 0x4002.3000</td>
</tr>
<tr>
<td>I2C 4 base: 0x400C.0000</td>
</tr>
<tr>
<td>I2C 5 base: 0x400C.1000</td>
</tr>
</tbody>
</table>

Offset (0xFC0)

Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>HS</td>
<td>RO</td>
<td>0x1</td>
<td>High-Speed Capable</td>
</tr>
</tbody>
</table>

  Value Description

  0    The interface is capable of Standard, Fast, or Fast mode plus operation.

  1    The interface is capable of High-Speed operation.
Register 23: \(I^2C\) Peripheral Configuration (I2CPC), offset 0xFC4

The I2CPC register allows software to enable features present in the \(I^2C\) module.

### I2C Peripheral Configuration (I2CPC)

| I2C 0 base: 0x4002.0000 |
| I2C 1 base: 0x4002.1000 |
| I2C 2 base: 0x4002.2000 |
| I2C 3 base: 0x4002.3000 |
| I2C 4 base: 0x400C.0000 |
| I2C 5 base: 0x400C.1000 |

Offset 0xFC4

Type RO, reset 0x0000.0001

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>HS</td>
<td>RW</td>
<td>1</td>
<td>High-Speed Capable</td>
</tr>
</tbody>
</table>

- **Value Description**
  - 0: The interface is set to Standard, Fast or Fast mode plus operation.
  - 1: The interface is set to High-Speed operation. Note that this encoding may only be used if the HS bit in the I2CPP register is set. Otherwise, this encoding is not available.
17 Controller Area Network (CAN) Module

Controller Area Network (CAN) is a multicast, shared serial bus standard for connecting electronic control units (ECUs). CAN was specifically designed to be robust in electromagnetically-noisy environments and can utilize a differential balanced line like RS-485 or a more robust twisted-pair wire. Originally created for automotive purposes, it is also used in many embedded control applications (such as industrial and medical). Bit rates up to 1 Mbps are possible at network lengths less than 40 meters. Decreased bit rates allow longer network distances (for example, 125 Kbps at 500 meters).

The TM4C123GH6PZ microcontroller includes two CAN units with the following features:

- CAN protocol version 2.0 part A/B
- Bit rates up to 1 Mbps
- 32 message objects with individual identifier masks
- Maskable interrupt
- Disable Automatic Retransmission mode for Time-Triggered CAN (TTCAN) applications
- Programmable loopback mode for self-test operation
- Programmable FIFO mode enables storage of multiple message objects
- Gluelessly attaches to an external CAN transceiver through the CANnTX and CANnRX signals
17.1 Block Diagram

Figure 17-1. CAN Controller Block Diagram

17.2 Signal Description

The following table lists the external signals of the CAN controller and describes the function of each. The CAN controller signals are alternate functions for some GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for the CAN signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the CAN controller function. The number in parentheses is the encoding that must be programmed into the PMCn field in the GPIO Port Control (GPIOPCTL) register (page 702) to assign the CAN signal to the specified GPIO port pin. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 659.
Table 17-1. Controller Area Network Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type*</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN0Rx</td>
<td>40 92 95</td>
<td>PF0 (3) PB4 (8) PE4 (8)</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 0 receive.</td>
</tr>
<tr>
<td>CAN0Tx</td>
<td>43 91 96</td>
<td>PF3 (3) PB5 (8) PE5 (8)</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 0 transmit.</td>
</tr>
<tr>
<td>CAN1Rx</td>
<td>26 89</td>
<td>PA0 (8) PE6 (8)</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 1 receive.</td>
</tr>
<tr>
<td>CAN1Tx</td>
<td>27 90</td>
<td>PA1 (8) PE7 (8)</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 1 transmit.</td>
</tr>
</tbody>
</table>

* The TTL designation indicates the pin has TTL-compatible voltage levels.

17.3 Functional Description

The TM4C123GH6PZ CAN controller conforms to the CAN protocol version 2.0 (parts A and B). Message transfers that include data, remote, error, and overload frames with an 11-bit identifier (standard) or a 29-bit identifier (extended) are supported. Transfer rates can be programmed up to 1 Mbps.

The CAN module consists of three major parts:

- CAN protocol controller and message handler
- Message memory
- CAN register interface

A data frame contains data for transmission, whereas a remote frame contains no data and is used to request the transmission of a specific message object. The CAN data/remote frame is constructed as shown in Figure 17-2.
The protocol controller transfers and receives the serial data from the CAN bus and passes the data on to the message handler. The message handler then loads this information into the appropriate message object based on the current filtering and identifiers in the message object memory. The message handler is also responsible for generating interrupts based on events on the CAN bus.

The message object memory is a set of 32 identical memory blocks that hold the current configuration, status, and actual data for each message object. These memory blocks are accessed via either of the CAN message object register interfaces.

The message memory is not directly accessible in the TM4C123GH6PZ memory map, so the TM4C123GH6PZ CAN controller provides an interface to communicate with the message memory via two CAN interface register sets for communicating with the message objects. These two interfaces must be used to read or write to each message object. The two message object interfaces allow parallel access to the CAN controller message objects when multiple objects may have new information that must be processed. In general, one interface is used for transmit data and one for receive data.

17.3.1 Initialization

To use the CAN controller, the peripheral clock must be enabled using the RCGC0 register (see page 461). In addition, the clock to the appropriate GPIO module must be enabled via the RCGC2 register (see page 469). To find out which GPIO port to enable, refer to Table 23-4 on page 1377. Set the GPIO AFSEL bits for the appropriate pins (see page 684). Configure the PMCn fields in the GPIOPCTL register to assign the CAN signals to the appropriate pins. See page 702 and Table 23-5 on page 1386.

Software initialization is started by setting the INIT bit in the CAN Control (CANCTL) register (with software or by a hardware reset) or by going bus-off, which occurs when the transmitter's error counter exceeds a count of 255. While INIT is set, all message transfers to and from the CAN bus are stopped and the CANnTX signal is held High. Entering the initialization state does not change the configuration of the CAN controller, the message objects, or the error counters. However, some configuration registers are only accessible while in the initialization state.
To initialize the CAN controller, set the CAN Bit Timing (CANBIT) register and configure each message object. If a message object is not needed, label it as not valid by clearing the MSGVAL bit in the CANIFn Arbitration 2 (CANIFnARB2) register. Otherwise, the whole message object must be initialized, as the fields of the message object may not have valid information, causing unexpected results. Both the INIT and CCE bits in the CANCTL register must be set in order to access the CANBIT register and the CAN Baud Rate Prescaler Extension (CANBRPE) register to configure the bit timing. To leave the initialization state, the INIT bit must be cleared. Afterwards, the internal Bit Stream Processor (BSP) synchronizes itself to the data transfer on the CAN bus by waiting for the occurrence of a sequence of 11 consecutive recessive bits (indicating a bus idle condition) before it takes part in bus activities and starts message transfers. Message object initialization does not require the CAN to be in the initialization state and can be done on the fly. However, message objects should all be configured to particular identifiers or set to not valid before message transfer starts. To change the configuration of a message object during normal operation, clear the MSGVAL bit in the CANIFnARB2 register to indicate that the message object is not valid during the change. When the configuration is completed, set the MSGVAL bit again to indicate that the message object is once again valid.

17.3.2 Operation

Two sets of CAN Interface Registers (CANIF1x and CANIF2x) are used to access the message objects in the Message RAM. The CAN controller coordinates transfers to and from the Message RAM to and from the registers. The two sets are independent and identical and can be used to queue transactions. Generally, one interface is used to transmit data and one is used to receive data.

Once the CAN module is initialized and the INIT bit in the CANCTL register is cleared, the CAN module synchronizes itself to the CAN bus and starts the message transfer. As each message is received, it goes through the message handler’s filtering process, and if it passes through the filter, is stored in the message object specified by the MNUM bit in the CANIFn Command Request (CANIFnCRQ) register. The whole message (including all arbitration bits, data-length code, and eight data bytes) is stored in the message object. If the Identifier Mask (the MSK bits in the CANIFn Mask 1 and CANIFn Mask 2 (CANIFnMSKn) registers) is used, the arbitration bits that are masked to “don’t care” may be overwritten in the message object.

The CPU may read or write each message at any time via the CAN Interface Registers. The message handler guarantees data consistency in case of concurrent accesses.

The transmission of message objects is under the control of the software that is managing the CAN hardware. Message objects can be used for one-time data transfers or can be permanent message objects used to respond in a more periodic manner. Permanent message objects have all arbitration and control set up, and only the data bytes are updated. At the start of transmission, the appropriate TXRQST bit in the CAN Transmission Request n (CANTXRQn) register and the NEWDAT bit in the CAN New Data n (CANNWDAn) register are set. If several transmit messages are assigned to the same message object (when the number of message objects is not sufficient), the whole message object has to be configured before the transmission of this message is requested.

The transmission of any number of message objects may be requested at the same time; they are transmitted according to their internal priority, which is based on the message identifier (MNUM) for the message object, with 1 being the highest priority and 32 being the lowest priority. Messages may be updated or set to not valid any time, even when their requested transmission is still pending. The old data is discarded when a message is updated before its pending transmission has started. Depending on the configuration of the message object, the transmission of a message may be requested autonomously by the reception of a remote frame with a matching identifier.
Transmission can be automatically started by the reception of a matching remote frame. To enable this mode, set the RMTEN bit in the CANIFn Message Control (CANIFnMCTL) register. A matching received remote frame causes the TXRQST bit to be set, and the message object automatically transfers its data or generates an interrupt indicating a remote frame was requested. A remote frame can be strictly a single message identifier, or it can be a range of values specified in the message object. The CAN mask registers, CANIFnMSKn, configure which groups of frames are identified as remote frame requests. The UMASK bit in the CANIFnMCTL register enables the MSK bits in the CANIFnMSKn register to filter which frames are identified as a remote frame request. The MXTD bit in the CANIFnMSK2 register should be set if a remote frame request is expected to be triggered by 29-bit extended identifiers.

17.3.3 Transmitting Message Objects

If the internal transmit shift register of the CAN module is ready for loading, and if a data transfer is not occurring between the CAN Interface Registers and message RAM, the valid message object with the highest priority that has a pending transmission request is loaded into the transmit shift register by the message handler and the transmission is started. The message object’s NEWDAT bit in the CANNWDAn register is cleared. After a successful transmission, and if no new data was written to the message object since the start of the transmission, the TXRQST bit in the CANTXRQn register is cleared. If the CAN controller is configured to interrupt on a successful transmission of a message object, (the TXIE bit in the CANIFn Message Control (CANIFnMCTL) register is set), the INTPND bit in the CANIFnMCTL register is set after a successful transmission. If the CAN module has lost the arbitration or if an error occurred during the transmission, the message is re-transmitted as soon as the CAN bus is free again. If, meanwhile, the transmission of a message with higher priority has been requested, the messages are transmitted in the order of their priority.

17.3.4 Configuring a Transmit Message Object

The following steps illustrate how to configure a transmit message object.

1. In the CANIFn Command Mask (CANIFnCMASK) register:
   - Set the WRNRD bit to specify a write to the CANIFnCMASK register; specify whether to transfer the IDMASK, DIR, and MXTD of the message object into the CANIFn registers using the MASK bit
   - Specify whether to transfer the ID, DIR, XTD, and MSGVAL of the message object into the interface registers using the ARB bit
   - Specify whether to transfer the control bits into the interface registers using the CONTROL bit
   - Specify whether to clear the INTFND bit in the CANIFnMCTL register using the CLRINTFND bit
   - Specify whether to clear the NEWDAT bit in the CANNWDAn register using the NEWDAT bit
   - Specify which bits to transfer using the DATAA and DATAB bits

2. In the CANIFnMSK1 register, use the MSK[15:0] bits to specify which of the bits in the 29-bit or 11-bit message identifier are used for acceptance filtering. Note that MSK[15:0] in this register are used for bits [15:0] of the 29-bit message identifier and are not used for an 11-bit identifier. A value of 0x00 enables all messages to pass through the acceptance filtering. Also
note that in order for these bits to be used for acceptance filtering, they must be enabled by setting the UMASK bit in the CANIFnMCTL register.

3. In the CANIFnMSK2 register, use the MSK[12:0] bits to specify which of the bits in the 29-bit or 11-bit message identifier are used for acceptance filtering. Note that MSK[12:0] are used for bits [28:16] of the 29-bit message identifier, whereas MSK[12:2] are used for bits [10:0] of the 11-bit message identifier. Use the MXTD and MDIR bits to specify whether to use XTD and DIR for acceptance filtering. A value of 0x00 enables all messages to pass through the acceptance filtering. Also note that in order for these bits to be used for acceptance filtering, they must be enabled by setting the UMASK bit in the CANIFnMCTL register.

4. For a 29-bit identifier, configure ID[15:0] in the CANIFnARB1 register for bits [15:0] of the message identifier and ID[12:0] in the CANIFnARB2 register for bits [28:16] of the message identifier. Set the XTD bit to indicate an extended identifier; set the DIR bit to indicate transmit; and set the MSGVAL bit to indicate that the message object is valid.

5. For an 11-bit identifier, disregard the CANIFnARB1 register and configure ID[12:2] in the CANIFnARB2 register for bits [10:0] of the message identifier. Clear the XTD bit to indicate a standard identifier; set the DIR bit to indicate transmit; and set the MSGVAL bit to indicate that the message object is valid.

6. In the CANIFnMCTL register:
   - Optionally set the UMASK bit to enable the mask (MSK, MXTD, and MDIR specified in the CANIFnMSK1 and CANIFnMSK2 registers) for acceptance filtering
   - Optionally set the TXIE bit to enable the INTPND bit to be set after a successful transmission
   - Optionally set the RMTEN bit to enable the TXRQST bit to be set on the reception of a matching remote frame allowing automatic transmission
   - Set the EOB bit for a single message object
   - Configure the DLC[3:0] field to specify the size of the data frame. Take care during this configuration not to set the NEWDAT, MSGLST, INTPND or TXRQST bits.

7. Load the data to be transmitted into the CANIFn Data (CANIFnDA1, CANIFnDA2, CANIFnDB1, CANIFnDB2) registers. Byte 0 of the CAN data frame is stored in DATA[7:0] in the CANIFnDA1 register.

8. Program the number of the message object to be transmitted in the MNUM field in the CANIFn Command Request (CANIFnCRQ) register.

9. When everything is properly configured, set the TXRQST bit in the CANIFnMCTL register. Once this bit is set, the message object is available to be transmitted, depending on priority and bus availability. Note that setting the RMTEN bit in the CANIFnMCTL register can also start message transmission if a matching remote frame has been received.

17.3.5 Updating a Transmit Message Object
The CPU may update the data bytes of a Transmit Message Object any time via the CAN Interface Registers and neither the MSGVAL bit in the CANIFnARB2 register nor the TXRQST bits in the CANIFnMCTL register have to be cleared before the update.
Even if only some of the data bytes are to be updated, all four bytes of the corresponding CANIFnDAn/CANIFnDBn register have to be valid before the content of that register is transferred to the message object. Either the CPU must write all four bytes into the CANIFnDAn/CANIFnDBn register or the message object is transferred to the CANIFnDAn/CANIFnDBn register before the CPU writes the new data bytes.

In order to only update the data in a message object, the WRNRD, DATAA and DATAB bits in the CANIFnMSKn register are set, followed by writing the updated data into CANIFnDA1, CANIFnDA2, CANIFnDB1, and CANIFnDB2 registers, and then the number of the message object is written to the MNUM field in the CANIFn Command Request (CANIFnCRQ) register. To begin transmission of the new data as soon as possible, set the TXRQST bit in the CANIFnMCTL register.

To prevent the clearing of the TXRQST bit in the CANIFnMCTL register at the end of a transmission that may already be in progress while the data is updated, the NEWDAT and TXRQST bits have to be set at the same time in the CANIFnMCTL register. When these bits are set at the same time, NEWDAT is cleared as soon as the new transmission has started.

17.3.6 Accepting Received Message Objects

When the arbitration and control field (the ID and XTD bits in the CANIFnARB2 and the RMTEN and DLC[3:0] bits of the CANIFnMCTL register) of an incoming message is completely shifted into the CAN controller, the message handling capability of the controller starts scanning the message RAM for a matching valid message object. To scan the message RAM for a matching message object, the controller uses the acceptance filtering programmed through the mask bits in the CANIFnMSKn register and enabled using the UMASK bit in the CANIFnMCTL register. Each valid message object, starting with object 1, is compared with the incoming message to locate a matching message object in the message RAM. If a match occurs, the scanning is stopped and the message handler proceeds depending on whether it is a data frame or remote frame that was received.

17.3.7 Receiving a Data Frame

The message handler stores the message from the CAN controller receive shift register into the matching message object in the message RAM. The data bytes, all arbitration bits, and the DLC bits are all stored into the corresponding message object. In this manner, the data bytes are connected with the identifier even if arbitration masks are used. The NEWDAT bit of the CANIFnMCTL register is set to indicate that new data has been received. The CPU should clear this bit when it reads the message object to indicate to the controller that the message has been received, and the buffer is free to receive more messages. If the CAN controller receives a message and the NEWDAT bit is already set, the MSGLST bit in the CANIFnMCTL register is set to indicate that the previous data was lost. If the system requires an interrupt on successful reception of a frame, the RXIE bit of the CANIFnMCTL register should be set. In this case, the INTPEND bit of the same register is set, causing the CANINT register to point to the message object that just received a message. The TXRQST bit of this message object should be cleared to prevent the transmission of a remote frame.

17.3.8 Receiving a Remote Frame

A remote frame contains no data, but instead specifies which object should be transmitted. When a remote frame is received, three different configurations of the matching message object have to be considered:
**Table 17-2. Message Object Configurations**

<table>
<thead>
<tr>
<th>Configuration in CANIFnMCTL</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIR = 1 (direction = transmit); programmed in the CANIFnARB2 register</td>
<td>At the reception of a matching remote frame, the TXRQST bit of this message object is set. The rest of the message object remains unchanged, and the controller automatically transfers the data in the message object as soon as possible.</td>
</tr>
<tr>
<td>RMTEN = 1 (set the TXRQST bit of the CANIFnMCTL register at reception of the frame to enable transmission)</td>
<td></td>
</tr>
<tr>
<td>UMASK = 1 or 0</td>
<td></td>
</tr>
<tr>
<td>DIR = 1 (direction = transmit); programmed in the CANIFnARB2 register</td>
<td>At the reception of a matching remote frame, the TXRQST bit of this message object remains unchanged, and the remote frame is ignored. This remote frame is disabled, the data is not transferred and nothing indicates that the remote frame ever happened.</td>
</tr>
<tr>
<td>RMTEN = 0 (do not change the TXRQST bit of the CANIFnMCTL register at reception of the frame)</td>
<td></td>
</tr>
<tr>
<td>UMASK = 0 (ignore mask in the CANIFnMSKn register)</td>
<td></td>
</tr>
<tr>
<td>DIR = 1 (direction = transmit); programmed in the CANIFnARB2 register</td>
<td>At the reception of a matching remote frame, the TXRQST bit of this message object is cleared. The arbitration and control field (ID + XTD + RMTEN + DLC) from the shift register is stored into the message object in the message RAM, and the NEWDAT bit of this message object is set. The data field of the message object remains unchanged; the remote frame is treated similar to a received data frame. This mode is useful for a remote data request from another CAN device for which the TM4C123GH6PZ controller does not have readily available data. The software must fill the data and answer the frame manually.</td>
</tr>
<tr>
<td>RMTEN = 0 (do not change the TXRQST bit of the CANIFnMCTL register at reception of the frame)</td>
<td></td>
</tr>
<tr>
<td>UMASK = 1 (use mask (MSK, MXTD, and MDIR in the CANIFnMSKn register) for acceptance filtering)</td>
<td></td>
</tr>
</tbody>
</table>

### 17.3.9 Receive/Transmit Priority

The receive/transmit priority for the message objects is controlled by the message number. Message object 1 has the highest priority, while message object 32 has the lowest priority. If more than one transmission request is pending, the message objects are transmitted in order based on the message object with the lowest message number. This prioritization is separate from that of the message identifier which is enforced by the CAN bus. As a result, if message object 1 and message object 2 both have valid messages to be transmitted, message object 1 is always transmitted first regardless of the message identifier in the message object itself.

### 17.3.10 Configuring a Receive Message Object

The following steps illustrate how to configure a receive message object.

1. Program the CANIFn Command Mask (CANIFnCMASK) register as described in the “Configuring a Transmit Message Object” on page 1074 section, except that the WRNRD bit is set to specify a write to the message RAM.

2. Program the CANIFnMSK1 and CANIFnMSK2 registers as described in the “Configuring a Transmit Message Object” on page 1074 section to configure which bits are used for acceptance filtering. Note that in order for these bits to be used for acceptance filtering, they must be enabled by setting the UMASK bit in the CANIFnMCTL register.

3. In the CANIFnMSK2 register, use the MSK[12:0] bits to specify which of the bits in the 29-bit or 11-bit message identifier are used for acceptance filtering. Note that MSK[12:0] are used for bits [28:16] of the 29-bit message identifier; whereas MSK[12:2] are used for bits [10:0] of the 11-bit message identifier. Use the MXTD and MDIR bits to specify whether to use XTD and
DIR for acceptance filtering. A value of 0x00 enables all messages to pass through the acceptance filtering. Also note that in order for these bits to be used for acceptance filtering, they must be enabled by setting the UMASK bit in the CANIFnMCTL register.

4. Program the CANIFnARB1 and CANIFnARB2 registers as described in the “Configuring a Transmit Message Object” on page 1074 section to program XTD and ID bits for the message identifier to be received; set the MSGVAL bit to indicate a valid message; and clear the DIR bit to specify receive.

5. In the CANIFnMCTL register:
   - Optionally set the UMASK bit to enable the mask (MSK, MXTD, and MDIR specified in the CANIFnMSK1 and CANIFnMSK2 registers) for acceptance filtering
   - Optionally set the RXIE bit to enable the INTPND bit to be set after a successful reception
   - Clear the RMTEN bit to leave the TXRQST bit unchanged
   - Set the EOB bit for a single message object
   - Configure the DLC[3:0] field to specify the size of the data frame

Take care during this configuration not to set the NEWDAT, MSGST, INTPND or TXRQST bits.

6. Program the number of the message object to be received in the MNUM field in the CANIFn Command Request (CANIFnCRQ) register. Reception of the message object begins as soon as a matching frame is available on the CAN bus.

When the message handler stores a data frame in the message object, it stores the received Data Length Code and eight data bytes in the CANIFnDA1, CANIFnDA2, CANIFnDB1, and CANIFnDB2 register. Byte 0 of the CAN data frame is stored in DATA[7:0] in the CANIFnDA1 register. If the Data Length Code is less than 8, the remaining bytes of the message object are overwritten by unspecified values.

The CAN mask registers can be used to allow groups of data frames to be received by a message object. The CAN mask registers, CANIFnMSK, configure which groups of frames are received by a message object. The UMASK bit in the CANIFnMCTL register enables the MSK bits in the CANIFnMSK register to filter which frames are received. The MXTD bit in the CANIFnMSK2 register should be set if only 29-bit extended identifiers are expected by this message object.

17.3.11 Handling of Received Message Objects

The CPU may read a received message any time via the CAN Interface registers because the data consistency is guaranteed by the message handler state machine.

Typically, the CPU first writes 0x007F to the CANIFnCMSK register and then writes the number of the message object to the CANIFnCRQ register. That combination transfers the whole received message from the message RAM into the Message Buffer registers (CANIFnMSK, CANIFnARB, and CANIFnMCTL). Additionally, the NEWDAT and INTPND bits are cleared in the message RAM, acknowledging that the message has been read and clearing the pending interrupt generated by this message object.

If the message object uses masks for acceptance filtering, the CANIFnARB registers show the full, unmasked ID for the received message.
The \texttt{NEWDAT} bit in the \texttt{CANIFnMCTL} register shows whether a new message has been received since the last time this message object was read. The \texttt{MSGLST} bit in the \texttt{CANIFnMCTL} register shows whether more than one message has been received since the last time this message object was read. \texttt{MSGLST} is not automatically cleared, and should be cleared by software after reading its status.

Using a remote frame, the CPU may request new data from another CAN node on the CAN bus. Setting the \texttt{TXRQST} bit of a receive object causes the transmission of a remote frame with the receive object's identifier. This remote frame triggers the other CAN node to start the transmission of the matching data frame. If the matching data frame is received before the remote frame could be transmitted, the \texttt{TXRQST} bit is automatically reset. This prevents the possible loss of data when the other device on the CAN bus has already transmitted the data slightly earlier than expected.

\subsection{17.3.11.1 Configuration of a FIFO Buffer}

With the exception of the \texttt{EOB} bit in the \texttt{CANIFnMCTL} register, the configuration of receive message objects belonging to a FIFO buffer is the same as the configuration of a single receive message object (see “Configuring a Receive Message Object” on page 1077). To concatenate two or more message objects into a FIFO buffer, the identifiers and masks (if used) of these message objects have to be programmed to matching values. Due to the implicit priority of the message objects, the message object with the lowest message object number is the first message object in a FIFO buffer. The \texttt{EOB} bit of all message objects of a FIFO buffer except the last one must be cleared. The \texttt{EOB} bit of the last message object of a FIFO buffer is set, indicating it is the last entry in the buffer.

\subsection{17.3.11.2 Reception of Messages with FIFO Buffers}

Received messages with identifiers matching to a FIFO buffer are stored starting with the message object with the lowest message number. When a message is stored into a message object of a FIFO buffer, the \texttt{NEWDAT} of the \texttt{CANIFnMCTL} register bit of this message object is set. By setting \texttt{NEWDAT} while \texttt{EOB} is clear, the message object is locked and cannot be written to by the message handler until the CPU has cleared the \texttt{NEWDAT} bit. Messages are stored into a FIFO buffer until the last message object of this FIFO buffer is reached. Until all of the preceding message objects have been released by clearing the \texttt{NEWDAT} bit, all further messages for this FIFO buffer are written into the last message object of the FIFO buffer and therefore overwrite previous messages.

\subsection{17.3.11.3 Reading from a FIFO Buffer}

When the CPU transfers the contents of a message object from a FIFO buffer by writing its number to the \texttt{CANIFnCRQ} register, the \texttt{TXRQST} and \texttt{CLRINTPND} bits in the \texttt{CANIFnCMSK} register should be set such that the \texttt{NEWDAT} and \texttt{INTPEND} bits in the \texttt{CANIFnMCTL} register are cleared after the read. The values of these bits in the \texttt{CANIFnMCTL} register always reflect the status of the message object before the bits are cleared. To assure the correct function of a FIFO buffer, the CPU should read out the message objects starting with the message object with the lowest message number. When reading from the FIFO buffer, the user should be aware that a new received message is placed in the message object with the lowest message number for which the \texttt{NEWDAT} bit of the \texttt{CANIFnMCTL} register is clear. As a result, the order of the received messages in the FIFO is not guaranteed. Figure 17-3 on page 1080 shows how a set of message objects which are concatenated to a FIFO Buffer can be handled by the CPU.
17.3.12 Handling of Interrupts

If several interrupts are pending, the CAN Interrupt (CANINT) register points to the pending interrupt with the highest priority, disregarding their chronological order. The status interrupt has the highest
priority. Among the message interrupts, the message object's interrupt with the lowest message number has the highest priority. A message interrupt is cleared by clearing the message object's INTPND bit in the CANIFnMCTL register or by reading the CAN Status (CANSTS) register. The status Interrupt is cleared by reading the CANSTS register.

The interrupt identifier INTID in the CANINT register indicates the cause of the interrupt. When no interrupt is pending, the register reads as 0x0000. If the value of the INTID field is different from 0, then an interrupt is pending. If the IE bit is set in the CANCTL register, the interrupt line to the interrupt controller is active. The interrupt line remains active until the INTID field is 0, meaning that all interrupt sources have been cleared (the cause of the interrupt is reset), or until IE is cleared, which disables interrupts from the CAN controller.

The INTID field of the CANINT register points to the pending message interrupt with the highest interrupt priority. The SIE bit in the CANCTL register controls whether a change of the RXOK, TXOK, and LEC bits in the CANSTS register can cause an interrupt. The EIE bit in the CANCTL register controls whether a change of the BOFF and EWARN bits in the CANSTS register can cause an interrupt. The IE bit in the CANCTL register controls whether any interrupt from the CAN controller actually generates an interrupt to the interrupt controller. The CANINT register is updated even when the IE bit in the CANCTL register is clear, but the interrupt is not indicated to the CPU.

A value of 0x8000 in the CANINT register indicates that an interrupt is pending because the CAN module has updated, but not necessarily changed, the CANSTS register, indicating that either an error or status interrupt has been generated. A write access to the CANSTS register can clear the RXOK, TXOK, and LEC bits in that same register; however, the only way to clear the source of a status interrupt is to read the CANSTS register.

The source of an interrupt can be determined in two ways during interrupt handling. The first is to read the INTID bit in the CANINT register to determine the highest priority interrupt that is pending, and the second is to read the CAN Message Interrupt Pending (CANMSGnINT) register to see all of the message objects that have pending interrupts.

An interrupt service routine reading the message that is the source of the interrupt may read the message and clear the message object's INTPND bit at the same time by setting the CLRINTPND bit in the CANIFnCMSK register. Once the INTPND bit has been cleared, the CANINT register contains the message number for the next message object with a pending interrupt.

17.3.13 Test Mode

A Test Mode is provided which allows various diagnostics to be performed. Test Mode is entered by setting the TEST bit in the CANCTL register. Once in Test Mode, the TX[1:0], LBACK, SILENT and BASIC bits in the CAN Test (CANTST) register can be used to put the CAN controller into the various diagnostic modes. The RX bit in the CANTST register allows monitoring of the CANnRX signal. All CANTST register functions are disabled when the TEST bit is cleared.

17.3.13.1 Silent Mode

Silent Mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits (Acknowledge Bits, Error Frames). The CAN Controller is put in Silent Mode setting the SILENT bit in the CANTST register. In Silent Mode, the CAN controller is able to receive valid data frames and valid remote frames, but it sends only recessive bits on the CAN bus and cannot start a transmission. If the CAN Controller is required to send a dominant bit (ACK bit, overload flag, or active error flag), the bit is rerouted internally so that the CAN Controller monitors this dominant bit, although the CAN bus remains in recessive state.
17.3.13.2 Loopback Mode

Loopback mode is useful for self-test functions. In Loopback Mode, the CAN Controller internally routes the CANnTX signal on to the CANnRX signal and treats its own transmitted messages as received messages and stores them (if they pass acceptance filtering) into the message buffer. The CAN Controller is put in Loopback Mode by setting the LBACK bit in the CANTST register. To be independent from external stimulation, the CAN Controller ignores acknowledge errors (a recessive bit sampled in the acknowledge slot of a data/remote frame) in Loopback Mode. The actual value of the CANnRX signal is disregarded by the CAN Controller. The transmitted messages can be monitored on the CANnTX signal.

17.3.13.3 Loopback Combined with Silent Mode

Loopback Mode and Silent Mode can be combined to allow the CAN Controller to be tested without affecting a running CAN system connected to the CANnTX and CANnRX signals. In this mode, the CANnRX signal is disconnected from the CAN Controller and the CANnTX signal is held recessive. This mode is enabled by setting both the LBACK and SILENT bits in the CANTST register.

17.3.13.4 Basic Mode

Basic Mode allows the CAN Controller to be operated without the Message RAM. In Basic Mode, the CANIFn registers are used as the transmit buffer. The transmission of the contents of the IF1 registers is requested by setting the BUSY bit of the CANIFnCRQ register. The CANIFn registers are locked while the BUSY bit is set. The BUSY bit indicates that a transmission is pending. As soon the CAN bus is idle, the CANIFn registers are loaded into the shift register of the CAN Controller and transmission is started. When the transmission has completed, the BUSY bit is cleared and the locked CANIFn registers are released. A pending transmission can be aborted at any time by clearing the BUSY bit in the CANIFnCRQ register while the CANIFn registers are locked. If the CPU has cleared the BUSY bit, a possible retransmission in case of lost arbitration or an error is disabled.

The CANIFn2 Registers are used as a receive buffer. After the reception of a message, the contents of the shift register are stored in the CANIFn2 registers, without any acceptance filtering. Additionally, the actual contents of the shift register can be monitored during the message transfer. Each time a read message object is initiated by setting the BUSY bit of the CANIFn2CRQ register, the contents of the shift register are stored into the CANIFn2 registers.

In Basic Mode, all message-object-related control and status bits and of the control bits of the CANIFnCMSK registers are not evaluated. The message number of the CANIFnCRQ registers is also not evaluated. In the CANIFn2MCTL register, the NEWDAT and MSGLST bits retain their function, the DLC[3:0] field shows the received DLC, the other control bits are cleared.

Basic Mode is enabled by setting the BASIC bit in the CANTST register.

17.3.13.5 Transmit Control

Software can directly override control of the CANnTX signal in four different ways.

- CANnTX is controlled by the CAN Controller
- The sample point is driven on the CANnTX signal to monitor the bit timing
- CANnTX drives a low value
- CANnTX drives a high value
The last two functions, combined with the readable CAN receive pin CANnRX, can be used to check the physical layer of the CAN bus.

The Transmit Control function is enabled by programming the TX[1:0] field in the CANTST register. The three test functions for the CANnTX signal interfere with all CAN protocol functions. TX[1:0] must be cleared when CAN message transfer or Loopback Mode, Silent Mode, or Basic Mode are selected.

17.3.14 Bit Timing Configuration Error Considerations

Even if minor errors in the configuration of the CAN bit timing do not result in immediate failure, the performance of a CAN network can be reduced significantly. In many cases, the CAN bit synchronization amends a faulty configuration of the CAN bit timing to such a degree that only occasionally an error frame is generated. In the case of arbitration, however, when two or more CAN nodes simultaneously try to transmit a frame, a misplaced sample point may cause one of the transmitters to become error passive. The analysis of such sporadic errors requires a detailed knowledge of the CAN bit synchronization inside a CAN node and of the CAN nodes' interaction on the CAN bus.

17.3.15 Bit Time and Bit Rate

The CAN system supports bit rates in the range of lower than 1 Kbps up to 1000 Kbps. Each member of the CAN network has its own clock generator. The timing parameter of the bit time can be configured individually for each CAN node, creating a common bit rate even though the CAN nodes' oscillator periods may be different.

Because of small variations in frequency caused by changes in temperature or voltage and by deteriorating components, these oscillators are not absolutely stable. As long as the variations remain inside a specific oscillator's tolerance range, the CAN nodes are able to compensate for the different bit rates by periodically resynchronizing to the bit stream.

According to the CAN specification, the bit time is divided into four segments (see Figure 17-4 on page 1084): the Synchronization Segment, the Propagation Time Segment, the Phase Buffer Segment 1, and the Phase Buffer Segment 2. Each segment consists of a specific, programmable number of time quanta (see Table 17-3 on page 1084). The length of the time quantum \( t_q \), which is the basic time unit of the bit time, is defined by the CAN controller's input clock \( f_{sys} \) and the Baud Rate Prescaler (BRP):

\[
t_q = \frac{BRP}{f_{sys}}
\]

The \( f_{sys} \) input clock is the system clock frequency as configured by the RCC or RCC2 registers (see page 254 or page 261).

The Synchronization Segment \( Sync \) is that part of the bit time where edges of the CAN bus level are expected to occur; the distance between an edge that occurs outside of \( Sync \) and the \( Sync \) is called the phase error of that edge.

The Propagation Time Segment \( Prop \) is intended to compensate for the physical delay times within the CAN network.

The Phase Buffer Segments Phase1 and Phase2 surround the Sample Point.

The (Re-)Synchronization Jump Width (SJW) defines how far a resynchronization may move the Sample Point inside the limits defined by the Phase Buffer Segments to compensate for edge phase errors.

A given bit rate may be met by different bit-time configurations, but for the proper function of the CAN network, the physical delay times and the oscillator's tolerance range have to be considered.
Figure 17-4. CAN Bit Time

Table 17-3. CAN Protocol Ranges

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>BRP</td>
<td>[1 .. 64]</td>
<td>Defines the length of the time quantum ( t_q ). The CANBRPE register can be used to extend the range to 1024.</td>
</tr>
<tr>
<td>Sync</td>
<td>1 ( t_q )</td>
<td>Fixed length, synchronization of bus input to system clock</td>
</tr>
<tr>
<td>Prop</td>
<td>[1 .. 8] ( t_q )</td>
<td>Compensates for the physical delay times</td>
</tr>
<tr>
<td>Phase1</td>
<td>[1 .. 8] ( t_q )</td>
<td>May be lengthened temporarily by synchronization</td>
</tr>
<tr>
<td>Phase2</td>
<td>[1 .. 8] ( t_q )</td>
<td>May be shortened temporarily by synchronization</td>
</tr>
<tr>
<td>SJW</td>
<td>[1 .. 4] ( t_q )</td>
<td>May not be longer than either Phase Buffer Segment</td>
</tr>
</tbody>
</table>

The bit timing configuration is programmed in two register bytes in the CANBIT register. In the CANBIT register, the four components TSEG2, TSEG1, SJW, and BRP have to be programmed to a numerical value that is one less than its functional value; so instead of values in the range of \([1..n]\), values in the range of \([0..n-1]\) are programmed. That way, for example, SJW (functional range of \([1..4]\)) is represented by only two bits in the SJW bit field. Table 17-4 shows the relationship between the CANBIT register values and the parameters.

Table 17-4. CANBIT Register Values

<table>
<thead>
<tr>
<th>CANBIT Register Field</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSEG2</td>
<td>Phase2 - 1</td>
</tr>
<tr>
<td>TSEG1</td>
<td>Prop + Phase1 - 1</td>
</tr>
<tr>
<td>SJW</td>
<td>SJW - 1</td>
</tr>
<tr>
<td>BRP</td>
<td>BRP</td>
</tr>
</tbody>
</table>

Therefore, the length of the bit time is (programmed values):

\[ TSEG1 + TSEG2 + 3 \times t_q \]

or (functional values):

\[ \text{Sync} + \text{Prop} + \text{Phase1} + \text{Phase2} \times t_q \]

The data in the CANBIT register is the configuration input of the CAN protocol controller. The baud rate prescaler (configured by the BRP field) defines the length of the time quantum, the basic time...
unit of the bit time; the bit timing logic (configured by TSEG1, TSEG2, and SJW) defines the number of time quanta in the bit time.

The processing of the bit time, the calculation of the position of the sample point, and occasional synchronizations are controlled by the CAN controller and are evaluated once per time quantum.

The CAN controller translates messages to and from frames. In addition, the controller generates and discards the enclosing fixed format bits, inserts and extracts stuff bits, calculates and checks the CRC code, performs the error management, and decides which type of synchronization is to be used. The bit value is received or transmitted at the sample point. The information processing time (IPT) is the time after the sample point needed to calculate the next bit to be transmitted on the CAN bus. The IPT includes any of the following: retrieving the next data bit, handling a CRC bit, determining if bit stuffing is required, generating an error flag or simply going idle.

The IPT is application-specific but may not be longer than 2 \( t_q \); the CAN's IPT is 0 \( t_q \). Its length is the lower limit of the programmed length of Phase2. In case of synchronization, Phase2 may be shortened to a value less than IPT, which does not affect bus timing.

17.3.16 Calculating the Bit Timing Parameters

Usually, the calculation of the bit timing configuration starts with a required bit rate or bit time. The resulting bit time \((1/\text{bit rate})\) must be an integer multiple of the system clock period.

The bit time may consist of 4 to 25 time quanta. Several combinations may lead to the required bit time, allowing iterations of the following steps.

The first part of the bit time to be defined is Prop. Its length depends on the delay times measured in the system. A maximum bus length as well as a maximum node delay has to be defined for expandable CAN bus systems. The resulting time for Prop is converted into time quanta (rounded up to the nearest integer multiple of \( t_q \)).

Sync is 1 \( t_q \) long (fixed), which leaves \((\text{bit time} - \text{Prop} - 1) \ t_q\) for the two Phase Buffer Segments. If the number of remaining \( t_q \) is even, the Phase Buffer Segments have the same length, that is, Phase2 = Phase1, else Phase2 = Phase1 + 1.

The minimum nominal length of Phase2 has to be regarded as well. Phase2 may not be shorter than the CAN controller's Information Processing Time, which is, depending on the actual implementation, in the range of \([0..2] \ t_q\).

The length of the synchronization jump width is set to the least of 4, Phase1 or Phase2.

The oscillator tolerance range necessary for the resulting configuration is calculated by the formula given below:

\[
(1 - df) \times fnom \leq fosc \leq (1 + df) \times fnom
\]

where:

- \( df \) = Maximum tolerance of oscillator frequency
- \( fosc \) = Actual oscillator frequency
- \( fnom \) = Nominal oscillator frequency

Maximum frequency tolerance must take into account the following formulas:
\[ df \leq \frac{(\text{Phase}_1, \text{Phase}_2)_{\text{min}}}{2 \times (13 \times \text{tbit} - \text{Phase}_2)} \]

\[ df_{\text{max}} = 2 \times df \times f_{\text{nom}} \]

where:

- Phase1 and Phase2 are from Table 17-3 on page 1084
- \( \text{tbit} \) = Bit Time
- \( df_{\text{max}} \) = Maximum difference between two oscillators

If more than one configuration is possible, that configuration allowing the highest oscillator tolerance range should be chosen.

CAN nodes with different system clocks require different configurations to come to the same bit rate. The calculation of the propagation time in the CAN network, based on the nodes with the longest delay times, is done once for the whole network.

The CAN system's oscillator tolerance range is limited by the node with the lowest tolerance range.

The calculation may show that bus length or bit rate have to be decreased or that the oscillator frequencies' stability has to be increased in order to find a protocol-compliant configuration of the CAN bit timing.

### 17.3.16.1 Example for Bit Timing at High Baud Rate

In this example, the frequency of CAN clock is 25 MHz, and the bit rate is 1 Mbps.

\[
\begin{align*}
\text{bit time} &= 1 \mu\text{s} = n \times t_q = 5 \times t_q \\
\text{t}_q &= 200 \text{ ns} \\
\text{t}_q &= (\text{Baud rate Prescaler})/\text{CAN Clock} \\
\text{Baud rate Prescaler} &= t_q \times \text{CAN Clock} \\
\text{Baud rate Prescaler} &= 200E-9 \times 25E6 = 5 \\
\text{t}_{\text{Sync}} &= 1 \times t_q = 200 \text{ ns} \quad \text{\textbackslash fixed at 1 time quanta} \\
\text{delay of bus driver} &= 50 \text{ ns} \\
\text{delay of receiver circuit} &= 30 \text{ ns} \\
\text{delay of bus line (40m)} &= 220 \text{ ns} \\
\text{t}_{\text{Prop}} &= 400 \text{ ns} = 2 \times t_q \\
\text{bit time} &= \text{t}_{\text{Sync}} + \text{t}_{\text{TSeg1}} + \text{t}_{\text{TSeg2}} = 5 \times t_q \\
\text{bit time} &= \text{t}_{\text{Sync}} + \text{t}_{\text{Prop}} + \text{t}_{\text{Phase1}} + \text{t}_{\text{Phase2}} \\
\text{t}_{\text{Phase1}} + \text{t}_{\text{Phase2}} &= \text{bit time} - \text{t}_{\text{Sync}} - \text{t}_{\text{Prop}} \\
\text{t}_{\text{Phase1}} + \text{t}_{\text{Phase2}} &= (5 \times t_q) - (1 \times t_q) - (2 \times t_q) \\
\text{t}_{\text{Phase1}} + \text{t}_{\text{Phase2}} &= 2 \times t_q \\
\text{t}_{\text{Phase1}} &= 1 \times t_q \\
\text{t}_{\text{Phase2}} &= 1 \times t_q \\
\text{t}_{\text{Phase2}} &= \text{t}_{\text{Phase1}} \\
\end{align*}
\]
tTSeg1 = tProp + tPhase1
\[ tTSeg1 = (2 \cdot t_q) + (1 \cdot t_q) \]
\[ tTSeg1 = 3 \cdot t_q \]

tTSeg2 = tPhase2
\[ tTSeg2 = (\text{Information Processing Time} + 1) \cdot t_q \]
\[ tTSeg2 = 1 \cdot t_q \]  \(\text{Assumes IPT}=0\)

tSJW = 1 \cdot t_q  \  \(\text{Least of 4, Phase1 and Phase2}\)

In the above example, the bit field values for the CANBIT register are:

<table>
<thead>
<tr>
<th>TSEG2</th>
<th>= TSeg2 -1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>= 1-1</td>
</tr>
<tr>
<td></td>
<td>= 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TSEG1</th>
<th>= TSeg1 -1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>= 3-1</td>
</tr>
<tr>
<td></td>
<td>= 2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SJW</th>
<th>= SJW -1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>= 1-1</td>
</tr>
<tr>
<td></td>
<td>= 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BRP</th>
<th>= Baud rate prescaler - 1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>= 5-1</td>
</tr>
<tr>
<td></td>
<td>= 4</td>
</tr>
</tbody>
</table>

The final value programmed into the CANBIT register = 0x0204.

**17.3.16.2 Example for Bit Timing at Low Baud Rate**

In this example, the frequency of the CAN clock is 50 MHz, and the bit rate is 100 Kbps.

\[ \text{bit time} = 10 \ \mu\text{s} = n \cdot t_q = 10 \cdot t_q \]
\[ t_q = 1 \ \mu\text{s} \]
\[ t_q = (\text{Baud rate prescaler})/\text{CAN Clock} \]
Baud rate Prescaler = \[ t_q \cdot \text{CAN Clock} \]
Baud rate Prescaler = \[ 1 \cdot 50E6 = 50 \]

\[ tSync = 1 \cdot t_q = 1 \ \mu\text{s} \]  \(\text{fixed at 1 time quanta}\)

delay of bus driver 200 ns
delay of receiver circuit 80 ns
delay of bus line (40m) 220 ns
\[ tProp = 1 \cdot t_q \]  \(\text{1 \ \mu\text{s} is next integer multiple of} \ t_q\)

\[ \text{bit time} = tSync + tTSeg1 + tTSeg2 = 10 \cdot t_q \]
\[ \text{bit time} = tSync + tProp + tPhase1 + tPhase2 \]
\[ tPhase1 + tPhase2 = \text{bit time} - tSync - tProp \]
\[ tPhase1 + tPhase2 = (10 \cdot t_q) - (1 \cdot t_q) - (1 \cdot t_q) \]
\[ tPhase1 + tPhase2 = 8 \cdot t_q \]
\[ tPhase1 = 4 \cdot t_q \]
\[ tPhase2 = 4 \cdot t_q \]  \(\text{\text{tPhase1 = tPhase2}}\)
\[ t_{\text{Seg1}} = t_{\text{Prop}} + t_{\text{Phase1}} \]
\[ t_{\text{Seg1}} = (1 \times t_q) + (4 \times t_q) \]
\[ t_{\text{Seg1}} = 5 \times t_q \]
\[ t_{\text{Seg2}} = t_{\text{Phase2}} \]
\[ t_{\text{Seg2}} = (\text{Information Processing Time} + 4) \times t_q \]
\[ t_{\text{Seg2}} = 4 \times t_q \quad \text{\\Assumes IPT}=0 \]
\[ t_{\text{SJW}} = 4 \times t_q \quad \text{\\Least of 4, Phase1, and Phase2} \]

<table>
<thead>
<tr>
<th>TSEG2</th>
<th>= TSeg2 -1</th>
<th>= 4-1</th>
<th>= 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSEG1</td>
<td>= TSeg1 -1</td>
<td>= 5-1</td>
<td>= 4</td>
</tr>
<tr>
<td>SJW</td>
<td>= SJW -1</td>
<td>= 4-1</td>
<td>= 3</td>
</tr>
<tr>
<td>BRP</td>
<td>= Baud rate prescaler - 1</td>
<td>= 50-1</td>
<td>= 49</td>
</tr>
</tbody>
</table>

The final value programmed into the CANBIT register = 0x34F1.

### 17.4 Register Map

Table 17-5 on page 1088 lists the registers. All addresses given are relative to the CAN base address of:

- CAN0: 0x4004.0000
- CAN1: 0x4004.1000

Note that the CAN controller clock must be enabled before the registers can be programmed (see page 354). There must be a delay of 3 system clocks after the CAN module clock is enabled before any CAN module registers are accessed.

Table 17-5. CAN Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>CANCTL</td>
<td>RW</td>
<td>0x0000.0001</td>
<td>CAN Control</td>
<td>1091</td>
</tr>
<tr>
<td>0x004</td>
<td>CANSTS</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN Status</td>
<td>1093</td>
</tr>
<tr>
<td>0x008</td>
<td>CANERR</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN Error Counter</td>
<td>1096</td>
</tr>
<tr>
<td>0x00C</td>
<td>CANBIT</td>
<td>RW</td>
<td>0x0000.2301</td>
<td>CAN Bit Timing</td>
<td>1097</td>
</tr>
<tr>
<td>0x010</td>
<td>CANINT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN Interrupt</td>
<td>1098</td>
</tr>
<tr>
<td>0x014</td>
<td>CANTST</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN Test</td>
<td>1099</td>
</tr>
<tr>
<td>0x018</td>
<td>CANBRPE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN Baud Rate Prescaler Extension</td>
<td>1101</td>
</tr>
<tr>
<td>0x020</td>
<td>CANIF1CRQ</td>
<td>RW</td>
<td>0x0000.0001</td>
<td>CAN IF1 Command Request</td>
<td>1102</td>
</tr>
</tbody>
</table>
### Table 17-5. CAN Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x024</td>
<td>CANIF1CMSK</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Command Mask</td>
<td>1103</td>
</tr>
<tr>
<td>0x028</td>
<td>CANIF1MSK1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Mask 1</td>
<td>1106</td>
</tr>
<tr>
<td>0x02C</td>
<td>CANIF1MSK2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Mask 2</td>
<td>1107</td>
</tr>
<tr>
<td>0x030</td>
<td>CANIF1ARB1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Arbitration 1</td>
<td>1109</td>
</tr>
<tr>
<td>0x034</td>
<td>CANIF1ARB2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Arbitration 2</td>
<td>1110</td>
</tr>
<tr>
<td>0x038</td>
<td>CANIF1MCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Message Control</td>
<td>1112</td>
</tr>
<tr>
<td>0x03C</td>
<td>CANIF1DA1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Data A1</td>
<td>1115</td>
</tr>
<tr>
<td>0x040</td>
<td>CANIF1DA2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Data A2</td>
<td>1115</td>
</tr>
<tr>
<td>0x044</td>
<td>CANIF1DB1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Data B1</td>
<td>1115</td>
</tr>
<tr>
<td>0x048</td>
<td>CANIF1DB2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF1 Data B2</td>
<td>1115</td>
</tr>
<tr>
<td>0x080</td>
<td>CANIF2CRQ</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Command Request</td>
<td>1102</td>
</tr>
<tr>
<td>0x084</td>
<td>CANIF2CMSK</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Command Mask</td>
<td>1103</td>
</tr>
<tr>
<td>0x088</td>
<td>CANIF2MSK1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Mask 1</td>
<td>1106</td>
</tr>
<tr>
<td>0x08C</td>
<td>CANIF2MSK2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Mask 2</td>
<td>1107</td>
</tr>
<tr>
<td>0x090</td>
<td>CANIF2ARB1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Arbitration 1</td>
<td>1109</td>
</tr>
<tr>
<td>0x094</td>
<td>CANIF2ARB2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Arbitration 2</td>
<td>1110</td>
</tr>
<tr>
<td>0x098</td>
<td>CANIF2MCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Message Control</td>
<td>1112</td>
</tr>
<tr>
<td>0x09C</td>
<td>CANIF2DA1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Data A1</td>
<td>1115</td>
</tr>
<tr>
<td>0x0A0</td>
<td>CANIF2DA2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Data A2</td>
<td>1115</td>
</tr>
<tr>
<td>0x0A4</td>
<td>CANIF2DB1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Data B1</td>
<td>1115</td>
</tr>
<tr>
<td>0x0A8</td>
<td>CANIF2DB2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>CAN IF2 Data B2</td>
<td>1115</td>
</tr>
<tr>
<td>0x100</td>
<td>CANTXRQ1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN Transmission Request 1</td>
<td>1116</td>
</tr>
<tr>
<td>0x104</td>
<td>CANTXRQ2</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN Transmission Request 2</td>
<td>1116</td>
</tr>
<tr>
<td>0x120</td>
<td>CANNWDA1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN New Data 1</td>
<td>1117</td>
</tr>
<tr>
<td>0x124</td>
<td>CANNWDA2</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN New Data 2</td>
<td>1117</td>
</tr>
<tr>
<td>0x140</td>
<td>CANMSG1INT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN Message 1 Interrupt Pending</td>
<td>1118</td>
</tr>
<tr>
<td>0x144</td>
<td>CANMSG2INT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN Message 2 Interrupt Pending</td>
<td>1118</td>
</tr>
<tr>
<td>0x160</td>
<td>CANMSG1VAL</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN Message 1 Valid</td>
<td>1119</td>
</tr>
<tr>
<td>0x164</td>
<td>CANMSG2VAL</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>CAN Message 2 Valid</td>
<td>1119</td>
</tr>
</tbody>
</table>

### 17.5 CAN Register Descriptions

The remainder of this section lists and describes the CAN registers, in numerical order by address offset. There are two sets of Interface Registers that are used to access the Message Objects in...
the Message RAM: CANIF1x and CANIF2x. The function of the two sets are identical and are used to queue transactions.
Register 1: CAN Control (CANCTL), offset 0x000

This control register initializes the module and enables test mode and interrupts.

The bus-off recovery sequence (see CAN Specification Rev. 2.0) cannot be shortened by setting or clearing INIT. If the device goes bus-off, it sets INIT, stopping all bus activities. Once INIT has been cleared by the CPU, the device then waits for 129 occurrences of Bus Idle (129 * 11 consecutive High bits) before resuming normal operations. At the end of the bus-off recovery sequence, the Error Management Counters are reset.

During the waiting time after INIT is cleared, each time a sequence of 11 High bits has been monitored, a BITERROR0 code is written to the CANSTS register (the LEC field = 0x5), enabling the CPU to readily check whether the CAN bus is stuck Low or continuously disturbed, and to monitor the proceeding of the bus-off recovery sequence.

### CAN Control (CANCTL)

<table>
<thead>
<tr>
<th>CAN0 base: 0x4004.0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN1 base: 0x4004.1000</td>
</tr>
<tr>
<td>Offset 0x000</td>
</tr>
<tr>
<td>Type RW, reset 0x0000.0001</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>0x0000.00 Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>TEST</td>
<td>RW</td>
<td>0</td>
<td>Test Mode Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The CAN controller is operating normally.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The CAN controller is in test mode.</td>
</tr>
<tr>
<td>6</td>
<td>CCE</td>
<td>RW</td>
<td>0</td>
<td>Configuration Change Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Write accesses to the CANBIT register are not allowed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Write accesses to the CANBIT register are allowed if the INIT bit is 1.</td>
</tr>
<tr>
<td>5</td>
<td>DAR</td>
<td>RW</td>
<td>0</td>
<td>Disable Automatic-Retransmission</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Auto-retransmission of disturbed messages is enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Auto-retransmission is disabled.</td>
</tr>
</tbody>
</table>
Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Error Interrupt Enable</td>
<td>RW</td>
<td>0</td>
<td>Error Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No error status interrupt is generated.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A change in the BOFF or WARN bits in the CANSTS register generates an interrupt.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Status Interrupt Enable</td>
<td>RW</td>
<td>0</td>
<td>Status Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No status interrupt is generated.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is generated when a message has successfully been transmitted or received, or a CAN bus error has been detected. A change in the TXOK, RXOK or LEC bits in the CANSTS register generates an interrupt.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CAN Interrupt Enable</td>
<td>RW</td>
<td>0</td>
<td>CAN Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Interrupts disabled.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Interrupts enabled.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Initialization</td>
<td>RW</td>
<td>1</td>
<td>Initialization</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Normal operation.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Initialization started.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 2: CAN Status (CANSTS), offset 0x004

Important: This register is read-sensitive. See the register description for details.

The status register contains information for interrupt servicing such as Bus-Off, error count threshold, and error types.

The LEC field holds the code that indicates the type of the last error to occur on the CAN bus. This field is cleared when a message has been transferred (reception or transmission) without error. The unused error code 0x7 may be written by the CPU to manually set this field to an invalid error so that it can be checked for a change later.

An error interrupt is generated by the BOFF and EWARN bits, and a status interrupt is generated by the RXOK, TXOK, and LEC bits, if the corresponding enable bits in the CAN Control (CANCTL) register are set. A change of the EPASS bit or a write to the RXOK, TXOK, or LEC bits does not generate an interrupt.

Reading the CAN Status (CANSTS) register clears the CAN Interrupt (CANINT) register, if it is pending.

CAN Status (CANSTS)
CAN0 base: 0x4004.0000
CAN1 base: 0x4004.1000
Offset 0x004
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>BOFF</td>
<td>RO</td>
<td>0</td>
<td>Bus-Off Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>EWARN</td>
<td>RO</td>
<td>0</td>
<td>Warning Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
### Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>EPASS</td>
<td>RO</td>
<td>0</td>
<td>Error Passive</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>RXOK</td>
<td>RW</td>
<td>0</td>
<td>Received a Message Successfully</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit must be cleared by writing a 0 to it.</td>
</tr>
<tr>
<td>3</td>
<td>TXOK</td>
<td>RW</td>
<td>0</td>
<td>Transmitted a Message Successfully</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit must be cleared by writing a 0 to it.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>2:0</td>
<td>LEC</td>
<td>RW</td>
<td>0x0</td>
<td>Last Error Code</td>
</tr>
</tbody>
</table>

This is the type of the last error to occur on the CAN bus.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>No Error</td>
</tr>
<tr>
<td>0x1</td>
<td>Stuff Error</td>
</tr>
</tbody>
</table>

More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x2</td>
<td>Format Error</td>
</tr>
</tbody>
</table>

A fixed format part of the received frame has the wrong format.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3</td>
<td>ACK Error</td>
</tr>
</tbody>
</table>

The message transmitted was not acknowledged by another node.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4</td>
<td>Bit 1 Error</td>
</tr>
</tbody>
</table>

When a message is transmitted, the CAN controller monitors the data lines to detect any conflicts. When the arbitration field is transmitted, data conflicts are a part of the arbitration protocol. When other frame fields are transmitted, data conflicts are considered errors.

A Bit 1 Error indicates that the device wanted to send a High level (logical 1) but the monitored bus value was Low (logical 0).

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x5</td>
<td>Bit 0 Error</td>
</tr>
</tbody>
</table>

A Bit 0 Error indicates that the device wanted to send a Low level (logical 0), but the monitored bus value was High (logical 1).

During bus-off recovery, this status is set each time a sequence of 11 High bits has been monitored. By checking for this status, software can monitor the proceeding of the bus-off recovery sequence without any disturbances to the bus.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x6</td>
<td>CRC Error</td>
</tr>
</tbody>
</table>

The CRC checksum was incorrect in the received message, indicating that the calculated value received did not match the calculated CRC of the data.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x7</td>
<td>No Event</td>
</tr>
</tbody>
</table>

When the LEC bit shows this value, no CAN bus event was detected since this value was written to the LEC field.
Register 3: CAN Error Counter (CANERR), offset 0x008

This register contains the error counter values, which can be used to analyze the cause of an error.

CAN Error Counter (CANERR)
CAN0 base: 0x4004.0000
CAN1 base: 0x4004.1000
Offset 0x008
Type RO, reset 0x0000.0000

Bit/Field  Name  Type  Reset  Description
31:16  reserved  RO  0x0000  Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
15  RP  RO  0  Received Error Passive
Value  Description
0  The Receive Error counter is below the Error Passive level (127 or less).
1  The Receive Error counter has reached the Error Passive level (128 or greater).
14:8  REC  RO  0x00  Receive Error Counter
This field contains the state of the receiver error counter (0 to 127).
7:0  TEC  RO  0x00  Transmit Error Counter
This field contains the state of the transmit error counter (0 to 255).
Register 4: CAN Bit Timing (CANBIT), offset 0x00C

This register is used to program the bit width and bit quantum. Values are programmed to the system clock frequency. This register is write-enabled by setting the CCE and INIT bits in the CANCTL register. See "Bit Time and Bit Rate" on page 1083 for more information.

### CAN Bit Timing (CANBIT)

CAN0 base: 0x4004.0000
CAN1 base: 0x4004.1000
Offset 0x00C
Type RW, reset 0x0000.2301

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:15</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>14:12</td>
<td>TSEG2</td>
<td>RW</td>
<td>0x2</td>
<td>Time Segment after Sample Point</td>
</tr>
<tr>
<td>11:8</td>
<td>TSEG1</td>
<td>RW</td>
<td>0x3</td>
<td>Time Segment Before Sample Point</td>
</tr>
<tr>
<td>7:6</td>
<td>SJW</td>
<td>RW</td>
<td>0x0</td>
<td>(Re)Synchronization Jump Width</td>
</tr>
<tr>
<td>5:0</td>
<td>BRP</td>
<td>RW</td>
<td>0x1</td>
<td>Baud Rate Prescaler</td>
</tr>
</tbody>
</table>

The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quantum.

0x00-0x03F: The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

During the start of frame (SOF), if the CAN controller detects a phase error (misalignment), it can adjust the length of TSEG2 or TSEG1 by the value in SJW. So the reset value of 0 adjusts the length by 1 bit time quanta.

The CANBRPE register can be used to further divide the bit time.
Register 5: CAN Interrupt (CANINT), offset 0x010

This register indicates the source of the interrupt.

If several interrupts are pending, the CAN Interrupt (CANINT) register points to the pending interrupt with the highest priority, disregarding the order in which the interrupts occurred. An interrupt remains pending until the CPU has cleared it. If the INTID field is not 0x0000 (the default) and the IE bit in the CANCTL register is set, the interrupt is active. The interrupt line remains active until the INTID field is cleared by reading the CANSTS register, or until the IE bit in the CANCTL register is cleared.

**Note:** Reading the CAN Status (CANSTS) register clears the CAN Interrupt (CANINT) register, if it is pending.

### CAN Interrupt (CANINT)

<table>
<thead>
<tr>
<th>CAN0 base: 0x4004.0000</th>
<th>CAN1 base: 0x4004.1000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset 0x010</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>Interrupt Identifier</td>
</tr>
</tbody>
</table>

The number in this field indicates the source of the interrupt.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>INTID</td>
<td>RO</td>
<td>0x0000</td>
<td>Interrupt Identifier</td>
</tr>
</tbody>
</table>

Value Description
0x0000 No interrupt pending
0x0001-0x0020 Number of the message object that caused the interrupt
0x0021-0x7FFF Reserved
0x8000 Status Interrupt
0x8001-0xFFF Reserved
Register 6: CAN Test (CANTST), offset 0x014

This register is used for self-test and external pin access. It is write-enabled by setting the TEST bit in the CANCTL register. Different test functions may be combined, however, CAN transfers are affected if the TX bits in this register are not zero.

**CAN Test (CANTST)**

| CAN0 base: 0x4004.0000 |
| CAN1 base: 0x4004.1000 |
| Offset 0x014 |
| Type RW, reset 0x0000.0000 |

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

| 31:8 | reserved |
| 7    | RX       |
| 6:5  | TX       |

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
<td>Receive Observation</td>
</tr>
<tr>
<td>RO</td>
<td>0x0</td>
<td>Transmit Control</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The CANnRx pin is low.</td>
</tr>
<tr>
<td>1</td>
<td>The CANnRx pin is high.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>CAN Module Control</td>
</tr>
<tr>
<td>0x1</td>
<td>Sample Point</td>
</tr>
<tr>
<td>0x2</td>
<td>Driven Low</td>
</tr>
<tr>
<td>0x3</td>
<td>Driven High</td>
</tr>
</tbody>
</table>

**CAN Module Control**

- **CANnTx** is controlled by the CAN module; default operation
- The sample point is driven on the CANnTx signal. This mode is useful to monitor bit timing.
- CANnTx drives a low value. This mode is useful for checking the physical layer of the CAN bus.
- CANnTx drives a high value. This mode is useful for checking the physical layer of the CAN bus.
### Controller Area Network (CAN) Module

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>LBACK</td>
<td>RW</td>
<td>0</td>
<td>Loopback Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>SILENT</td>
<td>RW</td>
<td>0</td>
<td>Silent Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>BASIC</td>
<td>RW</td>
<td>0</td>
<td>Basic Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 7: CAN Baud Rate Prescaler Extension (CANBRPE), offset 0x018

This register is used to further divide the bit time set with the BRP bit in the CANBIT register. It is write-enabled by setting the CCE bit in the CANCTL register.

CAN Baud Rate Prescaler Extension (CANBRPE)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3:0</td>
<td>BRPE</td>
<td>RW</td>
<td>0x0</td>
<td>Baud Rate Prescaler Extension</td>
</tr>
</tbody>
</table>

0x00-0x0F: Extend the BRP bit in the CANBIT register to values up to 1023. The actual interpretation by the hardware is one more than the value programmed by BRPE (MSBs) and BRP (LSBs).
A message transfer is started as soon as there is a write of the message object number to the MNUM field when the TXRQST bit in the CANIF1MCTL register is set. With this write operation, the BUSY bit is automatically set to indicate that a transfer between the CAN Interface Registers and the internal message RAM is in progress. After a wait time of 3 to 6 CAN_CLK periods, the transfer between the interface register and the message RAM completes, which then clears the BUSY bit.

CAN IFn Command Request (CANIFnCRQ)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Name</th>
<th>Bit/Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
<td>reserved</td>
<td>31:16</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
<td>BUSY</td>
<td>15</td>
<td>Busy Flag</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
<td>MNUM</td>
<td>5:0</td>
<td>Message Number</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
<td>MNUM</td>
<td>4:0</td>
<td>Message Number</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
Register 10: CAN IF1 Command Mask (CANIFnCMSK), offset 0x024

Register 11: CAN IF2 Command Mask (CANIFnCMSK), offset 0x084

Reading the Command Mask registers provides status for various functions. Writing to the Command Mask registers specifies the transfer direction and selects which buffer registers are the source or target of the data transfer.

Note that when a read from the message object buffer occurs when the \textit{WRNRD} bit is clear and the \textit{CLRINTPND} and/or \textit{NEWDAT} bits are set, the interrupt pending and/or new data flags in the message object buffer are cleared.

**CAN IFn Command Mask (CANIFnCMSK)**

- **CAN0 base:** 0x4004.0000
- **CAN1 base:** 0x4004.1000
- **Offset 0x024**
- **Type RW, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>WRNRD</td>
<td>RW</td>
<td>0</td>
<td>Write, Not Read</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>MASK</td>
<td>RW</td>
<td>0</td>
<td>Access Mask Bits</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Interrupt pending and new data conditions in the message buffer can be cleared by reading from the buffer (\textit{WRNRD} = 0) when the \textit{CLRINTPND} and/or \textit{NEWDAT} bits are set.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>ARB</td>
<td>RW</td>
<td>0</td>
<td>Access Arbitration Bits</td>
</tr>
<tr>
<td>4</td>
<td>CONTROL</td>
<td>RW</td>
<td>0</td>
<td>Access Control Bits</td>
</tr>
<tr>
<td>3</td>
<td>CLRINTPND</td>
<td>RW</td>
<td>0</td>
<td>Clear Interrupt Pending Bit</td>
</tr>
<tr>
<td>2</td>
<td>NEWDAT / TXRQST</td>
<td>RW</td>
<td>0</td>
<td>NEWDAT / TXRQST Bit</td>
</tr>
</tbody>
</table>

**Access Arbitration Bits**

- **Value**: 0
  - **Description**: Arbitration bits unchanged.
- **Value**: 1
  - **Description**: Transfer ID + DIR + XTD + MSGVAL of the message object into the Interface registers.

**Access Control Bits**

- **Value**: 0
  - **Description**: Control bits unchanged.
- **Value**: 1
  - **Description**: Transfer control bits from the CANIFnMCTL register into the Interface registers.

**Clear Interrupt Pending Bit**

- **Value**: 0
  - **Description**: If WRNRD is clear, the interrupt pending status is transferred from the message buffer into the CANIFnMCTL register.
  - **Description**: If WRNRD is set, the INTPND bit in the message object remains unchanged.
- **Value**: 1
  - **Description**: If WRNRD is clear, the interrupt pending status is cleared in the message buffer. Note the value of this bit that is transferred to the CANIFnMCTL register always reflects the status of the bits before clearing.
  - **Description**: If WRNRD is set, the INTPND bit is cleared in the message object.

**NEWDAT / TXRQST Bit**

- **Value**: 0
  - **Description**: If WRNRD is clear, the value of the new data status is transferred from the message buffer into the CANIFnMCTL register.
  - **Description**: If WRNRD is set, a transmission is not requested.
- **Value**: 1
  - **Description**: If WRNRD is clear, the new data status is cleared in the message buffer. Note the value of this bit that is transferred to the CANIFnMCTL register always reflects the status of the bits before clearing.
  - **Description**: If WRNRD is set, a transmission is requested. Note that when this bit is set, the TXRQST bit in the CANIFnMCTL register is ignored.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DATAA</td>
<td>RW</td>
<td>0</td>
<td>Access Data Byte 0 to 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The function of this bit depends on the configuration of the WRNRD bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>DATAB</td>
<td>RW</td>
<td>0</td>
<td>Access Data Byte 4 to 7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The function of this bit depends on the configuration of the WRNRD bit as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 12: CAN IF1 Mask 1 (CANIF1MSK1), offset 0x028

Register 13: CAN IF2 Mask 1 (CANIF2MSK1), offset 0x088

The mask information provided in this register accompanies the data (CANIFnDAn), arbitration information (CANIFnARBn), and control information (CANIFnMCTL) to the message object in the message RAM. The mask is used with the ID bit in the CANIFnARBn register for acceptance filtering. Additional mask information is contained in the CANIFnMSK2 register.

CAN IFn Mask 1 (CANIFnMSK1)
CAN0 base: 0x4004.0000
CAN1 base: 0x4004.1000
Offset 0x028
Type RW, reset 0x0000.FFFF

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>MSK</td>
<td>RW</td>
<td>0xFFFF</td>
<td>Identifier Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When using a 29-bit identifier, these bits are used for bits [15:0] of the ID. The MSK field in the CANIFnMSK2 register are used for bits [28:16] of the ID. When using an 11-bit identifier, these bits are ignored.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 14: CAN IF1 Mask 2 (CANIFnMSK2), offset 0x02C
Register 15: CAN IF2 Mask 2 (CANIFnMSK2), offset 0x08C

This register holds extended mask information that accompanies the CANIFnMSK1 register.

**CAN IFn Mask 2 (CANIFnMSK2)**

<table>
<thead>
<tr>
<th>CAN0 base: 0x4004.0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN1 base: 0x4004.1000</td>
</tr>
<tr>
<td>Offset 0x02C</td>
</tr>
<tr>
<td>Type RW, reset 0x0000.FFFF</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15</td>
<td>MXTD</td>
<td>RW</td>
<td>1</td>
<td>Mask Extended Identifier</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>14</td>
<td>MDIR</td>
<td>RW</td>
<td>1</td>
<td>Mask Message Direction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>13</td>
<td>reserved</td>
<td>RO</td>
<td>1</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
### Controller Area Network (CAN) Module

#### Bit/Field, Name, Type, Reset, Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12:0</td>
<td>MSK</td>
<td>RW</td>
<td>0xFF</td>
<td>Identifier Mask</td>
</tr>
</tbody>
</table>

When using a 29-bit identifier, these bits are used for bits [28:16] of the ID. The MSK field in the CANIFnMSK1 register are used for bits [15:0] of the ID. When using an 11-bit identifier, MSK[12:2] are used for bits [10:0] of the ID.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The corresponding identifier field (ID) in the message object cannot inhibit the match in acceptance filtering.</td>
</tr>
<tr>
<td>1</td>
<td>The corresponding identifier field (ID) is used for acceptance filtering.</td>
</tr>
</tbody>
</table>
Register 16: CAN IF1 Arbitration 1 (CANIF1ARB1), offset 0x030

Register 17: CAN IF2 Arbitration 1 (CANIF2ARB1), offset 0x090

These registers hold the identifiers for acceptance filtering.

CAN IFn Arbitration 1 (CANIFnARB1)
CAN0 base: 0x4004.0000
CAN1 base: 0x4004.1000
Offset 0x030
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>ID</td>
<td>RW</td>
<td>0x0000</td>
<td>This bit field is used with the ID field in the CANIFnARB2 register to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>create the message identifier.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When using a 29-bit identifier, bits 15:0 of the CANIFnARB1 register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>are [15:0] of the ID, while bits 12:0 of the CANIFnARB2 register are</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>[28:16] of the ID.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When using an 11-bit identifier, these bits are not used.</td>
</tr>
</tbody>
</table>
Register 18: CAN IF1 Arbitration 2 (CANIFnARB2), offset 0x034
Register 19: CAN IF2 Arbitration 2 (CANIFnARB2), offset 0x094

These registers hold information for acceptance filtering.

**CAN IFn Arbitration 2 (CANIFnARB2)**

CAN0 base: 0x4004.0000  
CAN1 base: 0x4004.1000  
Offset 0x034  
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15</td>
<td>MSGVAL</td>
<td>RW</td>
<td>0</td>
<td>Message Valid</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The message object is ignored by the message handler.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: The message object is configured and ready to be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>considered by the message handler within the CAN controller.</td>
</tr>
<tr>
<td>14</td>
<td>XTD</td>
<td>RW</td>
<td>0</td>
<td>Extended Identifier</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: An 11-bit Standard Identifier is used for this message object.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: A 29-bit Extended Identifier is used for this message object.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>13</td>
<td>DIR</td>
<td>RW</td>
<td>0</td>
<td>Message Direction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>12:0</td>
<td>ID</td>
<td>RW</td>
<td>0x000</td>
<td>Message Identifier</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit field is used with the ID field in the CANIFnARB2 register to create the message identifier.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When using a 29-bit identifier, ID[15:0] of the CANIFnARB1 register are [15:0] of the ID, while these bits, ID[12:0], are [28:16] of the ID.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When using an 11-bit identifier, ID[12:2] are used for bits [10:0] of the ID. The ID field in the CANIFnARB1 register is ignored.</td>
</tr>
</tbody>
</table>
Register 20: CAN IF1 Message Control (CANIF1MCTL), offset 0x038
Register 21: CAN IF2 Message Control (CANIF2MCTL), offset 0x098

This register holds the control information associated with the message object to be sent to the Message RAM.

**CAN IFn Message Control (CANIFnMCTL)**

- CAN0 base: 0x4004.0000
- CAN1 base: 0x4004.1000
- Offset 0x038
- Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15</td>
<td>NEWDAT</td>
<td>RW</td>
<td>0</td>
<td>New Data</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td>No new data has been written into the data portion of this message object by the message handler since the last time this flag was cleared by the CPU.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The message handler or the CPU has written new data into the data portion of this message object.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>MSGLST</td>
<td>RW</td>
<td>0</td>
<td>Message Lost</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td>No message was lost since the last time this bit was cleared by the CPU.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The message handler stored a new message into this object when NEWDAT was set; the CPU has lost a message.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>INTPND</td>
<td>RW</td>
<td>0</td>
<td>Interrupt Pending</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td>This message object is not the source of an interrupt.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>This message object is the source of an interrupt. The interrupt identifier in the CANINT register points to this message object if there is not another interrupt source with a higher priority.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>12</td>
<td>UMASK</td>
<td>RW</td>
<td>0</td>
<td>Use Acceptance Mask</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Mask is ignored.</td>
</tr>
<tr>
<td>1</td>
<td>Use mask (MSK, MXTD, and MDIR bits in the CANIFnMSKn registers) for acceptance filtering.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>11</th>
<th>TXIE</th>
<th>RW</th>
<th>0</th>
<th>Transmit Interrupt Enable</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The INTPND bit in the CANIFnMCTL register is unchanged after a successful transmission of a frame.</td>
</tr>
<tr>
<td>1</td>
<td>The INTPND bit in the CANIFnMCTL register is set after a successful transmission of a frame.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>10</th>
<th>RXIE</th>
<th>RW</th>
<th>0</th>
<th>Receive Interrupt Enable</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The INTPND bit in the CANIFnMCTL register is unchanged after a successful reception of a frame.</td>
</tr>
<tr>
<td>1</td>
<td>The INTPND bit in the CANIFnMCTL register is set after a successful reception of a frame.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>9</th>
<th>RMTEN</th>
<th>RW</th>
<th>0</th>
<th>Remote Enable</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>At the reception of a remote frame, the TXRQST bit in the CANIFnMCTL register is left unchanged.</td>
</tr>
<tr>
<td>1</td>
<td>At the reception of a remote frame, the TXRQST bit in the CANIFnMCTL register is set.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>8</th>
<th>TXRQST</th>
<th>RW</th>
<th>0</th>
<th>Transmit Request</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>This message object is not waiting for transmission.</td>
</tr>
<tr>
<td>1</td>
<td>The transmission of this message object is requested and is not yet done.</td>
</tr>
</tbody>
</table>

**Note:** If the WRNRD and TXRQST bits in the CANIFnCMSK register are set, this bit is ignored.
Controller Area Network (CAN) Module

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>EOB</td>
<td>RW</td>
<td>0</td>
<td>End of Buffer</td>
</tr>
</tbody>
</table>

Value | Description
--- | ---
0 | Message object belongs to a FIFO Buffer and is not the last message object of that FIFO Buffer.
1 | Single message object or last message object of a FIFO Buffer.

This bit is used to concatenate two or more message objects (up to 32) to build a FIFO buffer. For a single message object (thus not belonging to a FIFO buffer), this bit must be set.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Data Length Code</td>
</tr>
</tbody>
</table>

Value | Description
--- | ---
0x0-0x8 | Specifies the number of bytes in the data frame.
0x9-0xF | Defaults to a data frame with 8 bytes.

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

The **DLC** field in the **CANIFnMCTL** register of a message object must be defined the same as in all the corresponding objects with the same identifier at other nodes. When the message handler stores a data frame, it writes **DLC** to the value given by the received message.
Register 22: CAN IF1 Data A1 (CANIF1DA1), offset 0x03C
Register 23: CAN IF1 Data A2 (CANIF1DA2), offset 0x040
Register 24: CAN IF1 Data B1 (CANIF1DB1), offset 0x044
Register 25: CAN IF1 Data B2 (CANIF1DB2), offset 0x048
Register 26: CAN IF2 Data A1 (CANIF2DA1), offset 0x09C
Register 27: CAN IF2 Data A2 (CANIF2DA2), offset 0x0A0
Register 28: CAN IF2 Data B1 (CANIF2DB1), offset 0x0A4
Register 29: CAN IF2 Data B2 (CANIF2DB2), offset 0x0A8

These registers contain the data to be sent or that has been received. In a CAN data frame, data byte 0 is the first byte to be transmitted or received and data byte 7 is the last byte to be transmitted or received. In CAN's serial bit stream, the MSB of each byte is transmitted first.

CAN IF\(n\) Data nn (CANIFnDnn)
CAN0 base: 0x4004.0000
CAN1 base: 0x4004.1000
Offset 0x03C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>DATA</td>
<td>RW</td>
<td>0x0000</td>
<td>Data The CANIFnDA1 registers contain data bytes 1 and 0; CANIFnDA2 data bytes 3 and 2; CANIFnDB1 data bytes 5 and 4; and CANIFnDB2 data bytes 7 and 6.</td>
</tr>
</tbody>
</table>
The `CANTXRQ1` and `CANTXRQ2` registers hold the TXRQST bits of the 32 message objects. By reading out these bits, the CPU can check which message object has a transmission request pending. The TXRQST bit of a specific message object can be changed by three sources: (1) the CPU via the CANIFnMCTL register, (2) the message handler state machine after the reception of a remote frame, or (3) the message handler state machine after a successful transmission.

The `CANTXRQ1` register contains the TXRQST bits of the first 16 message objects in the message RAM; the `CANTXRQ2` register contains the TXRQST bits of the second 16 message objects.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>TXRQST</td>
<td>RO</td>
<td>0x0000</td>
<td>Transmission Request Bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>yet done.</td>
</tr>
</tbody>
</table>
Register 32: CAN New Data 1 (CANNWDA1), offset 0x120

Register 33: CAN New Data 2 (CANNWDA2), offset 0x124

The CANNWDA1 and CANNWDA2 registers hold the NEWDAT bits of the 32 message objects. By reading these bits, the CPU can check which message object has its data portion updated. The NEWDAT bit of a specific message object can be changed by three sources: (1) the CPU via the CANIFnMCTL register, (2) the message handler state machine after the reception of a data frame, or (3) the message handler state machine after a successful transmission.

The CANNWDA1 register contains the NEWDAT bits of the first 16 message objects in the message RAM; the CANNWDA2 register contains the NEWDAT bits of the second 16 message objects.

---

**CAN New Data n (CANNWDAn)**

<table>
<thead>
<tr>
<th>CAN0 base: 0x4004.0000</th>
<th>CAN1 base: 0x4004.1000</th>
<th>Offset 0x120</th>
<th>Type RO, reset 0x0000.0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>

| 31:16     | reserved   | RO    | 0x0000 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |

| 15:0      | NEWDAT     | RO    | 0x0000 | New Data Bits |

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No new data has been written into the data portion of the corresponding message object by the message handler since the last time this flag was cleared by the CPU.</td>
</tr>
<tr>
<td>1</td>
<td>The message handler or the CPU has written new data into the data portion of the corresponding message object.</td>
</tr>
</tbody>
</table>
Register 34: CAN Message 1 Interrupt Pending (CANMSG1INT), offset 0x140
Register 35: CAN Message 2 Interrupt Pending (CANMSG2INT), offset 0x144

The CANMSG1INT and CANMSG2INT registers hold the INTPND bits of the 32 message objects. By reading these bits, the CPU can check which message object has an interrupt pending. The INTPND bit of a specific message object can be changed through two sources: (1) the CPU via the CANIFnMCTL register, or (2) the message handler state machine after the reception or transmission of a frame.

This field is also encoded in the CANINT register.

The CANMSG1INT register contains the INTPND bits of the first 16 message objects in the message RAM; the CANMSG2INT register contains the INTPND bits of the second 16 message objects.

<table>
<thead>
<tr>
<th>CAN Message n Interrupt Pending (CANMSGnINT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN0 base: 0x4004.0000</td>
</tr>
<tr>
<td>CAN1 base: 0x4004.1000</td>
</tr>
<tr>
<td>Offset 0x140</td>
</tr>
<tr>
<td>Type RO, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
<tr>
<td>RO</td>
<td>0</td>
</tr>
</tbody>
</table>

Bit/Field   Name   Type   Reset   Description
-----------------------------------------------------------------------
31:16        reserved RO       0x0000  Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

15:0          INTPND    RO       0x0000  Interrupt Pending Bits

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The corresponding message object is not the source of an interrupt.</td>
</tr>
<tr>
<td>1</td>
<td>The corresponding message object is the source of an interrupt.</td>
</tr>
</tbody>
</table>
Register 36: CAN Message 1 Valid (CANMSG1VAL), offset 0x160
Register 37: CAN Message 2 Valid (CANMSG2VAL), offset 0x164

The CANMSG1VAL and CANMSG2VAL registers hold the MSGVAL bits of the 32 message objects. By reading these bits, the CPU can check which message object is valid. The message valid bit of a specific message object can be changed with the CANIFnARB2 register.

The CANMSG1VAL register contains the MSGVAL bits of the first 16 message objects in the message RAM; the CANMSG2VAL register contains the MSGVAL bits of the second 16 message objects in the message RAM.

### CAN Message n Valid (CANMSGnVAL)

- **CAN0 base:** 0x4004.0000
- **CAN1 base:** 0x4004.1000
- **Offset 0x160**
- **Type RO, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>MSGVAL</td>
<td>RO</td>
<td>0x0000</td>
<td>Message Valid Bits</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td>0</td>
<td>The corresponding message object is not configured and is ignored by the message handler.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The corresponding message object is configured and should be considered by the message handler.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
18 Universal Serial Bus (USB) Controller

The TM4C123GH6PZ USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB Host, Device, or OTG functions. The controller complies with the USB 2.0 standard, which includes SUSPEND and RESUME signaling. 16 endpoints including two hard-wired for control transfers (one endpoint for IN and one endpoint for OUT) plus 14 endpoints defined by firmware along with a dynamic sizable FIFO support multiple packet queueing. µDMA access to the FIFO allows minimal interference from system software. Software-controlled connect and disconnect allows flexibility during USB device start-up. The controller complies with OTG Standard’s Session Request Protocol (SRP) and Host Negotiation Protocol (HNP).

The TM4C123GH6PZ USB module has the following features:

- Complies with USB-IF (Implementer’s Forum) certification standards
- USB 2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps) operation with integrated PHY
- 4 transfer types: Control, Interrupt, Bulk, and Isochronous
- 16 endpoints
  - 1 dedicated control IN endpoint and 1 dedicated control OUT endpoint
  - 7 configurable IN endpoints and 7 configurable OUT endpoints
- 4 KB dedicated endpoint memory: one endpoint may be defined for double-buffered 1023-byte isochronous packet size
- VBUS droop and valid ID detection and interrupt
- Efficient transfers using Micro Direct Memory Access Controller (µDMA)
  - Separate channels for transmit and receive for up to three IN endpoints and three OUT endpoints
  - Channel requests asserted when FIFO contains required amount of data
18.1 Block Diagram

Figure 18-1. USB Module Block Diagram

18.2 Signal Description

The following table lists the external signals of the USB controller and describes the function of each. Some USB controller signals are alternate functions for some GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for these USB signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the USB function. The number in parentheses is the encoding that must be programmed into the PMCn field in the GPIOPortControl (GPIOPCTL) register (page 702) to assign the USB signal to the specified GPIO port pin. The USB0VBUS and USB0ID signals are configured by clearing the appropriate DEN bit in the GPIO Digital Enable (GPIODEN) register. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659. The remaining signals (with the word "fixed" in the Pin Mux/Pin Assignment column) have a fixed pin assignment and function.

**Note:** When used in OTG mode, USB0VBUS and USB0ID do not require any configuration as they are dedicated pins for the USB controller and directly connect to the USB connector's VBUS and ID signals. If the USB controller is used as either a dedicated Host or Device, the DEVMODOTG and DEVMOD bits in the USB General-Purpose Control and Status (USBGPCS) register can be used to connect the USB0VBUS and USB0ID inputs to fixed levels internally, freeing the PB0 and PB1 pins for GPIO use. For proper self-powered Device operation, the VBUS value must still be monitored to assure that if the Host removes VBUS, the self-powered Device disables the D+/D- pull-up resistors. This function can be accomplished by connecting a standard GPIO to VBUS.

The termination resistors for the USB PHY have been added internally, and thus there is no need for external resistors. For a device, there is a 1.5 KOhm pull-up on the D+ and for a host there are 15 KOhm pull-downs on both D+ and D-.
### Table 18-1. USB Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB0DM</td>
<td>68</td>
<td>PJ0</td>
<td>I/O</td>
<td>Analog</td>
<td>Bidirectional differential data pin (D- per USB specification) for USB0.</td>
</tr>
<tr>
<td>USB0DP</td>
<td>69</td>
<td>PJ1</td>
<td>I/O</td>
<td>Analog</td>
<td>Bidirectional differential data pin (D+ per USB specification) for USB0.</td>
</tr>
<tr>
<td>USB0EPEN</td>
<td>3, 23, 39, 74</td>
<td>PD2 (8), PC6 (8), PF4 (8), PG4 (8)</td>
<td>O</td>
<td>TTL</td>
<td>Optionally used in Host mode to control an external power source to supply power to the USB.</td>
</tr>
<tr>
<td>USB0ID</td>
<td>70</td>
<td>PB0</td>
<td>I</td>
<td>Analog</td>
<td>This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).</td>
</tr>
<tr>
<td>USB0PFLT</td>
<td>4, 22, 37, 75</td>
<td>PD3 (8), PC7 (8), PF5 (8), PG5 (8)</td>
<td>I</td>
<td>TTL</td>
<td>Optionally used in Host mode by an external power source to indicate an error state by that power source.</td>
</tr>
<tr>
<td>USB0VBUS</td>
<td>71</td>
<td>PB1</td>
<td>I/O</td>
<td>Analog</td>
<td>This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.</td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

### 18.3 Functional Description

The TM4C123GH6PZ USB controller provides full OTG negotiation by supporting both the Session Request Protocol (SRP) and the Host Negotiation Protocol (HNP). The session request protocol allows devices on the B side of a cable to request the A side device turn on VBUS. The host negotiation protocol is used after the initial session request protocol has powered the bus and provides a method to determine which end of the cable will act as the Host controller. When the device is connected to non-OTG peripherals or devices, the controller can detect which cable end was used and provides a register to indicate if the controller should act as the Host or the Device controller. This indication and the mode of operation are handled automatically by the USB controller. This auto-detection allows the system to use a single A/B connector instead of having both A and B connectors in the system and supports full OTG negotiations with other OTG devices.

In addition, the USB controller provides support for connecting to non-OTG peripherals or Host controllers. The USB controller can be configured to act as either a dedicated Host or Device, in which case, the USB0VBUS and USB0ID signals can be used as GPIOs or any corresponding alternate functions. However, when the USB controller is acting as a self-powered Device, a GPIO input or analog comparator input must be connected to VBUS and configured to generate an interrupt when the VBUS level drops. This interrupt is used to disable the pull-up resistor on the USB0DP signal.

**Note:** When the USB module is in operation, MOSC must be the clock source, either with or without using the PLL, and the system clock must be at least 20 MHz.

### 18.3.1 Operation as a Device

This section describes the TM4C123GH6PZ USB controller’s actions when it is being used as a USB Device. Before the USB controller’s operating mode is changed from Device to Host or Host to Device, software must reset the USB controller by setting the USB0 bit in the **Software Reset**
Control 2 (SRCR2) register (see page 459). IN endpoints, OUT endpoints, entry into and exit from SUSPEND mode, and recognition of Start of Frame (SOF) are all described.

When in Device mode, IN transactions are controlled by an endpoint's transmit interface and use the transmit endpoint registers for the given endpoint. OUT transactions are handled with an endpoint's receive interface and use the receive endpoint registers for the given endpoint.

When configuring the size of the FIFOs for endpoints, take into account the maximum packet size for an endpoint.

- **Bulk.** Bulk endpoints should be the size of the maximum packet (up to 64 bytes) or twice the maximum packet size if double buffering is used (described further in the following section).
- **Interrupt.** Interrupt endpoints should be the size of the maximum packet (up to 64 bytes) or twice the maximum packet size if double buffering is used.
- **Isochronous.** Isochronous endpoints are more flexible and can be up to 1023 bytes.
- **Control.** It is also possible to specify a separate control endpoint for a USB Device. However, in most cases the USB Device should use the dedicated control endpoint on the USB controller's endpoint 0.

### 18.3.1.1 Endpoints

When operating as a Device, the USB controller provides two dedicated control endpoints (IN and OUT) and 14 configurable endpoints (7 IN and 7 OUT) that can be used for communications with a Host controller. The endpoint number and direction associated with an endpoint is directly related to its register designation. For example, when the Host is transmitting to endpoint 1, all configuration and data is in the endpoint 1 transmit register interface.

Endpoint 0 is a dedicated control endpoint used for all control transactions to endpoint 0 during enumeration or when any other control requests are made to endpoint 0. Endpoint 0 uses the first 64 bytes of the USB controller's FIFO RAM as a shared memory for both IN and OUT transactions.

The remaining 14 endpoints can be configured as control, bulk, interrupt, or isochronous endpoints. They should be treated as 7 configurable IN and 7 configurable OUT endpoints. The endpoint pairs are not required to have the same type for their IN and OUT endpoint configuration. For example, the OUT portion of an endpoint pair could be a bulk endpoint, while the IN portion of that endpoint pair could be an interrupt endpoint. The address and size of the FIFOs attached to each endpoint can be modified to fit the application's needs.

### 18.3.1.2 IN Transactions as a Device

When operating as a USB Device, data for IN transactions is handled through the FIFOs attached to the transmit endpoints. The sizes of the FIFOs for the 7 configurable IN endpoints are determined by the **USB Transmit FIFO Start Address (USBTXFIFOADD)** register. The maximum size of a data packet that may be placed in a transmit endpoint's FIFO for transmission is programmable and is determined by the value written to the **USB Maximum Transmit Data Endpoint n (USBTXMAXPn)** register for that endpoint. The endpoint's FIFO can also be configured to use double-packet or single-packet buffering. When double-packet buffering is enabled, two data packets can be buffered in the FIFO, which also requires that the FIFO is at least two packets in size. When double-packet buffering is disabled, only one packet can be buffered, even if the packet size is less than half the FIFO size.

**Note:** The maximum packet size set for any endpoint must not exceed the FIFO size. The **USBTXMAXPn** register should not be written to while data is in the FIFO as unexpected results may occur.
**Single-Packet Buffering**

If the size of the transmit endpoint's FIFO is less than twice the maximum packet size for this endpoint (as set in the USB Transmit Dynamic FIFO Sizing (USBTXFIFOSZ) register), only one packet can be buffered in the FIFO and single-packet buffering is required. When each packet is completely loaded into the transmit FIFO, the TXRDY bit in the USB Transmit Control and Status Endpoint n Low (USBTXCSRLn) register must be set. If the AUTOSET bit in the USB Transmit Control and Status Endpoint n High (USBTXCSRHn) register is set, the TXRDY bit is automatically set when a maximum-sized packet is loaded into the FIFO. For packet sizes less than the maximum, the TXRDY bit must be set manually. When the TXRDY bit is set, either manually or automatically, the packet is ready to be sent. When the packet has been successfully sent, both TXRDY and FIFONE are cleared, and the appropriate transmit endpoint interrupt signaled. At this point, the next packet can be loaded into the FIFO.

**Double-Packet Buffering**

If the size of the transmit endpoint's FIFO is at least twice the maximum packet size for this endpoint, two packets can be buffered in the FIFO and double-packet buffering is allowed. As each packet is loaded into the transmit FIFO, the TXRDY bit in the USBTXCSRLn register must be set. If the AUTOSET bit in the USBTXCSRHn register is set, the TXRDY bit is automatically set when a maximum-sized packet is loaded into the FIFO. For packet sizes less than the maximum, TXRDY must be set manually. When the TXRDY bit is set, either manually or automatically, the packet is ready to be sent. After the first packet is loaded, TXRDY is immediately cleared and an interrupt is generated. A second packet can now be loaded into the transmit FIFO and TXRDY set again (either manually or automatically if the packet is the maximum size). At this point, both packets are ready to be sent. After each packet has been successfully sent, TXRDY is automatically cleared and the appropriate transmit endpoint interrupt signaled to indicate that another packet can now be loaded into the transmit FIFO. The state of the FIFONE bit in the USBTXCSRLn register at this point indicates how many packets may be loaded. If the FIFONE bit is set, then another packet is in the FIFO and only one more packet can be loaded. If the FIFONE bit is clear, then no packets are in the FIFO and two more packets can be loaded.

**Note:** Double-packet buffering is disabled if an endpoint's corresponding EPn bit is set in the USB Transmit Double Packet Buffer Disable (USBTXDPKTBUFDIS) register. This bit is set by default, so it must be cleared to enable double-packet buffering.

**18.3.1.3 OUT Transactions as a Device**

When in Device mode, OUT transactions are handled through the USB controller receive FIFOs. The sizes of the receive FIFOs for the 7 configurable OUT endpoints are determined by the USB Receive FIFO Start Address (USBRXFIIFOADD) register. The maximum amount of data received by an endpoint in any packet is determined by the value written to the USB Maximum Receive Data Endpoint n (USBRXMAXPn) register for that endpoint. When double-packet buffering is enabled, two data packets can be buffered in the FIFO. When double-packet buffering is disabled, only one packet can be buffered even if the packet is less than half the FIFO size.

**Note:** In all cases, the maximum packet size must not exceed the FIFO size.

**Single-Packet Buffering**

If the size of the receive endpoint FIFO is less than twice the maximum packet size for an endpoint, only one data packet can be buffered in the FIFO and single-packet buffering is required. When a packet is received and placed in the receive FIFO, the RXRDY and FULL bits in the USB Receive Control and Status Endpoint n Low (USBRXCSRLn) register are set and the appropriate receive endpoint is signaled, indicating that a packet can now be unloaded from the FIFO. After the packet
has been unloaded, the RXRDY bit must be cleared in order to allow further packets to be received. This action also generates the acknowledge signaling to the Host controller. If the AUTOCL bit in the USB Receive Control and Status Endpoint n High (USBRXCSRHn) register is set and a maximum-sized packet is unloaded from the FIFO, the RXRDY and FULL bits are cleared automatically. For packet sizes less than the maximum, RXRDY must be cleared manually.

Double-Packet Buffering

If the size of the receive endpoint FIFO is at least twice the maximum packet size for the endpoint, two data packets can be buffered and double-packet buffering can be used. When the first packet is received and loaded into the receive FIFO, the RXRDY bit in the USBRXCSRLn register is set and the appropriate receive endpoint interrupt is signaled to indicate that a packet can now be unloaded from the FIFO.

Note: The FULL bit in USBRXCSRLn is not set when the first packet is received. It is only set if a second packet is received and loaded into the receive FIFO.

After each packet has been unloaded, the RXRDY bit must be cleared to allow further packets to be received. If the AUTOCL bit in the USBRXCSRHn register is set and a maximum-sized packet is unloaded from the FIFO, the RXRDY bit is cleared automatically. For packet sizes less than the maximum, RXRDY must be cleared manually. If the FULL bit is set when RXRDY is cleared, the USB controller first clears the FULL bit, then sets RXRDY again to indicate that there is another packet waiting in the FIFO to be unloaded.

Note: Double-packet buffering is disabled if an endpoint's corresponding EPn bit is set in the USB Receive Double Packet Buffer Disable (USBRXDPKTBUFDIS) register. This bit is set by default, so it must be cleared to enable double-packet buffering.

18.3.1.4 Scheduling

The Device has no control over the scheduling of transactions as scheduling is determined by the Host controller. The TM4C123GH6PZ USB controller can set up a transaction at any time. The USB controller waits for the request from the Host controller and generates an interrupt when the transaction is complete or if it was terminated due to some error. If the Host controller makes a request and the Device controller is not ready, the USB controller sends a busy response (NAK) to all requests until it is ready.

18.3.1.5 Additional Actions

The USB controller responds automatically to certain conditions on the USB bus or actions by the Host controller such as when the USB controller automatically stalls a control transfer or unexpected zero length OUT data packets.

Stalled Control Transfer

The USB controller automatically issues a STALL handshake to a control transfer under the following conditions:

1. The Host sends more data during an OUT data phase of a control transfer than was specified in the Device request during the SETUP phase. This condition is detected by the USB controller when the Host sends an OUT token (instead of an IN token) after the last OUT packet has been unloaded and the DATAEND bit in the USB Control and Status Endpoint 0 Low (USBCSRL0) register has been set.

2. The Host requests more data during an IN data phase of a control transfer than was specified in the Device request during the SETUP phase. This condition is detected by the USB controller...
when the Host sends an IN token (instead of an OUT token) after the CPU has cleared TXRDY and set DATAEND in response to the ACK issued by the Host to what should have been the last packet.

3. The Host sends more than USBRXMAXPn bytes of data with an OUT data token.

4. The Host sends more than a zero length data packet for the OUT STATUS phase.

Zero Length OUT Data Packets

A zero-length OUT data packet is used to indicate the end of a control transfer. In normal operation, such packets should only be received after the entire length of the Device request has been transferred.

However, if the Host sends a zero-length OUT data packet before the entire length of Device request has been transferred, it is signaling the premature end of the transfer. In this case, the USB controller automatically flushes any IN token ready for the data phase from the FIFO and sets the DATAEND bit in the USBCSRL0 register.

Setting the Device Address

When a Host is attempting to enumerate the USB Device, it requests that the Device change its address from zero to some other value. The address is changed by writing the value that the Host requested to the USB Device Functional Address (USBFADDR) register. However, care should be taken when writing to USBFADDR to avoid changing the address before the transaction is complete. This register should only be set after the SET_ADDRESS command is complete. Like all control transactions, the transaction is only complete after the Device has left the STATUS phase.

In the case of a SET_ADDRESS command, the transaction is completed by responding to the IN request from the Host with a zero-byte packet. Once the Device has responded to the IN request, the USBFADDR register should be programmed to the new value as soon as possible to avoid missing any new commands sent to the new address.

Note: If the USBFADDR register is set to the new value as soon as the Device receives the OUT transaction with the SET_ADDRESS command in the packet, it changes the address during the control transfer. In this case, the Device does not receive the IN request that allows the USB transaction to exit the STATUS phase of the control transfer because it is sent to the old address. As a result, the Host does not get a response to the IN request, and the Host fails to enumerate the Device.

18.3.1.6 Device Mode SUSPEND

When no activity has occurred on the USB bus for 3 ms, the USB controller automatically enters SUSPEND mode. If the SUSPEND interrupt has been enabled in the USB Interrupt Enable (USBIE) register, an interrupt is generated at this time. When in SUSPEND mode, the PHY also goes into SUSPEND mode. When RESUME signaling is detected, the USB controller exits SUSPEND mode and takes the PHY out of SUSPEND. If the RESUME interrupt is enabled, an interrupt is generated. The USB controller can also be forced to exit SUSPEND mode by setting the RESUME bit in the USB Power (USBPOWER) register. When this bit is set, the USB controller exits SUSPEND mode and drives RESUME signaling onto the bus. The RESUME bit must be cleared after 10 ms (a maximum of 15 ms) to end RESUME signaling.

To meet USB power requirements, the controller can be put into Deep Sleep mode which keeps the controller in a static state. Hibernation mode should not be used for SUSPEND mode because all internal state information is lost in hibernation.
Important: When configured as a self-powered Device, the USB module meets the response timing and power draw requirements for USB compliance of SUSPEND mode. When configured as a bus-powered Device, the USB can operate in SUSPEND mode but produces a higher power draw than required to be compliant.

18.3.1.7 Start-of-Frame
When the USB controller is operating in Device mode, it receives a Start-Of-Frame (SOF) packet from the Host once every millisecond. When the SOF packet is received, the 11-bit frame number contained in the packet is written into the USB Frame Value (USBFRAME) register, and an SOF interrupt is also signaled and can be handled by the application. Once the USB controller has started to receive SOF packets, it expects one every millisecond. If no SOF packet is received after 1.00358 ms, the packet is assumed to have been lost, and the USBFRAME register is not updated. The USB controller continues and resynchronizes these pulses to the received SOF packets when these packets are successfully received again.

18.3.1.8 USB RESET
When the USB controller is in Device mode and a RESET condition is detected on the USB bus, the USB controller automatically performs the following actions:

- Clears the USBFADDR register.
- Clears the USB Endpoint Index (USBEPIDX) register.
- Flushes all endpoint FIFOs.
- Clears all control/status registers.
- Enables all endpoint interrupts.
- Generates a RESET interrupt.

When the application software driving the USB controller receives a RESET interrupt, any open pipes are closed and the USB controller waits for bus enumeration to begin.

18.3.1.9 Connect/Disconnect
The USB controller connection to the USB bus is handled by software. The USB PHY can be switched between normal mode and non-driving mode by setting or clearing the SOFTCONN bit of the USBPOWER register. When the SOFTCONN bit is set, the PHY is placed in its normal mode, and the USB_DP/USB_DM lines of the USB bus are enabled. At the same time, the USB controller is placed into a state, in which it does not respond to any USB signaling except a USB RESET.

When the SOFTCONN bit is cleared, the PHY is put into non-driving mode, USB_DP and USB_DM are tristated, and the USB controller appears to other devices on the USB bus as if it has been disconnected. The non-driving mode is the default so the USB controller appears disconnected until the SOFTCONN bit has been set. The application software can then choose when to set the PHY into its normal mode. Systems with a lengthy initialization procedure may use this to ensure that initialization is complete, and the system is ready to perform enumeration before connecting to the USB bus. Once the SOFTCONN bit has been set, the USB controller can be disconnected by clearing this bit.

Note: The USB controller does not generate an interrupt when the Device is connected to the Host. However, an interrupt is generated when the Host terminates a session.
18.3.2 Operation as a Host

When the TM4C123GH6PZ USB controller is operating in Host mode, it can either be used for point-to-point communications with another USB device or, when attached to a hub, for communication with multiple devices. Before the USB controller's operating mode is changed from Host to Device or Device to Host, software must reset the USB controller by setting the USB0 bit in the Software Reset Control 2 (SRCR2) register (see page 459). Full-speed and low-speed USB devices are supported, both for point-to-point communication and for operation through a hub. The USB controller automatically carries out the necessary transaction translation needed to allow a low-speed or full-speed device to be used with a USB 2.0 hub. Control, bulk, isochronous, and interrupt transactions are supported. This section describes the USB controller's actions when it is being used as a USB Host. Configuration of IN endpoints, OUT endpoints, entry into and exit from SUSPEND mode, and RESET are all described.

When in Host mode, IN transactions are controlled by an endpoint's receive interface. All IN transactions use the receive endpoint registers and all OUT endpoints use the transmit endpoint registers for a given endpoint. As in Device mode, the FIFOs for endpoints should take into account the maximum packet size for an endpoint.

- **Bulk.** Bulk endpoints should be the size of the maximum packet (up to 64 bytes) or twice the maximum packet size if double buffering is used (described further in the following section).

- **Interrupt.** Interrupt endpoints should be the size of the maximum packet (up to 64 bytes) or twice the maximum packet size if double buffering is used.

- **Isochronous.** Isochronous endpoints are more flexible and can be up to 1023 bytes.

- **Control.** It is also possible to specify a separate control endpoint to communicate with a Device. However, in most cases the USB controller should use the dedicated control endpoint to communicate with a Device's endpoint 0.

18.3.2.1 Endpoints

The endpoint registers are used to control the USB endpoint interfaces which communicate with Device(s) that are connected. The endpoints consist of a dedicated control IN endpoint, a dedicated control OUT endpoint, 7 configurable OUT endpoints, and 7 configurable IN endpoints. The dedicated control interface can only be used for control transactions to endpoint 0 of Devices. These control transactions are used during enumeration or other control functions that communicate using endpoint 0 of Devices. This control endpoint shares the first 64 bytes of the USB controller's FIFO RAM for IN and OUT transactions. The remaining IN and OUT interfaces can be configured to communicate with control, bulk, interrupt, or isochronous Device endpoints.

These USB interfaces can be used to simultaneously schedule as many as 7 independent OUT and 7 independent IN transactions to any endpoints on any Device. The IN and OUT controls are paired in three sets of registers. However, they can be configured to communicate with different types of endpoints and different endpoints on Devices. For example, the first pair of endpoint controls can be split so that the OUT portion is communicating with a Device's bulk OUT endpoint 1, while the IN portion is communicating with a Device's interrupt IN endpoint 2.

Before accessing any Device, whether for point-to-point communications or for communications via a hub, the relevant USB Receive Functional Address Endpoint n (USBRXFUNCADDRn) or USB Transmit Functional Address Endpoint n (USBTXFUNCADDRn) registers must be set for each receive or transmit endpoint to record the address of the Device being accessed.
The USB controller also supports connections to Devices through a USB hub by providing a register that specifies the hub address and port of each USB transfer. The FIFO address and size are customizable and can be specified for each USB IN and OUT transfer. Customization includes allowing one FIFO per transaction, sharing a FIFO across transactions, and allowing for double-buffered FIFOs.

### 18.3.2.2 IN Transactions as a Host

IN transactions are handled in a similar manner to the way in which OUT transactions are handled when the USB controller is in Device mode except that the transaction first must be initiated by setting the \texttt{REQPKT} bit in the \texttt{USBCSRL0} register, indicating to the transaction scheduler that there is an active transaction on this endpoint. The transaction scheduler then sends an IN token to the target Device. When the packet is received and placed in the receive FIFO, the \texttt{RXRDY} bit in the \texttt{USBCSRL0} register is set, and the appropriate receive endpoint interrupt is signaled to indicate that a packet can now be unloaded from the FIFO.

When the packet has been unloaded, \texttt{RXRDY} must be cleared. The \texttt{AUTOCN} bit in the \texttt{USBXCSRHn} register can be used to have \texttt{RXRDY} automatically cleared when a maximum-sized packet has been unloaded from the FIFO. The \texttt{AUTORQ} bit in \texttt{USBXCSRHN} causes the \texttt{REQPKT} bit to be automatically set when the \texttt{RXRDY} bit is cleared. The \texttt{AUTOCN} and \texttt{AUTORQ} bits can be used with µDMA accesses to perform complete bulk transfers without main processor intervention. When the \texttt{RXRDY} bit is cleared, the controller sends an acknowledge to the Device. When there is a known number of packets to be transferred, the \texttt{USB Request Packet Count in Block Transfer Endpoint n (USBRQPKTCOUNTn)} register associated with the endpoint should be configured to the number of packets to be transferred. The USB controller decrements the value in the \texttt{USBRQPKTCOUNTn} register following each request. When the \texttt{USBRQPKTCOUNTn} value decrements to 0, the \texttt{AUTORQ} bit is cleared to prevent any further transactions being attempted. For cases where the size of the transfer is unknown, \texttt{USBRQPKTCOUNTn} should be cleared. \texttt{AUTORQ} then remains set until cleared by the reception of a short packet (that is, less than the \texttt{MAXLOAD} value in the \texttt{USBXMAXPn} register) such as may occur at the end of a bulk transfer.

If the Device responds to a bulk or interrupt IN token with a NAK, the USB Host controller keeps retrying the transaction until any NAK Limit that has been set has been reached. If the target Device responds with a STALL, however, the USB Host controller does not retry the transaction but sets the \texttt{STALLn} bit in the \texttt{USBCSRL0} register. If the target Device does not respond to the IN token within the required time, or the packet contained a CRC or bit-stuff error, the USB Host controller retries the transaction. If after three attempts the target Device has still not responded, the USB Host controller clears the \texttt{REQPKT} bit and sets the \texttt{ERROR} bit in the \texttt{USBCSRL0} register.

### 18.3.2.3 OUT Transactions as a Host

OUT transactions are handled in a similar manner to the way in which IN transactions are handled when the USB controller is in Device mode. The \texttt{TXRDY} bit in the \texttt{USBTXCSRn} register must be set as each packet is loaded into the transmit FIFO. Again, setting the \texttt{AUTOSER} bit in the \texttt{USBTXCSRn} register automatically sets \texttt{TXRDY} when a maximum-sized packet has been loaded into the FIFO. Furthermore, \texttt{AUTOSER} can be used with the µDMA controller to perform complete bulk transfers without software intervention.

If the target Device responds to the OUT token with a NAK, the USB Host controller keeps retrying the transaction until the NAK Limit that has been set has been reached. However, if the target Device responds with a STALL, the USB controller does not retry the transaction but interrupts the main processor by setting the \texttt{STALLn} bit in the \texttt{USBTXCSRn} register. If the target Device does not respond to the OUT token within the required time, or the packet contained a CRC or bit-stuff error, the USB Host controller retries the transaction. If after three attempts the target Device has still not responded, the USB Host controller flushes the FIFO and sets the \texttt{ERROR} bit in the \texttt{USBTXCSRn} register.
18.3.2.4 Transaction Scheduling

Scheduling of transactions is handled automatically by the USB Host controller. The Host controller allows configuration of the endpoint communication scheduling based on the type of endpoint transaction. Interrupt transactions can be scheduled to occur in the range of every frame to every 255 frames in 1 frame increments. Bulk endpoints do not allow scheduling parameters, but do allow for a NAK timeout in the event an endpoint on a Device is not responding. Isochronous endpoints can be scheduled from every frame to every $2^{16}$ frames, in powers of 2.

The USB controller maintains a frame counter. If the target Device is a full-speed device, the USB controller automatically sends an SOF packet at the start of each frame and increments the frame counter. If the target Device is a low-speed device, a $K$ state is transmitted on the bus to act as a keep-alive to stop the low-speed device from going into SUSPEND mode.

After the SOF packet has been transmitted, the USB Host controller cycles through all the configured endpoints looking for active transactions. An active transaction is defined as a receive endpoint for which the REQPKT bit is set or a transmit endpoint for which the TXRDY bit and/or the FIFONE bit is set.

An isochronous or interrupt transaction is started if the transaction is found on the first scheduler cycle of a frame and if the interval counter for that endpoint has counted down to zero. As a result, only one interrupt or isochronous transaction occurs per endpoint every $n$ frames, where $n$ is the interval set via the USB Host Transmit Interval Endpoint n (USBTXINTERVALn) or USB Host Receive Interval Endpoint n (USBRXINTERVALn) register for that endpoint.

An active bulk transaction starts immediately, provided sufficient time is left in the frame to complete the transaction before the next SOF packet is due. If the transaction must be retried (for example, because a NAK was received or the target Device did not respond), then the transaction is not retried until the transaction scheduler has first checked all the other endpoints for active transactions. This process ensures that an endpoint that is sending a lot of NAKs does not block other transactions on the bus. The controller also allows the user to specify a limit to the length of time for NAKs to be received from a target Device before the endpoint times out.

18.3.2.5 USB Hubs

The following setup requirements apply to the USB Host controller only if it is used with a USB hub. When a full- or low-speed Device is connected to the USB controller via a USB 2.0 hub, details of the hub address and the hub port also must be recorded in the corresponding USB Receive Hub Address Endpoint n (USBRXHUBADDRn) and USB Receive Hub Port Endpoint n (USBRXHUBPORTn) or the USB Transmit Hub Address Endpoint n (USBTXHUBADDRn) and USB Transmit Hub Port Endpoint n (USBTXHUBPORTn) registers. In addition, the speed at which the Device operates (full or low) must be recorded in the USB Type Endpoint 0 (USBTYPE0) (endpoint 0), USB Host Configure Transmit Type Endpoint n (USBTXTYPEEn), or USB Host Configure Receive Type Endpoint n (USBRXTYPEEn) registers for each endpoint that is accessed by the Device.

For hub communications, the settings in these registers record the current allocation of the endpoints to the attached USB Devices. To maximize the number of Devices supported, the USB Host controller allows this allocation to be changed dynamically by simply updating the address and speed information recorded in these registers. Any changes in the allocation of endpoints to Device functions must be made following the completion of any on-going transactions on the endpoints affected.

18.3.2.6 Babble

The USB Host controller does not start a transaction until the bus has been inactive for at least the minimum inter-packet delay. The controller also does not start a transaction unless it can be finished.
before the end of the frame. If the bus is still active at the end of a frame, then the USB Host controller assumes that the target Device to which it is connected has malfunctioned, and the USB controller suspends all transactions and generates a babble interrupt.

18.3.2.7 Host SUSPEND

If the SUSPEND bit in the USBPOWER register is set, the USB Host controller completes the current transaction then stops the transaction scheduler and frame counter. No further transactions are started and no SOF packets are generated.

To exit SUSPEND mode, set the RESUME bit and clear the SUSPEND bit. While the RESUME bit is set, the USB Host controller generates RESUME signaling on the bus. After 20 ms, the RESUME bit must be cleared, at which point the frame counter and transaction scheduler start. The Host supports the detection of a remote wake-up.

18.3.2.8 USB RESET

If the RESET bit in the USBPOWER register is set, the USB Host controller generates USB RESET signaling on the bus. The RESET bit must be set for at least 20 ms to ensure correct resetting of the target Device. After the CPU has cleared the bit, the USB Host controller starts its frame counter and transaction scheduler.

18.3.2.9 Connect/Disconnect

A session is started by setting the SESSION bit in the USB Device Control (USBDEVCTL) register, enabling the USB controller to wait for a Device to be connected. When a Device is detected, a connect interrupt is generated. The speed of the Device that has been connected can be determined by reading the USBDEVCTL register where the FSDEV bit is set for a full-speed Device, and the LSDEV bit is set for a low-speed Device. The USB controller must generate a RESET to the Device, and then the USB Host controller can begin Device enumeration. If the Device is disconnected while a session is in progress, a disconnect interrupt is generated.

18.3.3 OTG Mode

To conserve power, the USB On-The-Go (OTG) supplement allows VBUS to only be powered up when required and to be turned off when the bus is not in use. VBUS is always supplied by the A device on the bus. The USB OTG controller determines whether it is the A device or the B device by sampling the ID input from the PHY. This signal is pulled Low when an A-type plug is sensed (signifying that the USB OTG controller should act as the A device) but taken High when a B-type plug is sensed (signifying that the USB controller is a B device). Note that when switching between OTG A and OTG B, the USB controller retains all register contents.

18.3.3.1 Starting a Session

When the USB OTG controller is ready to start a session, the SESSION bit must be set in the USBDEVCTL register. The USB OTG controller then enables ID pin sensing. The ID input is either taken Low if an A-type connection is detected or High if a B-type connection is detected. The DEV bit in the USBDEVCTL register is also set to indicate whether the USB OTG controller has adopted the role of the A device or the B device. The USB OTG controller also provides an interrupt to indicate that ID pin sensing has completed and the mode value in the USBDEVCTL register is valid. This interrupt is enabled in the USBDIVM register, and the status is checked in the USBDIVISC register. As soon as the USB controller has detected that it is on the A side of the cable, it must enable VBUS power within 100ms or the USB controller reverts to Device mode.

If the USB OTG controller is the A device, then the USB OTG controller enters Host mode (the A device is always the default Host), turns on VBUS, and waits for VBUS to go above the VBUS Valid
threshold, as indicated by the VBUS bit in the USBDEVCTL register going to 0x3. The USB OTG controller then waits for a peripheral to be connected. When a peripheral is detected, a Connect interrupt is signaled and either the FSDEV or LSDEV bit in the USBDEVCTL register is set, depending whether a full-speed or a low-speed peripheral is detected. The USB controller then issues a RESET to the connected Device. The SESSION bit in the USBDEVCTL register can be cleared to end a session. The USB OTG controller also automatically ends the session if babble is detected or if VBUS drops below session valid.

**Note:** The USB OTG controller may not remain in Host mode when connected to high-current devices. Some devices draw enough current to momentarily drop VBUS below the VBUS-valid level causing the controller to drop out of Host mode. The only way to get back into Host mode is to allow VBUS to go below the Session End level. In this situation, the device is causing VBUS to drop repeatedly and pull VBUS back low the next time VBUS is enabled.

In addition, the USB OTG controller may not remain in Host mode when a device is told that it can start using it’s active configuration. At this point the device starts drawing more current and can also drop VBUS below VBUS valid.

If the USB OTG controller is the B device, then the USB OTG controller requests a session using the session request protocol defined in the USB On-The-Go supplement, that is, it first discharges VBUS. Then when VBUS has gone below the Session End threshold (VBUS bit in the USBDEVCTL register goes to 0x0) and the line state has been a single-ended zero for > 2 ms, the USB OTG controller pulses the data line, then pulses VBUS. At the end of the session, the SESSION bit is cleared either by the USB OTG controller or by the application software. The USB OTG controller then causes the PHY to switch out the pull-up resistor on D+, signaling the A device to end the session.

### 18.3.3.2 Detecting Activity

When the other device of the OTG setup wishes to start a session, it either raises VBUS above the Session Valid threshold if it is the A device, or if it is the B device, it pulses the data line then pulses VBUS. Depending on which of these actions happens, the USB controller can determine whether it is the A device or the B device in the current setup and act accordingly. If VBUS is raised above the Session Valid threshold, then the USB controller is the B device. The USB controller sets the SESSION bit in the USBDEVCTL register. When RESET signaling is detected on the bus, a RESET interrupt is signaled, which is interpreted as the start of a session.

The USB controller is in Device mode as the B device is the default mode. At the end of the session, the A device turns off the power to VBUS. When VBUS drops below the Session Valid threshold, the USB controller detects this drop and clears the SESSION bit to indicate that the session has ended, causing a disconnect interrupt to be signaled. If data line and VBUS pulsing is detected, then the USB controller is the A device. The controller generates a SESSION REQUEST interrupt to indicate that the B device is requesting a session. The SESSION bit in the USBDEVCTL register must be set to start a session.

### 18.3.3.3 Host Negotiation

When the USB controller is the A device, ID is Low, and the controller automatically enters Host mode when a session starts. When the USB controller is the B device, ID is High, and the controller automatically enters Device mode when a session starts. However, software can request that the USB controller become the Host by setting the HOSTREQ bit in the USBDEVCTL register. This bit can be set either at the same time as requesting a Session Start by setting the SESSION bit in the USBDEVCTL register or at any time after a session has started. When the USB controller next enters SUSPEND mode and if the HOSTREQ bit remains set, the controller enters Host mode and
begins host negotiation (as specified in the USB On-The-Go supplement) by causing the PHY to
disconnect the pull-up resistor on the D+ line, causing the A device to switch to Device mode and
connect its own pull-up resistor. When the USB controller detects this, a Connect interrupt is
generated and the \texttt{RESET} bit in the \texttt{USBPOWER} register is set to begin resetting the A device. The
USB controller begins this reset sequence automatically to ensure that \texttt{RESET} is started as required
within 1 ms of the A device connecting its pull-up resistor. The main processor should wait at least
20 ms, then clear the \texttt{RESET} bit and enumerate the A device.

When the USB OTG controller B device has finished using the bus, the USB controller goes into
\texttt{SUSPEND} mode by setting the \texttt{SUSPEND} bit in the \texttt{USBPOWER} register. The A device detects this
and either terminates the session or reverts to Host mode. If the A device is USB OTG controller,
it generates a Disconnect interrupt.

\section*{18.3.4 DMA Operation}

The USB peripheral provides an interface connected to the \texttt{μDMA} controller with separate channels
for 3 transmit endpoints and 3 receive endpoints. Software selects which endpoints to service with
the \texttt{μDMA} channels using the \texttt{USB DMA Select (USBDMASEL)} register. The \texttt{μDMA} operation of
the USB is enabled through the \texttt{USBTXCSRhn} and \texttt{USBXCSRhn} registers, for the TX and RX
channels respectively. When \texttt{μDMA} operation is enabled, the USB asserts a \texttt{μDMA} request on the
enabled receive or transmit channel when the associated FIFO can transfer data. When either FIFO
can transfer data, the burst request for that channel is asserted. The \texttt{μDMA} channel must be
configured to operate in Basic mode, and the size of the \texttt{μDMA} transfer must be restricted to whole
multiples of the size of the USB FIFO. Both read and write transfers of the USB FIFOs using \texttt{μDMA}
must be configured in this manner. For example, if the USB endpoint is configured with a FIFO size
of 64 bytes, the \texttt{μDMA} channel can be used to transfer 64 bytes to or from the endpoint FIFO. If the
number of bytes to transfer is less than 64, then a programmed I/O method must be used to copy
the data to or from the FIFO.

If the \texttt{DMAMOD} bit in the \texttt{USBTXCSRhn/USBXCSRhn} register is clear, an interrupt is generated
after every packet is transferred, but the \texttt{μDMA} continues transferring data. If the \texttt{DMAMOD} bit is set,
an interrupt is generated only when the entire \texttt{μDMA} transfer is complete. The interrupt occurs on
the USB interrupt vector. Therefore, if interrupts are used for USB operation and the \texttt{μDMA} is
enabled, the USB interrupt handler must be designed to handle the \texttt{μDMA} completion interrupt.

Care must be taken when using the \texttt{μDMA} to unload the receive FIFO as data is read from the
receive FIFO in 4 byte chunks regardless of value of the \texttt{MAXLOAD} field in the \texttt{USBXCSRhn}
register. The \texttt{RXRDY} bit is cleared as follows.

\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
Value & Description \tabularnewline \hline
0 & MAXLOAD = 64 bytes \tabularnewline 1 & MAXLOAD = 61 bytes \tabularnewline 2 & MAXLOAD = 62 bytes \tabularnewline 3 & MAXLOAD = 63 bytes \tabularnewline \hline
\end{tabular}
\caption{Table 18-2. Remainder (MAXLOAD/4)}
\end{table}

\begin{table}[h]
\centering
\begin{tabular}{|c|c|}
\hline
Value & Description \tabularnewline \hline
0 & MAXLOAD \tabularnewline 1 & MAXLOAD+3 \tabularnewline 2 & MAXLOAD+2 \tabularnewline \hline
\end{tabular}
\caption{Table 18-3. Actual Bytes Read}
\end{table}
Table 18-3. Actual Bytes Read (continued)

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>MAXLOAD+1</td>
</tr>
</tbody>
</table>

Table 18-4. Packet Sizes That Clear RXRDY

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>MAXLOAD, MAXLOAD-1, MAXLOAD-2, MAXLOAD-3</td>
</tr>
<tr>
<td>1</td>
<td>MAXLOAD</td>
</tr>
<tr>
<td>2</td>
<td>MAXLOAD, MAXLOAD-1</td>
</tr>
<tr>
<td>3</td>
<td>MAXLOAD, MAXLOAD-1, MAXLOAD-2</td>
</tr>
</tbody>
</table>

To enable DMA operation for the endpoint receive channel, the DMAEN bit of the USBRXCSRHn register should be set. To enable DMA operation for the endpoint transmit channel, the DMAEN bit of the USBTXCSRHn register must be set.

See “Micro Direct Memory Access (μDMA)” on page 595 for more details about programming the μDMA controller.

18.4 Initialization and Configuration

To use the USB Controller, the peripheral clock must be enabled via the RCGCUSB register (see page 353). In addition, the clock to the appropriate GPIO module must be enabled via the RCGCGPIO register in the System Control module (see page 342). To find out which GPIO port to enable, refer to Table 23-4 on page 1377. Configure the PMCn fields in the GPIOPCTL register to assign the USB signals to the appropriate pins (see page 702 and Table 23-5 on page 1386).

The initial configuration in all cases requires that the processor enable the USB controller and USB controller's physical layer interface (PHY) before setting any registers. The next step is to enable the USB PLL so that the correct clocking is provided to the PHY. To ensure that voltage is not supplied to the bus incorrectly, the external power control signal, USB0EPEN, should be negated on start up by configuring the USB0EPEN and USB0PFLT pins to be controlled by the USB controller and not exhibit their default GPIO behavior.

**Note:** When used in OTG mode, USB0VBUS and USB0ID do not require any configuration as they are dedicated pins for the USB controller and directly connect to the USB connector's VBUS and ID signals. If the USB controller is used as either a dedicated Host or Device, the DEVMODOTG and DEVMOD bits in the USB General-Purpose Control and Status (USBGPCS) register can be used to connect the USB0VBUS and USB0ID inputs to fixed levels internally, freeing the PB0 and PB1 pins for GPIO use. For proper self-powered Device operation, the VBUS value must still be monitored to assure that if the Host removes VBUS, the self-powered Device disables the D+/D- pull-up resistors. This function can be accomplished by connecting a standard GPIO to VBUS.

The termination resistors for the USB PHY have been added internally, and thus there is no need for external resistors. For a device, there is a 1.5 KOhm pull-up on the D+ and for a host there are 15 KOhm pull-downs on both D+ and D-.

18.4.1 Pin Configuration

When using the Device controller portion of the USB controller in a system that also provides Host functionality, the power to VBUS must be disabled to allow the external Host controller to supply power. Usually, the USB0EPEN signal is used to control the external regulator and should be negated to avoid having two devices driving the USB0VUSB power pin on the USB connector.
When the USB controller is acting as a Host, it is in control of two signals that are attached to an external voltage supply that provides power to VBUS. The Host controller uses the USB0EPEN signal to enable or disable power to the USB0VBUS pin on the USB connector. An input pin, USB0PFLT, provides feedback when there has been a power fault on VBUS. The USB0PFLT signal can be configured to either automatically negate the USB0EPEN signal to disable power, and/or it can generate an interrupt to the interrupt controller to allow software to handle the power fault condition. The polarity and actions related to both USB0EPEN and USB0PFLT are fully configurable in the USB controller. The controller also provides interrupts on Device insertion and removal to allow the Host controller code to respond to these external events.

18.4.2 Endpoint Configuration

To start communication in Host or Device mode, the endpoint registers must first be configured. In Host mode, this configuration establishes a connection between an endpoint register and an endpoint on a Device. In Device mode, an endpoint must be configured before enumerating to the Host controller.

In both cases, the endpoint 0 configuration is limited because it is a fixed-function, fixed-FIFO-size endpoint. In Device and Host modes, the endpoint requires little setup but does require a software-based state machine to progress through the setup, data, and status phases of a standard control transaction. In Device mode, the configuration of the remaining endpoints is done once before enumerating and then only changed if an alternate configuration is selected by the Host controller. In Host mode, the endpoints must be configured to operate as control, bulk, interrupt or isochronous mode. Once the type of endpoint is configured, a FIFO area must be assigned to each endpoint. In the case of bulk, control and interrupt endpoints, each has a maximum of 64 bytes per transaction. Isochronous endpoints can have packets with up to 1023 bytes per packet. In either mode, the maximum packet size for the given endpoint must be set prior to sending or receiving data.

Configuring each endpoint’s FIFO involves reserving a portion of the overall USB FIFO RAM to each endpoint. The total FIFO RAM available is 2 Kbytes with the first 64 bytes reserved for endpoint 0. The endpoint’s FIFO must be at least as large as the maximum packet size. The FIFO can also be configured as a double-buffered FIFO so that interrupts occur at the end of each packet and allow filling the other half of the FIFO.

If operating as a Device, the USB Device controller’s soft connect must be enabled when the Device is ready to start communications, indicating to the Host controller that the Device is ready to start the enumeration process. If operating as a Host controller, the Device soft connect must be disabled and power must be provided to VBUS via the USB0EPEN signal.

18.5 Register Map

Table 18-5 on page 1135 lists the registers. All addresses given are relative to the USB base address of 0x4005.0000. Note that the USB controller clock must be enabled before the registers can be programmed (see page 353). There must be a delay of 3 system clocks after the USB module clock is enabled before any USB module registers are accessed.

Table 18-5. Universal Serial Bus (USB) Controller Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>USBFADDR</td>
<td>RW</td>
<td>0x00</td>
<td>USB Device Functional Address</td>
<td>1143</td>
</tr>
<tr>
<td>0x001</td>
<td>USBPOWER</td>
<td>RW</td>
<td>0x20</td>
<td>USB Power</td>
<td>1144</td>
</tr>
</tbody>
</table>
### Table 18-5. Universal Serial Bus (USB) Controller Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x002</td>
<td>USBTXIS</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Transmit Interrupt Status</td>
<td>1147</td>
</tr>
<tr>
<td>0x004</td>
<td>USBRXIS</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Receive Interrupt Status</td>
<td>1149</td>
</tr>
<tr>
<td>0x006</td>
<td>USBTXIE</td>
<td>RW</td>
<td>0xFFFF</td>
<td>USB Transmit Interrupt Enable</td>
<td>1150</td>
</tr>
<tr>
<td>0x008</td>
<td>USBRXIE</td>
<td>RW</td>
<td>0xFFFE</td>
<td>USB Receive Interrupt Enable</td>
<td>1152</td>
</tr>
<tr>
<td>0x00A</td>
<td>USBSIS</td>
<td>RO</td>
<td>0x00</td>
<td>USB General Interrupt Status</td>
<td>1153</td>
</tr>
<tr>
<td>0x00B</td>
<td>USBIE</td>
<td>RW</td>
<td>0x06</td>
<td>USB Interrupt Enable</td>
<td>1156</td>
</tr>
<tr>
<td>0x00C</td>
<td>USBFRAME</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Frame Value</td>
<td>1159</td>
</tr>
<tr>
<td>0x00E</td>
<td>USBEPIDX</td>
<td>RW</td>
<td>0x00</td>
<td>USB Endpoint Index</td>
<td>1160</td>
</tr>
<tr>
<td>0x00F</td>
<td>USBTEST</td>
<td>RW</td>
<td>0x00</td>
<td>USB Test Mode</td>
<td>1161</td>
</tr>
<tr>
<td>0x020</td>
<td>USBFIFO0</td>
<td>RW</td>
<td>0x0000 .0000</td>
<td>USB FIFO Endpoint 0</td>
<td>1163</td>
</tr>
<tr>
<td>0x024</td>
<td>USBFIFO1</td>
<td>RW</td>
<td>0x0000 .0000</td>
<td>USB FIFO Endpoint 1</td>
<td>1163</td>
</tr>
<tr>
<td>0x028</td>
<td>USBFIFO2</td>
<td>RW</td>
<td>0x0000 .0000</td>
<td>USB FIFO Endpoint 2</td>
<td>1163</td>
</tr>
<tr>
<td>0x02C</td>
<td>USBFIFO3</td>
<td>RW</td>
<td>0x0000 .0000</td>
<td>USB FIFO Endpoint 3</td>
<td>1163</td>
</tr>
<tr>
<td>0x030</td>
<td>USBFIFO4</td>
<td>RW</td>
<td>0x0000 .0000</td>
<td>USB FIFO Endpoint 4</td>
<td>1163</td>
</tr>
<tr>
<td>0x034</td>
<td>USBFIFO5</td>
<td>RW</td>
<td>0x0000 .0000</td>
<td>USB FIFO Endpoint 5</td>
<td>1163</td>
</tr>
<tr>
<td>0x038</td>
<td>USBFIFO6</td>
<td>RW</td>
<td>0x0000 .0000</td>
<td>USB FIFO Endpoint 6</td>
<td>1163</td>
</tr>
<tr>
<td>0x03C</td>
<td>USBFIFO7</td>
<td>RW</td>
<td>0x0000 .0000</td>
<td>USB FIFO Endpoint 7</td>
<td>1163</td>
</tr>
<tr>
<td>0x060</td>
<td>USBDEVCTL</td>
<td>RW</td>
<td>0x80</td>
<td>USB Device Control</td>
<td>1164</td>
</tr>
<tr>
<td>0x062</td>
<td>USBTXFIFOSZ</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Dynamic FIFO Sizing</td>
<td>1166</td>
</tr>
<tr>
<td>0x063</td>
<td>USBRXFIFOSZ</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Dynamic FIFO Sizing</td>
<td>1166</td>
</tr>
<tr>
<td>0x064</td>
<td>USBTXFIFOADD</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Transmit FIFO Start Address</td>
<td>1167</td>
</tr>
<tr>
<td>0x066</td>
<td>USBRXFIFOADD</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Receive FIFO Start Address</td>
<td>1167</td>
</tr>
<tr>
<td>0x07A</td>
<td>USBCONTIM</td>
<td>RW</td>
<td>0x5C</td>
<td>USB Connect Timing</td>
<td>1168</td>
</tr>
<tr>
<td>0x07B</td>
<td>USBVPLEN</td>
<td>RW</td>
<td>0x3C</td>
<td>USB OTG VBUS Pulse Timing</td>
<td>1169</td>
</tr>
<tr>
<td>0x07D</td>
<td>USBFSEOF</td>
<td>RW</td>
<td>0x77</td>
<td>USB Full-Speed Last Transaction to End of Frame Timing</td>
<td>1170</td>
</tr>
<tr>
<td>0x07E</td>
<td>USBLSEOF</td>
<td>RW</td>
<td>0x72</td>
<td>USB Low-Speed Last Transaction to End of Frame Timing</td>
<td>1171</td>
</tr>
<tr>
<td>0x080</td>
<td>USBTXFUNCADDR0</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Functional Address Endpoint 0</td>
<td>1172</td>
</tr>
<tr>
<td>0x082</td>
<td>USBTXHUBADDR0</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Address Endpoint 0</td>
<td>1173</td>
</tr>
<tr>
<td>0x083</td>
<td>USBTXHUBPORT0</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 0</td>
<td>1174</td>
</tr>
<tr>
<td>0x088</td>
<td>USBTXFUNCADDR1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Functional Address Endpoint 1</td>
<td>1172</td>
</tr>
<tr>
<td>0x08A</td>
<td>USBTXHUBADDR1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Address Endpoint 1</td>
<td>1173</td>
</tr>
</tbody>
</table>
Table 18-5. Universal Serial Bus (USB) Controller Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x08B</td>
<td>USBTXHUBPORT1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 1</td>
<td>1174</td>
</tr>
<tr>
<td>0x08C</td>
<td>USBRXFUNCADDR1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Functional Address Endpoint 1</td>
<td>1175</td>
</tr>
<tr>
<td>0x08E</td>
<td>USBRHUBADDR1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 1</td>
<td>1176</td>
</tr>
<tr>
<td>0x08F</td>
<td>USBTXHUBPORT1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Port Endpoint 1</td>
<td>1177</td>
</tr>
<tr>
<td>0x090</td>
<td>USBTXFUNCADDR2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Functional Address Endpoint 2</td>
<td>1172</td>
</tr>
<tr>
<td>0x092</td>
<td>USBTXHUBADDR2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Address Endpoint 2</td>
<td>1173</td>
</tr>
<tr>
<td>0x093</td>
<td>USBTXHUBPORT2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 2</td>
<td>1174</td>
</tr>
<tr>
<td>0x094</td>
<td>USBRXFUNCADDR2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Functional Address Endpoint 2</td>
<td>1175</td>
</tr>
<tr>
<td>0x096</td>
<td>USBRHUBADDR2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 2</td>
<td>1176</td>
</tr>
<tr>
<td>0x097</td>
<td>USBTXHUBPORT2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 2</td>
<td>1177</td>
</tr>
<tr>
<td>0x098</td>
<td>USBTXFUNCADDR3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Functional Address Endpoint 3</td>
<td>1172</td>
</tr>
<tr>
<td>0x09A</td>
<td>USBRHUBADDR3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 3</td>
<td>1173</td>
</tr>
<tr>
<td>0x09B</td>
<td>USBTXHUBPORT3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 3</td>
<td>1174</td>
</tr>
<tr>
<td>0x09C</td>
<td>USBRXFUNCADDR3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Functional Address Endpoint 3</td>
<td>1175</td>
</tr>
<tr>
<td>0x09E</td>
<td>USBTXHUBADDR3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 3</td>
<td>1176</td>
</tr>
<tr>
<td>0x09F</td>
<td>USBTXHUBPORT3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 3</td>
<td>1177</td>
</tr>
<tr>
<td>0xA0</td>
<td>USBTXFUNCADDR4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Functional Address Endpoint 4</td>
<td>1172</td>
</tr>
<tr>
<td>0xA2</td>
<td>USBRHUBADDR4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 4</td>
<td>1173</td>
</tr>
<tr>
<td>0xA3</td>
<td>USBTXHUBPORT4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 4</td>
<td>1174</td>
</tr>
<tr>
<td>0xA4</td>
<td>USBRHUBADDR4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 4</td>
<td>1175</td>
</tr>
<tr>
<td>0xA6</td>
<td>USBTXHUBPORT4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 4</td>
<td>1177</td>
</tr>
<tr>
<td>0xA7</td>
<td>USBRHUBADDR5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 5</td>
<td>1173</td>
</tr>
<tr>
<td>0xA8</td>
<td>USBTXHUBADDR5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Address Endpoint 5</td>
<td>1173</td>
</tr>
<tr>
<td>0xAA</td>
<td>USBRHUBADDR5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 5</td>
<td>1176</td>
</tr>
<tr>
<td>0xAB</td>
<td>USBRHUBADDR5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 5</td>
<td>1177</td>
</tr>
<tr>
<td>0xAC</td>
<td>USBRHUBADDR6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 6</td>
<td>1172</td>
</tr>
<tr>
<td>0xAE</td>
<td>USBRHUBADDR6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 5</td>
<td>1173</td>
</tr>
<tr>
<td>0xB0</td>
<td>USBRHUBADDR6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Address Endpoint 6</td>
<td>1173</td>
</tr>
<tr>
<td>0xB2</td>
<td>USBRHUBADDR6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Address Endpoint 6</td>
<td>1173</td>
</tr>
<tr>
<td>0xB3</td>
<td>USBTXHUBPORT6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 6</td>
<td>1174</td>
</tr>
<tr>
<td>0xB4</td>
<td>USBRHUBADDR6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Functional Address Endpoint 6</td>
<td>1175</td>
</tr>
</tbody>
</table>
### Table 18-5. Universal Serial Bus (USB) Controller Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0B6</td>
<td>USBRXHUBADDR6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Address Endpoint 6</td>
<td>1176</td>
</tr>
<tr>
<td>0x0B7</td>
<td>USBRXHUBPORT6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Port Endpoint 6</td>
<td>1177</td>
</tr>
<tr>
<td>0x0B8</td>
<td>USBTXFUNCADDR7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Functional Address Endpoint 7</td>
<td>1172</td>
</tr>
<tr>
<td>0x0B9</td>
<td>USBTXHUBADDR7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Address Endpoint 7</td>
<td>1173</td>
</tr>
<tr>
<td>0x0BB</td>
<td>USBTXHUBPORT7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Hub Port Endpoint 7</td>
<td>1174</td>
</tr>
<tr>
<td>0x0BF</td>
<td>USBRXHUBPORT7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Hub Port Endpoint 7</td>
<td>1177</td>
</tr>
<tr>
<td>0x102</td>
<td>USBCSRL0</td>
<td>W1C</td>
<td>0x00</td>
<td>USB Control and Status Endpoint 0 Low</td>
<td>1179</td>
</tr>
<tr>
<td>0x103</td>
<td>USBCSRH0</td>
<td>W1C</td>
<td>0x00</td>
<td>USB Control and Status Endpoint 0 High</td>
<td>1183</td>
</tr>
<tr>
<td>0x108</td>
<td>USBCOUNT0</td>
<td>RO</td>
<td>0x00</td>
<td>USB Receive Byte Count Endpoint 0</td>
<td>1185</td>
</tr>
<tr>
<td>0x10A</td>
<td>USBTYPE0</td>
<td>RW</td>
<td>0x00</td>
<td>USB Type Endpoint 0</td>
<td>1186</td>
</tr>
<tr>
<td>0x10B</td>
<td>USBNACLMT</td>
<td>RW</td>
<td>0x0000</td>
<td>USB NAK Limit</td>
<td>1187</td>
</tr>
<tr>
<td>0x110</td>
<td>USBTXMAXP1</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Transmit Data Endpoint 1</td>
<td>1178</td>
</tr>
<tr>
<td>0x112</td>
<td>USBTXCSR1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 1 Low</td>
<td>1188</td>
</tr>
<tr>
<td>0x113</td>
<td>USBTXSRH1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 1 High</td>
<td>1192</td>
</tr>
<tr>
<td>0x114</td>
<td>USBRXMAXP1</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Receive Data Endpoint 1</td>
<td>1196</td>
</tr>
<tr>
<td>0x116</td>
<td>USBRXCSR1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 1 Low</td>
<td>1197</td>
</tr>
<tr>
<td>0x117</td>
<td>USBRXSRH1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 1 High</td>
<td>1202</td>
</tr>
<tr>
<td>0x118</td>
<td>USBRXCOUNT1</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Receive Byte Count Endpoint 1</td>
<td>1206</td>
</tr>
<tr>
<td>0x11A</td>
<td>USBTXTYPE1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Configure Type Endpoint 1</td>
<td>1207</td>
</tr>
<tr>
<td>0x11B</td>
<td>USBTXINTERFACE1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Interval Endpoint 1</td>
<td>1209</td>
</tr>
<tr>
<td>0x11C</td>
<td>USBRXTYPE1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Configure Receive Type Endpoint 1</td>
<td>1210</td>
</tr>
<tr>
<td>0x11D</td>
<td>USBRXINTERFACE1</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Receive Polling Interval Endpoint 1</td>
<td>1212</td>
</tr>
<tr>
<td>0x120</td>
<td>USBTXMAXP2</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Transmit Data Endpoint 2</td>
<td>1178</td>
</tr>
<tr>
<td>0x122</td>
<td>USBTXCSR2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 2 Low</td>
<td>1188</td>
</tr>
<tr>
<td>0x123</td>
<td>USBTXCSR2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 2 High</td>
<td>1192</td>
</tr>
<tr>
<td>0x124</td>
<td>USBRXMAXP2</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Receive Data Endpoint 2</td>
<td>1196</td>
</tr>
<tr>
<td>0x126</td>
<td>USBRXCSR2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 2 Low</td>
<td>1197</td>
</tr>
<tr>
<td>0x127</td>
<td>USBRXCSR2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 2 High</td>
<td>1202</td>
</tr>
<tr>
<td>0x128</td>
<td>USBRXCOUNT2</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Receive Byte Count Endpoint 2</td>
<td>1206</td>
</tr>
<tr>
<td>0x12A</td>
<td>USBTXTYPE2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Configure Type Endpoint 2</td>
<td>1207</td>
</tr>
</tbody>
</table>
Table 18-5. Universal Serial Bus (USB) Controller Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x12B</td>
<td>USBTXINTERVAL2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Interval Endpoint 2</td>
<td>1209</td>
</tr>
<tr>
<td>0x12C</td>
<td>USBRXTYPE2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Configure Receive Type Endpoint 2</td>
<td>1210</td>
</tr>
<tr>
<td>0x12D</td>
<td>USBTXINTERVAL2</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Receive Polling Interval Endpoint 2</td>
<td>1212</td>
</tr>
<tr>
<td>0x130</td>
<td>USBTMAXXP3</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Transmit Data Endpoint 3</td>
<td>1178</td>
</tr>
<tr>
<td>0x132</td>
<td>USBTXCCTRLR3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 3 Low</td>
<td>1188</td>
</tr>
<tr>
<td>0x133</td>
<td>USBTXCSRH3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 3 High</td>
<td>1192</td>
</tr>
<tr>
<td>0x134</td>
<td>USBRMAXP3</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Receive Data Endpoint 3</td>
<td>1196</td>
</tr>
<tr>
<td>0x136</td>
<td>USBTXCTRLR3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 3 Low</td>
<td>1197</td>
</tr>
<tr>
<td>0x137</td>
<td>USBTXCSRH3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 3 High</td>
<td>1202</td>
</tr>
<tr>
<td>0x138</td>
<td>USBXCCTRLR3</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Receive Byte Count Endpoint 3</td>
<td>1206</td>
</tr>
<tr>
<td>0x13A</td>
<td>USBTTYPE3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Configure Type Endpoint 3</td>
<td>1207</td>
</tr>
<tr>
<td>0x13B</td>
<td>USBTXINTERVAL3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Interval Endpoint 3</td>
<td>1209</td>
</tr>
<tr>
<td>0x13C</td>
<td>USBRTYPE3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Configure Receive Type Endpoint 3</td>
<td>1210</td>
</tr>
<tr>
<td>0x13D</td>
<td>USBTXINTERVAL3</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Receive Polling Interval Endpoint 3</td>
<td>1212</td>
</tr>
<tr>
<td>0x140</td>
<td>USBTMAXP4</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Transmit Data Endpoint 4</td>
<td>1178</td>
</tr>
<tr>
<td>0x142</td>
<td>USBTXCSR4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 4 Low</td>
<td>1188</td>
</tr>
<tr>
<td>0x143</td>
<td>USBTXCRSR4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 4 High</td>
<td>1192</td>
</tr>
<tr>
<td>0x144</td>
<td>USBTMAXP4</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Receive Data Endpoint 4</td>
<td>1196</td>
</tr>
<tr>
<td>0x146</td>
<td>USBTXCSR4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 4 Low</td>
<td>1197</td>
</tr>
<tr>
<td>0x147</td>
<td>USBTXCSR4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 4 High</td>
<td>1202</td>
</tr>
<tr>
<td>0x148</td>
<td>USBTXCTRL4</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Receive Byte Count Endpoint 4</td>
<td>1206</td>
</tr>
<tr>
<td>0x14A</td>
<td>USBTTYPE4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Configure Type Endpoint 4</td>
<td>1207</td>
</tr>
<tr>
<td>0x14B</td>
<td>USBTXINTERVAL4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Interval Endpoint 4</td>
<td>1209</td>
</tr>
<tr>
<td>0x14C</td>
<td>USBRSTYPE4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Configure Receive Type Endpoint 4</td>
<td>1210</td>
</tr>
<tr>
<td>0x14D</td>
<td>USBTXINTERVAL4</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Receive Polling Interval Endpoint 4</td>
<td>1212</td>
</tr>
<tr>
<td>0x150</td>
<td>USBTMAXP5</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Transmit Data Endpoint 5</td>
<td>1178</td>
</tr>
<tr>
<td>0x152</td>
<td>USBTXCSR5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 5 Low</td>
<td>1188</td>
</tr>
<tr>
<td>0x153</td>
<td>USBTXCSR5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 5 High</td>
<td>1192</td>
</tr>
<tr>
<td>0x154</td>
<td>USBRMAXP5</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Receive Data Endpoint 5</td>
<td>1196</td>
</tr>
<tr>
<td>0x156</td>
<td>USBTXCSR5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 5 Low</td>
<td>1197</td>
</tr>
<tr>
<td>0x157</td>
<td>USBTXCSR5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 5 High</td>
<td>1202</td>
</tr>
<tr>
<td>0x158</td>
<td>USBTXCTRL4</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Receive Byte Count Endpoint 5</td>
<td>1206</td>
</tr>
</tbody>
</table>
Table 18-5. Universal Serial Bus (USB) Controller Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x15A</td>
<td>USBTXTYPE5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Configure Type Endpoint 5</td>
<td>1207</td>
</tr>
<tr>
<td>0x15B</td>
<td>USBTXINTERVAL5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Interval Endpoint 5</td>
<td>1209</td>
</tr>
<tr>
<td>0x15C</td>
<td>USBRXTYPE5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Configure Receive Type Endpoint 5</td>
<td>1210</td>
</tr>
<tr>
<td>0x15D</td>
<td>USBXINTERVAL5</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Receive Polling Interval Endpoint 5</td>
<td>1212</td>
</tr>
<tr>
<td>0x160</td>
<td>USBTXMAXP6</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Transmit Data Endpoint 6</td>
<td>1178</td>
</tr>
<tr>
<td>0x162</td>
<td>USBTXSRL6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 6 Low</td>
<td>1188</td>
</tr>
<tr>
<td>0x163</td>
<td>USBTXCSRH6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 6 High</td>
<td>1192</td>
</tr>
<tr>
<td>0x164</td>
<td>USBRXMAXP6</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Receive Data Endpoint 6</td>
<td>1196</td>
</tr>
<tr>
<td>0x166</td>
<td>USBRXSRL6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 6 Low</td>
<td>1197</td>
</tr>
<tr>
<td>0x167</td>
<td>USBRXCSRH6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 6 High</td>
<td>1202</td>
</tr>
<tr>
<td>0x168</td>
<td>USBRXCOUNT6</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Receive Byte Count Endpoint 6</td>
<td>1206</td>
</tr>
<tr>
<td>0x16A</td>
<td>USBTXTYPE6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Configure Type Endpoint 6</td>
<td>1207</td>
</tr>
<tr>
<td>0x16B</td>
<td>USBXINTERVAL6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Interval Endpoint 6</td>
<td>1209</td>
</tr>
<tr>
<td>0x16C</td>
<td>USBRXTYPE6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Configure Type Endpoint 6</td>
<td>1210</td>
</tr>
<tr>
<td>0x16D</td>
<td>USBXINTERVAL6</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Receive Polling Interval Endpoint 6</td>
<td>1212</td>
</tr>
<tr>
<td>0x170</td>
<td>USBTXMAXP7</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Transmit Data Endpoint 7</td>
<td>1178</td>
</tr>
<tr>
<td>0x172</td>
<td>USBTXCSR7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 7 Low</td>
<td>1188</td>
</tr>
<tr>
<td>0x173</td>
<td>USBTXCSRH7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Transmit Control and Status Endpoint 7 High</td>
<td>1192</td>
</tr>
<tr>
<td>0x174</td>
<td>USBRXMAXP7</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Maximum Receive Data Endpoint 7</td>
<td>1196</td>
</tr>
<tr>
<td>0x176</td>
<td>USBRXCSR7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 7 Low</td>
<td>1197</td>
</tr>
<tr>
<td>0x177</td>
<td>USBRXCSRH7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Receive Control and Status Endpoint 7 High</td>
<td>1202</td>
</tr>
<tr>
<td>0x178</td>
<td>USBRXCOUNT7</td>
<td>RO</td>
<td>0x0000</td>
<td>USB Receive Byte Count Endpoint 7</td>
<td>1206</td>
</tr>
<tr>
<td>0x17A</td>
<td>USBTXTYPE7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Configure Type Endpoint 7</td>
<td>1207</td>
</tr>
<tr>
<td>0x17B</td>
<td>USBXINTERVAL7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Transmit Interval Endpoint 7</td>
<td>1209</td>
</tr>
<tr>
<td>0x17C</td>
<td>USBRXTYPE7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Configure Receive Type Endpoint 7</td>
<td>1210</td>
</tr>
<tr>
<td>0x17D</td>
<td>USBXINTERVAL7</td>
<td>RW</td>
<td>0x00</td>
<td>USB Host Receive Polling Interval Endpoint 7</td>
<td>1212</td>
</tr>
<tr>
<td>0x304</td>
<td>USBRQPKTCOUNT1</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Request Packet Count in Block Transfer Endpoint 1</td>
<td>1213</td>
</tr>
<tr>
<td>0x308</td>
<td>USBRQPKTCOUNT2</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Request Packet Count in Block Transfer Endpoint 2</td>
<td>1213</td>
</tr>
<tr>
<td>0x30C</td>
<td>USBRQPKTCOUNT3</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Request Packet Count in Block Transfer Endpoint 3</td>
<td>1213</td>
</tr>
<tr>
<td>0x310</td>
<td>USBRQPKTCOUNT4</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Request Packet Count in Block Transfer Endpoint 4</td>
<td>1213</td>
</tr>
</tbody>
</table>
Table 18-5. Universal Serial Bus (USB) Controller Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x314</td>
<td>USBRQPKTCOUNT5</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Request Packet Count in Block Transfer Endpoint 5</td>
<td>1213</td>
</tr>
<tr>
<td>0x318</td>
<td>USBRQPKTCOUNT6</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Request Packet Count in Block Transfer Endpoint 6</td>
<td>1213</td>
</tr>
<tr>
<td>0x31C</td>
<td>USBRQPKTCOUNT7</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Request Packet Count in Block Transfer Endpoint 7</td>
<td>1213</td>
</tr>
<tr>
<td>0x340</td>
<td>USBRXDPKTDIS</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Receive Double Packet Buffer Disable</td>
<td>1214</td>
</tr>
<tr>
<td>0x342</td>
<td>USBTXDPKTDIS</td>
<td>RW</td>
<td>0x0000</td>
<td>USB Transmit Double Packet Buffer Disable</td>
<td>1215</td>
</tr>
<tr>
<td>0x400</td>
<td>USBEPC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>USB External Power Control</td>
<td>1216</td>
</tr>
<tr>
<td>0x404</td>
<td>USBEPCRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>USB External Power Control Raw Interrupt Status</td>
<td>1219</td>
</tr>
<tr>
<td>0x408</td>
<td>USBEPCIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>USB External Power Control Interrupt Mask</td>
<td>1220</td>
</tr>
<tr>
<td>0x40C</td>
<td>USBEPCISC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>USB External Power Control Interrupt Status and Clear</td>
<td>1221</td>
</tr>
<tr>
<td>0x410</td>
<td>USBDRRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>USB Device RESUME Raw Interrupt Status</td>
<td>1222</td>
</tr>
<tr>
<td>0x414</td>
<td>USBDRIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>USB Device RESUME Interrupt Mask</td>
<td>1223</td>
</tr>
<tr>
<td>0x418</td>
<td>USBDRISC</td>
<td>W1C</td>
<td>0x0000.0000</td>
<td>USB Device RESUME Interrupt Status and Clear</td>
<td>1224</td>
</tr>
<tr>
<td>0x41C</td>
<td>USBGPCS</td>
<td>RW</td>
<td>0x0000.0003</td>
<td>USB General-Purpose Control and Status</td>
<td>1225</td>
</tr>
<tr>
<td>0x430</td>
<td>USBVDC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>USB VBUS Droop Control</td>
<td>1226</td>
</tr>
<tr>
<td>0x434</td>
<td>USBVDCRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>USB VBUS Droop Control Raw Interrupt Status</td>
<td>1227</td>
</tr>
<tr>
<td>0x438</td>
<td>USBVDCIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>USB VBUS Droop Control Interrupt Mask</td>
<td>1228</td>
</tr>
<tr>
<td>0x43C</td>
<td>USBVDCISC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>USB VBUS Droop Control Interrupt Status and Clear</td>
<td>1229</td>
</tr>
<tr>
<td>0x444</td>
<td>USBIDVRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>USB ID Valid Detect Raw Interrupt Status</td>
<td>1230</td>
</tr>
<tr>
<td>0x448</td>
<td>USBIDVIM</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>USB ID Valid Detect Interrupt Mask</td>
<td>1231</td>
</tr>
<tr>
<td>0x44C</td>
<td>USBIDVISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>USB ID Valid Detect Interrupt Status and Clear</td>
<td>1232</td>
</tr>
<tr>
<td>0x450</td>
<td>USBDMASEL</td>
<td>RW</td>
<td>0x0033.2211</td>
<td>USB DMA Select</td>
<td>1233</td>
</tr>
<tr>
<td>0xFC0</td>
<td>USBPP</td>
<td>RO</td>
<td>0x0000.10D0</td>
<td>USB Peripheral Properties</td>
<td>1235</td>
</tr>
</tbody>
</table>

18.6 Register Descriptions

The TM4C123GH6PZ USB controller has On-The-Go (OTG) capabilities as specified in the USB0 bit field in the DC6 register (see page 447).

This icon indicates that the register is used in OTG B or Device mode. Some registers are used for both Host and Device mode and may have different bit definitions depending on the mode.

This icon indicates that the register is used in OTG A or Host mode. Some registers are used for both Host and Device mode and may have different bit definitions depending on the mode. The USB controller is in OTG B or Device mode upon reset, so the reset values shown for these registers apply to the Device mode definition.
This icon indicates that the register is used for OTG-specific functions such as ID detection and negotiation. Once OTG negotiation is complete, then the USB controller registers are used according to their Host or Device mode meanings depending on whether the OTG negotiations made the USB controller OTG A (Host) or OTG B (Device).
Register 1: USB Device Functional Address (USBFADDR), offset 0x000

**USBFADDR** is an 8-bit register that contains the 7-bit address of the Device part of the transaction. When the USB controller is being used in Device mode (the HOST bit in the USBDEVCTL register is clear), this register must be written with the address received through a SET_ADDRESS command, which is then used for decoding the function address in subsequent token packets.

**Important:** See the section called “Setting the Device Address” on page 1126 for special considerations when writing this register.

---

**USB Device Functional Address (USBFADDR)**
Base 0x4005.0000
Offset 0x000
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6:0</td>
<td>FUNCADDR</td>
<td>RW</td>
<td>0x00</td>
<td>Function Address of Device as received through SET_ADDRESS.</td>
</tr>
</tbody>
</table>
Register 2: USB Power (USBPOWER), offset 0x001

**USBPOWER** is an 8-bit register used for controlling SUSPEND and RESUME signaling and some basic operational aspects of the USB controller.

### OTG A / Host Mode

**USB Power (USBPOWER)**

Base 0x4005.0000  
Offset 0x001  
Type RW, reset 0x20

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x2</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>RESET</td>
<td>RW</td>
<td>0</td>
<td>RESUME Signaling</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Ends RESET signaling on the bus.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables RESET signaling on the bus.</td>
</tr>
<tr>
<td>2</td>
<td>RESUME</td>
<td>RW</td>
<td>0</td>
<td>RESUME Signaling</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Ends RESUME signaling on the bus.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables RESUME signaling when the Device is in SUSPEND mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit must be cleared by software 20 ms after being set.</td>
</tr>
<tr>
<td>1</td>
<td>SUSPEND</td>
<td>RW1S</td>
<td>0</td>
<td>SUSPEND Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables SUSPEND mode.</td>
</tr>
</tbody>
</table>
### OTG B / Device Mode

#### USB Power (USBPOWER)

Base 0x4005.0000  
Offset 0x001  
Type RW, reset 0x20

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>ISOUP</td>
<td>RW</td>
<td>0</td>
<td>Isochronous Update</td>
</tr>
<tr>
<td>6</td>
<td>SOFTCONN</td>
<td>RW</td>
<td>0</td>
<td>Soft Connect/Disconnect</td>
</tr>
<tr>
<td>5:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x2</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>RESET</td>
<td>RO</td>
<td>0</td>
<td>RESET Signaling</td>
</tr>
</tbody>
</table>

**Value Description**

0 | No effect.  
1 | Powers down the internal USB PHY.  

**Note:** This bit is only valid for isochronous transfers.

---

**ISOUP**  
The USB controller waits for an SOF token from the time the TXRDY bit is set in the USBTXCSRLn register before sending the packet. If an IN token is received before an SOF token, then a zero-length data packet is sent.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>RESUME</td>
<td>RW</td>
<td>0</td>
<td>RESUME Signaling</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Ends RESUME signaling on the bus.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables RESUME signaling when the Device is in SUSPEND mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit must be cleared by software 10 ms (a maximum of 15 ms) after being set.</td>
</tr>
<tr>
<td>1</td>
<td>SUSPEND</td>
<td>RO</td>
<td>0</td>
<td>SUSPEND Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 This bit is cleared when software reads the interrupt register or sets the RESUME bit above.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The USB controller is in SUSPEND mode.</td>
</tr>
<tr>
<td>0</td>
<td>PWRDNPHY</td>
<td>RW</td>
<td>0</td>
<td>Power Down PHY</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Powers down the internal USB PHY.</td>
</tr>
</tbody>
</table>
Register 3: USB Transmit Interrupt Status (USBTXIS), offset 0x002

**Important:** This register is read-sensitive. See the register description for details.

**USBTXIS** is a 16-bit read-only register that indicates which interrupts are currently active for endpoint 0 and the transmit endpoints 1–7. The meaning of the EPn bits in this register is based on the mode of the device. The EP1 through EP7 bits always indicate that the USB controller is sending data; however, in Host mode, the bits refer to OUT endpoints; while in Device mode, the bits refer to IN endpoints. The EP0 bit is special in Host and Device modes and indicates that either a control IN or control OUT endpoint has generated an interrupt.

**Note:** Bits relating to endpoints that have not been configured always return 0. Note also that all active interrupts are cleared when this register is read.

**USB Transmit Interrupt Status (USBTXIS)**

<table>
<thead>
<tr>
<th>Base 0x4005.0000</th>
<th>Offset 0x002</th>
<th>Type RO, reset 0x0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>15:8</th>
<th>reserved</th>
<th>RO</th>
<th>0</th>
<th>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>EP7</td>
<td>RO</td>
<td>0</td>
<td>TX Endpoint 7 Interrupt Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>EP6</td>
<td>RO</td>
<td>0</td>
<td>TX Endpoint 6 Interrupt Same description as EP7.</td>
</tr>
<tr>
<td>5</td>
<td>EP5</td>
<td>RO</td>
<td>0</td>
<td>TX Endpoint 5 Interrupt Same description as EP7.</td>
</tr>
<tr>
<td>3</td>
<td>EP3</td>
<td>RO</td>
<td>0</td>
<td>TX Endpoint 3 Interrupt Same description as EP7.</td>
</tr>
<tr>
<td>2</td>
<td>EP2</td>
<td>RO</td>
<td>0</td>
<td>TX Endpoint 2 Interrupt Same description as EP7.</td>
</tr>
<tr>
<td>1</td>
<td>EP1</td>
<td>RO</td>
<td>0</td>
<td>TX Endpoint 1 Interrupt Same description as EP7.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>0</td>
<td>EP0</td>
<td>RO</td>
<td>0</td>
<td>TX and RX Endpoint 0 Interrupt</td>
</tr>
</tbody>
</table>

Value  Description
0      No interrupt.
1      The Endpoint 0 transmit and receive interrupt is asserted.
## Register 4: USB Receive Interrupt Status (USBRXIS), offset 0x004

### Important: This register is read-sensitive. See the register description for details.

**USBRXIS** is a 16-bit read-only register that indicates which of the interrupts for receive endpoints 1–7 are currently active.

**Note:** Bits relating to endpoints that have not been configured always return 0. Note also that all active interrupts are cleared when this register is read.

### USB Receive Interrupt Status (USBRXIS)

Base 0x4005.0000  
Offset 0x004  
Type RO, reset 0x0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>EP7</td>
<td>RO</td>
<td>0</td>
<td>RX Endpoint 7 Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The Endpoint 7 transmit interrupt is asserted.</td>
</tr>
<tr>
<td>6</td>
<td>EP6</td>
<td>RO</td>
<td>0</td>
<td>RX Endpoint 6 Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>5</td>
<td>EP5</td>
<td>RO</td>
<td>0</td>
<td>RX Endpoint 5 Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>4</td>
<td>EP4</td>
<td>RO</td>
<td>0</td>
<td>RX Endpoint 4 Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>3</td>
<td>EP3</td>
<td>RO</td>
<td>0</td>
<td>RX Endpoint 3 Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>2</td>
<td>EP2</td>
<td>RO</td>
<td>0</td>
<td>RX Endpoint 2 Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>1</td>
<td>EP1</td>
<td>RO</td>
<td>0</td>
<td>RX Endpoint 1 Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
**Register 5: USB Transmit Interrupt Enable (USBTXIE), offset 0x006**

**USBTXIE** is a 16-bit register that provides interrupt enable bits for the interrupts in the **USBTXIS** register. When a bit is set, the USB interrupt is asserted to the interrupt controller when the corresponding interrupt bit in the **USBTXIS** register is set. When a bit is cleared, the interrupt in the **USBTXIS** register is still set but the USB interrupt to the interrupt controller is not asserted. On reset, all interrupts are enabled.

USB Transmit Interrupt Enable (USBTXIE)

Base 0x4005.0000
Offset 0x006

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>TX Endpoint 7 Interrupt Enable</td>
</tr>
<tr>
<td>7</td>
<td>EP7</td>
<td>RW</td>
<td>1</td>
<td>TX Endpoint 7 Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The EP7 transmit interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the EP7 bit in the USBTXIS register is set.</td>
</tr>
<tr>
<td>6</td>
<td>EP6</td>
<td>RW</td>
<td>1</td>
<td>TX Endpoint 6 Interrupt Enable</td>
</tr>
<tr>
<td>5</td>
<td>EP5</td>
<td>RW</td>
<td>1</td>
<td>TX Endpoint 5 Interrupt Enable</td>
</tr>
<tr>
<td>4</td>
<td>EP4</td>
<td>RW</td>
<td>1</td>
<td>TX Endpoint 4 Interrupt Enable</td>
</tr>
<tr>
<td>3</td>
<td>EP3</td>
<td>RW</td>
<td>1</td>
<td>TX Endpoint 3 Interrupt Enable</td>
</tr>
<tr>
<td>2</td>
<td>EP2</td>
<td>RW</td>
<td>1</td>
<td>TX Endpoint 2 Interrupt Enable</td>
</tr>
<tr>
<td>1</td>
<td>EP1</td>
<td>RW</td>
<td>1</td>
<td>TX Endpoint 1 Interrupt Enable</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>EP0</td>
<td>RW</td>
<td>1</td>
<td>TX and RX Endpoint 0 Interrupt Enable</td>
</tr>
</tbody>
</table>

**Value** | **Description**                                |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The EP0 transmit and receive interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the EP0 bit in the USBTXIS register is set.</td>
</tr>
</tbody>
</table>
Register 6: USB Receive Interrupt Enable (USBRXIE), offset 0x008

**USBRXIE** is a 16-bit register that provides interrupt enable bits for the interrupts in the **USBRXIS** register. When a bit is set, the USB interrupt is asserted to the interrupt controller when the corresponding interrupt bit in the **USBRXIS** register is set. When a bit is cleared, the interrupt in the **USBRXIS** register is still set but the USB interrupt to the interrupt controller is not asserted. On reset, all interrupts are enabled.

**USB Receive Interrupt Enable (USBRXIE)**

Type RW, reset 0xFFFE

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>EP7</td>
<td>RW</td>
<td>1</td>
<td>RX Endpoint 7 Interrupt Enable</td>
</tr>
<tr>
<td>6</td>
<td>EP6</td>
<td>RW</td>
<td>1</td>
<td>RX Endpoint 6 Interrupt Enable</td>
</tr>
<tr>
<td>5</td>
<td>EP5</td>
<td>RW</td>
<td>1</td>
<td>RX Endpoint 5 Interrupt Enable</td>
</tr>
<tr>
<td>4</td>
<td>EP4</td>
<td>RW</td>
<td>1</td>
<td>RX Endpoint 4 Interrupt Enable</td>
</tr>
<tr>
<td>3</td>
<td>EP3</td>
<td>RW</td>
<td>1</td>
<td>RX Endpoint 3 Interrupt Enable</td>
</tr>
<tr>
<td>2</td>
<td>EP2</td>
<td>RW</td>
<td>1</td>
<td>RX Endpoint 2 Interrupt Enable</td>
</tr>
<tr>
<td>1</td>
<td>EP1</td>
<td>RW</td>
<td>1</td>
<td>RX Endpoint 1 Interrupt Enable</td>
</tr>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 7: USB General Interrupt Status (USBIS), offset 0x00A

**Important:** This register is read-sensitive. See the register description for details.

USBIS is an 8-bit read-only register that indicates which USB interrupts are currently active. All active interrupts are cleared when this register is read.

### OTG A / Host Mode

USB General Interrupt Status (USBIS)

- **Base:** 0x4005.0000
- **Offset:** 0x00A
- **Type:** RO, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>VBUSERR</td>
<td>RO</td>
<td>0</td>
<td>VBUS Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: VBUS has dropped below the VBUS Valid threshold during a session.</td>
</tr>
<tr>
<td>6</td>
<td>SESREQ</td>
<td>RO</td>
<td>0</td>
<td>SESSION REQUEST</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: SESSION REQUEST signaling has been detected.</td>
</tr>
<tr>
<td>5</td>
<td>DISCON</td>
<td>RO</td>
<td>0</td>
<td>Session Disconnect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: A Device disconnect has been detected.</td>
</tr>
<tr>
<td>4</td>
<td>CONN</td>
<td>RO</td>
<td>0</td>
<td>Session Connect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: A Device connection has been detected.</td>
</tr>
</tbody>
</table>
**Universal Serial Bus (USB) Controller**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>SOF</td>
<td>RO</td>
<td>0</td>
<td>Start of Frame</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  A new frame has started.</td>
</tr>
<tr>
<td>2</td>
<td>BABBLE</td>
<td>RO</td>
<td>0</td>
<td>Babble Detected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Babble has been detected. This interrupt is active only after the first SOF has been sent.</td>
</tr>
<tr>
<td>1</td>
<td>RESUME</td>
<td>RO</td>
<td>0</td>
<td>RESUME Signaling Detected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  RESUME signaling has been detected on the bus while the USB controller is in SUSPEND mode. This interrupt can only be used if the USB controller's system clock is enabled. If the user disables the clock programming, the <strong>USBDRRIS</strong>, <strong>USBDRIM</strong>, and <strong>USBDRISC</strong> registers should be used.</td>
</tr>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

**OTG B / Device Mode**

**USB General Interrupt Status (USBIS)**

Base 0x4005.0000  
Offset 0x00A  
Type RO, reset 0x00

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

**OTG.B/DeviceMode**

**USB General Interrupt Status (USBIS)**

Base 0x4005.0000  
Offset 0x00A  
Type RO, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>DISCON</td>
<td>RO</td>
<td>0</td>
<td>Session Disconnect</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>SOF</td>
<td>RO</td>
<td>0</td>
<td>Start of Frame</td>
</tr>
<tr>
<td>2</td>
<td>RESET</td>
<td>RO</td>
<td>0</td>
<td>RESET Signaling Detected</td>
</tr>
<tr>
<td>1</td>
<td>RESUME</td>
<td>RO</td>
<td>0</td>
<td>RESUME Signaling Detected</td>
</tr>
<tr>
<td>0</td>
<td>SUSPEND</td>
<td>RO</td>
<td>0</td>
<td>SUSPEND Signaling Detected</td>
</tr>
</tbody>
</table>

**SOF**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt.</td>
</tr>
<tr>
<td>1</td>
<td>A new frame has started.</td>
</tr>
</tbody>
</table>

**RESET**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt.</td>
</tr>
<tr>
<td>1</td>
<td>RESET signaling has been detected on the bus.</td>
</tr>
</tbody>
</table>

**RESUME**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt.</td>
</tr>
<tr>
<td>1</td>
<td>RESUME signaling has been detected on the bus while the USB controller is in SUSPEND mode.</td>
</tr>
</tbody>
</table>

This interrupt can only be used if the USB controller's system clock is enabled. If the user disables the clock programming, the **USBDRRIS**, **USBDRIM**, and **USBDRISC** registers should be used.

**SUSPEND**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt.</td>
</tr>
<tr>
<td>1</td>
<td>SUSPEND signaling has been detected on the bus.</td>
</tr>
</tbody>
</table>
Register 8: USB Interrupt Enable (USBIE), offset 0x00B

USBIE is an 8-bit register that provides interrupt enable bits for each of the interrupts in USBIS. At reset interrupts 1 and 2 are enabled in Device mode.

OTG A / Host

OTG B / Device

OTG A / Host Mode

USB Interrupt Enable (USBIE)
Base 0x4005.0000
Offset 0x00B
Type RW, reset 0x06

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>VBUSERR</td>
<td>RW</td>
<td>0</td>
<td>Enable VBUS Error Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The VBUSERR interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the VBUSERR bit in the USBIS register is set.</td>
</tr>
<tr>
<td>6</td>
<td>SESREQ</td>
<td>RW</td>
<td>0</td>
<td>Enable Session Request</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The SESREQ interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the SESREQ bit in the USBIS register is set.</td>
</tr>
<tr>
<td>5</td>
<td>DISCON</td>
<td>RW</td>
<td>0</td>
<td>Enable Disconnect Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The DISCON interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the DISCON bit in the USBIS register is set.</td>
</tr>
</tbody>
</table>
Enable Connect Interrupt

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>CONN</td>
<td>RW</td>
<td>0</td>
<td>Enable Connect Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The CONN interrupt is suppressed and not</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       An interrupt is sent to the interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controller when the CONN bit in the USBIS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is set.</td>
</tr>
</tbody>
</table>

Enable Start-of-Frame Interrupt

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>SOF</td>
<td>RW</td>
<td>0</td>
<td>Enable Start-of-Frame Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The SOF interrupt is suppressed and not</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       An interrupt is sent to the interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controller when the SOF bit in the USBIS register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>is set.</td>
</tr>
</tbody>
</table>

Enable Babble Interrupt

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>BABBLE</td>
<td>RW</td>
<td>1</td>
<td>Enable Babble Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The BABBLE interrupt is suppressed and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       An interrupt is sent to the interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controller when the BABBLE bit in the USBIS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is set.</td>
</tr>
</tbody>
</table>

Enable RESUME Interrupt

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RESUME</td>
<td>RW</td>
<td>1</td>
<td>Enable RESUME Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The RESUME interrupt is suppressed and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       An interrupt is sent to the interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controller when the RESUME bit in the USBIS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is set.</td>
</tr>
</tbody>
</table>

OTG B / Device Mode

USB Interrupt Enable (USBIE)

Base 0x4005.0000
Offset 0x00B
Type RW, reset 0x06

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>DISCON</td>
<td>RW</td>
<td>0</td>
<td>Enable Disconnect Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The DISCON interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the DISCON bit in the USBIS register is set.</td>
</tr>
<tr>
<td>4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>SOF</td>
<td>RW</td>
<td>0</td>
<td>Enable Start-of-Frame Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The SOF interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the SOF bit in the USBIS register is set.</td>
</tr>
<tr>
<td>2</td>
<td>RESET</td>
<td>RW</td>
<td>1</td>
<td>Enable RESET Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The RESET interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the RESET bit in the USBIS register is set.</td>
</tr>
<tr>
<td>1</td>
<td>RESUME</td>
<td>RW</td>
<td>1</td>
<td>Enable RESUME Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The RESUME interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the RESUME bit in the USBIS register is set.</td>
</tr>
<tr>
<td>0</td>
<td>SUSPEND</td>
<td>RW</td>
<td>0</td>
<td>Enable SUSPEND Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The SUSPEND interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the SUSPEND bit in the USBIS register is set.</td>
</tr>
</tbody>
</table>

Universal Serial Bus (USB) Controller

Texas Instruments-Production Data

June 12, 2014
Register 9: USB Frame Value (USBFRAME), offset 0x00C

USBFRAME is a 16-bit read-only register that holds the last received frame number.

USB Frame Value (USBFRAME)
Base 0x4005.0000
Offset 0x00C
Type RO, reset 0x0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:11</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10:0</td>
<td>FRAME</td>
<td>RO</td>
<td>0x000</td>
<td>Frame Number</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
Register 10: USB Endpoint Index (USBEPIDX), offset 0x00E

Each endpoint’s buffer can be accessed by configuring a FIFO size and starting address. The USBEPIDX 8-bit register is used with the USBTXFIFOSZ, USBRXFIFOSZ, USBTXFIFOADD, and USBRXFIFOADD registers.

USB Endpoint Index (USBEPIDX)
Base 0x4005.0000
Offset 0x00E
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3:0</td>
<td>EPIDX</td>
<td>RW</td>
<td>0x0</td>
<td>Endpoint Index</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit field configures which endpoint is accessed when reading or writing to one of the USB controller’s indexed registers. A value of 0x0 corresponds to Endpoint 0 and a value of 0x7 corresponds to Endpoint 7.</td>
</tr>
</tbody>
</table>
Register 11: USB Test Mode (USBTEST), offset 0x00F

USBTEST is an 8-bit register that is primarily used to put the USB controller into one of the four test modes for operation described in the USB 2.0 Specification, in response to a SET FEATURE: USBTESTMODE command. This register is not used in normal operation.

**Note:** Only one of these bits should be set at any time.

### OTG A / Host Mode

**USB Test Mode (USBTEST)**

<table>
<thead>
<tr>
<th>Base 0x4005.0000</th>
<th>Offset 0x00F</th>
<th>Type RW, reset 0x00</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 6 5 4 3 2 1 0</td>
<td>FORCEH FIFOACC FORCEFS reserved</td>
<td></td>
</tr>
<tr>
<td>Type RW RW1S RW RO RO RO RO RO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset 0 0 0 0 0 0 0 0 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bit/Field** | **Name** | **Type** | **Reset** | **Description** |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>FORCEH</td>
<td>RW</td>
<td>0</td>
<td>Force Host Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Forces the USB controller to enter Host mode when the SESSION bit is set, regardless of whether the USB controller is connected to any peripheral. The state of the USB0DP and USB0DM signals is ignored. The USB controller then remains in Host mode until the SESSION bit is cleared, even if a Device is disconnected. If the FORCEH bit remains set, the USB controller re-enters Host mode the next time the SESSION bit is set. While in this mode, status of the bus connection may be read using the DEV bit of the USBDEVCTL register. The operating speed is determined from the FORCEFS bit.</td>
</tr>
<tr>
<td>6</td>
<td>FIFOACC</td>
<td>RW1S</td>
<td>0</td>
<td>FIFO Access</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Transfers the packet in the endpoint 0 transmit FIFO to the endpoint 0 receive FIFO. This bit is cleared automatically.</td>
</tr>
<tr>
<td>5</td>
<td>FORCEFS</td>
<td>RW</td>
<td>0</td>
<td>Force Full-Speed Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The USB controller operates at Low Speed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Forces the USB controller into Full-Speed mode upon receiving a USB RESET.</td>
</tr>
</tbody>
</table>
Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

OTG B / Device Mode

USB Test Mode (USBTEST)

Base 0x4005.0000
Offset 0x00F
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6</td>
<td>FIFOACC</td>
<td>RW1S</td>
<td>0</td>
<td>FIFO Access</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Transfers the packet in the endpoint 0 transmit FIFO to the endpoint 0 receive FIFO.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared automatically.</td>
</tr>
<tr>
<td>5</td>
<td>FORCEFS</td>
<td>RW</td>
<td>0</td>
<td>Force Full-Speed Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The USB controller operates at Low Speed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Forces the USB controller into Full-Speed mode upon receiving a USB RESET.</td>
</tr>
<tr>
<td>4:0</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 12: USB FIFO Endpoint 0 (USBFIFO0), offset 0x020
Register 13: USB FIFO Endpoint 1 (USBFIFO1), offset 0x024
Register 14: USB FIFO Endpoint 2 (USBFIFO2), offset 0x028
Register 15: USB FIFO Endpoint 3 (USBFIFO3), offset 0x02C
Register 16: USB FIFO Endpoint 4 (USBFIFO4), offset 0x030
Register 17: USB FIFO Endpoint 5 (USBFIFO5), offset 0x034
Register 18: USB FIFO Endpoint 6 (USBFIFO6), offset 0x038
Register 19: USB FIFO Endpoint 7 (USBFIFO7), offset 0x03C

Important: This register is read-sensitive. See the register description for details.

These 32-bit registers provide an address for CPU access to the FIFOs for each endpoint. Writing to these addresses loads data into the Transmit FIFO for the corresponding endpoint. Reading from these addresses unloads data from the Receive FIFO for the corresponding endpoint.

Transfers to and from FIFOs may be 8-bit, 16-bit or 32-bit as required, and any combination of accesses is allowed provided the data accessed is contiguous. All transfers associated with one packet must be of the same width so that the data is consistently byte-, halfword- or word-aligned. However, the last transfer may contain fewer bytes than the previous transfers in order to complete an odd-byte or odd-word transfer.

Depending on the size of the FIFO and the expected maximum packet size, the FIFOs support either single-packet or double-packet buffering (see the section called “Single-Packet Buffering” on page 1124). Burst writing of multiple packets is not supported as flags must be set after each packet is written.

Following a STALL response or a transmit error on endpoint 1–7, the associated FIFO is completely flushed.

USB FIFO Endpoint n (USBFIFO0n)

<table>
<thead>
<tr>
<th>Base 0x4005.0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset 0x020</td>
</tr>
<tr>
<td>Type RW, reset 0x0000.0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>EPDATA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Endpoint Data</td>
</tr>
</tbody>
</table>

Writing to this register loads the data into the Transmit FIFO and reading unloads data from the Receive FIFO.
**Register 20: USB Device Control (USBDEVCTL), offset 0x060**

USBDEVCTL is an 8-bit register used for controlling and monitoring the USB VBUS line. If the PHY is suspended, no PHY clock is received and the VBUS is not sampled. In addition, in Host mode, USBDEVCTL provides the status information for the current operating mode (Host or Device) of the USB controller. If the USB controller is in Host mode, this register also indicates if a full- or low-speed Device has been connected.

### USB Device Control (USBDEVCTL)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>DEV</td>
<td>RO</td>
<td>1</td>
<td>Device Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The USB controller is operating on the OTG A side of the cable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The USB controller is operating on the OTG B side of the cable.</td>
</tr>
<tr>
<td>6</td>
<td>FSDEV</td>
<td>RO</td>
<td>0</td>
<td>Full-Speed Device Detected</td>
</tr>
<tr>
<td>5</td>
<td>LSDEV</td>
<td>RO</td>
<td>0</td>
<td>Low-Speed Device Detected</td>
</tr>
<tr>
<td>4:3</td>
<td>VBUS</td>
<td>RO</td>
<td>0x0</td>
<td>VBUS Level</td>
</tr>
</tbody>
</table>

#### Bit Descriptions:

- **Device Mode**
  - **Value Description**
  - **0**: The USB controller is operating on the OTG A side of the cable.
  - **1**: The USB controller is operating on the OTG B side of the cable.

- **Full-Speed Device Detected**
  - **Value Description**
  - **0**: A full-speed Device has not been detected on the port.
  - **1**: A full-speed Device has been detected on the port.

- **Low-Speed Device Detected**
  - **Value Description**
  - **0**: A low-speed Device has not been detected on the port.
  - **1**: A low-speed Device has been detected on the port.

- **VBUS Level**
  - **Value Description**
  - **0x0**: Below SessionEnd
    - VBUS is detected as under 0.5 V.
  - **0x1**: Above SessionEnd, below AValid
    - VBUS is detected as above 0.5 V and under 1.5 V.
  - **0x2**: Above AValid, below VBUSValid
    - VBUS is detected as above 1.5 V and below 4.75 V.
  - **0x3**: Above VBUSValid
    - VBUS is detected as above 4.75 V.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>HOST</td>
<td>RO</td>
<td>0</td>
<td>Host Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The USB controller is acting as a Device.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The USB controller is acting as a Host.</td>
</tr>
<tr>
<td>1</td>
<td>HOSTREQ</td>
<td>RW</td>
<td>0</td>
<td>Host Request</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       Initiates the Host Negotiation when SUSPEND mode is entered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared when Host Negotiation is completed.</td>
</tr>
<tr>
<td>0</td>
<td>SESSION</td>
<td>RW</td>
<td>0</td>
<td>Session Start/End</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>When operating as an OTG A device:</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       When cleared by software, this bit ends a session.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       When set by software, this bit starts a session.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>When operating as an OTG B device:</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0       The USB controller has ended a session. When the USB controller is in SUSPEND mode, this bit may be cleared by software to perform a software disconnect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1       The USB controller has started a session. When set by software, the Session Request Protocol is initiated.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> Clearing this bit when the USB controller is not suspended results in undefined behavior.</td>
</tr>
</tbody>
</table>
Register 21: USB Transmit Dynamic FIFO Sizing (USBTXFIFOSZ), offset 0x062
Register 22: USB Receive Dynamic FIFO Sizing (USBRXFIFOSZ), offset 0x063

These 8-bit registers allow the selected TX/RX endpoint FIFOs to be dynamically sized. **USBEPIDX** is used to configure each transmit endpoint's FIFO size.

### USB Dynamic FIFO Sizing (USBnXFIFOSZ)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4005.0000</td>
<td>0x062</td>
<td>RW, reset 0x00</td>
<td></td>
<td>These 8-bit registers allow the selected TX/RX endpoint FIFOs to be dynamically sized. USBEPIDX is used to configure each transmit endpoint's FIFO size.</td>
</tr>
</tbody>
</table>

#### OTG A / Host

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>DPB</td>
<td>RW</td>
<td>0</td>
<td>Double Packet Buffer Support</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Only single-packet buffering is supported.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Double-packet buffering is supported.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>SIZE</td>
<td>RW</td>
<td>0x0</td>
<td>Max Packet Size</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Maximum packet size to be allowed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If DPB = 0, the FIFO also is this size; if DPB = 1, the FIFO is twice this size.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Packet Size (Bytes)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 32</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 64</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x4 128</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x5 256</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x6 512</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x7 1024</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x8 2048</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x9-0xFF Reserved</td>
</tr>
</tbody>
</table>
Register 23: USB Transmit FIFO Start Address (USBTXFIFOADD), offset 0x064

Register 24: USB Receive FIFO Start Address (USBRXFIFOADD), offset 0x066

**OTG A / Host**

**OTG B / Device**

**USBTXFIFOADD** and **USBRXFIFOADD** are 16-bit registers that control the start address of the selected transmit and receive endpoint FIFOs.

**USB Transmit FIFO Start Address (USBnXFIFOADD)**

Base 0x4005.0000
Offset 0x064
Type RW, reset 0x0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:9</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>8:0</td>
<td>ADDR</td>
<td>RW</td>
<td>0x00</td>
<td>Transmit/Receive Start Address</td>
</tr>
</tbody>
</table>

Start address of the endpoint FIFO.

<table>
<thead>
<tr>
<th>Value</th>
<th>Start Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0</td>
</tr>
<tr>
<td>0x1</td>
<td>8</td>
</tr>
<tr>
<td>0x2</td>
<td>16</td>
</tr>
<tr>
<td>0x3</td>
<td>24</td>
</tr>
<tr>
<td>0x4</td>
<td>32</td>
</tr>
<tr>
<td>0x5</td>
<td>40</td>
</tr>
<tr>
<td>0x6</td>
<td>48</td>
</tr>
<tr>
<td>0x7</td>
<td>56</td>
</tr>
<tr>
<td>0x8</td>
<td>64</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0x1FF</td>
<td>4095</td>
</tr>
</tbody>
</table>
Register 25: USB Connect Timing (USBCONTIM), offset 0x07A

This 8-bit configuration register specifies connection and negotiation delays.

USB Connect Timing (USBCONTIM)
Base 0x4005.0000
Offset 0x07A
Type RW, reset 0x5C

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7:4       | WTCON| RW   | 0x5   | Connect Wait
This field configures the wait required to allow for the user's connect/disconnect filter, in units of 533.3 ns. The default corresponds to 2.667 µs. |
| 3:0       | WTID | RW   | 0xC   | Wait ID
This field configures the delay required from the enable of the ID detection to when the ID value is valid, in units of 4.369 ms. The default corresponds to 52.43 ms. |
Register 26: USB OTG VBUS Pulse Timing (USBVPLEN), offset 0x07B

This 8-bit configuration register specifies the duration of the VBUS pulsing charge.

USB OTG VBUS Pulse Timing (USBVPLEN)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>VPLEN</td>
<td>RW</td>
<td>0x3C</td>
<td>VBUS Pulse Length</td>
</tr>
</tbody>
</table>

This field configures the duration of the VBUS pulsing charge in units of 546.1 µs. The default corresponds to 32.77 ms.
Register 27: USB Full-Speed Last Transaction to End of Frame Timing (USBFSEOF), offset 0x07D

This 8-bit configuration register specifies the minimum time gap allowed between the start of the last transaction and the EOF for full-speed transactions.

USB Full-Speed Last Transaction to End of Frame Timing (USBFSEOF)

Base 0x4005.0000
Offset 0x07D
Type RW, reset 0x77

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>FSEOFG</td>
<td>RW</td>
<td>0x77</td>
<td>Full-Speed End-of-Frame Gap</td>
</tr>
</tbody>
</table>

This field is used during full-speed transactions to configure the gap between the last transaction and the End-of-Frame (EOF), in units of 533.3 ns. The default corresponds to 63.46 µs.
Register 28: USB Low-Speed Last Transaction to End of Frame Timing (USBLSEOF), offset 0x07E

This 8-bit configuration register specifies the minimum time gap that is to be allowed between the start of the last transaction and the EOF for low-speed transactions.

USB Low-Speed Last Transaction to End of Frame Timing (USBLSEOF)

Base 0x4005.0000
Offset 0x07E
Type RW, reset 0x72

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>LSEOFG</td>
<td>RW</td>
<td>0x72</td>
<td>Low-Speed End-of-Frame Gap</td>
</tr>
</tbody>
</table>

This field is used during low-speed transactions to set the gap between the last transaction and the End-of-Frame (EOF), in units of 1.067 µs. The default corresponds to 121.6 µs.
Register 29: USB Transmit Functional Address Endpoint 0 (USBTXFUNCADDR0), offset 0x080

Register 30: USB Transmit Functional Address Endpoint 1 (USBTXFUNCADDR1), offset 0x088

Register 31: USB Transmit Functional Address Endpoint 2 (USBTXFUNCADDR2), offset 0x090

Register 32: USB Transmit Functional Address Endpoint 3 (USBTXFUNCADDR3), offset 0x098

Register 33: USB Transmit Functional Address Endpoint 4 (USBTXFUNCADDR4), offset 0x0A0

Register 34: USB Transmit Functional Address Endpoint 5 (USBTXFUNCADDR5), offset 0x0A8

Register 35: USB Transmit Functional Address Endpoint 6 (USBTXFUNCADDR6), offset 0x0B0

Register 36: USB Transmit Functional Address Endpoint 7 (USBTXFUNCADDR7), offset 0x0B8

USBTXFUNCADDRn is an 8-bit read/write register that records the address of the target function to be accessed through the associated endpoint (EPn). USBTXFUNCADDRn must be defined for each transmit endpoint that is used.

Note: USBTXFUNCADDR0 is used for both receive and transmit for endpoint 0.

USB Transmit Functional Address Endpoint n (USBTXFUNCADDRn)
Base 0x4005.0000
Offset 0x080
Type RW, reset 0x00

Bit/Field | Name | Type | Reset | Description
---|---|---|---|---
7 | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

6:0 | ADDR | RW | 0x00 | Device Address
Specifies the USB bus address for the target Device.
Register 37: USB Transmit Hub Address Endpoint 0 (USBTXHUBADDR0), offset 0x082

Register 38: USB Transmit Hub Address Endpoint 1 (USBTXHUBADDR1), offset 0x08A

Register 39: USB Transmit Hub Address Endpoint 2 (USBTXHUBADDR2), offset 0x092

Register 40: USB Transmit Hub Address Endpoint 3 (USBTXHUBADDR3), offset 0x09A

Register 41: USB Transmit Hub Address Endpoint 4 (USBTXHUBADDR4), offset 0x0A2

Register 42: USB Transmit Hub Address Endpoint 5 (USBTXHUBADDR5), offset 0x0AA

Register 43: USB Transmit Hub Address Endpoint 6 (USBTXHUBADDR6), offset 0x0B2

Register 44: USB Transmit Hub Address Endpoint 7 (USBTXHUBADDR7), offset 0x0BA

USB Transmit Hub Address Endpoint n (USBTXHUBADDRn)
Base 0x4005.0000
Offset 0x082
Type RW, reset 0x00

**Bit/Field** | **Name** | **Type** | **Reset** | **Description**
--- | --- | --- | --- | ---
7 | reserved | RO | 0 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

6:0 | ADDR | RW | 0x00 | Hub Address
This field specifies the USB bus address for the USB 2.0 hub.
Register 45: USB Transmit Hub Port Endpoint 0 (USBTXHUBPORT0), offset 0x083
Register 46: USB Transmit Hub Port Endpoint 1 (USBTXHUBPORT1), offset 0x08B
Register 47: USB Transmit Hub Port Endpoint 2 (USBTXHUBPORT2), offset 0x093
Register 48: USB Transmit Hub Port Endpoint 3 (USBTXHUBPORT3), offset 0x09B
Register 49: USB Transmit Hub Port Endpoint 4 (USBTXHUBPORT4), offset 0x0A3
Register 50: USB Transmit Hub Port Endpoint 5 (USBTXHUBPORT5), offset 0x0AB
Register 51: USB Transmit Hub Port Endpoint 6 (USBTXHUBPORT6), offset 0x0B3
Register 52: USB Transmit Hub Port Endpoint 7 (USBTXHUBPORT7), offset 0x0BB

USBTXHUBPORTn is an 8-bit read/write register that, like USBTXHUBADDRn, only must be written when a full- or low-speed Device is connected to transmit endpoint EPn via a USB 2.0 hub. This register records the port of the USB 2.0 hub through which the target associated with the endpoint is accessed.

Note: USBTXHUBPORT0 is used for both receive and transmit for endpoint 0.
Register 53: USB Receive Functional Address Endpoint 1 (USBRXFUNCADDR1), offset 0x08C
Register 54: USB Receive Functional Address Endpoint 2 (USBRXFUNCADDR2), offset 0x094
Register 55: USB Receive Functional Address Endpoint 3 (USBRXFUNCADDR3), offset 0x09C
Register 56: USB Receive Functional Address Endpoint 4 (USBRXFUNCADDR4), offset 0x0A4
Register 57: USB Receive Functional Address Endpoint 5 (USBRXFUNCADDR5), offset 0x0AC
Register 58: USB Receive Functional Address Endpoint 6 (USBRXFUNCADDR6), offset 0x0B4
Register 59: USB Receive Functional Address Endpoint 7 (USBRXFUNCADDR7), offset 0x0BC

**OTG A / Host**

USBRXFUNCADDRn is an 8-bit read/write register that records the address of the target function accessed through the associated endpoint (EPn). **USBRXFUNCADDRn** must be defined for each receive endpoint that is used.

**Note:** **USBTXFUNCADDR0** is used for both receive and transmit for endpoint 0.

**USB Receive Functional Address Endpoint n (USBRXFUNCADDRn)**

Base 0x4005.0000
Offset 0x08C
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6:0</td>
<td>ADDR</td>
<td>RW</td>
<td>0x00</td>
<td>Device Address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field specifies the USB bus address for the target Device.</td>
</tr>
</tbody>
</table>
Register 60: USB Receive Hub Address Endpoint 1 (USBRXHUBADDR1), offset 0x08E
Register 61: USB Receive Hub Address Endpoint 2 (USBRXHUBADDR2), offset 0x096
Register 62: USB Receive Hub Address Endpoint 3 (USBRXHUBADDR3), offset 0x09E
Register 63: USB Receive Hub Address Endpoint 4 (USBRXHUBADDR4), offset 0x0A6
Register 64: USB Receive Hub Address Endpoint 5 (USBRXHUBADDR5), offset 0x0AE
Register 65: USB Receive Hub Address Endpoint 6 (USBRXHUBADDR6), offset 0x0B6
Register 66: USB Receive Hub Address Endpoint 7 (USBRXHUBADDR7), offset 0x0BE

**USBRXHUBADDRn** is an 8-bit read/write register that, like **USBRXHUBPORTn**, only must be written when a full- or low-speed Device is connected to receive endpoint EPn via a USB 2.0 hub. This register records the address of the USB 2.0 hub through which the target associated with the endpoint is accessed.

**Note**: **USBTXHUBADDR0** is used for both receive and transmit for endpoint 0.

USB Receive Hub Address Endpoint n (USBRXHUBADDRn)
Base 0x4005.0000
Offset 0x08E
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 6:0       | ADDR       | RW   | 0x00  | Hub Address
This field specifies the USB bus address for the USB 2.0 hub. |
Register 67: USB Receive Hub Port Endpoint 1 (USBRXHUBPORT1), offset 0x08F

Register 68: USB Receive Hub Port Endpoint 2 (USBRXHUBPORT2), offset 0x097

Register 69: USB Receive Hub Port Endpoint 3 (USBRXHUBPORT3), offset 0x09F

Register 70: USB Receive Hub Port Endpoint 4 (USBRXHUBPORT4), offset 0x0A7

Register 71: USB Receive Hub Port Endpoint 5 (USBRXHUBPORT5), offset 0x0AF

Register 72: USB Receive Hub Port Endpoint 6 (USBRXHUBPORT6), offset 0x0B7

Register 73: USB Receive Hub Port Endpoint 7 (USBRXHUBPORT7), offset 0x0BF

**OTG A / Host**

**USBRXHUBPORTn** is an 8-bit read/write register that, like **USBRXHUBADDRn**, only must be written when a full- or low-speed Device is connected to receive endpoint EPn via a USB 2.0 hub. This register records the port of the USB 2.0 hub through which the target associated with the endpoint is accessed.

**Note:** **USBTXHUBPORT0** is used for both receive and transmit for endpoint 0.

USB Receive Hub Port Endpoint n (USBRXHUBPORTn)
Base 0x4005.0000
Offset 0x08F
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Type</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>7</td>
<td>reserved</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RW</td>
<td>6:0</td>
<td>PORT</td>
<td>0x00</td>
<td>Hub Port</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field specifies the USB hub port number.</td>
</tr>
</tbody>
</table>
Register 74: USB Maximum Transmit Data Endpoint 1 (USBTXMAXP1), offset 0x110
Register 75: USB Maximum Transmit Data Endpoint 2 (USBTXMAXP2), offset 0x120
Register 76: USB Maximum Transmit Data Endpoint 3 (USBTXMAXP3), offset 0x130
Register 77: USB Maximum Transmit Data Endpoint 4 (USBTXMAXP4), offset 0x140
Register 78: USB Maximum Transmit Data Endpoint 5 (USBTXMAXP5), offset 0x150
Register 79: USB Maximum Transmit Data Endpoint 6 (USBTXMAXP6), offset 0x160
Register 80: USB Maximum Transmit Data Endpoint 7 (USBTXMAXP7), offset 0x170

The **USBTXMAXPn** 16-bit register defines the maximum amount of data that can be transferred through the transmit endpoint in a single operation.

Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the **USB Specification** on packet sizes for bulk, interrupt and isochronous transfers in full-speed operation.

The total amount of data represented by the value written to this register must not exceed the FIFO size for the transmit endpoint, and must not exceed half the FIFO size if double-buffering is required.

If this register is changed after packets have been sent from the endpoint, the transmit endpoint FIFO must be completely flushed (using the **FLUSH** bit in **USBTXCSRLn**) after writing the new value to this register.

**Note:** **USBTXMAXPn** must be set to an even number of bytes for proper interrupt generation in µDMA Basic Mode.
Register 81: USB Control and Status Endpoint 0 Low (USBCSRL0), offset 0x102

USBCSRL0 is an 8-bit register that provides control and status bits for endpoint 0.

OTG A / Host Mode

USB Control and Status Endpoint 0 Low (USBCSRL0)
Base 0x4005.0000
Offset 0x102
Type W1C, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>NAKTO</td>
<td>RW</td>
<td>0</td>
<td>NAK Timeout</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No timeout.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Indicates that endpoint 0 is halted following the receipt of NAK responses for longer than the time set by the USBNAKLMT register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must clear this bit to allow the endpoint to continue.</td>
</tr>
<tr>
<td>6</td>
<td>STATUS</td>
<td>RW</td>
<td>0</td>
<td>STATUS Packet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No transaction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Initiates a STATUS stage transaction. This bit must be set at the same time as the TXRDY or REQPKT bit is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Setting this bit ensures that the DT bit is set in the USBCSRH0 register so that a DATA1 packet is used for the STATUS stage transaction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is automatically cleared when the STATUS stage is over.</td>
</tr>
<tr>
<td>5</td>
<td>REQPKT</td>
<td>RW</td>
<td>0</td>
<td>Request Packet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  Requests an IN transaction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared when the RXRDY bit is set.</td>
</tr>
</tbody>
</table>
### Universal Serial Bus (USB) Controller

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>ERROR</td>
<td>RW</td>
<td>0</td>
<td>Error</td>
</tr>
<tr>
<td>3</td>
<td>SETUP</td>
<td>RW</td>
<td>0</td>
<td>Setup Packet</td>
</tr>
<tr>
<td>2</td>
<td>STALLED</td>
<td>RW</td>
<td>0</td>
<td>Endpoint Stalled</td>
</tr>
<tr>
<td>1</td>
<td>TXRDY</td>
<td>RW</td>
<td>0</td>
<td>Transmit Packet Ready</td>
</tr>
<tr>
<td>0</td>
<td>RXRDY</td>
<td>RW</td>
<td>0</td>
<td>Receive Packet Ready</td>
</tr>
</tbody>
</table>

#### Description

- **Value Description**
- **0** No error.
- **1** Three attempts have been made to perform a transaction with no response from the peripheral. The EP0 bit in the USBTXIS register is also set in this situation.

Software must clear this bit.

- **Value Description**
- **0** Sends an OUT token.
- **1** Sends a SETUP token instead of an OUT token for the transaction. This bit should be set at the same time as the TXRDY bit is set.

Setting this bit always clears the DT bit in the USBCSRH0 register to send a DATA0 packet.

- **Value Description**
- **0** No handshake has been received.
- **1** A STALL handshake has been received.

Software must clear this bit.

- **Value Description**
- **0** No transmit packet is ready.
- **1** Software sets this bit after loading a data packet into the TX FIFO. The EP0 bit in the USBTXIS register is also set in this situation.

If both the TXRDY and SETUP bits are set, a setup packet is sent. If just TXRDY is set, an OUT packet is sent.

This bit is cleared automatically when the data packet has been transmitted.

- **Value Description**
- **0** No received packet has been received.
- **1** Indicates that a data packet has been received in the RX FIFO. The EP0 bit in the USBTXIS register is also set in this situation.

Software must clear this bit after the packet has been read from the FIFO to acknowledge that the data has been read from the FIFO.
OTG B / Device Mode

USB Control and Status Endpoint 0 Low (USBCSRL0)

Base 0x4005.0000
Offset 0x102
Type W1C, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>SETENDC</td>
<td>W1C</td>
<td>0</td>
<td>Setup End Clear&lt;br&gt;Writing a 1 to this bit clears the SETEND bit.</td>
</tr>
<tr>
<td>6</td>
<td>RXRDYC</td>
<td>W1C</td>
<td>0</td>
<td>RXRDY Clear&lt;br&gt;Writing a 1 to this bit clears the RXRDY bit.</td>
</tr>
<tr>
<td>5</td>
<td>STALL</td>
<td>RW</td>
<td>0</td>
<td>Send Stall&lt;br&gt;Value Description&lt;br&gt;0: No effect.&lt;br&gt;1: Terminates the current transaction and transmits the STALL handshake. This bit is cleared automatically after the STALL handshake is transmitted.</td>
</tr>
<tr>
<td>4</td>
<td>SETEND</td>
<td>RO</td>
<td>0</td>
<td>Setup End&lt;br&gt;Value Description&lt;br&gt;0: A control transaction has not ended or ended after the DATAEND bit was set.&lt;br&gt;1: A control transaction has ended before the DATAEND bit has been set. The EP0 bit in the USBTXIS register is also set in this situation. This bit is cleared by writing a 1 to the SETENDC bit.</td>
</tr>
<tr>
<td>3</td>
<td>DATAEND</td>
<td>RW</td>
<td>0</td>
<td>Data End&lt;br&gt;Value Description&lt;br&gt;0: No effect.&lt;br&gt;1: Set this bit in the following situations:&lt;br&gt;  ■ When setting TXRDY for the last data packet&lt;br&gt;  ■ When clearing RXRDY after unloading the last data packet&lt;br&gt;  ■ When setting TXRDY for a zero-length data packet&lt;br&gt;This bit is cleared automatically.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------</td>
<td>------</td>
<td>-------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>STALLED</td>
<td>RW</td>
<td>0</td>
<td>Endpoint Stalled</td>
</tr>
<tr>
<td>1</td>
<td>TXRDY</td>
<td>RW</td>
<td>0</td>
<td>Transmit Packet Ready</td>
</tr>
<tr>
<td>0</td>
<td>RXRDY</td>
<td>RO</td>
<td>0</td>
<td>Receive Packet Ready</td>
</tr>
</tbody>
</table>

**STALLED**

- **Value**
  - 0: A STALL handshake has not been transmitted.
  - 1: A STALL handshake has been transmitted.

Software must clear this bit.

**TXRDY**

- **Value**
  - 0: No transmit packet is ready.
  - 1: Software sets this bit after loading an IN data packet into the TX FIFO. The EP0 bit in the USBTXIS register is also set in this situation.

This bit is cleared automatically when the data packet has been transmitted.

**RXRDY**

- **Value**
  - 0: No data packet has been received.
  - 1: A data packet has been received. The EP0 bit in the USBTXIS register is also set in this situation.

This bit is cleared by writing a 1 to the RXRDYC bit.
Register 82: USB Control and Status Endpoint 0 High (USBCSRH0), offset 0x103

**OTG A / Host**

**OTG B / Device**

**USBSRH0** is an 8-bit register that provides control and status bits for endpoint 0.

### OTG A / Host Mode

**USB Control and Status Endpoint 0 High (USBCSRH0)**

<table>
<thead>
<tr>
<th>Base 0x4005.0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset 0x103</td>
</tr>
<tr>
<td>Type WR, reset 0x00</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>DTWE</td>
<td>RW</td>
<td>0</td>
<td>Data Toggle Write Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The DT bit cannot be written.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables the current state of the endpoint 0 data toggle to be written</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(see DT bit).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is automatically cleared once the new value is written.</td>
</tr>
<tr>
<td>1</td>
<td>DT</td>
<td>RW</td>
<td>0</td>
<td>Data Toggle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When read, this bit indicates the current state of the endpoint 0 data</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>toggle.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If DTWE is set, this bit may be written with the required setting of the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>data toggle. If DTWE is Low, this bit cannot be written. Care should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>taken when writing to this bit as it should only be changed to RESET USB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>endpoint 0.</td>
</tr>
</tbody>
</table>

**June 12, 2014**  
**Texas Instruments-Production Data**
Flush FIFO

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>FLUSH</td>
<td>RW</td>
<td>0</td>
<td>Flush FIFO</td>
</tr>
</tbody>
</table>

**Value** | **Description**
---|---
0 | No effect.
1 | Flushes the next packet to be transmitted/read from the endpoint 0 FIFO. The FIFO pointer is reset and the TXRDY/RXRDY bit is cleared.

This bit is automatically cleared after the flush is performed.

**Important:** This bit should only be set when TXRDY is clear and RXRDY is set. At other times, it may cause data to be corrupted.

---

**OTG B / Device Mode**

USB Control and Status Endpoint 0 High (USBCSRH0)

Base 0x4005.0000
Offset 0x103
Type W1C, reset 0x00

---

**Bit/Field** | **Name** | **Type** | **Reset** | **Description**
---|---|---|---|---
7:1 | reserved | RO | 0x00 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
0 | FLUSH | RW | 0 | Flush FIFO

**Value** | **Description**
---|---
0 | No effect.
1 | Flushes the next packet to be transmitted/read from the endpoint 0 FIFO. The FIFO pointer is reset and the TXRDY/RXRDY bit is cleared.

This bit is automatically cleared after the flush is performed.

**Important:** This bit should only be set when TXRDY is clear and RXRDY is set. At other times, it may cause data to be corrupted.
Register 83: USB Receive Byte Count Endpoint 0 (USBCOUNT0), offset 0x108

**USBCOUNT0** is an 8-bit read-only register that indicates the number of received data bytes in the endpoint 0 FIFO. The value returned changes as the contents of the FIFO change and is only valid while the **RXRDY** bit is set.

### USB Receive Byte Count Endpoint 0 (USBCOUNT0)

- **Base**: 0x4005.0000
- **Offset**: 0x108
- **Type**: RO, reset 0x00

```
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6:0</td>
<td>COUNT</td>
<td>RO</td>
<td>0x00</td>
<td><strong>FIFO Count</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>COUNT</strong> is a read-only value that indicates the number of received data bytes in the endpoint 0 FIFO.</td>
</tr>
</tbody>
</table>
```
## Register 84: USB Type Endpoint 0 (USBTYPE0), offset 0x10A

This is an 8-bit register that must be written with the operating speed of the targeted Device being communicated with using endpoint 0.

**USB Type Endpoint 0 (USBTYPE0)**

This register must be written with the operating speed of the Device being communicated with using endpoint 0.

**OTG A / Host**

**Offset 0x10A**  
**Type RW, reset 0x00**

### Bit/Field Name Type Reset Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7:6       | SPEED | RW   | 0x0   | Operating Speed  
This field specifies the operating speed of the target Device. If selected, the target is assumed to have the same connection speed as the USB controller. |
| 5:0       | reserved | RO | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
|           |       |     |       | Value Description                                 |
|           |       |     |       | 0x0 - 0x1 Reserved                                |
|           |       |     |       | 0x2 Full                                          |
|           |       |     |       | 0x3 Low                                          |
Register 85: USB NAK Limit (USBNAKLMT), offset 0x10B

USBNAKLMT is an 8-bit register that sets the number of frames after which endpoint 0 should time out on receiving a stream of NAK responses. (Equivalent settings for other endpoints can be made through their USBTXINTERVALn and USBRXINTERVALn registers.)

The number of frames selected is $2^{(m-1)}$ (where $m$ is the value set in the register, with valid values of 2–16). If the Host receives NAK responses from the target for more frames than the number represented by the limit set in this register, the endpoint is halted.

**Note:** A value of 0 or 1 disables the NAK timeout function.
Register 86: USB Transmit Control and Status Endpoint 1 Low (USBTXCSRL1), offset 0x112
Register 87: USB Transmit Control and Status Endpoint 2 Low (USBTXCSRL2), offset 0x122
Register 88: USB Transmit Control and Status Endpoint 3 Low (USBTXCSRL3), offset 0x132
Register 89: USB Transmit Control and Status Endpoint 4 Low (USBTXCSRL4), offset 0x142
Register 90: USB Transmit Control and Status Endpoint 5 Low (USBTXCSRL5), offset 0x152
Register 91: USB Transmit Control and Status Endpoint 6 Low (USBTXCSRL6), offset 0x162
Register 92: USB Transmit Control and Status Endpoint 7 Low (USBTXCSRL7), offset 0x172

USBTXCSRLn is an 8-bit register that provides control and status bits for transfers through the currently selected transmit endpoint.

### OTG A / Host Mode

USB Transmit Control and Status Endpoint n Low (USBTXCSRLn)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>NAKTO</td>
<td>RW</td>
<td>0</td>
<td>NAK Timeout</td>
</tr>
</tbody>
</table>

Value Description
0 No timeout.
1 *Bulk endpoints only:* Indicates that the transmit endpoint is halted following the receipt of NAK responses for longer than the time set by the NAKLMT field in the USBXINTERVALn register.

Software must clear this bit to allow the endpoint to continue.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>CLRDT</td>
<td>RW</td>
<td>0</td>
<td>Clear Data Toggle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the DT bit in the USBTXCSRHn register.</td>
</tr>
<tr>
<td>5</td>
<td>STALLED</td>
<td>RW</td>
<td>0</td>
<td>Endpoint Stalled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>any µDMA request that is in progress is stopped, the FIFO is completely</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>flushed, and the TXRDY bit is cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must clear this bit.</td>
</tr>
<tr>
<td>4</td>
<td>SETUP</td>
<td>RW</td>
<td>0</td>
<td>Setup Packet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>should be set at the same time as the TXRDY bit is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> Setting this bit also clears the DT bit in the USBTXCSRHn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>3</td>
<td>FLUSH</td>
<td>RW</td>
<td>0</td>
<td>Flush FIFO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pointer is reset and the TXRDY bit is cleared. The EPn bit in the USBTXIS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is also set in this situation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit may be set simultaneously with the TXRDY bit to abort the packet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>that is currently being loaded into the FIFO. Note that if the FIFO is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>double-buffered, FLUSH may have to be set twice to completely clear the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>FIFO.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Important:</strong> This bit should only be set when the TXRDY bit is clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>At other times, it may cause data to be corrupted.</td>
</tr>
<tr>
<td>2</td>
<td>ERROR</td>
<td>RW</td>
<td>0</td>
<td>Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>has been received. The TXRDY bit is cleared, the EPn bit in the USBTXIS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is set, and the FIFO is completely flushed in this situation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must clear this bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This is valid only when the endpoint is operating in Bulk or</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Interrupt mode.</td>
</tr>
</tbody>
</table>

**Texas Instruments-Production Data**
### OTG B / Device Mode

#### USB Transmit Control and Status Endpoint n Low (USBTXCSRLn)

Base 0x4005.0000
Offset 0x112
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>6</td>
<td>CLRDT</td>
<td>RW</td>
<td>0</td>
<td>Clear Data Toggle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the DT bit in the USBTXCSRHn register.</td>
</tr>
<tr>
<td>5</td>
<td>STALLED</td>
<td>RW</td>
<td>0</td>
<td>Endpoint Stalled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>A STALL handshake has not been transmitted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>A STALL handshake has been transmitted. The FIFO is flushed and the TXRDY bit is cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must clear this bit.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>4</td>
<td>STALL</td>
<td>RW</td>
<td>0</td>
<td>Send STALL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software clears this bit to terminate the STALL condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This bit has no effect in isochronous transfers.</td>
</tr>
<tr>
<td>3</td>
<td>FLUSH</td>
<td>RW</td>
<td>0</td>
<td>Flush FIFO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit may be set simultaneously with the TXRDY bit to abort the packet that is currently being loaded into the FIFO. Note that if the FIFO is double-buffered, FLUSH may have to be set twice to completely clear the FIFO.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Important:</strong> This bit should only be set when the TXRDY bit is clear. At other times, it may cause data to be corrupted.</td>
</tr>
<tr>
<td>2</td>
<td>UNDRN</td>
<td>RW</td>
<td>0</td>
<td>Underrun</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must clear this bit.</td>
</tr>
<tr>
<td>1</td>
<td>FIFONE</td>
<td>RW</td>
<td>0</td>
<td>FIFO Not Empty</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>TXRDY</td>
<td>RW</td>
<td>0</td>
<td>Transmit Packet Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared automatically when a data packet has been transmitted. The $EP_n$ bit in the $USBTXIS$ register is also set at this point. TXRDY is also automatically cleared prior to loading a second packet into a double-buffered FIFO.</td>
</tr>
</tbody>
</table>
Register 93: USB Transmit Control and Status Endpoint 1 High (USBTXCSRH1), offset 0x113

Register 94: USB Transmit Control and Status Endpoint 2 High (USBTXCSRH2), offset 0x123

Register 95: USB Transmit Control and Status Endpoint 3 High (USBTXCSRH3), offset 0x133

Register 96: USB Transmit Control and Status Endpoint 4 High (USBTXCSRH4), offset 0x143

Register 97: USB Transmit Control and Status Endpoint 5 High (USBTXCSRH5), offset 0x153

Register 98: USB Transmit Control and Status Endpoint 6 High (USBTXCSRH6), offset 0x163

Register 99: USB Transmit Control and Status Endpoint 7 High (USBTXCSRH7), offset 0x173

USBTXCSRHn is an 8-bit register that provides additional control for transfers through the currently selected transmit endpoint.

**OTG A / Host Mode**

**USB Transmit Control and Status Endpoint n High (USBTXCSRHn)**

Base 0x4005.0000
Offset 0x113
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUTOSET</td>
<td>reserved</td>
<td>MODE</td>
<td>DMAEN</td>
<td>FDT</td>
<td>DMAMOD</td>
<td>DTWE</td>
<td>DT</td>
</tr>
</tbody>
</table>

**Type**

- RW: Read/Write
- RO: Read Only

**Reset**

- 0: Auto Set

**Bit/Field**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>AUTOSET</td>
<td>RW</td>
<td>0</td>
<td>Auto Set</td>
</tr>
</tbody>
</table>

**Description**

- **Value**
- **Description**

- 0: The TXRDY bit must be set manually.

- 1: Enables the TXRDY bit to be automatically set when data of the maximum packet size (value in USBTXMAXPn) is loaded into the transmit FIFO. If a packet of less than the maximum packet size is loaded, then the TXRDY bit must be set manually.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>MODE</td>
<td>RW</td>
<td>0</td>
<td>Mode</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Enables the endpoint direction as RX.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enables the endpoint direction as TX.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Note: This bit only has an effect when the same endpoint FIFO is used for both transmit and receive transactions.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>DMAEN</td>
<td>RW</td>
<td>0</td>
<td>DMA Request Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Disables the DMA request for the transmit endpoint.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enables the DMA request for the transmit endpoint.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Note: 3 TX and 3 RX endpoints can be connected to the µDMA module. If this bit is set for a particular endpoint, the DMAATX, DMABTX, or DMACTX field in the USB DMA Select (USBDMASEL) register must be programmed correspondingly.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>FDT</td>
<td>RW</td>
<td>0</td>
<td>Force Data Toggle</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No effect.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Forces the endpoint DT bit to switch and the data packet to be cleared from the FIFO, regardless of whether an ACK was received. This bit can be used by interrupt transmit endpoints that are used to communicate rate feedback for isochronous endpoints.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>DMAMOD</td>
<td>RW</td>
<td>0</td>
<td>DMA Request Mode</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>An interrupt is generated after every DMA packet transfer.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is generated only after the entire DMA transfer is complete.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Note: This bit must not be cleared either before or in the same cycle as the above DMAEN bit is cleared.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>DTWE</td>
<td>RW</td>
<td>0</td>
<td>Data Toggle Write Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>The DT bit cannot be written.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Enables the current state of the transmit endpoint data to be written (see DT bit).</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This bit is automatically cleared once the new value is written.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**Data Toggle**

When read, this bit indicates the current state of the transmit endpoint data toggle.

If DTWE is High, this bit may be written with the required setting of the data toggle. If DTWE is Low, any value written to this bit is ignored. Care should be taken when writing to this bit as it should only be changed to RESET the transmit endpoint.

### OTG B / Device Mode

**USB Transmit Control and Status Endpoint n High (USBTXCSRHn)**

<table>
<thead>
<tr>
<th>Base 0x4005.0000</th>
<th>Offset 0x113</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type RW, reset 0x00</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>AUTOSET</td>
<td>RW</td>
<td>0</td>
<td>Auto Set</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Value** | **Description**
---|---
0 | The TXRDY bit must be set manually.
1 | Enables the TXRDY bit to be automatically set when data of the maximum packet size (value in USBTXMAXPn) is loaded into the transmit FIFO. If a packet of less than the maximum packet size is loaded, then the TXRDY bit must be set manually.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>ISO</td>
<td>RW</td>
<td>0</td>
<td>Isochronous Transfers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Value** | **Description**
---|---
0 | Enables the transmit endpoint for bulk or interrupt transfers.
1 | Enables the transmit endpoint for isochronous transfers.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>MODE</td>
<td>RW</td>
<td>0</td>
<td>Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Value** | **Description**
---|---
0 | Enables the endpoint direction as RX.
1 | Enables the endpoint direction as TX.

**Note:** This bit only has an effect where the same endpoint FIFO is used for both transmit and receive transactions.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>DMAEN</td>
<td>RW</td>
<td>0</td>
<td>DMA Request Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>3 TX and 3 RX endpoints can be connected to the µDMA module. If this bit is set for a particular endpoint, the DMAATX, DMABTX, or DMACTX field in the USB DMA Select (USBDMASEL) register must be programmed correspondingly.</td>
</tr>
<tr>
<td>3</td>
<td>FDT</td>
<td>RW</td>
<td>0</td>
<td>Force Data Toggle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>DMAMOD</td>
<td>RW</td>
<td>0</td>
<td>DMA Request Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Note:</td>
<td></td>
<td></td>
<td></td>
<td>This bit must not be cleared either before or in the same cycle as the above DMAEN bit is cleared.</td>
</tr>
<tr>
<td>1:0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 100: USB Maximum Receive Data Endpoint 1 (USBRXMAXP1), offset 0x114

Register 101: USB Maximum Receive Data Endpoint 2 (USBRXMAXP2), offset 0x124

Register 102: USB Maximum Receive Data Endpoint 3 (USBRXMAXP3), offset 0x134

Register 103: USB Maximum Receive Data Endpoint 4 (USBRXMAXP4), offset 0x144

Register 104: USB Maximum Receive Data Endpoint 5 (USBRXMAXP5), offset 0x154

Register 105: USB Maximum Receive Data Endpoint 6 (USBRXMAXP6), offset 0x164

Register 106: USB Maximum Receive Data Endpoint 7 (USBRXMAXP7), offset 0x174

OTG A / Host

OTG B / Device

The USBRXMAXPn is a 16-bit register which defines the maximum amount of data that can be transferred through the selected receive endpoint in a single operation.

Bits 10:0 define (in bytes) the maximum payload transmitted in a single transaction. The value set can be up to 1024 bytes but is subject to the constraints placed by the USB Specification on packet sizes for bulk, interrupt and isochronous transfers in full-speed operations.

The total amount of data represented by the value written to this register must not exceed the FIFO size for the receive endpoint, and must not exceed half the FIFO size if double-buffering is required.

Note: USBRXMAXPn must be set to an even number of bytes for proper interrupt generation in µDMA Basic mode.

USB Maximum Receive Data Endpoint n (USBRXMAXPn)

Base 0x4005.0000
Offset 0x114
Type RW, reset 0x0000

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:11</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 10:0      | MAXLOAD   | RW   | 0x000 | Maximum Payload
The maximum payload in bytes per transaction.
Register 107: USB Receive Control and Status Endpoint 1 Low (USBRXCSRL1), offset 0x116
Register 108: USB Receive Control and Status Endpoint 2 Low (USBRXCSRL2), offset 0x126
Register 109: USB Receive Control and Status Endpoint 3 Low (USBRXCSRL3), offset 0x136
Register 110: USB Receive Control and Status Endpoint 4 Low (USBRXCSRL4), offset 0x146
Register 111: USB Receive Control and Status Endpoint 5 Low (USBRXCSRL5), offset 0x156
Register 112: USB Receive Control and Status Endpoint 6 Low (USBRXCSRL6), offset 0x166
Register 113: USB Receive Control and Status Endpoint 7 Low (USBRXCSRL7), offset 0x176

USBRXCSRLn is an 8-bit register that provides control and status bits for transfers through the currently selected receive endpoint.

OTG A / Host Mode

USB Receive Control and Status Endpoint n Low (USBRXCSRLn)
Base 0x4005.0000
Offset 0x116
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>CLRDT</td>
<td>W1C</td>
<td>0</td>
<td>Clear Data Toggle</td>
</tr>
</tbody>
</table>

Writing a 1 to this bit clears the DT bit in the USBXCSRn register.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>STALLED</td>
<td>RW</td>
<td>0</td>
<td>Endpoint Stalled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>A STALL handshake has not been received.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 A STALL handshake has been received. The EPn bit in the USBRXIS register is also set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Software must clear this bit.</strong></td>
</tr>
<tr>
<td>5</td>
<td>REQPKT</td>
<td>RW</td>
<td>0</td>
<td>Request Packet</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Requests an IN transaction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>This bit is cleared when RXRDY is set.</strong></td>
</tr>
<tr>
<td>4</td>
<td>FLUSH</td>
<td>RW</td>
<td>0</td>
<td>Flush FIFO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Flushes the next packet to be read from the endpoint receive FIFO. The FIFO pointer is reset and the RXRDY bit is cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note that if the FIFO is double-buffered, FLUSH may have to be set twice to completely clear the FIFO.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Important:</strong> This bit should only be set when the RXRDY bit is set. At other times, it may cause data to be corrupted.</td>
</tr>
<tr>
<td>3</td>
<td>DATAERR / NAKTO</td>
<td>RW</td>
<td>0</td>
<td>Data Error / NAK Timeout</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Normal operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Isochronous endpoints only: Indicates that RXRDY is set and the data packet has a CRC or bit-stuff error. This bit is cleared when RXRDY is cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Bulk endpoints only: Indicates that the receive endpoint is halted following the receipt of NAK responses for longer than the time set by the NAXLMT field in the USBRXINTERVALn register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must clear this bit to allow the endpoint to continue.</td>
</tr>
<tr>
<td>2</td>
<td>ERROR</td>
<td>RW</td>
<td>0</td>
<td>Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Three attempts have been made to receive a packet and no data packet has been received. The EPn bit in the USBRXIS register is set in this situation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Software must clear this bit.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This bit is only valid when the receive endpoint is operating in Bulk or Interrupt mode. In Isochronous mode, it always returns zero.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>1</td>
<td>FULL</td>
<td>RO</td>
<td>0</td>
<td>FIFO Full</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0             The receive FIFO is not full.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1             No more packets can be loaded into the receive FIFO.</td>
</tr>
<tr>
<td>0</td>
<td>RXRDY</td>
<td>RW</td>
<td>0</td>
<td>Receive Packet Ready</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0             No data packet has been received.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1             A data packet has been received. The ( EP_n ) bit in the USBRXIS register is also set in this situation.</td>
</tr>
</tbody>
</table>

If the AUTOCLR bit in the USBRXCSR\(Rn\) register is set, then the this bit is automatically cleared when a packet of USBRXMAX\(P_n\) bytes has been unloaded from the receive FIFO. If the AUTOCLR bit is clear, or if packets of less than the maximum packet size are unloaded, then software must clear this bit manually when the packet has been unloaded from the receive FIFO.

**OTG B / Device Mode**

USB Receive Control and Status Endpoint n Low (USBRXCSR\(Ln\))

Base 0x4005.0000
Offset 0x116
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Type</th>
<th>W1C</th>
<th>RW</th>
<th>RW</th>
<th>RW</th>
<th>RO</th>
<th>RW</th>
<th>RO</th>
<th>RW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>CLRDT</td>
<td>W1C</td>
<td>0</td>
<td>Clear Data Toggle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears the DT bit in the USBRXCSR(Rn) register.</td>
</tr>
<tr>
<td>6</td>
<td>STALLED</td>
<td>RW</td>
<td>0</td>
<td>Endpoint Stalled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0             A STALL handshake has not been transmitted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1             A STALL handshake has been transmitted.</td>
</tr>
</tbody>
</table>

Software must clear this bit.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>STALL</td>
<td>RW</td>
<td>0</td>
<td>Send STALL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must clear this bit to terminate the STALL condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This bit has no effect where the endpoint is being used for isochronous transfers.</td>
</tr>
<tr>
<td>4</td>
<td>FLUSH</td>
<td>RW</td>
<td>0</td>
<td>Flush FIFO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The CPU writes a 1 to this bit to flush the next packet to be read from the endpoint receive FIFO. The FIFO pointer is reset and the RXRDY bit is cleared. Note that if the FIFO is double-buffered, FLUSH may have to be set twice to completely clear the FIFO.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Important:</strong> This bit should only be set when the RXRDY bit is set. At other times, it may cause data to be corrupted.</td>
</tr>
<tr>
<td>3</td>
<td>DATAERR</td>
<td>RO</td>
<td>0</td>
<td>Data Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared when RXRDY is cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This bit is only valid when the endpoint is operating in Isochronous mode. In Bulk mode, it always returns zero.</td>
</tr>
<tr>
<td>2</td>
<td>OVER</td>
<td>RW</td>
<td>0</td>
<td>Overrun</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must clear this bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> This bit is only valid when the endpoint is operating in Isochronous mode. In Bulk mode, it always returns zero.</td>
</tr>
<tr>
<td>1</td>
<td>FULL</td>
<td>RO</td>
<td>0</td>
<td>FIFO Full</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>0</td>
<td>RXRDY</td>
<td>RW</td>
<td>0</td>
<td>Receive Packet Ready</td>
</tr>
</tbody>
</table>

Value Description

- 0 No data packet has been received.
- 1 A data packet has been received. The EPn bit in the USBRXIS register is also set in this situation.

If the AUTOCLR bit in the USBRXCSRHn register is set, then this bit is automatically cleared when a packet of USBRXMAXPn bytes has been unloaded from the receive FIFO. If the AUTOCLR bit is clear, or if packets of less than the maximum packet size are unloaded, then software must clear this bit manually when the packet has been unloaded from the receive FIFO.
Register 114: USB Receive Control and Status Endpoint 1 High (USBRXCSRH1), offset 0x117
Register 115: USB Receive Control and Status Endpoint 2 High (USBRXCSRH2), offset 0x127
Register 116: USB Receive Control and Status Endpoint 3 High (USBRXCSRH3), offset 0x137
Register 117: USB Receive Control and Status Endpoint 4 High (USBRXCSRH4), offset 0x147
Register 118: USB Receive Control and Status Endpoint 5 High (USBRXCSRH5), offset 0x157
Register 119: USB Receive Control and Status Endpoint 6 High (USBRXCSRH6), offset 0x167
Register 120: USB Receive Control and Status Endpoint 7 High (USBRXCSRH7), offset 0x177

USBRXCSRHn is an 8-bit register that provides additional control and status bits for transfers through the currently selected receive endpoint.

OTG A / Host

OTG B / Device

OTG A / Host Mode

USB Receive Control and Status Endpoint n High (USBRXCSRHn)
Base 0x4005.0000
Offset 0x117
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUTOCL</td>
<td>AUTORQ</td>
<td>DMAEN</td>
<td>PIDERR</td>
<td>DMAMOD</td>
<td>DTWE</td>
<td>DT</td>
<td>reserved</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>RW</th>
<th>RW</th>
<th>RW</th>
<th>RO</th>
<th>RW</th>
<th>RO</th>
<th>RO</th>
<th>RO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----------</td>
<td>---------</td>
<td>------</td>
<td>-------</td>
<td>----------------------------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>AUTOCL</td>
<td>RW</td>
<td>0</td>
<td>Auto Clear</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>AUTORQ</td>
<td>RW</td>
<td>0</td>
<td>Auto Request</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DMAEN</td>
<td>RW</td>
<td>0</td>
<td>DMA Request Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PIDERR</td>
<td>RO</td>
<td>0</td>
<td>PID Error</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>DMAMOD</td>
<td>RW</td>
<td>0</td>
<td>DMA Request Mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### AUTOCL

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No effect.</td>
</tr>
<tr>
<td>1</td>
<td>Enables the RXRDY bit to be automatically cleared when a packet of USBRXMAXPn bytes has been unloaded from the receive FIFO. When packets of less than the maximum packet size are unloaded, RXRDY must be cleared manually. Care must be taken when using µDMA to unload the receive FIFO as data is read from the receive FIFO in 4 byte chunks regardless of the value of the MAXLOAD field in the USBRXMAXPn register; see &quot;DMA Operation&quot; on page 1133.</td>
</tr>
</tbody>
</table>

**Note:** This bit is automatically cleared when a short packet is received.

### AUTORQ

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No effect.</td>
</tr>
<tr>
<td>1</td>
<td>Enables the REQPKT bit to be automatically set when the RXRDY bit is cleared.</td>
</tr>
</tbody>
</table>

**Note:** This bit is automatically cleared when a short packet is received.

### DMAEN

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Disables the µDMA request for the receive endpoint.</td>
</tr>
<tr>
<td>1</td>
<td>Enables the µDMA request for the receive endpoint.</td>
</tr>
</tbody>
</table>

**Note:** 3 TX and 3 RX endpoints can be connected to the µDMA module. If this bit is set for a particular endpoint, the DMAARX, DMABRX, or DMACRX field in the USB DMA Select (USBDMASEL) register must be programmed correspondingly.

### PIDERR

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No error.</td>
</tr>
<tr>
<td>1</td>
<td>Indicates a PID error in the received packet of an isochronous transaction.</td>
</tr>
</tbody>
</table>

This bit is ignored in bulk or interrupt transactions.

### DMAMOD

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An interrupt is generated after every µDMA packet transfer.</td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is generated only after the entire µDMA transfer is complete.</td>
</tr>
</tbody>
</table>

**Note:** This bit must not be cleared either before or in the same cycle as the above DMAEN bit is cleared.
**Data Toggle (DTWE)**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>DTWE</td>
<td>RO</td>
<td>0</td>
<td>Data Toggle Write Enable</td>
</tr>
</tbody>
</table>

**Value**  
- **0**: The DT bit cannot be written.  
- **1**: Enables the current state of the receive endpoint data to be written (see DT bit).

This bit is automatically cleared once the new value is written.

**Data Toggle (DT)**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DT</td>
<td>RO</td>
<td>0</td>
<td>Data Toggle</td>
</tr>
</tbody>
</table>

When read, this bit indicates the current state of the receive data toggle. If DTWE is High, this bit may be written with the required setting of the data toggle. If DTWE is Low, any value written to this bit is ignored. Care should be taken when writing to this bit as it should only be changed to RESET the receive endpoint.

**Software reserved (reserved)**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 0         | reserved | RO   | 0     | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

---

**OTG B / Device Mode**

USB Receive Control and Status Endpoint n High (USBRXCSRHn)

**Base 0x4005.0000**  
**Offset 0x117**  
**Type RW, reset 0x00**

```
7 6 5 4 3 2 1 0
AUTOCL ISO DMAEN DISKIT/PIDERR DMAMOD reserved
```

**Bit/Field**  
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>AUTOCL</td>
<td>RW</td>
<td>0</td>
<td>Auto Clear</td>
</tr>
</tbody>
</table>

**Value**  
- **0**: No effect.  
- **1**: Enables the RXRDY bit to be automatically cleared when a packet of USBRXMAXPn bytes has been unloaded from the receive FIFO. When packets of less than the maximum packet size are unloaded, RXRDY must be cleared manually. Care must be taken when using µDMA to unload the receive FIFO as data is read from the receive FIFO in 4 byte chunks regardless of the value of the MAXLOAD field in the USBRXMAXPn register, see “DMA Operation” on page 1133.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>ISO</td>
<td>RW</td>
<td>0</td>
<td>Isochronous Transfers</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Enables the receive endpoint for isochronous transfers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables the receive endpoint for bulk/interrupt transfers.</td>
</tr>
<tr>
<td>5</td>
<td>DMAEN</td>
<td>RW</td>
<td>0</td>
<td>DMA Request Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Disables the (\mu)DMA request for the receive endpoint.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables the (\mu)DMA request for the receive endpoint.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> 3 TX and 3 RX endpoints can be connected to the (\mu)DMA module. If this bit is set for a particular endpoint, the DMAARX, DMABRX, or DMACRX field in the USB DMA Select (USBDMASEL) register must be programmed correspondingly.</td>
</tr>
<tr>
<td>4</td>
<td>DISNYET / PIDERR</td>
<td>RW</td>
<td>0</td>
<td>Disable NYET / PID Error</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No effect.</td>
</tr>
</tbody>
</table>
|           |            |      |       | 1 *For bulk or interrupt transactions:* Disables the sending of NYET handshakes. When this bit is set, all successfully received packets are acknowledged, including at the point at which the FIFO becomes full.  
*For isochronous transactions:* Indicates a PID error in the received packet. |
| 3         | DMAMOD     | RW   | 0     | DMA Request Mode |
|           |            |      |       | Value Description |
|           |            |      |       | 0 An interrupt is generated after every \(\mu\)DMA packet transfer. |
|           |            |      |       | 1 An interrupt is generated only after the entire \(\mu\)DMA transfer is complete. |
|           |            |      |       | **Note:** This bit must not be cleared either before or in the same cycle as the above DMAEN bit is cleared. |
| 2:0       | reserved   | RO   | 0x0   | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation. |
Register 121: USB Receive Byte Count Endpoint 1 (USBRXCOUNT1), offset 0x118
Register 122: USB Receive Byte Count Endpoint 2 (USBRXCOUNT2), offset 0x128
Register 123: USB Receive Byte Count Endpoint 3 (USBRXCOUNT3), offset 0x138
Register 124: USB Receive Byte Count Endpoint 4 (USBRXCOUNT4), offset 0x148
Register 125: USB Receive Byte Count Endpoint 5 (USBRXCOUNT5), offset 0x158
Register 126: USB Receive Byte Count Endpoint 6 (USBRXCOUNT6), offset 0x168
Register 127: USB Receive Byte Count Endpoint 7 (USBRXCOUNT7), offset 0x178

Note: The value returned changes as the FIFO is unloaded and is only valid while the RXRDY bit in the USBRXCSRLn register is set.

USBRXCOUNTn is a 16-bit read-only register that holds the number of data bytes in the packet currently in line to be read from the receive FIFO. If the packet is transmitted as multiple bulk packets, the number given is for the combined packet.

USB Receive Byte Count Endpoint n (USBRXCOUNTn)
Base 0x4005.0000
Offset 0x118

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:13</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 12:0      | COUNT  | RO   | 0x000 | Receive Packet Count
Indicates the number of bytes in the receive packet. |
Register 128: USB Host Transmit Configure Type Endpoint 1 (USBTXTYPE1), offset 0x11A
Register 129: USB Host Transmit Configure Type Endpoint 2 (USBTXTYPE2), offset 0x12A
Register 130: USB Host Transmit Configure Type Endpoint 3 (USBTXTYPE3), offset 0x13A
Register 131: USB Host Transmit Configure Type Endpoint 4 (USBTXTYPE4), offset 0x14A
Register 132: USB Host Transmit Configure Type Endpoint 5 (USBTXTYPE5), offset 0x15A
Register 133: USB Host Transmit Configure Type Endpoint 6 (USBTXTYPE6), offset 0x16A
Register 134: USB Host Transmit Configure Type Endpoint 7 (USBTXTYPE7), offset 0x17A

USBTXTYPEEn is an 8-bit register that must be written with the endpoint number to be targeted by the endpoint, the transaction protocol to use for the currently selected transmit endpoint, and its operating speed.

**Description**

Operating Speed
This bit field specifies the operating speed of the target Device:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Default</td>
</tr>
<tr>
<td></td>
<td>The target is assumed to be using the same connection speed as the USB controller.</td>
</tr>
<tr>
<td>0x1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x2</td>
<td>Full</td>
</tr>
<tr>
<td>0x3</td>
<td>Low</td>
</tr>
</tbody>
</table>

**Bit/Field**

7:6 SPEED RW 0x0
**Universal Serial Bus (USB) Controller**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5:4</td>
<td>PROTO</td>
<td>RW</td>
<td>0x0</td>
<td>Protocol</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must configure this bit field to select the required protocol for the transmit endpoint:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value  Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0    Control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1    Isochronous</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2    Bulk</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3    Interrupt</td>
</tr>
<tr>
<td>3:0</td>
<td>TEP</td>
<td>RW</td>
<td>0x0</td>
<td>Target Endpoint Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must configure this value to the endpoint number contained in the transmit endpoint descriptor returned to the USB controller during Device enumeration.</td>
</tr>
</tbody>
</table>
Register 135: USB Host Transmit Interval Endpoint 1 (USBTXINTERVAL1), offset 0x11B
Register 136: USB Host Transmit Interval Endpoint 2 (USBTXINTERVAL2), offset 0x12B
Register 137: USB Host Transmit Interval Endpoint 3 (USBTXINTERVAL3), offset 0x13B
Register 138: USB Host Transmit Interval Endpoint 4 (USBTXINTERVAL4), offset 0x14B
Register 139: USB Host Transmit Interval Endpoint 5 (USBTXINTERVAL5), offset 0x15B
Register 138: USB Host Transmit Interval Endpoint 6 (USBTXINTERVAL6), offset 0x16B
Register 131: USB Host Transmit Interval Endpoint 7 (USBTXINTERVAL7), offset 0x17B

**OTG A / Host**

**USBTXINTERVALn** is an 8-bit register that, for interrupt and isochronous transfers, defines the polling interval for the currently selected transmit endpoint. For bulk endpoints, this register defines the number of frames after which the endpoint should time out on receiving a stream of NAK responses.

The **USBTXINTERVALn** register value defines a number of frames, as follows:

<table>
<thead>
<tr>
<th>Transfer Type</th>
<th>Speed</th>
<th>Valid values (m)</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt</td>
<td>Low-Speed or Full-Speed</td>
<td>0x01 – 0xFF</td>
<td>The polling interval is ( m ) frames.</td>
</tr>
<tr>
<td>Isochronous</td>
<td>Full-Speed</td>
<td>0x01 – 0x10</td>
<td>The polling interval is ( 2^{(m-1)} ) frames/microframes.</td>
</tr>
<tr>
<td>Bulk</td>
<td>Full-Speed</td>
<td>0x02 – 0x10</td>
<td>The NAK Limit is ( 2^{(m-1)} ) frames/microframes. A value of 0 or 1 disables the NAK timeout function.</td>
</tr>
</tbody>
</table>

**USB Host Transmit Interval Endpoint n (USBTXINTERVALn)**

Base 0x4005.0000
Offset 0x11B
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7:0       | TXPOLL / NAKLMT  | RW   | 0x00  | TX Polling / NAK Limit
The polling interval for interrupt/isochronous transfers; the NAK limit for bulk transfers. See table above for valid entries; other values are reserved. |
Register 142: USB Host Configure Receive Type Endpoint 1 (USBRXTYPE1), offset 0x11C
Register 143: USB Host Configure Receive Type Endpoint 2 (USBRXTYPE2), offset 0x12C
Register 144: USB Host Configure Receive Type Endpoint 3 (USBRXTYPE3), offset 0x13C
Register 145: USB Host Configure Receive Type Endpoint 4 (USBRXTYPE4), offset 0x14C
Register 146: USB Host Configure Receive Type Endpoint 5 (USBRXTYPE5), offset 0x15C
Register 147: USB Host Configure Receive Type Endpoint 6 (USBRXTYPE6), offset 0x16C
Register 148: USB Host Configure Receive Type Endpoint 7 (USBRXTYPE7), offset 0x17C

USBRXTYPE\textsubscript{n} is an 8-bit register that must be written with the endpoint number to be targeted by the endpoint, the transaction protocol to use for the currently selected receive endpoint, and its operating speed.

**Base 0x4005.0000**
**Offset 0x11C**
**Type RW, reset 0x00**

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:6</td>
<td>SPEED</td>
<td>RW</td>
<td>0x0</td>
<td>Operating Speed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit field specifies the operating speed of the target Device:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Default</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The target is assumed to be using the same connection speed as the USB controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 Full</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 Low</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>5:4</td>
<td>PROTO</td>
<td>RW</td>
<td>0x0</td>
<td>Protocol</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must configure this bit field to select the required protocol for the receive endpoint:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value    Description</td>
</tr>
<tr>
<td>0x0</td>
<td></td>
<td></td>
<td></td>
<td>Control</td>
</tr>
<tr>
<td>0x1</td>
<td></td>
<td></td>
<td></td>
<td>Isochronous</td>
</tr>
<tr>
<td>0x2</td>
<td></td>
<td></td>
<td></td>
<td>Bulk</td>
</tr>
<tr>
<td>0x3</td>
<td></td>
<td></td>
<td></td>
<td>Interrupt</td>
</tr>
<tr>
<td>3:0</td>
<td>TEP</td>
<td>RW</td>
<td>0x0</td>
<td>Target Endpoint Number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Software must set this value to the endpoint number contained in the receive endpoint descriptor returned to the USB controller during Device enumeration.</td>
</tr>
</tbody>
</table>
Register 149: USB Host Receive Polling Interval Endpoint 1 (USBRXINTERVAL1), offset 0x11D
Register 150: USB Host Receive Polling Interval Endpoint 2 (USBRXINTERVAL2), offset 0x12D
Register 151: USB Host Receive Polling Interval Endpoint 3 (USBRXINTERVAL3), offset 0x13D
Register 152: USB Host Receive Polling Interval Endpoint 4 (USBRXINTERVAL4), offset 0x14D
Register 153: USB Host Receive Polling Interval Endpoint 5 (USBRXINTERVAL5), offset 0x15D
Register 154: USB Host Receive Polling Interval Endpoint 6 (USBRXINTERVAL6), offset 0x16D
Register 155: USB Host Receive Polling Interval Endpoint 7 (USBRXINTERVAL7), offset 0x17D

USBRXINTERVALn is an 8-bit register that, for interrupt and isochronous transfers, defines the polling interval for the currently selected receive endpoint. For bulk endpoints, this register defines the number of frames after which the endpoint should time out on receiving a stream of NAK responses.

The USBXINTERVALn register value defines a number of frames, as follows:

<table>
<thead>
<tr>
<th>Transfer Type</th>
<th>Speed</th>
<th>Valid values (m)</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupt</td>
<td>Low-Speed or Full-Speed</td>
<td>0x01 – 0xFF</td>
<td>The polling interval is m frames.</td>
</tr>
<tr>
<td>Isochronous</td>
<td>Full-Speed</td>
<td>0x01 – 0x10</td>
<td>The polling interval is $2^{(m-1)}$ frames/microframes.</td>
</tr>
<tr>
<td>Bulk</td>
<td>Full-Speed</td>
<td>0x02 – 0x10</td>
<td>The NAK Limit is $2^{(m-1)}$ frames/microframes. A value of 0 or 1 disables the NAK timeout function.</td>
</tr>
</tbody>
</table>

USB Host Receive Polling Interval Endpoint n (USBRXINTERVALn)
Base 0x4005.0000
Offset 0x11D
Type RW, reset 0x00

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 7:0       | TXPOLL / NAKLMT  | RW   | 0x00  | RX Polling / NAK Limit
The polling interval for interrupt/isochronous transfers; the NAK limit for bulk transfers. See table above for valid entries; other values are reserved.
Register 156: USB Request Packet Count in Block Transfer Endpoint 1 (USBRQPKTCOUNT1), offset 0x304
Register 157: USB Request Packet Count in Block Transfer Endpoint 2 (USBRQPKTCOUNT2), offset 0x308
Register 158: USB Request Packet Count in Block Transfer Endpoint 3 (USBRQPKTCOUNT3), offset 0x30C
Register 159: USB Request Packet Count in Block Transfer Endpoint 4 (USBRQPKTCOUNT4), offset 0x310
Register 160: USB Request Packet Count in Block Transfer Endpoint 5 (USBRQPKTCOUNT5), offset 0x314
Register 161: USB Request Packet Count in Block Transfer Endpoint 6 (USBRQPKTCOUNT6), offset 0x318
Register 162: USB Request Packet Count in Block Transfer Endpoint 7 (USBRQPKTCOUNT7), offset 0x31C

This 16-bit read/write register is used in Host mode to specify the number of packets that are to be transferred in a block transfer of one or more bulk packets to receive endpoint n. The USB controller uses the value recorded in this register to determine the number of requests to issue where the AUTORQ bit in the USBRXCSRHN register has been set. See "IN Transactions as a Host" on page 1129.

Note: Multiple packets combined into a single bulk packet within the FIFO count as one packet.

USB Request Packet Count in Block Transfer Endpoint n (USBRQPKTCOUNTn)
Base 0x4005.0000
Offset 0x304
Type RW, reset 0x0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 15:0      | COUNT      | RW   | 0x0000| Block Transfer Packet Count
Sets the number of packets of the size defined by the MAXLOAD bit field that are to be transferred in a block transfer. |

Note: This is only used in Host mode when AUTORQ is set. The bit has no effect in Device mode or when AUTORQ is not set.
Register 163: USB Receive Double Packet Buffer Disable (USBRXDPKTBUFDIS), offset 0x340

USBRXDPKTBUFDIS is a 16-bit register that indicates which of the receive endpoints have disabled the double-packet buffer functionality (see the section called “Double-Packet Buffering” on page 1125).

OTG A / Host

OTG B / Device

USB Receive Double Packet Buffer Disable (USBRXDPKTBUFDIS)

Base 0x4005.0000
Offset 0x340
Type RW, reset 0x0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>EP7</td>
<td>RW</td>
<td>0</td>
<td>EP7 RX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Disables double-packet buffering.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables double-packet buffering.</td>
</tr>
<tr>
<td>6</td>
<td>EP6</td>
<td>RW</td>
<td>0</td>
<td>EP6 RX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>5</td>
<td>EP5</td>
<td>RW</td>
<td>0</td>
<td>EP5 RX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>4</td>
<td>EP4</td>
<td>RW</td>
<td>0</td>
<td>EP4 RX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>3</td>
<td>EP3</td>
<td>RW</td>
<td>0</td>
<td>EP3 RX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>2</td>
<td>EP2</td>
<td>RW</td>
<td>0</td>
<td>EP2 RX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>1</td>
<td>EP1</td>
<td>RW</td>
<td>0</td>
<td>EP1 RX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 164: USB Transmit Double Packet Buffer Disable (USBTXDPKTBUDIS), offset 0x342

**USBTXDPKTBUDIS** is a 16-bit register that indicates which of the transmit endpoints have disabled the double-packet buffer functionality (see the section called “Double-Packet Buffering” on page 1124).

**USB Transmit Double Packet Buffer Disable (USBTXDPKTBUDIS)**
Base 0x4005.0000
Offset 0x342
Type RW, reset 0x0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:8</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>EP7</td>
<td>RW</td>
<td>0</td>
<td>EP7 TX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Enables double-packet buffering.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Enables double-packet buffering.</td>
</tr>
<tr>
<td>6</td>
<td>EP6</td>
<td>RW</td>
<td>0</td>
<td>EP6 TX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>5</td>
<td>EP5</td>
<td>RW</td>
<td>0</td>
<td>EP5 TX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>4</td>
<td>EP4</td>
<td>RW</td>
<td>0</td>
<td>EP4 TX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>3</td>
<td>EP3</td>
<td>RW</td>
<td>0</td>
<td>EP3 TX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>2</td>
<td>EP2</td>
<td>RW</td>
<td>0</td>
<td>EP2 TX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>1</td>
<td>EP1</td>
<td>RW</td>
<td>0</td>
<td>EP1 TX Double-Packet Buffer Disable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Same description as EP7.</td>
</tr>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Register 165: USB External Power Control (USBEPC), offset 0x400

This 32-bit register specifies the function of the two-pin external power interface (USBOEPEN and USBOPFLT). The assertion of the power fault input may generate an automatic action, as controlled by the hardware configuration registers. The automatic action is necessary because the fault condition may require a response faster than one provided by firmware.

### USB External Power Control (USBEPC)

- **Base**: 0x4005.0000
- **Offset**: 0x400
- **Type**: RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0x000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9:8</td>
<td>PFLTACT</td>
<td>RW</td>
<td>0x0</td>
<td>Power Fault Action</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit field specifies how the USBOEPEN signal is changed when detecting a USB power fault.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Unchanged</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>USBOEPEN is controlled by the combination of the EPEN and EPENDE bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 Tristate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>USBOEPEN is undriven (tristate).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 Low</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>USBOEPEN is driven Low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 High</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>USBOEPEN is driven High.</td>
</tr>
<tr>
<td>7</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
### Bit/Field: PFLTAEN

**Type:** RW  **Reset:** 0

**Description:** Power Fault Action Enable

This bit specifies whether a USB power fault triggers any automatic corrective action regarding the driven state of the USB0EPEN signal.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Disabled</td>
</tr>
<tr>
<td></td>
<td>The USB0EPEN output is controlled by the combination of the EPEN and EPENDE bits.</td>
</tr>
<tr>
<td>1</td>
<td>Enabled</td>
</tr>
<tr>
<td></td>
<td>The USB0EPEN output is automatically changed to the state specified by the PFLTACT field.</td>
</tr>
</tbody>
</table>

### Bit/Field: PFLTSEN

**Type:** RW  **Reset:** 0

**Description:** Power Fault Sense

This bit specifies the logical sense of the USB0PFLT input signal that indicates an error condition.

The complementary state is the inactive state.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Low Fault</td>
</tr>
<tr>
<td></td>
<td>If USB0PFLT is driven Low, the power fault is signaled internally (if enabled by the PFLTEN bit).</td>
</tr>
<tr>
<td>1</td>
<td>High Fault</td>
</tr>
<tr>
<td></td>
<td>If USB0PFLT is driven High, the power fault is signaled internally (if enabled by the PFLTEN bit).</td>
</tr>
</tbody>
</table>

### Bit/Field: PFLTEN

**Type:** RW  **Reset:** 0

**Description:** Power Fault Input Enable

This bit specifies whether the USB0PFLT input signal is used in internal logic.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Not Used</td>
</tr>
<tr>
<td></td>
<td>The USB0PFLT signal is ignored.</td>
</tr>
<tr>
<td>1</td>
<td>Used</td>
</tr>
<tr>
<td></td>
<td>The USB0PFLT signal is used internally.</td>
</tr>
</tbody>
</table>

### Bit/Field: reserved

**Type:** RO  **Reset:** 0

**Description:** Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
### Description

**EPEN Drive Enable**

This bit specifies whether the **USB0EPEN** signal is driven or undriven (tristate). When driven, the signal value is specified by the **EPEN** field. When not driven, the **EPEN** field is ignored and the **USB0EPEN** signal is placed in a high-impedance state.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Not Driven</td>
</tr>
<tr>
<td>1</td>
<td>Driven</td>
</tr>
</tbody>
</table>

The **USB0EPEN** signal is undriven at reset because the sense of the external power supply enable is unknown. By adding the high-impedance state, system designers may bias the power supply enable to the disabled state using a large resistor (100 kΩ) and later configure and drive the output signal to enable the power supply.

### Description

**External Power Supply Enable Configuration**

This bit field specifies and controls the logical value driven on the **USB0EPEN** signal.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Power Enable Active Low</td>
</tr>
<tr>
<td></td>
<td>The <strong>USB0EPEN</strong> signal is driven Low if the <strong>EPENDE</strong> bit is set.</td>
</tr>
<tr>
<td>0x1</td>
<td>Power Enable Active High</td>
</tr>
<tr>
<td></td>
<td>The <strong>USB0EPEN</strong> signal is driven High if the <strong>EPENDE</strong> bit is set.</td>
</tr>
<tr>
<td>0x2</td>
<td>Power Enable High if VBUS Low</td>
</tr>
<tr>
<td></td>
<td>The <strong>USB0EPEN</strong> signal is driven High when the A device is not recognized.</td>
</tr>
<tr>
<td>0x3</td>
<td>Power Enable High if VBUS High</td>
</tr>
<tr>
<td></td>
<td>The <strong>USB0EPEN</strong> signal is driven High when the A device is recognized.</td>
</tr>
</tbody>
</table>
Register 166: USB External Power Control Raw Interrupt Status (USBEPCRIS), offset 0x404

This 32-bit register specifies the unmasked interrupt status of the two-pin external power interface.

USB External Power Control Raw Interrupt Status (USBEPCRIS)
Base 0x4005.0000
Offset 0x404
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>PF</td>
<td>RO</td>
<td>0</td>
<td>USB Power Fault Interrupt Status</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td>1</td>
<td>A Power Fault status has been detected.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the PF bit in the USBEPISC register.
Register 167: USB External Power Control Interrupt Mask (USBEPCIM), offset 0x408

This 32-bit register specifies the interrupt mask of the two-pin external power interface.

USB External Power Control Interrupt Mask (USBEPCIM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>PF</td>
<td>RW</td>
<td>0</td>
<td>USB Power Fault Interrupt Mask</td>
</tr>
</tbody>
</table>

Value Description

0 A detected power fault does not affect the interrupt status.

1 The raw interrupt signal from a detected power fault is sent to the interrupt controller.
Register 168: USB External Power Control Interrupt Status and Clear (USBEPCISC), offset 0x40C

This 32-bit register specifies the masked interrupt status of the two-pin external power interface. It also provides a method to clear the interrupt state.

USB External Power Control Interrupt Status and Clear (USBEPCISC)
Base 0x4005.0000
Offset 0x40C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>PF</td>
<td>RW1C</td>
<td>0</td>
<td>USB Power Fault Interrupt Status and Clear</td>
</tr>
</tbody>
</table>

Value Description

- 0  No interrupt has occurred or the interrupt is masked.
- 1  The PF bits in the USBEPCRIS and USBEPCIM registers are set, providing an interrupt to the interrupt controller.

This bit is cleared by writing a 1. Clearing this bit also clears the PF bit in the USBEPCRIS register.
Register 169: USB Device RESUME Raw Interrupt Status (USBDRRIS), offset 0x410

The USBDRRIS 32-bit register is the raw interrupt status register. On a read, this register gives the current raw status value of the corresponding interrupt prior to masking. A write has no effect.

USB Device RESUME Raw Interrupt Status (USBDRRIS)
Base 0x4005.0000
Offset 0x410
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>RESUME</td>
<td>RO</td>
<td>0</td>
<td>RESUME Interrupt Status</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td>1</td>
<td>A RESUME status has been detected.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the RESUME bit in the USBDRISC register.
Register 170: USB Device RESUME Interrupt Mask (USBDRIM), offset 0x414

The **USBDRIM** 32-bit register is the masked interrupt status register. On a read, this register gives the current value of the mask on the corresponding interrupt. Setting a bit sets the mask, preventing the interrupt from being signaled to the interrupt controller. Clearing a bit clears the corresponding mask, enabling the interrupt to be sent to the interrupt controller.

### USB Device RESUME Interrupt Mask (USBDRIM)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4005.0000</td>
<td>0x414</td>
<td>RW</td>
<td>0x0000</td>
<td>RESUME Interrupt Mask</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>RESUME</td>
<td>RW</td>
<td>0</td>
<td>RESUME Interrupt Mask</td>
</tr>
</tbody>
</table>

**Value Description**

0 A detected RESUME does not affect the interrupt status.

1 The raw interrupt signal from a detected RESUME is sent to the interrupt controller. This bit should only be set when a SUSPEND has been detected (the SUSPEND bit in the USBIS register is set).
Register 171: USB Device RESUME Interrupt Status and Clear (USBDRISC), offset 0x418

The USBDRISC 32-bit register is the interrupt clear register. On a write of 1, the corresponding interrupt is cleared. A write of 0 has no effect.

USB Device RESUME Interrupt Status and Clear (USBDRISC)
Base 0x4005.0000
Offset 0x418
Type W1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>RESUME</td>
<td>RW1C</td>
<td>0</td>
<td>RESUME Interrupt Status and Clear</td>
</tr>
</tbody>
</table>

Value Description

0  No interrupt has occurred or the interrupt is masked.
1  The RESUME bits in the USBDRRIS and USBDRCIM registers are set, providing an interrupt to the interrupt controller.

This bit is cleared by writing a 1. Clearing this bit also clears the RESUME bit in the USBDRCRIS register.
Register 172: USB General-Purpose Control and Status (USBGPCS), offset 0x41C

**USBGPCS** provides the state of the internal ID signal.

**Note:** When used in OTG mode, `USB0VBUS` and `USB0ID` do not require any configuration as they are dedicated pins for the USB controller and directly connect to the USB connector's VBUS and ID signals. If the USB controller is used as either a dedicated Host or Device, the `DEVMODOTG` and `DEVMOD` bits in the **USB General-Purpose Control and Status (USBGPCS)** register can be used to connect the `USB0VBUS` and `USB0ID` inputs to fixed levels internally, freeing the PB0 and PB1 pins for GPIO use. For proper self-powered Device operation, the VBUS value must still be monitored to assure that if the Host removes VBUS, the self-powered Device disables the D+/D- pull-up resistors. This function can be accomplished by connecting a standard GPIO to VBUS.

The termination resistors for the USB PHY have been added internally, and thus there is no need for external resistors. For a device, there is a 1.5 KOhm pull-up on the D+ and for a host there are 15 KOhm pull-downs on both D+ and D-.
Register 173: USB VBUS Droop Control (USBVDC), offset 0x430

This 32-bit register enables a controlled masking of VBUS to compensate for any in-rush current by a Device that is connected to the Host controller. The in-rush current can cause VBUS to droop, causing the USB controller's behavior to be unexpected. The USB Host controller allows VBUS to fall lower than the VBUS Valid level (4.75 V) but not below AValid (2.0 V) for 65 microseconds without signaling a VBUSERR interrupt in the controller. Without this, any glitch on VBUS would force the USB Host controller to remove power from VBUS and then re-enumerate the Device.

USB VBUS Droop Control (USBVDC)
Base 0x4005.0000
Offset 0x430
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>31:1</th>
<th>reserved</th>
<th>RO</th>
<th>0x0000.0000</th>
<th>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>VBDEN</td>
<td>RW</td>
<td>0</td>
<td>VBUS Droop Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Any changes from VBUSVALID are masked when VBUS goes below 4.75 V but not lower than 2.0 V for 65 microseconds. During this time, the VBUS state indicates VBUSVALID.</td>
</tr>
</tbody>
</table>
Register 174: USB VBUS Droop Control Raw Interrupt Status (USBVDCRIS), offset 0x434

This 32-bit register specifies the unmasked interrupt status of the VBUS droop limit of 65 microseconds.

USB VBUS Droop Control Raw Interrupt Status (USBVDCRIS)

Offset 0x434
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>VD</td>
<td>RO</td>
<td>0</td>
<td>VBUS Droop Raw Interrupt Status</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td>1</td>
<td>A VBUS droop lasting for 65 microseconds has been detected.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the VD bit in the USBVDCISC register.
### Register 175: USB VBUS Droop Control Interrupt Mask (USBVDCIM), offset 0x438

This 32-bit register specifies the interrupt mask of the VBUS droop.

**USB VBUS Droop Control Interrupt Mask (USBVDCIM)**

Base 0x4005.0000
Offset 0x438
Type RW, reset 0x0000.0000

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| Type | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO |
| Reset | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>VD</td>
<td>RW</td>
<td>0</td>
<td>VBUS Droop Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 176: USB VBUS Droop Control Interrupt Status and Clear (USBVDCISC), offset 0x43C

This 32-bit register specifies the masked interrupt status of the VBUS droop and provides a method to clear the interrupt state.

USB VBUS Droop Control Interrupt Status and Clear (USBVDCISC)
Base 0x4005.0000
Offset 0x43C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>VD</td>
<td>RW1C</td>
<td>0</td>
<td>VBUS Droop Interrupt Status and Clear</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt has occurred or the interrupt is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The VD bits in the USBVDCRIS and USBVDCIM registers are set, providing an interrupt to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1. Clearing this bit also clears the VD bit in the USBVDCRIS register.</td>
</tr>
</tbody>
</table>
This 32-bit register specifies whether the unmasked interrupt status of the ID value is valid.

USB ID Valid Detect Raw Interrupt Status (USBIDVRIS)

Base 0x4005.0000
Offset 0x444
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>ID</td>
<td>RO</td>
<td>0</td>
<td>ID Valid Detect Raw Interrupt Status</td>
</tr>
</tbody>
</table>

Value Description

0   An interrupt has not occurred.
1   A valid ID has been detected.

This bit is cleared by writing a 1 to the ID bit in the USBIDVISC register.
Register 178: USB ID Valid Detect Interrupt Mask (USBIDVIM), offset 0x448

This 32-bit register specifies the interrupt mask of the ID valid detection.

USB ID Valid Detect Interrupt Mask (USBIDVIM)

Base 0x4005.0000
Offset 0x448
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>ID</td>
<td>RW</td>
<td>0</td>
<td>ID Valid Detect Interrupt Mask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 A detected ID valid does not affect the interrupt status.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The raw interrupt signal from a detected ID valid is sent to the interrupt controller.</td>
</tr>
</tbody>
</table>
Register 179: USB ID Valid Detect Interrupt Status and Clear (USBIDVISC), offset 0x44C

This 32-bit register specifies the masked interrupt status of the ID valid detect. It also provides a method to clear the interrupt state.

USB ID Valid Detect Interrupt Status and Clear (USBIDVISC)
Base 0x4005.0000
Offset 0x44C
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>ID</td>
<td>RW1C</td>
<td>0</td>
<td>ID Valid Detect Interrupt Status and Clear</td>
</tr>
</tbody>
</table>

Value Description

0  No interrupt has occurred or the interrupt is masked.
1  The ID bits in the USBIDVRIS and USBIDVIM registers are set, providing an interrupt to the interrupt controller.

This bit is cleared by writing a 1. Clearing this bit also clears the ID bit in the USBIDVRIS register.
Register 180: USB DMA Select (USBDMASEL), offset 0x450

This 32-bit register specifies which endpoints are mapped to the 6 allocated µDMA channels, see Table 9-1 on page 597 for more information on channel assignments.

USB DMA Select (USBDMASEL)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4005.0000</td>
<td>0x450</td>
<td>RW</td>
<td>0x0033.2211</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td>0x00</td>
<td>RO</td>
<td>31:24</td>
</tr>
<tr>
<td>DMA C TX Select</td>
<td>0x3</td>
<td>RW</td>
<td>23:20</td>
</tr>
</tbody>
</table>

### Table: Bit/Field Information

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>23:20</td>
<td>DMACTX</td>
<td>RW</td>
<td>0x3</td>
<td>DMA C TX Select</td>
</tr>
</tbody>
</table>

Specifications the TX mapping of the third USB endpoint on µDMA channel 5 (primary assignment).

### Table: DMA C TX Select Values

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>reserved</td>
</tr>
<tr>
<td>0x1</td>
<td>Endpoint 1 TX</td>
</tr>
<tr>
<td>0x2</td>
<td>Endpoint 2 TX</td>
</tr>
<tr>
<td>0x3</td>
<td>Endpoint 3 TX</td>
</tr>
<tr>
<td>0x4</td>
<td>Endpoint 4 TX</td>
</tr>
<tr>
<td>0x5</td>
<td>Endpoint 5 TX</td>
</tr>
<tr>
<td>0x6</td>
<td>Endpoint 6 TX</td>
</tr>
<tr>
<td>0x7</td>
<td>Endpoint 7 TX</td>
</tr>
<tr>
<td>0x8 - 0xFF</td>
<td>reserved</td>
</tr>
</tbody>
</table>
### Universal Serial Bus (USB) Controller

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 19:16     | DMACRX   | RW   | 0x3   | DMA C RX Select  
           |          |      |       | Specifies the RX and TX mapping of the third USB endpoint on µDMA channel 4 (primary assignment). |
|           |          |      |       | Value Description |
|           |          |      |       | 0x0  reserved |
|           |          |      |       | 0x1  Endpoint 1 RX |
|           |          |      |       | 0x2  Endpoint 2 RX |
|           |          |      |       | 0x3  Endpoint 3 RX |
|           |          |      |       | 0x4  Endpoint 4 RX |
|           |          |      |       | 0x5  Endpoint 5 RX |
|           |          |      |       | 0x6  Endpoint 6 RX |
|           |          |      |       | 0x7  Endpoint 7 RX |
|           |          |      |       | 0x8 - 0xF reserved |
| 15:12     | DMABTX   | RW   | 0x2   | DMA B TX Select  
           |          |      |       | Specifies the TX mapping of the second USB endpoint on µDMA channel 3 (primary assignment). |
|           |          |      |       | Same bit definitions as the DMACTX field. |
| 11:8      | DMABRX   | RW   | 0x2   | DMA B RX Select  
           |          |      |       | Specifies the RX mapping of the second USB endpoint on µDMA channel 2 (primary assignment). |
|           |          |      |       | Same bit definitions as the DMACRX field. |
| 7:4       | DMAATX   | RW   | 0x1   | DMA A TX Select  
           |          |      |       | Specifies the TX mapping of the first USB endpoint on µDMA channel 1 (primary assignment). |
|           |          |      |       | Same bit definitions as the DMACTX field. |
| 3:0       | DMAARX   | RW   | 0x1   | DMA A RX Select  
           |          |      |       | Specifies the RX mapping of the first USB endpoint on µDMA channel 0 (primary assignment). |
|           |          |      |       | Same bit definitions as the DMACRX field. |
Register 181: USB Peripheral Properties (USBPP), offset 0xFC0

The **USBPP** register provides information regarding the properties of the USB module.

### USB Peripheral Properties (USBPP)
- **Base**: 0x4005.0000
- **Offset**: 0xFC0
- **Type**: RO, reset 0x0000.10D0

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:8</td>
<td>ECNT</td>
<td>RO</td>
<td>0x10</td>
<td>Endpoint Count</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field indicates the hex value for the number of endpoints provided.</td>
</tr>
<tr>
<td>7:6</td>
<td>USB</td>
<td>RO</td>
<td>0x3</td>
<td>USB Capability</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>0x0</td>
<td>NA</td>
<td></td>
<td></td>
<td>USB is not present.</td>
</tr>
<tr>
<td>0x1</td>
<td>DEVICE</td>
<td></td>
<td></td>
<td>Device Only</td>
</tr>
<tr>
<td>0x2</td>
<td>HOST</td>
<td></td>
<td></td>
<td>Device or Host</td>
</tr>
<tr>
<td>0x3</td>
<td>OTG</td>
<td></td>
<td></td>
<td>Device, Host, or OTG</td>
</tr>
<tr>
<td>5</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>4</td>
<td>PHY</td>
<td>RO</td>
<td>0x1</td>
<td>PHY Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>0</td>
<td>A PHY is not integrated with the USB MAC.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A PHY is integrated with the USB MAC.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3:0</td>
<td>TYPE</td>
<td>RO</td>
<td>0x0</td>
<td>Controller Type</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td>0x0</td>
<td>The first-generation USB controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1-0xF</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**June 12, 2014**

Texas Instruments-Production Data
Analog Comparators

An analog comparator is a peripheral that compares two analog voltages and provides a logical output that signals the comparison result.

**Note:** Not all comparators have the option to drive an output pin. See “Signal Description” on page 1237 for more information.

The comparator can provide its output to a device pin, acting as a replacement for an analog comparator on the board. In addition, the comparator can signal the application via interrupts or trigger the start of a sample sequence in the ADC. The interrupt generation and ADC triggering logic is separate and independent. This flexibility means, for example, that an interrupt can be generated on a rising edge and the ADC triggered on a falling edge.

The TM4C123GH6PZ microcontroller provides three independent integrated analog comparators with the following functions:

- Compare external pin input to external pin input or to internal programmable voltage reference
- Compare a test voltage against any one of the following voltages:
  - An individual external reference voltage
  - A shared single external reference voltage
  - A shared internal reference voltage
19.1 Block Diagram

Figure 19-1. Analog Comparator Module Block Diagram

Note: This block diagram depicts the maximum number of analog comparators and comparator outputs for the family of microcontrollers; the number for this specific device may vary. See page 1250 for what is included on this device.

19.2 Signal Description

The following table lists the external signals of the Analog Comparators and describes the function of each. The Analog Comparator output signals are alternate functions for some GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for the Analog Comparator signals. The \textit{AFSEL} bit in the GPIO \textit{Alternate Function Select} (GPIOAFSEL) register (page 684) should be set to choose the Analog Comparator function. The number in parentheses is the encoding that must be programmed into the \textit{PMCn} field in the GPIOPortControl (GPIOPCTL) register (page 702) to assign the Analog Comparator signal to the specified GPIO port pin. The positive and negative input signals are configured by clearing the \textit{DEN} bit in the GPIOPortControl (GPIODEN) register. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659.

Table 19-1. Analog Comparators Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type(^a)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0+</td>
<td>23</td>
<td>PC6</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 0 positive input.</td>
</tr>
</tbody>
</table>
Table 19-1. Analog Comparators Signals (100LQFP) (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type(^a)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0-</td>
<td>22</td>
<td>PC7</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 0 negative input.</td>
</tr>
<tr>
<td>C0o</td>
<td>40</td>
<td>PF0 (9)</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 0 output.</td>
</tr>
<tr>
<td>C1+</td>
<td>24</td>
<td>PC5</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 1 positive input.</td>
</tr>
<tr>
<td>C1-</td>
<td>25</td>
<td>PC4</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 1 negative input.</td>
</tr>
<tr>
<td>C1o</td>
<td>41</td>
<td>PF1 (9)</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 1 output.</td>
</tr>
<tr>
<td>C2+</td>
<td>87</td>
<td>PG6</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 2 positive input.</td>
</tr>
<tr>
<td>C2-</td>
<td>88</td>
<td>PG7</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 2 negative input.</td>
</tr>
<tr>
<td>C2o</td>
<td>42</td>
<td>PF2 (9)</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 2 output.</td>
</tr>
</tbody>
</table>

\(^a\) The TTL designation indicates the pin has TTL-compatible voltage levels.

19.3 Functional Description

The comparator compares the VIN- and VIN+ inputs to produce an output, VOUT.

\[
\text{VIN-} < \text{VIN+}, \quad \text{VOUT} = 1 \\
\text{VIN-} > \text{VIN+}, \quad \text{VOUT} = 0
\]

As shown in Figure 19-2 on page 1238, the input source for VIN- is an external input, C\(_n\)-, where \(n\) is the analog comparator number. In addition to an external input, C\(_n\)+, input sources for VIN+ can be the C0+ or an internal reference, V\(_{\text{IREF}}\).

Figure 19-2. Structure of Comparator Unit

A comparator is configured through two status/control registers, Analog Comparator Control (ACCTL) and Analog Comparator Status (ACSTAT). The internal reference is configured through one control register, Analog Comparator Reference Voltage Control (ACREFCTL). Interrupt status and control are configured through three registers, Analog Comparator Masked Interrupt Status (ACMIS), Analog Comparator Raw Interrupt Status (ACRIS), and Analog Comparator Interrupt Enable (ACINTEN).

Typically, the comparator output is used internally to generate an interrupt as controlled by the ISEN bit in the ACCTL register. The output may also be used to drive one of the external pins (C\(_n\)O), or generate an analog-to-digital converter (ADC) trigger.
19.3.1 Internal Reference Programming

The structure of the internal reference is shown in Figure 19-3 on page 1239. The internal reference is controlled by a single configuration register (ACREFCTL).

Figure 19-3. Comparator Internal Reference Structure

Note: In the figure above, N*R represents a multiple of the R value that produces the results specified in Table 19-2 on page 1239.

The internal reference can be programmed in one of two modes (low range or high range) depending on the RNG bit in the ACREFCTL register. When RNG is clear, the internal reference is in high-range mode, and when RNG is set the internal reference is in low-range mode.

In each range, the internal reference, V_{IREF}, has 16 preprogrammed thresholds or step values. The threshold to be used to compare the external input voltage against is selected using the VREF field in the ACREFCTL register.

In the high-range mode, the V_{IREF} threshold voltages start at the ideal high-range starting voltage of V_{DDA}/4.2 and increase in ideal constant voltage steps of V_{DDA}/29.4.

In the low-range mode, the V_{IREF} threshold voltages start at 0 V and increase in ideal constant voltage steps of V_{DDA}/22.12. The ideal V_{IREF} step voltages for each mode and their dependence on the RNG and VREF fields are summarized in Table 19-2.

Table 19-2. Internal Reference Voltage and ACREFCTL Field Values

<table>
<thead>
<tr>
<th>ACREFCTL Register</th>
<th>Output Reference Voltage Based on VREF Field Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN Bit Value</td>
<td>RNG Bit Value</td>
</tr>
<tr>
<td>EN=0</td>
<td>RNG=X</td>
</tr>
</tbody>
</table>
Table 19-2. Internal Reference Voltage and ACREFCTL Field Values (continued)

<table>
<thead>
<tr>
<th>ACREFCTL Register</th>
<th>Output Reference Voltage Based on VREF Field Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>EN Bit Value</strong></td>
<td><strong>RNG Bit Value</strong></td>
</tr>
<tr>
<td>EN=1</td>
<td>RNG=0</td>
</tr>
<tr>
<td></td>
<td>( V_{\text{REF}} ) High Range: 16 voltage threshold values indexed by ( V_{\text{REF}} = 0x0 .. 0xF )</td>
</tr>
<tr>
<td></td>
<td>Ideal starting voltage ( (V_{\text{REF}}=0) ): ( V_{\text{DDA}} / 4.2 )</td>
</tr>
<tr>
<td></td>
<td>Ideal step size: ( V_{\text{DDA}} / 29.4 )</td>
</tr>
<tr>
<td></td>
<td>Ideal ( V_{\text{REF}} ) threshold values: ( V_{\text{REF}} (V_{\text{REF}}) = V_{\text{DDA}} / 4.2 + V_{\text{REF}} \times (V_{\text{DDA}} / 29.4) ), for ( V_{\text{REF}} = 0x0 .. 0xF )</td>
</tr>
<tr>
<td></td>
<td>For minimum and maximum ( V_{\text{REF}} ) threshold values, see Table 19-3 on page 1240.</td>
</tr>
<tr>
<td>RNG=1</td>
<td>( V_{\text{REF}} ) Low Range: 16 voltage threshold values indexed by ( V_{\text{REF}} = 0x0 .. 0xF )</td>
</tr>
<tr>
<td></td>
<td>Ideal starting voltage ( (V_{\text{REF}}=0) ): 0 V</td>
</tr>
<tr>
<td></td>
<td>Ideal step size: ( V_{\text{DDA}} / 22.12 )</td>
</tr>
<tr>
<td></td>
<td>Ideal ( V_{\text{REF}} ) threshold values: ( V_{\text{REF}} (V_{\text{REF}}) = V_{\text{REF}} \times (V_{\text{DDA}} / 22.12) ), for ( V_{\text{REF}} = 0x0 .. 0xF )</td>
</tr>
<tr>
<td></td>
<td>For minimum and maximum ( V_{\text{REF}} ) threshold values, see Table 19-4 on page 1241.</td>
</tr>
</tbody>
</table>

Note that the values shown in Table 19-2 are the ideal values of the \( V_{\text{REF}} \) thresholds. These values actually vary between minimum and maximum values for each threshold step, depending on process and temperature. The minimum and maximum values for each step are given by:

- \( V_{\text{REF}} (V_{\text{REF}}) [\text{Min}] = \text{Ideal } V_{\text{REF}} (V_{\text{REF}}) - (\text{Ideal Step size} - 2 \text{ mV}) / 2 \)
- \( V_{\text{REF}} (V_{\text{REF}}) [\text{Max}] = \text{Ideal } V_{\text{REF}} (V_{\text{REF}}) + (\text{Ideal Step size} - 2 \text{ mV}) / 2 \)

Examples of minimum and maximum \( V_{\text{REF}} \) values for \( V_{\text{DDA}} = 3.3V \) for high and low ranges, are shown in Table 19-3 and Table 19-4. Note that these examples are only valid for \( V_{\text{DDA}} = 3.3V \); values scale up and down with \( V_{\text{DDA}} \).

Table 19-3. Analog Comparator Voltage Reference Characteristics, \( V_{\text{DDA}} = 3.3V, \text{EN}=1 \), and \( \text{RNG} = 0 \)

<table>
<thead>
<tr>
<th>VREF Value</th>
<th>( V_{\text{REF}} ) Min</th>
<th>Ideal ( V_{\text{REF}} )</th>
<th>( V_{\text{REF}} ) Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0.731</td>
<td>0.786</td>
<td>0.841</td>
<td>V</td>
</tr>
<tr>
<td>0x1</td>
<td>0.843</td>
<td>0.898</td>
<td>0.953</td>
<td>V</td>
</tr>
<tr>
<td>0x2</td>
<td>0.955</td>
<td>1.010</td>
<td>1.065</td>
<td>V</td>
</tr>
<tr>
<td>0x3</td>
<td>1.067</td>
<td>1.122</td>
<td>1.178</td>
<td>V</td>
</tr>
<tr>
<td>0x4</td>
<td>1.180</td>
<td>1.235</td>
<td>1.290</td>
<td>V</td>
</tr>
<tr>
<td>0x5</td>
<td>1.292</td>
<td>1.347</td>
<td>1.402</td>
<td>V</td>
</tr>
<tr>
<td>0x6</td>
<td>1.404</td>
<td>1.459</td>
<td>1.514</td>
<td>V</td>
</tr>
<tr>
<td>0x7</td>
<td>1.516</td>
<td>1.571</td>
<td>1.627</td>
<td>V</td>
</tr>
<tr>
<td>0x8</td>
<td>1.629</td>
<td>1.684</td>
<td>1.739</td>
<td>V</td>
</tr>
<tr>
<td>0x9</td>
<td>1.741</td>
<td>1.796</td>
<td>1.851</td>
<td>V</td>
</tr>
<tr>
<td>0xA</td>
<td>1.853</td>
<td>1.908</td>
<td>1.963</td>
<td>V</td>
</tr>
<tr>
<td>0xB</td>
<td>1.965</td>
<td>2.020</td>
<td>2.076</td>
<td>V</td>
</tr>
<tr>
<td>0xC</td>
<td>2.078</td>
<td>2.133</td>
<td>2.188</td>
<td>V</td>
</tr>
<tr>
<td>0xD</td>
<td>2.190</td>
<td>2.245</td>
<td>2.300</td>
<td>V</td>
</tr>
<tr>
<td>0xE</td>
<td>2.302</td>
<td>2.357</td>
<td>2.412</td>
<td>V</td>
</tr>
<tr>
<td>0xF</td>
<td>2.414</td>
<td>2.469</td>
<td>2.525</td>
<td>V</td>
</tr>
</tbody>
</table>
Table 19-4. Analog Comparator Voltage Reference Characteristics, $V_{DDA} = 3.3V$, EN= 1, and RNG = 1

<table>
<thead>
<tr>
<th>VREF Value</th>
<th>$V_{IREF}$ Min</th>
<th>Ideal $V_{IREF}$</th>
<th>$V_{IREF}$ Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0.000</td>
<td>0.000</td>
<td>0.074</td>
<td>V</td>
</tr>
<tr>
<td>0x1</td>
<td>0.076</td>
<td>0.149</td>
<td>0.223</td>
<td>V</td>
</tr>
<tr>
<td>0x2</td>
<td>0.225</td>
<td>0.298</td>
<td>0.372</td>
<td>V</td>
</tr>
<tr>
<td>0x3</td>
<td>0.374</td>
<td>0.448</td>
<td>0.521</td>
<td>V</td>
</tr>
<tr>
<td>0x4</td>
<td>0.523</td>
<td>0.597</td>
<td>0.670</td>
<td>V</td>
</tr>
<tr>
<td>0x5</td>
<td>0.672</td>
<td>0.746</td>
<td>0.820</td>
<td>V</td>
</tr>
<tr>
<td>0x6</td>
<td>0.822</td>
<td>0.895</td>
<td>0.969</td>
<td>V</td>
</tr>
<tr>
<td>0x7</td>
<td>0.971</td>
<td>1.044</td>
<td>1.118</td>
<td>V</td>
</tr>
<tr>
<td>0x8</td>
<td>1.120</td>
<td>1.193</td>
<td>1.267</td>
<td>V</td>
</tr>
<tr>
<td>0x9</td>
<td>1.269</td>
<td>1.343</td>
<td>1.416</td>
<td>V</td>
</tr>
<tr>
<td>0xA</td>
<td>1.418</td>
<td>1.492</td>
<td>1.565</td>
<td>V</td>
</tr>
<tr>
<td>0xB</td>
<td>1.567</td>
<td>1.641</td>
<td>1.715</td>
<td>V</td>
</tr>
<tr>
<td>0xC</td>
<td>1.717</td>
<td>1.790</td>
<td>1.864</td>
<td>V</td>
</tr>
<tr>
<td>0xD</td>
<td>1.866</td>
<td>1.939</td>
<td>2.013</td>
<td>V</td>
</tr>
<tr>
<td>0xE</td>
<td>2.015</td>
<td>2.089</td>
<td>2.162</td>
<td>V</td>
</tr>
<tr>
<td>0xF</td>
<td>2.164</td>
<td>2.238</td>
<td>2.311</td>
<td>V</td>
</tr>
</tbody>
</table>

19.4 Initialization and Configuration

The following example shows how to configure an analog comparator to read back its output value from an internal register.

1. Enable the analog comparator clock by writing a value of 0x0000.0001 to the RCGCACMP register in the System Control module (see page 356).

2. Enable the clock to the appropriate GPIO modules via the RCGCGPIO register (see page 342). To find out which GPIO ports to enable, refer to Table 23-5 on page 1386.

3. In the GPIO module, enable the GPIO port/pin associated with the input signals as GPIO inputs. To determine which GPIO to configure, see Table 23-4 on page 1377.

4. Configure the PMCn fields in the GPIOPCTL register to assign the analog comparator output signals to the appropriate pins (see page 702 and Table 23-5 on page 1386).

5. Configure the internal voltage reference to 1.65 V by writing the ACREFCTL register with the value 0x0000.030C.

6. Configure the comparator to use the internal voltage reference and to not invert the output by writing the ACCTLn register with the value of 0x0000.040C.

7. Delay for 10 µs.

8. Read the comparator output value by reading the ACSTATn register’s OVAL value. Change the level of the comparator negative input signal C− to see the OVAL value change.
19.5 Register Map

Table 19-5 on page 1242 lists the comparator registers. The offset listed is a hexadecimal increment to the register's address, relative to the Analog Comparator base address of 0x4003.C000. Note that the analog comparator clock must be enabled before the registers can be programmed (see page 356). There must be a delay of 3 system clocks after the analog comparator module clock is enabled before any analog comparator module registers are accessed.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>ACMIS</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>Analog Comparator Masked Interrupt Status</td>
<td>1243</td>
</tr>
<tr>
<td>0x004</td>
<td>ACRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Analog Comparator Raw Interrupt Status</td>
<td>1244</td>
</tr>
<tr>
<td>0x008</td>
<td>ACINTEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Interrupt Enable</td>
<td>1245</td>
</tr>
<tr>
<td>0x010</td>
<td>ACREFCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Reference Voltage Control</td>
<td>1246</td>
</tr>
<tr>
<td>0x020</td>
<td>ACSTAT0</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Analog Comparator Status 0</td>
<td>1247</td>
</tr>
<tr>
<td>0x024</td>
<td>ACCTL0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Control 0</td>
<td>1248</td>
</tr>
<tr>
<td>0x040</td>
<td>ACSTAT1</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Analog Comparator Status 1</td>
<td>1247</td>
</tr>
<tr>
<td>0x044</td>
<td>ACCTL1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Control 1</td>
<td>1248</td>
</tr>
<tr>
<td>0x060</td>
<td>ACSTAT2</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Analog Comparator Status 2</td>
<td>1247</td>
</tr>
<tr>
<td>0x064</td>
<td>ACCTL2</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Analog Comparator Control 2</td>
<td>1248</td>
</tr>
<tr>
<td>0xFC0</td>
<td>ACMPPP</td>
<td>RO</td>
<td>0x0007.0007</td>
<td>Analog Comparator Peripheral Properties</td>
<td>1250</td>
</tr>
</tbody>
</table>

19.6 Register Descriptions

The remainder of this section lists and describes the Analog Comparator registers, in numerical order by address offset.
Register 1: Analog Comparator Masked Interrupt Status (ACMIS), offset 0x000

This register provides a summary of the interrupt status (masked) of the comparators.

Analog Comparator Masked Interrupt Status (ACMIS)
Base 0x4003.C000
Offset 0x000
Type RW1C, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>IN2</td>
<td>RW1C</td>
<td>0</td>
<td>Comparator 2 Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt has occurred or the interrupt is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The IN2 bits in the ACRIS register and the ACINTEN registers are set, providing an interrupt to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1. Clearing this bit also clears the IN2 bit in the ACRIS register.</td>
</tr>
<tr>
<td>1</td>
<td>IN1</td>
<td>RW1C</td>
<td>0</td>
<td>Comparator 1 Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt has occurred or the interrupt is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The IN1 bits in the ACRIS register and the ACINTEN registers are set, providing an interrupt to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1. Clearing this bit also clears the IN1 bit in the ACRIS register.</td>
</tr>
<tr>
<td>0</td>
<td>IN0</td>
<td>RW1C</td>
<td>0</td>
<td>Comparator 0 Masked Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 No interrupt has occurred or the interrupt is masked.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The IN0 bits in the ACRIS register and the ACINTEN registers are set, providing an interrupt to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1. Clearing this bit also clears the IN0 bit in the ACRIS register.</td>
</tr>
</tbody>
</table>
Register 2: Analog Comparator Raw Interrupt Status (ACRIS), offset 0x004

This register provides a summary of the interrupt status (raw) of the comparators. The bits in this register must be enabled to generate interrupts using the ACINTEN register.

Analog Comparator Raw Interrupt Status (ACRIS)
Base 0x4003.C000
Offset 0x004
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>IN2</td>
<td>RO</td>
<td>0</td>
<td>Comparator 2 Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the IN2 bit in the ACMIS register.</td>
</tr>
<tr>
<td>1</td>
<td>IN1</td>
<td>RO</td>
<td>0</td>
<td>Comparator 1 Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the IN1 bit in the ACMIS register.</td>
</tr>
<tr>
<td>0</td>
<td>IN0</td>
<td>RO</td>
<td>0</td>
<td>Comparator 0 Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the IN0 bit in the ACMIS register.</td>
</tr>
</tbody>
</table>
Register 3: Analog Comparator Interrupt Enable (ACINTEN), offset 0x008

This register provides the interrupt enable for the comparators.

### Analog Comparator Interrupt Enable (ACINTEN)

<table>
<thead>
<tr>
<th>Base</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x4003.C000</td>
<td>0x008</td>
<td>RW</td>
<td>0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>IN2</td>
<td>RW</td>
<td>0</td>
<td>Comparator 2 Interrupt Enable</td>
</tr>
<tr>
<td>1</td>
<td>IN1</td>
<td>RW</td>
<td>0</td>
<td>Comparator 1 Interrupt Enable</td>
</tr>
<tr>
<td>0</td>
<td>IN0</td>
<td>RW</td>
<td>0</td>
<td>Comparator 0 Interrupt Enable</td>
</tr>
</tbody>
</table>

Value Description

| 0 | A comparator 2 interrupt does not affect the interrupt status. |
| 1 | The raw interrupt signal comparator 2 is sent to the interrupt controller. |

| 0 | A comparator 1 interrupt does not affect the interrupt status. |
| 1 | The raw interrupt signal comparator 1 is sent to the interrupt controller. |

| 0 | A comparator 0 interrupt does not affect the interrupt status. |
| 1 | The raw interrupt signal comparator 0 is sent to the interrupt controller. |
Register 4: Analog Comparator Reference Voltage Control (ACREFCTL), offset 0x010

This register specifies whether the resistor ladder is powered on as well as the range and tap.

**Analog Comparator Reference Voltage Control (ACREFCTL)**

Base 0x4003.C000
Offset 0x010
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>9</td>
<td>EN</td>
<td>RW</td>
<td>0</td>
<td>Resistor Ladder Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The resistor ladder is unpowered.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Powers on the resistor ladder. The resistor ladder is connected to VDDA.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared at reset so that the internal reference consumes the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>least amount of power if it is not used.</td>
</tr>
<tr>
<td>8</td>
<td>RNG</td>
<td>RW</td>
<td>0</td>
<td>Resistor Ladder Range</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The ideal step size for the internal reference is VDDA / 29.4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The ideal step size for the internal reference is VDDA / 22.12.</td>
</tr>
<tr>
<td>7:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3:0</td>
<td>VREF</td>
<td>RW</td>
<td>0x0</td>
<td>Resistor Ladder Voltage Ref</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The VREF bit field specifies the resistor ladder tap that is passed through</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>an analog multiplexer. The voltage corresponding to the tap position is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the internal reference voltage available for comparison. See Table</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>19-2 on page 1239 for some output reference voltage examples.</td>
</tr>
</tbody>
</table>
Register 5: Analog Comparator Status 0 (ACSTAT0), offset 0x020
Register 6: Analog Comparator Status 1 (ACSTAT1), offset 0x040
Register 7: Analog Comparator Status 2 (ACSTAT2), offset 0x060

These registers specify the current output value of the comparator.

### Analog Comparator Status n (ACSTATn)

Base 0x4003.C000
Offset 0x020
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 1         | OVAL    | RO   | 0     | Comparator Output Value

**Value Description**

- **0**: VIN- > VIN+
- **1**: VIN- < VIN+

VIN- is the voltage on the Cn- pin. VIN+ is the voltage on the Cn+ pin, the C0+ pin, or the internal voltage reference (VREF) as defined by the ASRCP bit in the ACCTL register.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
Analog Comparators

Register 8: Analog Comparator Control 0 (ACCTL0), offset 0x024
Register 9: Analog Comparator Control 1 (ACCTL1), offset 0x044
Register 10: Analog Comparator Control 2 (ACCTL2), offset 0x064

These registers configure the comparator's input and output.

Analog Comparator Control n (ACCTLn)
Base 0x4003.C000
Offset 0x024
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit and Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11</td>
<td>TOEN</td>
<td>Trigger Output Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>10:9</td>
<td>ASRCP</td>
<td>Analog Source Positive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The ASRCP field specifies the source of input voltage to the VIN+ terminal</td>
</tr>
<tr>
<td></td>
<td></td>
<td>of the comparator. The encodings for this field are as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x3</td>
</tr>
<tr>
<td>8</td>
<td>reserved</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>TSLVAL</td>
<td>Trigger Sense Level Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
The **TSEN** field specifies the sense of the comparator output that generates an ADC event. The sense conditioning is as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Level sense, see TSLVAL</td>
</tr>
<tr>
<td>0x1</td>
<td>Falling edge</td>
</tr>
<tr>
<td>0x2</td>
<td>Rising edge</td>
</tr>
<tr>
<td>0x3</td>
<td>Either edge</td>
</tr>
</tbody>
</table>

### Interrupt Sense Level Value

The **ISLVAL** field specifies the sense of the comparator output that generates an interrupt. The sense conditioning is as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An interrupt is generated if the comparator output is Low.</td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is generated if the comparator output is High.</td>
</tr>
</tbody>
</table>

### Interrupt Sense

The **ISEN** field specifies the sense of the comparator output that generates an interrupt. The sense conditioning is as follows:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Level sense, see ISLVAL</td>
</tr>
<tr>
<td>0x1</td>
<td>Falling edge</td>
</tr>
<tr>
<td>0x2</td>
<td>Rising edge</td>
</tr>
<tr>
<td>0x3</td>
<td>Either edge</td>
</tr>
</tbody>
</table>

### Comparator Output Invert

The output of the comparator is unchanged. The output of the comparator is inverted prior to being processed by hardware.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The output of the comparator is unchanged.</td>
</tr>
<tr>
<td>1</td>
<td>The output of the comparator is inverted prior to being processed by hardware.</td>
</tr>
</tbody>
</table>

Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.
Register 11: Analog Comparator Peripheral Properties (ACMPPP), offset 0xFC0

The ACMPPP register provides information regarding the properties of the analog comparator module.

Analog Comparator Peripheral Properties (ACMPPP)
Base 0x4003.C000
Offset 0xFC0
Type RO, reset 0x0007.0007

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:19</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>18</td>
<td>CMP2</td>
<td>RO</td>
<td>0x1</td>
<td>Comparator Output 2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Comparator output 2 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Comparator output 2 is present.</td>
</tr>
<tr>
<td>17</td>
<td>CMP1</td>
<td>RO</td>
<td>0x1</td>
<td>Comparator Output 1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Comparator output 1 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Comparator output 1 is present.</td>
</tr>
<tr>
<td>16</td>
<td>CMP0</td>
<td>RO</td>
<td>0x1</td>
<td>Comparator Output 0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Comparator output 0 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Comparator output 0 is present.</td>
</tr>
<tr>
<td>15:3</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>2</td>
<td>CMP2</td>
<td>RO</td>
<td>0x1</td>
<td>Comparator 2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 Comparator 2 is not present.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 Comparator 2 is present.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>1</td>
<td>CMP1</td>
<td>RO</td>
<td>0x1</td>
<td>Comparator 1 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>CMP0</td>
<td>RO</td>
<td>0x1</td>
<td>Comparator 0 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Pulse Width Modulator (PWM)

Pulse width modulation (PWM) is a powerful technique for digitally encoding analog signal levels. High-resolution counters are used to generate a square wave, and the duty cycle of the square wave is modulated to encode an analog signal. Typical applications include switching power supplies and motor control.

The TM4C123GH6PZ microcontroller contains two PWM modules, each with four PWM generator blocks and a control block, for a total of 16 PWM outputs. The control block determines the polarity of the PWM signals, and which signals are passed through to the pins.

Each PWM generator block produces two PWM signals that share the same timer and frequency and can either be programmed with independent actions or as a single pair of complementary signals with dead-band delays inserted. The output signals, pwmA' and pwmB', of the PWM generation blocks are managed by the output control block before being passed to the device pins as MnPWM0 and MnPWM1 or MnPWM2 and MnPWM3, and so on.

Each TM4C123GH6PZ PWM module provides a great deal of flexibility and can generate simple PWM signals, such as those required by a simple charge pump as well as paired PWM signals with dead-band delays, such as those required by a half-H bridge driver. Three generator blocks can also generate the full six channels of gate controls required by a 3-phase inverter bridge.

Each PWM generator block has the following features:

- Four fault-condition handling inputs to quickly provide low-latency shutdown and prevent damage to the motor being controlled, for a total of eight inputs
- One 16-bit counter
  - Runs in Down or Up/Down mode
  - Output frequency controlled by a 16-bit load value
  - Load value updates can be synchronized
  - Produces output signals at zero and load value
- Two PWM comparators
  - Comparator value updates can be synchronized
  - Produces output signals on match
- PWM signal generator
  - Output PWM signal is constructed based on actions taken as a result of the counter and PWM comparator output signals
  - Produces two independent PWM signals
- Dead-band generator
  - Produces two PWM signals with programmable dead-band delays suitable for driving a half-H bridge
  - Can be bypassed, leaving input PWM signals unmodified
■ Can initiate an ADC sample sequence

The control block determines the polarity of the PWM signals and which signals are passed through to the pins. The output of the PWM generation blocks are managed by the output control block before being passed to the device pins. The PWM control block has the following options:

■ PWM output enable of each PWM signal
■ Optional output inversion of each PWM signal (polarity control)
■ Optional fault handling for each PWM signal
■ Synchronization of timers in the PWM generator blocks
■ Synchronization of timer/comparator updates across the PWM generator blocks
■ Extended PWM synchronization of timer/comparator updates across the PWM generator blocks
■ Interrupt status summary of the PWM generator blocks
■ Extended PWM fault handling, with multiple fault signals, programmable polarities, and filtering
■ PWM generators can be operated independently or synchronized with other generators

20.1 Block Diagram

Figure 20-1 on page 1254 provides the TM4C123GH6PZ PWM module diagram and Figure 20-2 on page 1254 provides a more detailed diagram of a TM4C123GH6PZ PWM generator. The TM4C123GH6PZ controller contains two PWM modules, each with four generator blocks that generate eight independent PWM signals or four paired PWM signals with dead-band delays inserted.
Figure 20-1. PWM Module Diagram

Figure 20-2. PWM Generator Block Diagram
20.2 Signal Description

The following table lists the external signals of the PWM modules and describes the function of each. The PWM controller signals are alternate functions for some GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for these PWM signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the PWM function. The number in parentheses is the encoding that must be programmed into the PMcn field in the GPIO Port Control (GPIOPCTL) register (page 702) to assign the PWM signal to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659.

Table 20-1. PWM Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0FAULT0</td>
<td>3</td>
<td>PD2 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>PH0 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>42</td>
<td>PF2 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>99</td>
<td>PD6 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0FAULT1</td>
<td>17</td>
<td>PH1 (6)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>43</td>
<td>PF3 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>60</td>
<td>PG2 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>PD7 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0FAULT2</td>
<td>18</td>
<td>PH2 (6)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td>39</td>
<td>PF4 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>59</td>
<td>PG3 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0FAULT3</td>
<td>19</td>
<td>PH3 (6)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 3.</td>
</tr>
<tr>
<td></td>
<td>37</td>
<td>PF5 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM0</td>
<td>16</td>
<td>PH0 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td>M0PWM1</td>
<td>17</td>
<td>PH1 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td>M0PWM2</td>
<td>18</td>
<td>PH2 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>92</td>
<td>PB4 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM3</td>
<td>19</td>
<td>PH3 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>91</td>
<td>PB5 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM4</td>
<td>74</td>
<td>PG4 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>79</td>
<td>PH4 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>95</td>
<td>PE4 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM5</td>
<td>75</td>
<td>PG5 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>78</td>
<td>PH5 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>96</td>
<td>PE5 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM6</td>
<td>1</td>
<td>PD0 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>PC4 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>77</td>
<td>PH6 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>87</td>
<td>PG6 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM7</td>
<td>2</td>
<td>PD1 (4)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>24</td>
<td>PC5 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>76</td>
<td>PH7 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>88</td>
<td>PG7 (4)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT0</td>
<td>39</td>
<td>PF4 (5)</td>
<td></td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>49</td>
<td>PK0 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>58</td>
<td>PF7 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 20-1. PWM Signals (100LQFP) (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1FAULT1</td>
<td>48</td>
<td>PK1 (6)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>62</td>
<td>PG0 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT2</td>
<td>47</td>
<td>PK2 (6)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>PG1 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT3</td>
<td>46</td>
<td>PK3 (6)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 3.</td>
</tr>
<tr>
<td>M1PWM0</td>
<td>1</td>
<td>PD0 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 0. This signal is</td>
</tr>
<tr>
<td></td>
<td>60</td>
<td>PG2 (5)</td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td>M1PWM1</td>
<td>2</td>
<td>PD1 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 1. This signal is</td>
</tr>
<tr>
<td></td>
<td>59</td>
<td>PG3 (5)</td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td>M1PWM2</td>
<td>34</td>
<td>PA6 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 2. This signal is</td>
</tr>
<tr>
<td></td>
<td>74</td>
<td>PG4 (5)</td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>95</td>
<td>PE4 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1PWM3</td>
<td>35</td>
<td>PA7 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 3. This signal is</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>PG5 (5)</td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>96</td>
<td>PE5 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1PWM4</td>
<td>40</td>
<td>PF0 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 4. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 2.</td>
</tr>
<tr>
<td>M1PWM5</td>
<td>41</td>
<td>PF1 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 5. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 2.</td>
</tr>
<tr>
<td>M1PWM6</td>
<td>42</td>
<td>PF2 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 6. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 3.</td>
</tr>
<tr>
<td>M1PWM7</td>
<td>43</td>
<td>PF3 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 7. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 3.</td>
</tr>
</tbody>
</table>

<sup>a</sup> The TTL designation indicates the pin has TTL-compatible voltage levels.

---

### 20.3 Functional Description

#### 20.3.1 Clock Configuration

The PWM has two clock source options:

- The System Clock
- A predivided System Clock

The clock source is selected by programming the USPWMDIV bit in the Run-Mode Clock Configuration (RCC) register at System Control offset 0x060. The PWMDIV bitfield specifies the divisor of the System Clock that is used to create the PWM Clock.

#### 20.3.2 PWM Timer

The timer in each PWM generator runs in one of two modes: Count-Down mode or Count-Up/Down mode. In Count-Down mode, the timer counts from the load value to zero, goes back to the load value, and continues counting down. In Count-Up/Down mode, the timer counts from zero up to the load value, back down to zero, back up to the load value, and so on. Generally, Count-Down mode is used for generating left- or right-aligned PWM signals, while the Count-Up/Down mode is used for generating center-aligned PWM signals.

The timers output three signals that are used in the PWM generation process: the direction signal (this is always Low in Count-Down mode, but alternates between Low and High in Count-Up/Down mode), a single-clock-cycle-width High pulse when the counter is zero, and a single-clock-cycle-width...
High pulse when the counter is equal to the load value. Note that in Count-Down mode, the zero pulse is immediately followed by the load pulse. In the figures in this chapter, these signals are labelled "dir," "zero," and "load."

20.3.3 PWM Comparators

Each PWM generator has two comparators that monitor the value of the counter; when either comparator matches the counter, they output a single-clock-cycle-width High pulse, labeled "cmpA" and "cmpB" in the figures in this chapter. When in Count-Up/Down mode, these comparators match both when counting up and when counting down, and thus are qualified by the counter direction signal. These qualified pulses are used in the PWM generation process. If either comparator match value is greater than the counter load value, then that comparator never outputs a High pulse.

Figure 20-3 on page 1257 shows the behavior of the counter and the relationship of these pulses when the counter is in Count-Down mode. Figure 20-4 on page 1258 shows the behavior of the counter and the relationship of these pulses when the counter is in Count-Up/Down mode. In these figures, the following definitions apply:

- **LOAD** is the value in the PWMnLOAD register
- **COMPA** is the value in the PWMnCMPA register
- **COMPB** is the value in the PWMnCMPB register
- **0** is the value zero
- **load** is the internal signal that has a single-clock-cycle-width High pulse when the counter is equal to the load value
- **zero** is the internal signal that has a single-clock-cycle-width High pulse when the counter is zero
- **cmpA** is the internal signal that has a single-clock-cycle-width High pulse when the counter is equal to **COMPA**
- **cmpB** is the internal signal that has a single-clock-cycle-width High pulse when the counter is equal to **COMPB**
- **dir** is the internal signal that indicates the count direction

**Figure 20-3. PWM Count-Down Mode**
20.3.4 PWM Signal Generator

Each PWM generator takes the load, zero, cmpA, and cmpB pulses (qualified by the dir signal) and generates two internal PWM signals, pwmA and pwmB. In Count-Down mode, there are four events that can affect these signals: zero, load, match A down, and match B down. In Count-Up/Down mode, there are six events that can affect these signals: zero, load, match A down, match A up, match B down, and match B up. The match A or match B events are ignored when they coincide with the zero or load events. If the match A and match B events coincide, the first signal, pwmA, is generated based only on the match A event, and the second signal, pwmB, is generated based only on the match B event.

For each event, the effect on each output PWM signal is programmable: it can be left alone (ignoring the event), it can be toggled, it can be driven Low, or it can be driven High. These actions can be used to generate a pair of PWM signals of various positions and duty cycles, which do or do not overlap. Figure 20-5 on page 1258 shows the use of Count-Up/Down mode to generate a pair of center-aligned, overlapped PWM signals that have different duty cycles. This figure shows the pwmA and pwmB signals before they have passed through the dead-band generator.

20.3.5 Dead-Band Generator

The pwmA and pwmB signals produced by each PWM generator are passed to the dead-band generator. If the dead-band generator is disabled, the PWM signals simply pass through to the
pwmA' and pwmB' signals unmodified. If the dead-band generator is enabled, the pwmB signal is lost and two PWM signals are generated based on the pwmA signal. The first output PWM signal, pwmA', is the pwmA signal with the rising edge delayed by a programmable amount. The second output PWM signal, pwmB', is the inversion of the pwmA signal with a programmable delay added between the falling edge of the pwmA signal and the rising edge of the pwmB' signal.

The resulting signals are a pair of active High signals where one is always High, except for a programmable amount of time at transitions where both are Low. These signals are therefore suitable for driving a half-H bridge, with the dead-band delays preventing shoot-through current from damaging the power electronics. Figure 20-6 on page 1259 shows the effect of the dead-band generator on the pwmA signal and the resulting pwmA' and pwmB' signals that are transmitted to the output control block.

![Figure 20-6. PWM Dead-Band Generator](image)

### 20.3.6 Interrupt/ADC-Trigger Selector

Each PWM generator also takes the same four (or six) counter events and uses them to generate an interrupt or an ADC trigger. Any of these events or a set of these events can be selected as a source for an interrupt; when any of the selected events occur, an interrupt is generated. Additionally, the same event, a different event, the same set of events, or a different set of events can be selected as a source for an ADC trigger; when any of these selected events occur, an ADC trigger pulse is generated. The selection of events allows the interrupt or ADC trigger to occur at a specific position within the pwmA or pwmB signal. Note that interrupts and ADC triggers are based on the raw events; delays in the PWM signal edges caused by the dead-band generator are not taken into account.

### 20.3.7 Synchronization Methods

Each PWM module provides four PWM generators, each providing two PWM outputs that may be used in a wide variety of applications. Generally speaking, the PWM is used in one of two categories of operation:

- **Unsynchronized.** The PWM generator and its two output signals are used alone, independent of other PWM generators.

- **Synchronized.** The PWM generator and its two outputs signals are used in conjunction with other PWM generators using a common, unified time base. If multiple PWM generators are configured with the same counter load value, synchronization can be used to guarantee that they also have the same count value (the PWM generators must be configured before they are synchronized). With this feature, more than two \( MnPWMn \) signals can be produced with a known relationship between the edges of those signals because the counters always have the same values. Other states in the module provide mechanisms to maintain the common time base and mutual synchronization.

The counter in a PWM generator can be reset to zero by writing the PWM Time Base Sync (PWMSYNC) register and setting the \( Syncn \) bit associated with the generator. Multiple PWM...
generators can be synchronized together by setting all necessary \texttt{SYNCn} bits in one access. For example, setting the \texttt{SYNC0} and \texttt{SYNC1} bits in the \texttt{PWMSYNC} register causes the counters in PWM generators 0 and 1 to reset together.

Additional synchronization can occur between multiple PWM generators by updating register contents in one of the following three ways:

- **Immediately.** The write value has immediate effect, and the hardware reacts immediately.

- **Locally Synchronized.** The write value does not affect the logic until the counter reaches the value zero at the end of the PWM cycle. In this case, the effect of the write is deferred, providing a guaranteed defined behavior and preventing overly short or overly long output PWM pulses.

- **Globally Synchronized.** The write value does not affect the logic until two sequential events have occurred: (1) the Update mode for the generator function is programmed for global synchronization in the \texttt{PWMnCTL} register, and (2) the counter reaches zero at the end of the PWM cycle. In this case, the effect of the write is deferred until the end of the PWM cycle following the end of all updates. This mode allows multiple items in multiple PWM generators to be updated simultaneously without odd effects during the update; everything runs from the old values until a point at which they all run from the new values. The Update mode of the load and comparator match values can be individually configured in each PWM generator block. It typically makes sense to use the synchronous update mechanism across PWM generator blocks when the timers in those blocks are synchronized, although this is not required in order for this mechanism to function properly.

The following registers provide either local or global synchronization based on the state of various Update mode bits and fields in the \texttt{PWMnCTL} register (\texttt{LOADUPD}; \texttt{CMPAUPD}; \texttt{CMFBUPD}):

- **Generator Registers:** \texttt{PWMnLOAD}, \texttt{PWMnCMPA}, and \texttt{PWMnCMPB}

The following registers default to immediate update, but are provided with the optional functionality of synchronously updating rather than having all updates take immediate effect:

- **Module-Level Register:** \texttt{PWMENABLE} (based on the state of the \texttt{ENUPDn} bits in the \texttt{PWMENUPD} register).

- **Generator Register:** \texttt{PWMnGENA}, \texttt{PWMnGENB}, \texttt{PWMnDBCTL}, \texttt{PWMnDBRISE}, and \texttt{PWMnDBFALL} (based on the state of various Update mode bits and fields in the \texttt{PWMnCTL} register (\texttt{GENAUPD}; \texttt{GENBUPD}; \texttt{DBCTLUPD}; \texttt{DBRISEUPD}; \texttt{DBFALLUPD})).

All other registers are considered statically provisioned for the execution of an application or are used dynamically for purposes unrelated to maintaining synchronization and therefore do not need synchronous update functionality.

### 20.3.8 Fault Conditions

A fault condition is one in which the controller must be signaled to stop normal PWM function and then set the \texttt{MnPWMn} signals to a safe state. Two basic situations cause fault conditions:

- The microcontroller is stalled and cannot perform the necessary computation in the time required for motion control

- An external error or event is detected

Each PWM generator can use the following inputs to generate a fault condition, including:
- MnFAULTn pin assertion
- A stall of the controller generated by the debugger
- The trigger of an ADC digital comparator

Fault conditions are calculated on a per-PWM generator basis. Each PWM generator configures the necessary conditions to indicate a fault condition exists. This method allows the development of applications with dependent and independent control.

Eight fault input pins (MnFAULTn) are available. These inputs may be used with circuits that generate an active High or active Low signal to indicate an error condition. A MnFAULTn pins may be individually programmed for the appropriate logic sense using the PWMnFLTSEN register.

The PWM generator's mode control, including fault condition handling, is provided in the PWMnCTL register. The PWMnCTL register also selects whether the fault condition is maintained as long as the external condition lasts or if it is latched until the fault condition until cleared by software. Finally, this register also enables a counter that may be used to extend the period of a fault condition for external events to assure that the duration is a minimum length. The minimum fault period count is specified in the PWMnMINFLTPER register.

**Note:** When using an ADC digital comparator as a fault source, the LATCH and MINFLTPER bits in the PWMnCTL register should be set to 1 to ensure trigger assertions are captured.

Status regarding the specific fault cause is provided in the PWMnFLTSTAT0 and PWMnFLTSTAT1 registers. Note that the fault status registers, PWMnFLTSTAT0 and PWMnFLTSTAT1, reflect the status of all fault sources, regardless of what fault sources are enabled for that particular generator.

PWM generator fault conditions may be promoted to a controller interrupt using the PWMINTEN register.

### 20.3.9 Output Control Block

The output control block takes care of the final conditioning of the pwmA' and pwmB' signals before they go to the pins as the MnPWMn signals. Via a single register, the PWM Output Enable (PWMENABLE) register, the set of PWM signals that are actually enabled to the pins can be modified. This function can be used, for example, to perform commutation of a brushless DC motor with a single register write (and without modifying the individual PWM generators, which are modified by the feedback control loop). In addition, the updating of the bits in the PWMENABLE register can be configured to be immediate or locally or globally synchronized to the next synchronous update using the PWM Enable Update (PWMENUPD) register.

During fault conditions, the PWM output signals, MnPWMn, usually must be driven to safe values so that external equipment may be safely controlled. The PWMFAULT register specifies whether during a fault condition, the generated signal continues to be passed driven or to an encoding specified in the PWMFAULTVAL register.

A final inversion can be applied to any of the MnPWMn signals, making them active Low instead of the default active High using the PWM Output Inversion (PWMINVERT). The inversion is applied even if a value has been enabled in the PWMFAULT register and specified in the PWMFAULTVAL register. In other words, if a bit is set in the PWMFAULT, PWMFAULTVAL, and PWMINVERT registers, the output on the MnPWMn signal is 0, not 1 as specified in the PWMFAULTVAL register.
20.4 Initialization and Configuration

The following example shows how to initialize PWM Generator 0 with a 25-kHz frequency, a 25% duty cycle on the MnPWM0 pin, and a 75% duty cycle on the MnPWM1 pin. This example assumes the system clock is 20 MHz.

1. Enable the PWM clock by writing a value of 0x0010.0000 to the RCGC0 register in the System Control module (see page 461).

2. Enable the clock to the appropriate GPIO module via the RCGC2 register in the System Control module (see page 469).

3. In the GPIO module, enable the appropriate pins for their alternate function using the GPIOAFSEL register. To determine which GPIOs to configure, see Table 23-4 on page 1377.

4. Configure the PMCn fields in the GPIOPCTL register to assign the PWM signals to the appropriate pins (see page 702 and Table 23-5 on page 1386).

5. Configure the Run-Mode Clock Configuration (RCC) register in the System Control module to use the PWM divide (USEPWMDIV) and set the divider (PWMDIV) to divide by 2 (000).

6. Configure the PWM generator for countdown mode with immediate updates to the parameters.

   - Write the PWM0CTL register with a value of 0x0000.0000.
   - Write the PWM0GENA register with a value of 0x0000.008C.
   - Write the PWM0GENB register with a value of 0x0000.080C.

7. Set the period. For a 25-KHz frequency, the period = 1/25,000, or 40 microseconds. The PWM clock source is 10 MHz; the system clock divided by 2. Thus there are 400 clock ticks per period. Use this value to set the PWM0LOAD register. In Count-Down mode, set the LOAD field in the PWM0LOAD register to the requested period minus one.

   - Write the PWM0LOAD register with a value of 0x0000.018F.

8. Set the pulse width of the MnPWM0 pin for a 25% duty cycle.

   - Write the PWM0CMPA register with a value of 0x0000.012B.

9. Set the pulse width of the MnPWM1 pin for a 75% duty cycle.

   - Write the PWM0CMPB register with a value of 0x0000.0063.

10. Start the timers in PWM generator 0.

   - Write the PWM0CTL register with a value of 0x0000.0001.

11. Enable PWM outputs.

   - Write the PWMENABLE register with a value of 0x0000.0003.

20.5 Register Map

Table 20-2 on page 1263 lists the PWM registers. The offset listed is a hexadecimal increment to the register’s address, relative to the PWM module’s base address:
PWM0: 0x4002.8000
PWM1: 0x4002.9000

Note that the PWM module clock must be enabled before the registers can be programmed (see page 461). There must be a delay of 3 system clocks after the PWM module clock is enabled before any PWM module registers are accessed.

Table 20-2. PWM Register Map

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>PWMCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM Master Control</td>
<td>1266</td>
</tr>
<tr>
<td>0x004</td>
<td>PWMSYNC</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM Time Base Sync</td>
<td>1268</td>
</tr>
<tr>
<td>0x008</td>
<td>PWMENABLE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM Output Enable</td>
<td>1269</td>
</tr>
<tr>
<td>0x00C</td>
<td>PWMINVERT</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM Output Inversion</td>
<td>1271</td>
</tr>
<tr>
<td>0x010</td>
<td>PWMFAULT</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM Output Fault</td>
<td>1273</td>
</tr>
<tr>
<td>0x014</td>
<td>PWMINTEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM Interrupt Enable</td>
<td>1275</td>
</tr>
<tr>
<td>0x018</td>
<td>PWMRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM Raw Interrupt Status</td>
<td>1277</td>
</tr>
<tr>
<td>0x01C</td>
<td>PWMIISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>PWM Interrupt Status and Clear</td>
<td>1280</td>
</tr>
<tr>
<td>0x020</td>
<td>PWMSTATUS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM Status</td>
<td>1283</td>
</tr>
<tr>
<td>0x024</td>
<td>PWMFAULTVAL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM Fault Condition Value</td>
<td>1285</td>
</tr>
<tr>
<td>0x028</td>
<td>PWMEMUPD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM Enable Update</td>
<td>1287</td>
</tr>
<tr>
<td>0x040</td>
<td>PWM0CTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Control</td>
<td>1291</td>
</tr>
<tr>
<td>0x044</td>
<td>PWM0INTEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Interrupt and Trigger Enable</td>
<td>1296</td>
</tr>
<tr>
<td>0x048</td>
<td>PWMR0RIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM0 Raw Interrupt Status</td>
<td>1299</td>
</tr>
<tr>
<td>0x04C</td>
<td>PWMOISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>PWM0 Interrupt Status and Clear</td>
<td>1301</td>
</tr>
<tr>
<td>0x050</td>
<td>PWMOLOAD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Load</td>
<td>1303</td>
</tr>
<tr>
<td>0x054</td>
<td>PWMOCOUNT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM0 Counter</td>
<td>1304</td>
</tr>
<tr>
<td>0x058</td>
<td>PWMOCMPA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Compare A</td>
<td>1305</td>
</tr>
<tr>
<td>0x05C</td>
<td>PWMOCMPB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Compare B</td>
<td>1306</td>
</tr>
<tr>
<td>0x060</td>
<td>PWMOGENA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Generator A Control</td>
<td>1307</td>
</tr>
<tr>
<td>0x064</td>
<td>PWMOGENB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Generator B Control</td>
<td>1310</td>
</tr>
<tr>
<td>0x068</td>
<td>PWM0DBCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Dead-Band Control</td>
<td>1313</td>
</tr>
<tr>
<td>0x06C</td>
<td>PWM0DBRISE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Dead-Band Rising-Edge Delay</td>
<td>1314</td>
</tr>
<tr>
<td>0x070</td>
<td>PWM0DBFALL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Dead-Band Falling-Edge-Delay</td>
<td>1315</td>
</tr>
<tr>
<td>0x074</td>
<td>PWM0FLTSRC0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Fault Source 0</td>
<td>1316</td>
</tr>
<tr>
<td>0x078</td>
<td>PWM0FLTSRC1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Fault Source 1</td>
<td>1318</td>
</tr>
<tr>
<td>0x07C</td>
<td>PWM0MINFLTPER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Minimum Fault Period</td>
<td>1321</td>
</tr>
</tbody>
</table>
Table 20-2. PWM Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x080</td>
<td>PWM1CTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Control</td>
<td>1291</td>
</tr>
<tr>
<td>0x084</td>
<td>PWM1INTEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Interrupt and Trigger Enable</td>
<td>1296</td>
</tr>
<tr>
<td>0x088</td>
<td>PWM1RIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM1 Raw Interrupt Status</td>
<td>1299</td>
</tr>
<tr>
<td>0x08C</td>
<td>PWM1ISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>PWM1 Interrupt Status and Clear</td>
<td>1301</td>
</tr>
<tr>
<td>0x090</td>
<td>PWM1LOAD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Load</td>
<td>1303</td>
</tr>
<tr>
<td>0x094</td>
<td>PWM1COUNT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM1 Counter</td>
<td>1304</td>
</tr>
<tr>
<td>0x098</td>
<td>PWM1CMPA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Compare A</td>
<td>1305</td>
</tr>
<tr>
<td>0x09C</td>
<td>PWM1CMPB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Compare B</td>
<td>1306</td>
</tr>
<tr>
<td>0x0A0</td>
<td>PWM1GENA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Generator A Control</td>
<td>1307</td>
</tr>
<tr>
<td>0x0A4</td>
<td>PWM1GENB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Generator B Control</td>
<td>1310</td>
</tr>
<tr>
<td>0x0A8</td>
<td>PWM1DBCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Dead-Band Control</td>
<td>1313</td>
</tr>
<tr>
<td>0x0AC</td>
<td>PWM1DBRISE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Dead-Band Rising-Edge Delay</td>
<td>1314</td>
</tr>
<tr>
<td>0x0B0</td>
<td>PWM1DBFALL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Dead-Band Falling-Edge-Delay</td>
<td>1315</td>
</tr>
<tr>
<td>0x0B4</td>
<td>PWM1FLTSRC0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Fault Source 0</td>
<td>1316</td>
</tr>
<tr>
<td>0x0B8</td>
<td>PWM1FLTSRC1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Fault Source 1</td>
<td>1318</td>
</tr>
<tr>
<td>0x0BC</td>
<td>PWM1MINFLT.PER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Minimum Fault Period</td>
<td>1321</td>
</tr>
<tr>
<td>0x0C0</td>
<td>PWM2CTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Control</td>
<td>1291</td>
</tr>
<tr>
<td>0x0C4</td>
<td>PWM2INTEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Interrupt and Trigger Enable</td>
<td>1296</td>
</tr>
<tr>
<td>0x0C8</td>
<td>PWM2RIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM2 Raw Interrupt Status</td>
<td>1299</td>
</tr>
<tr>
<td>0x0CC</td>
<td>PWM2ISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>PWM2 Interrupt Status and Clear</td>
<td>1301</td>
</tr>
<tr>
<td>0x0D0</td>
<td>PWM2LOAD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Load</td>
<td>1303</td>
</tr>
<tr>
<td>0x0D4</td>
<td>PWM2COUNT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM2 Counter</td>
<td>1304</td>
</tr>
<tr>
<td>0x0D8</td>
<td>PWM2CMPA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Compare A</td>
<td>1305</td>
</tr>
<tr>
<td>0x0DC</td>
<td>PWM2CMPB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Compare B</td>
<td>1306</td>
</tr>
<tr>
<td>0x0E0</td>
<td>PWM2GENA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Generator A Control</td>
<td>1307</td>
</tr>
<tr>
<td>0x0E4</td>
<td>PWM2GENB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Generator B Control</td>
<td>1310</td>
</tr>
<tr>
<td>0x0E8</td>
<td>PWM2DBCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Dead-Band Control</td>
<td>1313</td>
</tr>
<tr>
<td>0x0EC</td>
<td>PWM2DBRISE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Dead-Band Rising-Edge Delay</td>
<td>1314</td>
</tr>
<tr>
<td>0x0F0</td>
<td>PWM2DBFALL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Dead-Band Falling-Edge-Delay</td>
<td>1315</td>
</tr>
<tr>
<td>0x0F4</td>
<td>PWM2FLTSRC0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Fault Source 0</td>
<td>1316</td>
</tr>
<tr>
<td>0x0F8</td>
<td>PWM2FLTSRC1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Fault Source 1</td>
<td>1318</td>
</tr>
<tr>
<td>0x0FC</td>
<td>PWM2MINFLT.PER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Minimum Fault Period</td>
<td>1321</td>
</tr>
</tbody>
</table>
Table 20-2. PWM Register Map (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x100</td>
<td>PWM3CTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Control</td>
<td>1291</td>
</tr>
<tr>
<td>0x104</td>
<td>PWM3INTEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Interrupt and Trigger Enable</td>
<td>1296</td>
</tr>
<tr>
<td>0x108</td>
<td>PWM3RIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM3 Raw Interrupt Status</td>
<td>1299</td>
</tr>
<tr>
<td>0x10C</td>
<td>PWM3ISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>PWM3 Interrupt Status and Clear</td>
<td>1301</td>
</tr>
<tr>
<td>0x110</td>
<td>PWM3LOAD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Load</td>
<td>1303</td>
</tr>
<tr>
<td>0x114</td>
<td>PWM3COUNT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>PWM3 Counter</td>
<td>1304</td>
</tr>
<tr>
<td>0x118</td>
<td>PWM3CMPA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Compare A</td>
<td>1305</td>
</tr>
<tr>
<td>0x11C</td>
<td>PWM3CMPB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Compare B</td>
<td>1306</td>
</tr>
<tr>
<td>0x120</td>
<td>PWM3GENA</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Generator A Control</td>
<td>1307</td>
</tr>
<tr>
<td>0x124</td>
<td>PWM3GENB</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Generator B Control</td>
<td>1310</td>
</tr>
<tr>
<td>0x128</td>
<td>PWM3DBCTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Dead-Band Control</td>
<td>1313</td>
</tr>
<tr>
<td>0x12C</td>
<td>PWM3DBRISE</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Dead-Band Rising-Edge Delay</td>
<td>1314</td>
</tr>
<tr>
<td>0x130</td>
<td>PWM3DBFALL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Dead-Band Falling-Edge-Delay</td>
<td>1315</td>
</tr>
<tr>
<td>0x134</td>
<td>PWM3FLTSC0</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Fault Source 0</td>
<td>1316</td>
</tr>
<tr>
<td>0x138</td>
<td>PWM3FLTSC1</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Fault Source 1</td>
<td>1318</td>
</tr>
<tr>
<td>0x13C</td>
<td>PWM3MINFLTPER</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Minimum Fault Period</td>
<td>1321</td>
</tr>
<tr>
<td>0x800</td>
<td>PWM0FLTSEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM0 Fault Pin Logic Sense</td>
<td>1322</td>
</tr>
<tr>
<td>0x804</td>
<td>PWM0FLTSTAT0</td>
<td>-</td>
<td>0x0000.0000</td>
<td>PWM0 Fault Status 0</td>
<td>1323</td>
</tr>
<tr>
<td>0x808</td>
<td>PWM0FLTSTAT1</td>
<td>-</td>
<td>0x0000.0000</td>
<td>PWM0 Fault Status 1</td>
<td>1325</td>
</tr>
<tr>
<td>0x880</td>
<td>PWM1FLTSEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM1 Fault Pin Logic Sense</td>
<td>1322</td>
</tr>
<tr>
<td>0x884</td>
<td>PWM1FLTSTAT0</td>
<td>-</td>
<td>0x0000.0000</td>
<td>PWM1 Fault Status 0</td>
<td>1323</td>
</tr>
<tr>
<td>0x888</td>
<td>PWM1FLTSTAT1</td>
<td>-</td>
<td>0x0000.0000</td>
<td>PWM1 Fault Status 1</td>
<td>1325</td>
</tr>
<tr>
<td>0x900</td>
<td>PWM2FLTSEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM2 Fault Pin Logic Sense</td>
<td>1322</td>
</tr>
<tr>
<td>0x904</td>
<td>PWM2FLTSTAT0</td>
<td>-</td>
<td>0x0000.0000</td>
<td>PWM2 Fault Status 0</td>
<td>1323</td>
</tr>
<tr>
<td>0x908</td>
<td>PWM2FLTSTAT1</td>
<td>-</td>
<td>0x0000.0000</td>
<td>PWM2 Fault Status 1</td>
<td>1325</td>
</tr>
<tr>
<td>0x980</td>
<td>PWM3FLTSEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>PWM3 Fault Pin Logic Sense</td>
<td>1322</td>
</tr>
<tr>
<td>0x984</td>
<td>PWM3FLTSTAT0</td>
<td>-</td>
<td>0x0000.0000</td>
<td>PWM3 Fault Status 0</td>
<td>1323</td>
</tr>
<tr>
<td>0x988</td>
<td>PWM3FLTSTAT1</td>
<td>-</td>
<td>0x0000.0000</td>
<td>PWM3 Fault Status 1</td>
<td>1325</td>
</tr>
<tr>
<td>0xFC0</td>
<td>PWMPP</td>
<td>RO</td>
<td>0x0000.0344</td>
<td>PWM Peripheral Properties</td>
<td>1328</td>
</tr>
</tbody>
</table>

20.6 Register Descriptions

The remainder of this section lists and describes the PWM registers, in numerical order by address offset.
Register 1: PWM Master Control (PWMCTL), offset 0x000

This register provides master control over the PWM generation blocks.

---

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>GLOBALSYNC3</td>
<td>RW</td>
<td>0</td>
<td>Update PWM Generator 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>applied the next time the corresponding counter becomes zero.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit automatically clears when the updates have completed; it cannot</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>be cleared by software.</td>
</tr>
<tr>
<td>2</td>
<td>GLOBALSYNC2</td>
<td>RW</td>
<td>0</td>
<td>Update PWM Generator 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>applied the next time the corresponding counter becomes zero.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit automatically clears when the updates have completed; it cannot</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>be cleared by software.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>1</td>
<td>GLOBALSYNC1</td>
<td>RW</td>
<td>0</td>
<td>Update PWM Generator 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>GLOBALSYNC0</td>
<td>RW</td>
<td>0</td>
<td>Update PWM Generator 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 2: PWM Time Base Sync (PWMSYNC), offset 0x004

This register provides a method to perform synchronization of the counters in the PWM generation blocks. Setting a bit in this register causes the specified counter to reset back to 0; setting multiple bits resets multiple counters simultaneously. The bits auto-clear after the reset has occurred; reading them back as zero indicates that the synchronization has completed.

PWM Time Base Sync (PWMSYNC)
PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x004
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>SYNC3</td>
<td>RW</td>
<td>0</td>
<td>Reset Generator 3 Counter</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>No effect.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Resets the PWM generator 3 counter.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>SYNC2</td>
<td>RW</td>
<td>0</td>
<td>Reset Generator 2 Counter</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>No effect.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Resets the PWM generator 2 counter.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>SYNC1</td>
<td>RW</td>
<td>0</td>
<td>Reset Generator 1 Counter</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>No effect.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Resets the PWM generator 1 counter.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>SYNC0</td>
<td>RW</td>
<td>0</td>
<td>Reset Generator 0 Counter</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>No effect.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Resets the PWM generator 0 counter.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 3: PWM Output Enable (PWMEENABLE), offset 0x008

This register provides a master control of which generated pwmA' and pwmB' signals are output to the MnPWMn pins. By disabling a PWM output, the generation process can continue (for example, when the time bases are synchronized) without driving PWM signals to the pins. When bits in this register are set, the corresponding pwmA' or pwmB' signal is passed through to the output stage. When bits are clear, the pwmA' or pwmB' signal is replaced by a zero value which is also passed to the output stage. The PWMINVERT register controls the output stage, so if the corresponding bit is set in that register, the value seen on the MnPWMn signal is inverted from what is configured by the bits in this register. Updates to the bits in this register can be immediate or locally or globally synchronized to the next synchronous update as controlled by the ENUPDn fields in the PWMEMUPD register.

PWM Output Enable (PWMEENABLE)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>PWM7EN</td>
<td>RW</td>
<td>0</td>
<td>MnPWM7 Output Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The MnPWM7 signal has a zero value.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The generated pwn3B' signal is passed to the MnPWM7 pin.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PWM6EN</td>
<td>RW</td>
<td>0</td>
<td>MnPWM6 Output Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The MnPWM6 signal has a zero value.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The generated pwn3A' signal is passed to the MnPWM6 pin.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>PWM5EN</td>
<td>RW</td>
<td>0</td>
<td>MnPWM5 Output Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The MnPWM5 signal has a zero value.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The generated pwn2B' signal is passed to the MnPWM5 pin.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Pulse Width Modulator (PWM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>PWM4EN</td>
<td>RW</td>
<td>0</td>
<td>MnPWM4 Output Enable</td>
</tr>
<tr>
<td>3</td>
<td>PWM3EN</td>
<td>RW</td>
<td>0</td>
<td>MnPWM3 Output Enable</td>
</tr>
<tr>
<td>2</td>
<td>PWM2EN</td>
<td>RW</td>
<td>0</td>
<td>MnPWM2 Output Enable</td>
</tr>
<tr>
<td>1</td>
<td>PWM1EN</td>
<td>RW</td>
<td>0</td>
<td>MnPWM1 Output Enable</td>
</tr>
<tr>
<td>0</td>
<td>PWM0EN</td>
<td>RW</td>
<td>0</td>
<td>MnPWM0 Output Enable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The MnPWM signal has a zero value.</td>
</tr>
<tr>
<td>1</td>
<td>The generated pwm2A' signal is passed to the MnPWM4 pin.</td>
</tr>
<tr>
<td>0</td>
<td>The MnPWM3 signal has a zero value.</td>
</tr>
<tr>
<td>1</td>
<td>The generated pwm1B' signal is passed to the MnPWM3 pin.</td>
</tr>
<tr>
<td>0</td>
<td>The MnPWM2 signal has a zero value.</td>
</tr>
<tr>
<td>1</td>
<td>The generated pwm1A' signal is passed to the MnPWM2 pin.</td>
</tr>
<tr>
<td>0</td>
<td>The MnPWM1 signal has a zero value.</td>
</tr>
<tr>
<td>1</td>
<td>The generated pwm0B' signal is passed to the MnPWM1 pin.</td>
</tr>
<tr>
<td>0</td>
<td>The MnPWM0 signal has a zero value.</td>
</tr>
<tr>
<td>1</td>
<td>The generated pwm0A' signal is passed to the MnPWM0 pin.</td>
</tr>
</tbody>
</table>
Register 4: PWM Output Inversion (PWMINVERT), offset 0x00C

This register provides a master control of the polarity of the MnPWMn signals on the device pins. The pwmA' and pwmB' signals generated by the PWM generator are active High; but can be made active Low via this register. Disabled PWM channels are also passed through the output inverter (if so configured) so that inactive signals can be High. In addition, if the PWMFAULT register enables a specific value to be placed on the MnPWMn signals during a fault condition, that value is inverted if the corresponding bit in this register is set.

### PWM Output Inversion (PWMINVERT)

PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x00C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>PWM7INV</td>
<td>RW</td>
<td>0</td>
<td>Invert MnPWM7 Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The MnPWM7 signal is not inverted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The MnPWM7 signal is inverted.</td>
</tr>
<tr>
<td>6</td>
<td>PWM6INV</td>
<td>RW</td>
<td>0</td>
<td>Invert MnPWM6 Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The MnPWM6 signal is not inverted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The MnPWM6 signal is inverted.</td>
</tr>
<tr>
<td>5</td>
<td>PWM5INV</td>
<td>RW</td>
<td>0</td>
<td>Invert MnPWM5 Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The MnPWM5 signal is not inverted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The MnPWM5 signal is inverted.</td>
</tr>
<tr>
<td>4</td>
<td>PWM4INV</td>
<td>RW</td>
<td>0</td>
<td>Invert MnPWM4 Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The MnPWM4 signal is not inverted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The MnPWM4 signal is inverted.</td>
</tr>
</tbody>
</table>
### Pulse Width Modulator (PWM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>PWM3INV</td>
<td>RW</td>
<td>0</td>
<td>Invert MnPWM3 Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>0</td>
<td>The MnPWM3 signal is not inverted.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
<td>The MnPWM3 signal is inverted.</td>
</tr>
<tr>
<td>2</td>
<td>PWM2INV</td>
<td>RW</td>
<td>0</td>
<td>Invert MnPWM2 Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>0</td>
<td>The MnPWM2 signal is not inverted.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
<td>The MnPWM2 signal is inverted.</td>
</tr>
<tr>
<td>1</td>
<td>PWM1INV</td>
<td>RW</td>
<td>0</td>
<td>Invert MnPWM1 Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>0</td>
<td>The MnPWM1 signal is not inverted.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
<td>The MnPWM1 signal is inverted.</td>
</tr>
<tr>
<td>0</td>
<td>PWM0INV</td>
<td>RW</td>
<td>0</td>
<td>Invert MnPWM0 Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>0</td>
<td>The MnPWM0 signal is not inverted.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>1</td>
<td>The MnPWM0 signal is inverted.</td>
</tr>
</tbody>
</table>
Register 5: PWM Output Fault (PWMFAULT), offset 0x010

This register controls the behavior of the MnPWMn outputs in the presence of fault conditions. Both the fault inputs (MnFAULTn pins and digital comparator outputs) and debug events are considered fault conditions. On a fault condition, each pwmA’ or pwmB’ signal can be passed through unmodified or driven to the value specified by the corresponding bit in the PWMFAULTVAL register. For outputs that are configured for pass-through, the debug event handling on the corresponding PWM generator also determines if the pwmA’ or pwmB’ signal continues to be generated.

Fault condition control occurs before the output inverter, so PWM signals driven to a specified value on fault are inverted if the channel is configured for inversion (therefore, the pin is driven to the logical complement of the specified value on a fault condition).

PWM Output Fault (PWMFAULT)
PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x010
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>FAULT7</td>
<td>RW</td>
<td>0</td>
<td>MnPWM7 Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The generated pwm3B' signal is passed to the MnPWM7 pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MnPWM7 output signal is driven to the value specified by the PWM7 bit in the PWMFAULTVAL register.</td>
</tr>
<tr>
<td>6</td>
<td>FAULT6</td>
<td>RW</td>
<td>0</td>
<td>MnPWM6 Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The generated pwm3A' signal is passed to the MnPWM6 pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MnPWM6 output signal is driven to the value specified by the PWM6 bit in the PWMFAULTVAL register.</td>
</tr>
<tr>
<td>5</td>
<td>FAULT5</td>
<td>RW</td>
<td>0</td>
<td>MnPWM5 Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The generated pwm2B' signal is passed to the MnPWM5 pin.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MnPWM5 output signal is driven to the value specified by the PWM5 bit in the PWMFAULTVAL register.</td>
</tr>
</tbody>
</table>
## Pulse Width Modulator (PWM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>FAULT4</td>
<td>RW</td>
<td>0</td>
<td>MnPWM4 Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>FAULT3</td>
<td>RW</td>
<td>0</td>
<td>MnPWM3 Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>FAULT2</td>
<td>RW</td>
<td>0</td>
<td>MnPWM2 Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>FAULT1</td>
<td>RW</td>
<td>0</td>
<td>MnPWM1 Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>FAULT0</td>
<td>RW</td>
<td>0</td>
<td>MnPWM0 Fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>
Register 6: PWM Interrupt Enable (PWMINTEN), offset 0x014

This register controls the global interrupt generation capabilities of the PWM module. The events that can cause an interrupt are the fault input and the individual interrupts from the PWM generators.

Note: The "n" in the INTFAULTn and INTPWMn bits in this register correspond to the PWM generators, not to the FAULTn signals.

PWM Interrupt Enable (PWMINTEN)
PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x014
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19</td>
<td>INTFAULT3</td>
<td>RW</td>
<td>0</td>
<td>Interrupt Fault 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The fault condition for PWM generator 3 is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the fault condition for PWM generator 3 is asserted.</td>
</tr>
<tr>
<td>18</td>
<td>INTFAULT2</td>
<td>RW</td>
<td>0</td>
<td>Interrupt Fault 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The fault condition for PWM generator 2 is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the fault condition for PWM generator 2 is asserted.</td>
</tr>
<tr>
<td>17</td>
<td>INTFAULT1</td>
<td>RW</td>
<td>0</td>
<td>Interrupt Fault 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The fault condition for PWM generator 1 is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the fault condition for PWM generator 1 is asserted.</td>
</tr>
</tbody>
</table>
### Pulse Width Modulator (PWM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>INTFAULT0</td>
<td>RW</td>
<td>0</td>
<td>Interrupt Fault 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The fault condition for PWM generator 0 is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the fault condition for PWM generator 0 is asserted.</td>
</tr>
<tr>
<td>15:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>INTPWM3</td>
<td>RW</td>
<td>0</td>
<td>PWM3 Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The PWM generator 3 interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the PWM generator 3 block asserts an interrupt.</td>
</tr>
<tr>
<td>2</td>
<td>INTPWM2</td>
<td>RW</td>
<td>0</td>
<td>PWM2 Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The PWM generator 2 interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the PWM generator 2 block asserts an interrupt.</td>
</tr>
<tr>
<td>1</td>
<td>INTPWM1</td>
<td>RW</td>
<td>0</td>
<td>PWM1 Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The PWM generator 1 interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the PWM generator 1 block asserts an interrupt.</td>
</tr>
<tr>
<td>0</td>
<td>INTPWM0</td>
<td>RW</td>
<td>0</td>
<td>PWM0 Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> <strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The PWM generator 0 interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An interrupt is sent to the interrupt controller when the PWM generator 0 block asserts an interrupt.</td>
</tr>
</tbody>
</table>
Register 7: PWM Raw Interrupt Status (PWMRIS), offset 0x018

This register provides the current set of interrupt sources that are asserted, regardless of whether they are enabled to cause an interrupt to be asserted to the interrupt controller. The fault interrupt is asserted based on the fault condition source that is specified by the PWMnCTL, PWMnFLTSRC0 and PWMnFLTSRC1 registers. The fault interrupt is latched on detection and must be cleared through the PWM Interrupt Status and Clear (PWMISC) register. The actual value of the MnFAULTn signals can be observed using the PWMSTATUS register.

The PWM generator interrupts simply reflect the status of the PWM generators and are cleared via the interrupt status register in the PWM generator blocks. If a bit is set, the event is active; if a bit is clear the event is not active.

PWM Raw Interrupt Status (PWMRIS)
PWM0 base: 0x4002.8000
PWN1 base: 0x4002.9000
Offset 0x018
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19</td>
<td>INTFAULT3</td>
<td>RO</td>
<td>0</td>
<td>Interrupt Fault PWM 3</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 The fault condition for PWM generator 3 has not been asserted.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 The fault condition for PWM generator 3 is asserted.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Note:</td>
<td>If the LATCH bit is set in the PWM3CTL register, the INTFAULT3 bit in this register can be cleared by writing a 1 to the INTFAULT3 bit in the PWMISC register. If the LATCH bit is 0 in the PWM3CTL register, writing a 1 to the INTFAULT3 bit in the PWMISC register has no effect.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>INTFAULT2</td>
<td>RO</td>
<td>0</td>
<td>Interrupt Fault PWM 2</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 The fault condition for PWM generator 2 has not been asserted.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 The fault condition for PWM generator 2 is asserted.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Note:</td>
<td>If the LATCH bit is set in the PWM2CTL register, the INTFAULT2 bit in this register can be cleared by writing a 1 to the INTFAULT2 bit in the PWMISC register. If the LATCH bit is 0 in the PWM2CTL register, writing a 1 to the INTFAULT2 bit in the PWMISC register has no effect.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Pulse Width Modulator (PWM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>17</td>
<td>INTFAULT1</td>
<td>RO</td>
<td>0</td>
<td>Interrupt Fault PWM 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> If the <code>LATCH</code> bit is set in the <code>PWM1CTL</code> register, the <code>INTFAULT1</code> bit in this register can be cleared by writing a 1 to the <code>INTFAULT1</code> bit in the <code>PWMISC</code> register. If the <code>LATCH</code> bit is 0 in the <code>PWM1CTL</code> register, writing a 1 to the <code>INTFAULT1</code> bit in the <code>PWMISC</code> register has no effect.</td>
</tr>
<tr>
<td>16</td>
<td>INTFAULT0</td>
<td>RO</td>
<td>0</td>
<td>Interrupt Fault PWM 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> If the <code>LATCH</code> bit is set in the <code>PWM0CTL</code> register, the <code>INTFAULT0</code> bit in this register can be cleared by writing a 1 to the <code>INTFAULT0</code> bit in the <code>PWMISC</code> register. If the <code>LATCH</code> bit is 0 in the <code>PWM0CTL</code> register, writing a 1 to the <code>INTFAULT0</code> bit in the <code>PWMISC</code> register has no effect.</td>
</tr>
<tr>
<td>15:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>INTPWM3</td>
<td>RO</td>
<td>0</td>
<td>PWM3 Interrupt Asserted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <code>PWM3RIS</code> register shows the source of this interrupt. This bit is cleared by writing a 1 to the corresponding bit in the <code>PWM3ISC</code> register.</td>
</tr>
<tr>
<td>2</td>
<td>INTPWM2</td>
<td>RO</td>
<td>0</td>
<td>PWM2 Interrupt Asserted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <code>PWM2RIS</code> register shows the source of this interrupt. This bit is cleared by writing a 1 to the corresponding bit in the <code>PWM2ISC</code> register.</td>
</tr>
<tr>
<td>1</td>
<td>INTPWM1</td>
<td>RO</td>
<td>0</td>
<td>PWM1 Interrupt Asserted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The <code>PWM1RIS</code> register shows the source of this interrupt. This bit is cleared by writing a 1 to the corresponding bit in the <code>PWM1ISC</code> register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>0</td>
<td>INTPWM0</td>
<td>RO</td>
<td>0</td>
<td>PWM0 Interrupt Asserted</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The PWM generator 0 block interrupt has not been asserted.</td>
</tr>
<tr>
<td>1</td>
<td>The PWM generator 0 block interrupt is asserted.</td>
</tr>
</tbody>
</table>

The **PWM0RIS** register shows the source of this interrupt. This bit is cleared by writing a 1 to the corresponding bit in the **PWM0ISC** register.
Register 8: PWM Interrupt Status and Clear (PWMISC), offset 0x01C

This register provides a summary of the interrupt status of the individual PWM generator blocks. If a fault interrupt is set, the corresponding MnFAULTn input has caused an interrupt. For the fault interrupt, a write of 1 to that bit position clears the latched interrupt status. If an block interrupt bit is set, the corresponding generator block is asserting an interrupt. The individual interrupt status registers, PWMnISC, in each block must be consulted to determine the reason for the interrupt and used to clear the interrupt.

### PWM Interrupt Status and Clear (PWMISC)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19</td>
<td>INTFAULT3</td>
<td>RW1C</td>
<td>0</td>
<td>FAULT3 Interrupt Asserted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value: Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The fault condition for PWM generator 3 has not been asserted or is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>not enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: An enabled interrupt for the fault condition for PWM generator 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>is asserted or is latched.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears it and the INTFAULT3 bit in the PWMRIS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>18</td>
<td>INTFAULT2</td>
<td>RW1C</td>
<td>0</td>
<td>FAULT2 Interrupt Asserted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value: Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0: The fault condition for PWM generator 2 has not been asserted or is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>not enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1: An enabled interrupt for the fault condition for PWM generator 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>is asserted or is latched.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears it and the INTFAULT2 bit in the PWMRIS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>17</td>
<td>INTFAULT1</td>
<td>RW1C</td>
<td>0</td>
<td>FAULT1 Interrupt Asserted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears it and the INTFAULT1 bit in the PWMRIS register.</td>
</tr>
<tr>
<td>16</td>
<td>INTFAULT0</td>
<td>RW1C</td>
<td>0</td>
<td>FAULT0 Interrupt Asserted</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writing a 1 to this bit clears it and the INTFAULT0 bit in the PWMRIS register.</td>
</tr>
<tr>
<td>15:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>INTPWM3</td>
<td>RO</td>
<td>0</td>
<td>PWM3 Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The PWM3RIS register shows the source of this interrupt. This bit is cleared by writing a 1 to the corresponding bit in the PWM3ISC register.</td>
</tr>
<tr>
<td>2</td>
<td>INTPWM2</td>
<td>RO</td>
<td>0</td>
<td>PWM2 Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The PWM2RIS register shows the source of this interrupt. This bit is cleared by writing a 1 to the corresponding bit in the PWM2ISC register.</td>
</tr>
<tr>
<td>1</td>
<td>INTPWM1</td>
<td>RO</td>
<td>0</td>
<td>PWM1 Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The PWM1RIS register shows the source of this interrupt. This bit is cleared by writing a 1 to the corresponding bit in the PWM1ISC register.</td>
</tr>
</tbody>
</table>
PWM0 Interrupt Status

Value  Description
0  The PWM generator 0 block interrupt is not asserted or is not enabled.
1  An enabled interrupt for the PWM generator 0 block is asserted.

The PWM0RIS register shows the source of this interrupt. This bit is cleared by writing a 1 to the corresponding bit in the PWM0ISC register.
Register 9: PWM Status (PWMSTATUS), offset 0x020

This register provides the unlatched status of the PWM generator fault condition.

**PWM Status (PWMSTATUS)**
- **PWM0 base:** 0x4002.8000
- **PWM1 base:** 0x4002.9000
- **Offset:** 0x020
- **Type:** RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>FAULT3</td>
<td>RO</td>
<td>0</td>
<td>Generator 3 Fault Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The fault condition for PWM generator 3 is not asserted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The fault condition for PWM generator 3 is asserted. If the <strong>FLTSRC</strong> bit in the <strong>PWM3CTL</strong> register is clear, the input is the source of the fault condition, and is therefore asserted.</td>
</tr>
<tr>
<td>2</td>
<td>FAULT2</td>
<td>RO</td>
<td>0</td>
<td>Generator 2 Fault Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The fault condition for PWM generator 2 is not asserted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The fault condition for PWM generator 2 is asserted. If the <strong>FLTSRC</strong> bit in the <strong>PWM2CTL</strong> register is clear, the input is the source of the fault condition, and is therefore asserted.</td>
</tr>
<tr>
<td>1</td>
<td>FAULT1</td>
<td>RO</td>
<td>0</td>
<td>Generator 1 Fault Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong> Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The fault condition for PWM generator 1 is not asserted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The fault condition for PWM generator 1 is asserted. If the <strong>FLTSRC</strong> bit in the <strong>PWM1CTL</strong> register is clear, the input is the source of the fault condition, and is therefore asserted.</td>
</tr>
</tbody>
</table>
### Pulse Width Modulator (PWM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>FAULT0</td>
<td>RO</td>
<td>0</td>
<td>Generator 0 Fault Status</td>
</tr>
</tbody>
</table>

**Value Description**

- **0**: The fault condition for PWM generator 0 is not asserted.
- **1**: The fault condition for PWM generator 0 is asserted.

If the FLTSRC bit in the PWM0CTL register is clear, the input is the source of the fault condition, and is therefore asserted.
Register 10: PWM Fault Condition Value (PWMFAULTVAL), offset 0x024

This register specifies the output value driven on the MnPWMn signals during a fault condition if enabled by the corresponding bit in the PWMFAULT register. Note that if the corresponding bit in the PWMINVERT register is set, the output value is driven to the logical NOT of the bit value in this register.

PWM Fault Condition Value (PWMFAULTVAL)

<table>
<thead>
<tr>
<th>Base Address</th>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM0: 0x4002.8000</td>
<td>0x024</td>
<td>RO, RW</td>
<td>0x0000.0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>PWM1: 0x4002.9000</td>
<td>0x024</td>
<td>RO, RW</td>
<td>0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

Bit/Field | Name | Type | Description
---|------|------|----------------|
31:8 | reserved | RO, RW | 0x0000.0000 | Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>PWM7</td>
<td>RW</td>
<td>MnPWM7 Fault Value</td>
</tr>
<tr>
<td>6</td>
<td>PWM6</td>
<td>RW</td>
<td>MnPWM6 Fault Value</td>
</tr>
<tr>
<td>5</td>
<td>PWM5</td>
<td>RW</td>
<td>MnPWM5 Fault Value</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
# Pulse Width Modulator (PWM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>PWM4</td>
<td>RW</td>
<td>0</td>
<td>MnPWM4 Fault Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The MnPWM4 output signal is driven Low during fault conditions if the FAULT4 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MnPWM4 output signal is driven High during fault conditions if the FAULT4 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td>3</td>
<td>PWM3</td>
<td>RW</td>
<td>0</td>
<td>MnPWM3 Fault Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The MnPWM3 output signal is driven Low during fault conditions if the FAULT3 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MnPWM3 output signal is driven High during fault conditions if the FAULT3 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td>2</td>
<td>PWM2</td>
<td>RW</td>
<td>0</td>
<td>MnPWM2 Fault Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The MnPWM2 output signal is driven Low during fault conditions if the FAULT2 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MnPWM2 output signal is driven High during fault conditions if the FAULT2 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td>1</td>
<td>PWM1</td>
<td>RW</td>
<td>0</td>
<td>MnPWM1 Fault Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The MnPWM1 output signal is driven Low during fault conditions if the FAULT1 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MnPWM1 output signal is driven High during fault conditions if the FAULT1 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td>0</td>
<td>PWM0</td>
<td>RW</td>
<td>0</td>
<td>MnPWM0 Fault Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The MnPWM0 output signal is driven Low during fault conditions if the FAULT0 bit in the PWMFAULT register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 The MnPWM0 output signal is driven High during fault conditions if the FAULT0 bit in the PWMFAULT register is set.</td>
</tr>
</tbody>
</table>
Register 11: PWM Enable Update (PWMENUPD), offset 0x028

This register specifies when updates to the PWMnEN bit in the PWMENABLE register are performed. The PWMnEN bit enables the pwmA' or pwmB' output to be passed to the microcontroller's pin. Updates can be immediate or locally or globally synchronized to the next synchronous update.

### PWM Enable Update (PWMENUPD)

- **PWM0 base:** 0x4002.8000
- **PWM1 base:** 0x4002.9000
- **Offset:** 0x028
- **Type:** RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:14</td>
<td>RW</td>
<td>0</td>
<td>MnPWM7 Enable Update Mode</td>
</tr>
</tbody>
</table>

#### Value Description

- **0x0** Immediate
  - Writes to the PWM7EN bit in the PWMENABLE register are used by the PWM generator immediately.
- **0x1** Reserved
- **0x2** Locally Synchronized
  - Writes to the PWM7EN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0.
- **0x3** Globally Synchronized
  - Writes to the PWM7EN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0 after a synchronous update has been requested through the PWM Master Control (PWMCTL) register.
### Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13:12</td>
<td>ENUPD6</td>
<td>RW</td>
<td>0</td>
<td>MnPWM6 Enable Update Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Immediate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>Locally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>Globally Synchronized</td>
</tr>
<tr>
<td>11:10</td>
<td>ENUPD5</td>
<td>RW</td>
<td>0</td>
<td>MnPWM5 Enable Update Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Immediate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>Locally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>Globally Synchronized</td>
</tr>
<tr>
<td>9:8</td>
<td>ENUPD4</td>
<td>RW</td>
<td>0</td>
<td>MnPWM4 Enable Update Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>Immediate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>Locally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>Globally Synchronized</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------</td>
</tr>
<tr>
<td>7:6</td>
<td>ENUPD3</td>
<td>RW</td>
<td>0</td>
<td>MnPWM3 Enable Update Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Immediate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWMEN bit in the PWMENABLE register are used by the PWM generator immediately.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 Locally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWMEN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 Globally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWMEN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0 after a synchronous update has been requested through the PWM Master Control (PWMCTL) register.</td>
</tr>
<tr>
<td>5:4</td>
<td>ENUPD2</td>
<td>RW</td>
<td>0</td>
<td>MnPWM2 Enable Update Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Immediate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWM2EN bit in the PWMENABLE register are used by the PWM generator immediately.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 Locally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWM2EN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 Globally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWM2EN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0 after a synchronous update has been requested through the PWM Master Control (PWMCTL) register.</td>
</tr>
<tr>
<td>3:2</td>
<td>ENUPD1</td>
<td>RW</td>
<td>0</td>
<td>MnPWM1 Enable Update Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 Immediate</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWM1EN bit in the PWMENABLE register are used by the PWM generator immediately.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2 Locally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWM1EN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3 Globally Synchronized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Writes to the PWM1EN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0 after a synchronous update has been requested through the PWM Master Control (PWMCTL) register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------</td>
<td>------</td>
<td>-------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>1:0</td>
<td>ENUPD0</td>
<td>RW</td>
<td>0</td>
<td>MnPWM0 Enable Update Mode</td>
</tr>
</tbody>
</table>

**Value Description**

- **0x0 Immediate**
  - Writes to the PWM0EN bit in the PWMENABLE register are used by the PWM generator immediately.

- **0x1 Reserved**

- **0x2 Locally Synchronized**
  - Writes to the PWM0EN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0.

- **0x3 Globally Synchronized**
  - Writes to the PWM0EN bit in the PWMENABLE register are used by the PWM generator the next time the counter is 0 after a synchronous update has been requested through the PWM Master Control (PWMCTL) register.
Register 12: PWM0 Control (PWM0CTL), offset 0x040
Register 13: PWM1 Control (PWM1CTL), offset 0x080
Register 14: PWM2 Control (PWM2CTL), offset 0x0C0
Register 15: PWM3 Control (PWM3CTL), offset 0x100

These registers configure the PWM signal generation blocks (PWM0CTL controls the PWM generator 0 block, and so on). The Register Update mode, Debug mode, Counting mode, and Block Enable mode are all controlled via these registers. The blocks produce the PWM signals, which can be either two independent PWM signals (from the same counter), or a paired set of PWM signals with dead-band delays added.

The PWM0 block produces the MnPWM0 and MnPWM1 outputs, the PWM1 block produces the MnPWM2 and MnPWM3 outputs, the PWM2 block produces the MnPWM4 and MnPWM5 outputs, and the PWM3 block produces the MnPWM6 and MnPWM7 outputs.

PWMn Control (PWMnCTL)
PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x040
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:19</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>18</td>
<td>LATCH</td>
<td>RW</td>
<td>0</td>
<td>Latch Fault Input</td>
</tr>
</tbody>
</table>

Value Description

0  Fault Condition Not Latched
   A fault condition is in effect for as long as the generating source is asserting.

1  Fault Condition Latched
   A fault condition is set as the result of the assertion of the faulting source and is held (latched) while the PWMISC INTFAULTn bit is set. Clearing the INTFAULTn bit clears the fault condition.

Note: When using an ADC digital comparator as a fault source, the LATCH and MINFLTPER bits in the PWMnCTL register should be set to 1 to ensure trigger assertions are captured.
Minimum Fault Period

This bit specifies that the PWM generator enables a one-shot counter to provide a minimum fault condition period.

The timer begins counting on the rising edge of the fault condition to extend the condition for a minimum duration of the count value. The timer ignores the state of the fault condition while counting.

The minimum fault delay is in effect only when the MINFLTPER bit is set. If a detected fault is in the process of being extended when the MINFLTPER bit is cleared, the fault condition extension is aborted.

The delay time is specified by the PWMnMINFLTPER register MFP field value. The effect of this is to pulse stretch the fault condition input.

The delay value is defined by the PWM clock period. Because the fault input is not synchronized to the PWM clock, the period of the time is PWMClock * (MFP value + 1) or PWMClock * (MFP value + 2).

The delay function makes sense only if the fault source is unlatched. A latched fault source makes the fault condition appear asserted until cleared by software and negates the utility of the extend feature. It applies to all fault condition sources as specified in the FLTSRC field.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The FAULT input deassertion is unaffected.</td>
</tr>
<tr>
<td>1</td>
<td>The PWMnMINFLTPER one-shot counter is active and extends the period of the fault condition to a minimum period.</td>
</tr>
</tbody>
</table>

**Note:** When using an ADC digital comparator as a fault source, the LATCH and MINFLTPER bits in the PWMnCTL register should be set to 1 to ensure trigger assertions are captured.

Fault Condition Source

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The Fault condition is determined by the Fault0 input.</td>
</tr>
<tr>
<td>1</td>
<td>The Fault condition is determined by the configuration of the PWMnFLTSRC0 and PWMnFLTSRC1 registers.</td>
</tr>
</tbody>
</table>

PWMnDBFALL Update Mode

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Immediate</td>
</tr>
<tr>
<td></td>
<td>The PWMnDBFALL register value is immediately updated on a write.</td>
</tr>
<tr>
<td>0x1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x2</td>
<td>Locally Synchronized</td>
</tr>
<tr>
<td></td>
<td>Updates to the register are reflected to the generator the next time the counter is 0.</td>
</tr>
<tr>
<td>0x3</td>
<td>Globally Synchronized</td>
</tr>
<tr>
<td></td>
<td>Updates to the register are delayed until the next time the counter is 0 after a synchronous update has been requested through the PWMCTL register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>-----------</td>
<td>-------------</td>
</tr>
<tr>
<td>13:12</td>
<td>DBRISEUPD</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>11:10</td>
<td>DBCTLUPD</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>9:8</td>
<td>GENBUPD</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### PWMnGENA Update Mode

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Immediate</td>
<td>0x0</td>
<td>The PWMnGENA register value is immediately updated on a write.</td>
</tr>
<tr>
<td>Reserved</td>
<td>0x1</td>
<td></td>
</tr>
<tr>
<td>Locally Synchronized</td>
<td>0x2</td>
<td>Updates to the register are reflected to the generator the next time the counter is 0.</td>
</tr>
<tr>
<td>Globally Synchronized</td>
<td>0x3</td>
<td>Updates to the register are delayed until the next time the counter is 0 after a synchronous update has been requested through the PWMCTL register.</td>
</tr>
</tbody>
</table>

#### Comparator B Update Mode

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Locally Synchronized</td>
<td>0</td>
<td>Updates to the PWMnCMPB register are reflected to the generator the next time the counter is 0.</td>
</tr>
<tr>
<td>Globally Synchronized</td>
<td>1</td>
<td>Updates to the register are delayed until the next time the counter is 0 after a synchronous update has been requested through the PWMCTL register.</td>
</tr>
</tbody>
</table>

#### Comparator A Update Mode

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Locally Synchronized</td>
<td>0</td>
<td>Updates to the PWMnCMPA register are reflected to the generator the next time the counter is 0.</td>
</tr>
<tr>
<td>Globally Synchronized</td>
<td>1</td>
<td>Updates to the register are delayed until the next time the counter is 0 after a synchronous update has been requested through the PWMCTL register.</td>
</tr>
</tbody>
</table>

#### Load Register Update Mode

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Locally Synchronized</td>
<td>0</td>
<td>Updates to the PWMnLOAD register are reflected to the generator the next time the counter is 0.</td>
</tr>
<tr>
<td>Globally Synchronized</td>
<td>1</td>
<td>Updates to the register are delayed until the next time the counter is 0 after a synchronous update has been requested through the PWMCTL register.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
</tr>
<tr>
<td>----------</td>
<td>--------</td>
<td>------</td>
</tr>
<tr>
<td>2</td>
<td>DEBUG</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>MODE</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>ENABLE</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 16: PWM0 Interrupt and Trigger Enable (PWM0INTEN), offset 0x044
Register 17: PWM1 Interrupt and Trigger Enable (PWM1INTEN), offset 0x084
Register 18: PWM2 Interrupt and Trigger Enable (PWM2INTEN), offset 0x0C4
Register 19: PWM3 Interrupt and Trigger Enable (PWM3INTEN), offset 0x104

These registers control the interrupt and ADC trigger generation capabilities of the PWM generators (PWM0INTEN controls the PWM generator 0 block, and so on). The events that can cause an interrupt, or an ADC trigger are:

- The counter being equal to the load register
- The counter being equal to zero
- The counter being equal to the PWMnCMPA register while counting up
- The counter being equal to the PWMnCMPA register while counting down
- The counter being equal to the PWMnCMPB register while counting up
- The counter being equal to the PWMnCMPB register while counting down

Any combination of these events can generate either an interrupt or an ADC trigger, though no determination can be made as to the actual event that caused an ADC trigger if more than one is specified. The PWMnRIS register provides information about which events have caused raw interrupts.

Pulse Width Modulator (PWM)

PWMn Interrupt and Trigger Enable (PWMnINTEN)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:14</td>
<td>reserved</td>
<td>RO</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>TRCMPBD</td>
<td>RW</td>
<td>Trigger for Counter=PWMnCMPB Down</td>
</tr>
</tbody>
</table>

Value Description

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No ADC trigger is output.</td>
</tr>
<tr>
<td>1</td>
<td>An ADC trigger pulse is output when the counter matches the value in the PWMnCMPB register value while counting down.</td>
</tr>
</tbody>
</table>
### Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>TRCMPBU</td>
<td>RW</td>
<td>0</td>
<td>Trigger for Counter=PWMnCMPB Up</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No ADC trigger is output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An ADC trigger pulse is output when the counter matches the value in the PWMnCMPB register value while counting up.</td>
</tr>
<tr>
<td>11</td>
<td>TRCMPAD</td>
<td>RW</td>
<td>0</td>
<td>Trigger for Counter=PWMnCMPA Down</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No ADC trigger is output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An ADC trigger pulse is output when the counter matches the value in the PWMnCMPA register value while counting down.</td>
</tr>
<tr>
<td>10</td>
<td>TRCMPAU</td>
<td>RW</td>
<td>0</td>
<td>Trigger for Counter=PWMnCMPA Up</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No ADC trigger is output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An ADC trigger pulse is output when the counter matches the value in the PWMnCMPA register value while counting up.</td>
</tr>
<tr>
<td>9</td>
<td>TRCNTLOAD</td>
<td>RW</td>
<td>0</td>
<td>Trigger for Counter=PWMnLOAD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No ADC trigger is output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An ADC trigger pulse is output when the counter matches the PWMnLOAD register.</td>
</tr>
<tr>
<td>8</td>
<td>TRCNTZERO</td>
<td>RW</td>
<td>0</td>
<td>Trigger for Counter=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No ADC trigger is output.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An ADC trigger pulse is output when the counter is 0.</td>
</tr>
<tr>
<td>7:6</td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>INTCMPBD</td>
<td>RW</td>
<td>0</td>
<td>Interrupt for Counter=PWMnCMPB Down</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  A raw interrupt occurs when the counter matches the value in the PWMnCMPB register value while counting down.</td>
</tr>
</tbody>
</table>
## Pulse Width Modulator (PWM)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>INTCMPBU</td>
<td>RW</td>
<td>0</td>
<td>Interrupt for Counter=PWMnCMPB Up</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   A raw interrupt occurs when the counter matches the value in the PWMnCMPB register value while counting up.</td>
</tr>
<tr>
<td>3</td>
<td>INTCMPAD</td>
<td>RW</td>
<td>0</td>
<td>Interrupt for Counter=PWMnCMPA Down</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   A raw interrupt occurs when the counter matches the value in the PWMnCMPA register value while counting down.</td>
</tr>
<tr>
<td>2</td>
<td>INTCMPAU</td>
<td>RW</td>
<td>0</td>
<td>Interrupt for Counter=PWMnCMPA Up</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   A raw interrupt occurs when the counter matches the value in the PWMnCMPA register value while counting up.</td>
</tr>
<tr>
<td>1</td>
<td>INTCNTLOAD</td>
<td>RW</td>
<td>0</td>
<td>Interrupt for Counter=PWMnLOAD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   A raw interrupt occurs when the counter matches the value in the PWMnLOAD register value.</td>
</tr>
<tr>
<td>0</td>
<td>INTCNTZERO</td>
<td>RW</td>
<td>0</td>
<td>Interrupt for Counter=0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0   No interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1   A raw interrupt occurs when the counter is zero.</td>
</tr>
</tbody>
</table>
Register 20: PWM0 Raw Interrupt Status (PWM0RIS), offset 0x048
Register 21: PWM1 Raw Interrupt Status (PWM1RIS), offset 0x088
Register 22: PWM2 Raw Interrupt Status (PWM2RIS), offset 0x0C8
Register 23: PWM3 Raw Interrupt Status (PWM3RIS), offset 0x108

These registers provide the current set of interrupt sources that are asserted, regardless of whether they cause an interrupt to be asserted to the controller (PWM0RIS controls the PWM generator 0 block, and so on). If a bit is set, the event has occurred; if a bit is clear, the event has not occurred. Bits in this register are cleared by writing a 1 to the corresponding bit in the PWMnISC register.

### PWMn Raw Interrupt Status (PWMnRIS)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>INTCMPBD</td>
<td>RO</td>
<td>0</td>
<td>Comparator B Down Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>An interrupt has not occurred.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The counter has matched the value in the PWMnCMPB register while counting down.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to the INTCMPBD bit in the PWMnISC register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>INTCMPBU</td>
<td>RO</td>
<td>0</td>
<td>Comparator B Up Interrupt Status</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>An interrupt has not occurred.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The counter has matched the value in the PWMnCMPB register while counting up.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>This bit is cleared by writing a 1 to the INTCMPBU bit in the PWMnISC register.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------------</td>
<td>------</td>
<td>-------</td>
<td>-------------</td>
</tr>
<tr>
<td>3</td>
<td>INTCMPAD</td>
<td>RO</td>
<td>0</td>
<td>Comparator A Down Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the INTCMPAD bit in the PWMnISC register.</td>
</tr>
<tr>
<td>2</td>
<td>INTCMPAU</td>
<td>RO</td>
<td>0</td>
<td>Comparator A Up Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the INTCMPAU bit in the PWMnISC register.</td>
</tr>
<tr>
<td>1</td>
<td>INTCNTLOAD</td>
<td>RO</td>
<td>0</td>
<td>Counter=Load Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the INTCNTLOAD bit in the PWMnISC register.</td>
</tr>
<tr>
<td>0</td>
<td>INTCNTZERO</td>
<td>RO</td>
<td>0</td>
<td>Counter=0 Interrupt Status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This bit is cleared by writing a 1 to the INTCNTZERO bit in the PWMnISC register.</td>
</tr>
</tbody>
</table>
Register 24: PWM0 Interrupt Status and Clear (PWM0ISC), offset 0x04C
Register 25: PWM1 Interrupt Status and Clear (PWM1ISC), offset 0x08C
Register 26: PWM2 Interrupt Status and Clear (PWM2ISC), offset 0x0CC
Register 27: PWM3 Interrupt Status and Clear (PWM3ISC), offset 0x10C

These registers provide the current set of interrupt sources that are asserted to the interrupt controller (PWM0ISC controls the PWM generator 0 block, and so on). A bit is set if the event has occurred and is enabled in the PWMnINTEN register; if a bit is clear, the event has not occurred or is not enabled. These are RW1C registers; writing a 1 to a bit position clears the corresponding interrupt reason.

**Note:** The interrupt status can only be cleared one PWM Clock cycle after the interrupt occurs. The larger the PWM Clock Divider (PWMDIV) value in PWMCC register, the longer the system delay is to clear the interrupt.

PWMn Interrupt Status and Clear (PWMnISC)

<table>
<thead>
<tr>
<th>Offset 0x04C</th>
<th>Type RW1C, reset 0x0000.0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:6</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>5</td>
<td>INTCMPBD</td>
<td>RW1C</td>
<td>0</td>
<td>Comparator B Down Interrupt</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No interrupt has occurred or the interrupt is masked.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The INTCMPBD bits in the PWMnRIS and PWMnINTEN registers are set, providing an interrupt to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1. Clearing this bit also clears the INTCMPBD bit in the PWMnRIS register.

| 4           | INTCMPBU        | RW1C | 0     | Comparator B Up Interrupt |
|             | Value | Description |
| 0           | No interrupt has occurred or the interrupt is masked. |
| 1           | The INTCMPBU bits in the PWMnRIS and PWMnINTEN registers are set, providing an interrupt to the interrupt controller. |

This bit is cleared by writing a 1. Clearing this bit also clears the INTCMPBU bit in the PWMnRIS register.
## Description

The PWMnRIS and PWMnINTEN registers are set, providing an interrupt to the interrupt controller. This bit is cleared by writing a 1. Clearing this bit also clears the INTCMPAD bit in the PWMnRIS register.

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>INTCMPAD</td>
<td>RW1C</td>
<td>0</td>
<td>Comparator A Down Interrupt&lt;br&gt;Value Description&lt;br&gt;0 No interrupt has occurred or the interrupt is masked.&lt;br&gt;1 The INTCMPAD bits in the PWMnRIS and PWMnINTEN registers are set, providing an interrupt to the interrupt controller. This bit is cleared by writing a 1. Clearing this bit also clears the INTCMPAD bit in the PWMnRIS register.</td>
</tr>
<tr>
<td>2</td>
<td>INTCMPAU</td>
<td>RW1C</td>
<td>0</td>
<td>Comparator A Up Interrupt&lt;br&gt;Value Description&lt;br&gt;0 No interrupt has occurred or the interrupt is masked.&lt;br&gt;1 The INTCMPAU bits in the PWMnRIS and PWMnINTEN registers are set, providing an interrupt to the interrupt controller. This bit is cleared by writing a 1. Clearing this bit also clears the INTCMPAU bit in the PWMnRIS register.</td>
</tr>
<tr>
<td>1</td>
<td>INTCNTLOAD</td>
<td>RW1C</td>
<td>0</td>
<td>Counter=Load Interrupt&lt;br&gt;Value Description&lt;br&gt;0 No interrupt has occurred or the interrupt is masked.&lt;br&gt;1 The INTCNTLOAD bits in the PWMnRIS and PWMnINTEN registers are set, providing an interrupt to the interrupt controller. This bit is cleared by writing a 1. Clearing this bit also clears the INTCNTLOAD bit in the PWMnRIS register.</td>
</tr>
<tr>
<td>0</td>
<td>INTCNTZERO</td>
<td>RW1C</td>
<td>0</td>
<td>Counter=0 Interrupt&lt;br&gt;Value Description&lt;br&gt;0 No interrupt has occurred or the interrupt is masked.&lt;br&gt;1 The INTCNTZERO bits in the PWMnRIS and PWMnINTEN registers are set, providing an interrupt to the interrupt controller. This bit is cleared by writing a 1. Clearing this bit also clears the INTCNTZERO bit in the PWMnRIS register.</td>
</tr>
</tbody>
</table>
Register 28: PWM0 Load (PWM0LOAD), offset 0x050
Register 29: PWM1 Load (PWM1LOAD), offset 0x090
Register 30: PWM2 Load (PWM2LOAD), offset 0x0D0
Register 31: PWM3 Load (PWM3LOAD), offset 0x110

These registers contain the load value for the PWM counter (PWM0LOAD controls the PWM generator 0 block, and so on). Based on the counter mode configured by the MODE bit in the PWMnCTL register, this value is either loaded into the counter after it reaches zero or is the limit of up-counting after which the counter decrements back to zero. When this value matches the counter, a pulse is output which can be configured to drive the generation of the pwmA and/or pwmB signal (via the PWMnGENA/PWMnGENB register) or drive an interruptor ADC trigger (via the PWMnINTEN register).

If the Load Value Update mode is locally synchronized (based on the LOADUPD field encoding in the PWMnCTL register), the 16-bit LOAD value is used the next time the counter reaches zero. If the update mode is globally synchronized, it is used the next time the counter reaches zero after a synchronous update has been requested through the PWM Master Control (PWMCTL) register (see page 1266). If this register is re-written before the actual update occurs, the previous value is never used and is lost.

---

**PWMn Load (PWMnLOAD)**

- **PWM0 base**: 0x4002.8000
- **PWM1 base**: 0x4002.9000
- **Offset**: 0x050
- **Type**: RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>LOAD</td>
<td>RW</td>
<td>0x0000</td>
<td>Counter Load Value</td>
</tr>
</tbody>
</table>

The counter load value.
Register 32: PWM0 Counter (PWM0COUNT), offset 0x054
Register 33: PWM1 Counter (PWM1COUNT), offset 0x094
Register 34: PWM2 Counter (PWM2COUNT), offset 0x0D4
Register 35: PWM3 Counter (PWM3COUNT), offset 0x114

These registers contain the current value of the PWM counter (PWM0COUNT is the value of the PWM generator 0 block, and so on). When this value matches zero or the value in the PWMnLOAD, PWMnCMPA, or PWMnCMPB registers, a pulse is output which can be configured to drive the generation of a PWM signal or drive an interrupt or ADC trigger.

**Note:** Disabling the PWM by clearing the **ENABLE** bit does not clear the **COUNT** field of the PWMnCOUNT register. Before re-enabling the PWM (ENABLE = 0x1), the **COUNT** field should be cleared by resetting the PWM registers through the SRPWM register in the System Control Module.

### PWMn Counter (PWMnCOUNT)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>COUNT</td>
<td>RO</td>
<td>0x0000</td>
<td>Counter Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The current value of the counter.</td>
</tr>
</tbody>
</table>

PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x054
Type RO, reset 0x0000.0000
Register 36: PWM0 Compare A (PWM0CMPA), offset 0x058
Register 37: PWM1 Compare A (PWM1CMPA), offset 0x098
Register 38: PWM2 Compare A (PWM2CMPA), offset 0x0D8
Register 39: PWM3 Compare A (PWM3CMPA), offset 0x118

These registers contain a value to be compared against the counter (PWM0CMPA controls the PWM generator 0 block, and so on). When this value matches the counter, a pulse is output which can be configured to drive the generation of the pwmA and pwmB signals (via the PWMnGENA and PWMnGENB registers) or drive an interrupt or ADC trigger (via the PWMnINTEN register). If the value of this register is greater than the PWMnLOAD register (see page 1303), then no pulse is ever output.

If the comparator A update mode is locally synchronized (based on the CMPAUPD bit in the PWMnCTL register), the 16-bit COMPA value is used the next time the counter reaches zero. If the update mode is globally synchronized, it is used the next time the counter reaches zero after a synchronous update has been requested through the PWM Master Control (PWMCTL) register (see page 1266). If this register is rewritten before the actual update occurs, the previous value is never used and is lost.

PWMn Compare A (PWMnCMPA)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>15:0</td>
<td>COMPA</td>
<td>RW</td>
<td>0x00</td>
<td>Comparator A Value</td>
</tr>
</tbody>
</table>

The value to be compared against the counter.
Register 40: PWM0 Compare B (PWM0CMPB), offset 0x05C
Register 41: PWM1 Compare B (PWM1CMPB), offset 0x09C
Register 42: PWM2 Compare B (PWM2CMPB), offset 0x0DC
Register 43: PWM3 Compare B (PWM3CMPB), offset 0x11C

These registers contain a value to be compared against the counter (PWM0CMPB controls the PWM generator 0 block, and so on). When this value matches the counter, a pulse is output which can be configured to drive the generation of the pwmA and pwmB signals (via the PWMnGENA and PWMnGENB registers) or drive an interrupt or ADC trigger (via the PWMnINTEN register). If the value of this register is greater than the PWMnLOAD register, no pulse is ever output.

If the comparator B update mode is locally synchronized (based on the CMPBUPD bit in the PWMnCTL register), the 16-bit COMPB value is used the next time the counter reaches zero. If the update mode is globally synchronized, it is used the next time the counter reaches zero after a synchronous update has been requested through the PWM Master Control (PWMCTL) register (see page 1266). If this register is rewritten before the actual update occurs, the previous value is never used and is lost.

PWNm Compare B (PWMnCMPB)
PWN0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x05C
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 15:0      | COMPB  | RW   | 0x0000 | Comparator B Value
The value to be compared against the counter. |
Register 44: PWM0 Generator A Control (PWM0GENA), offset 0x060
Register 45: PWM1 Generator A Control (PWM1GENA), offset 0x0A0
Register 46: PWM2 Generator A Control (PWM2GENA), offset 0x0E0
Register 47: PWM3 Generator A Control (PWM3GENA), offset 0x120

These registers control the generation of the pwmA signal based on the load and zero output pulses from the counter, as well as the compare A and compare B pulses from the comparators (PWM0GENA controls the PWM generator 0 block, and so on). When the counter is running in Count-Down mode, only four of these events occur; when running in Count-Up/Down mode, all six occur. These events provide great flexibility in the positioning and duty cycle of the resulting PWM signal.

The PWM0GENA register controls generation of the pwm0A signal; PWM1GENA, the pwm1A signal; PWM2GENA, the pwm2A signal; and PWM3GENA, the pwm3A signal.

If a zero or load event coincides with a compare A or compare B event, the zero or load action is taken and the compare A or compare B action is ignored. If a compare A event coincides with a compare B event, the compare A action is taken and the compare B action is ignored.

If the Generator A update mode is immediate (based on the GENAUPD field encoding in the PWMnCTL register), the ACTCMPBD, ACTCMPBU, ACTCMPAD, ACTMPAU, ACTLOAD, and ACTZERO values are used immediately. If the update mode is locally synchronized, these values are used the next time the counter reaches zero. If the update mode is globally synchronized, these values are used the next time the counter reaches zero after a synchronous update has been requested through the PWM Master Control (PWMCTL) register (see page 1266). If this register is rewritten before the actual update occurs, the previous value is never used and is lost.

### PWMMn Generator A Control (PWMMnGENA)

<table>
<thead>
<tr>
<th>Field</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
### Description

This field specifies the action to be taken when the counter matches comparator **B** while counting **down**.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Do nothing.</td>
<td>0x0</td>
</tr>
<tr>
<td>Invert pwmA.</td>
<td>0x1</td>
</tr>
<tr>
<td>Drive pwmA Low.</td>
<td>0x2</td>
</tr>
<tr>
<td>Drive pwmA High.</td>
<td>0x3</td>
</tr>
</tbody>
</table>

### Description

This field specifies the action to be taken when the counter matches comparator **B** while counting **up**. This action can only occur when the **MODE** bit in the **PWMctl** register is set.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Do nothing.</td>
<td>0x0</td>
</tr>
<tr>
<td>Invert pwmA.</td>
<td>0x1</td>
</tr>
<tr>
<td>Drive pwmA Low.</td>
<td>0x2</td>
</tr>
<tr>
<td>Drive pwmA High.</td>
<td>0x3</td>
</tr>
</tbody>
</table>

### Description

This field specifies the action to be taken when the counter matches comparator **A** while counting **down**.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Do nothing.</td>
<td>0x0</td>
</tr>
<tr>
<td>Invert pwmA.</td>
<td>0x1</td>
</tr>
<tr>
<td>Drive pwmA Low.</td>
<td>0x2</td>
</tr>
<tr>
<td>Drive pwmA High.</td>
<td>0x3</td>
</tr>
</tbody>
</table>

### Description

This field specifies the action to be taken when the counter matches comparator **A** while counting **up**. This action can only occur when the **MODE** bit in the **PWMctl** register is set.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Do nothing.</td>
<td>0x0</td>
</tr>
<tr>
<td>Invert pwmA.</td>
<td>0x1</td>
</tr>
<tr>
<td>Drive pwmA Low.</td>
<td>0x2</td>
</tr>
<tr>
<td>Drive pwmA High.</td>
<td>0x3</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
</tr>
<tr>
<td>3:2</td>
<td>ACTLOAD</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>1:0</td>
<td>ACTZERO</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Register 48: PWM0 Generator B Control (PWM0GENB), offset 0x064
Register 49: PWM1 Generator B Control (PWM1GENB), offset 0x0A4
Register 50: PWM2 Generator B Control (PWM2GENB), offset 0x0E4
Register 51: PWM3 Generator B Control (PWM3GENB), offset 0x124

These registers control the generation of the pwmB signal based on the load and zero output pulses from the counter, as well as the compare A and compare B pulses from the comparators (PWM0GENB controls the PWM generator 0 block, and so on). When the counter is running in Count-Down mode, only four of these events occur; when running in Count-Up/Down mode, all six occur. These events provide great flexibility in the positioning and duty cycle of the resulting PWM signal.

The PWM0GENB register controls generation of the pwm0B signal; PWM1GENB, the pwm1B signal; PWM2GENB, the pwm2B signal; and PWM3GENB, the pwm3B signal.

If a zero or load event coincides with a compare A or compare B event, the zero or load action is taken and the compare A or compare B action is ignored. If a compare A event coincides with a compare B event, the compare B action is taken and the compare A action is ignored.

If the Generator B update mode is immediate (based on the GENBUPD field encoding in the PWMnCTL register), the ACTCMPBD, ACTCMPBU, ACTCMPAD, ACTMPAU, ACTLOAD, and ACTZERO values are used immediately. If the update mode is locally synchronized, these values are used the next time the counter reaches zero. If the update mode is globally synchronized, these values are used the next time the counter reaches zero after a synchronous update has been requested through the PWM Master Control (PWMCTL) register (see page 1266). If this register is rewritten before the actual update occurs, the previous value is never used and is lost.

PWMn Generator B Control (PWMnGENB), offset 0x064
PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x064
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>------------</td>
<td>------</td>
<td>-------</td>
<td>-----------------------------------</td>
</tr>
<tr>
<td>11:10</td>
<td>ACTCMPBD</td>
<td>RW</td>
<td>0x0</td>
<td>Action for Comparator B Down</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field specifies the action to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>be taken when the counter matches</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>comparator B while counting down.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0  Do nothing.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1  Invert pwmB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2  Drive pwmB Low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3  Drive pwmB High.</td>
</tr>
<tr>
<td>9:8</td>
<td>ACTCMPBU</td>
<td>RW</td>
<td>0x0</td>
<td>Action for Comparator B Up</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field specifies the action to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>be taken when the counter matches</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>comparator B while counting up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This action can only occur when</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the MODE bit in the PWMnCTL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0  Do nothing.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1  Invert pwmB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2  Drive pwmB Low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3  Drive pwmB High.</td>
</tr>
<tr>
<td>7:6</td>
<td>ACTCMPAD</td>
<td>RW</td>
<td>0x0</td>
<td>Action for Comparator A Down</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field specifies the action</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>to be taken when the counter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>matches comparator A while</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>counting down.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0  Do nothing.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1  Invert pwmB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2  Drive pwmB Low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3  Drive pwmB High.</td>
</tr>
<tr>
<td>5:4</td>
<td>ACTCMPAU</td>
<td>RW</td>
<td>0x0</td>
<td>Action for Comparator A Up</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field specifies the action</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>to be taken when the counter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>matches comparator A while</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>counting up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This action can only occur when</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the MODE bit in the PWMnCTL</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is set.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0  Do nothing.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x1  Invert pwmB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x2  Drive pwmB Low.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x3  Drive pwmB High.</td>
</tr>
</tbody>
</table>
### Description

**Description of the action to be taken when the counter matches the load value.**

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Do nothing.</td>
<td>0x0</td>
</tr>
<tr>
<td>Invert pwmB.</td>
<td>0x1</td>
</tr>
<tr>
<td>Drive pwmB Low.</td>
<td>0x2</td>
</tr>
<tr>
<td>Drive pwmB High.</td>
<td>0x3</td>
</tr>
</tbody>
</table>

### Description of the action to be taken when the counter is 0.

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Do nothing.</td>
<td>0x0</td>
</tr>
<tr>
<td>Invert pwmB.</td>
<td>0x1</td>
</tr>
<tr>
<td>Drive pwmB Low.</td>
<td>0x2</td>
</tr>
<tr>
<td>Drive pwmB High.</td>
<td>0x3</td>
</tr>
</tbody>
</table>

---

**Bit/Field**  | **Name**  | **Type** | **Reset** | **Description**
--- | --- | --- | --- | ---
3:2 | ACTLOAD | RW | 0x0 | Action for Counter=LOAD

This field specifies the action to be taken when the counter matches the load value.

Value Description
---
0x0 Do nothing.
0x1 Invert pwmB.
0x2 Drive pwmB Low.
0x3 Drive pwmB High.

---

1:0 | ACTZERO | RW | 0x0 | Action for Counter=0

This field specifies the action to be taken when the counter is 0.

Value Description
---
0x0 Do nothing.
0x1 Invert pwmB.
0x2 Drive pwmB Low.
0x3 Drive pwmB High.
Register 52: PWM0 Dead-Band Control (PWM0DBCTL), offset 0x068
Register 53: PWM1 Dead-Band Control (PWM1DBCTL), offset 0x0A8
Register 54: PWM2 Dead-Band Control (PWM2DBCTL), offset 0x0E8
Register 55: PWM3 Dead-Band Control (PWM3DBCTL), offset 0x128

The PWMnDBCTL register controls the dead-band generator, which produces the MnPWMn signals based on the pwmA and pwmB signals. When disabled, the pwmA signal passes through to the pwmA' signal and the pwmB signal passes through to the pwmB' signal. When dead-band control is enabled, the pwmB signal is ignored, the pwmA' signal is generated by delaying the rising edge(s) of the pwmA signal by the value in the PWMnDBRISE register (see page 1314), and the pwmB' signal is generated by inverting the pwmA signal and delaying the falling edge(s) of the pwmA signal by the value in the PWMnDBFALL register (see page 1315). The Output Control block outputs the pwm0A' signal on the MnPWM0 signal and the pwm0B' signal on the MnPWM1 signal. In a similar manner, MnPWM2 and MnPWM3 are produced from the pwm1A' and pwm1B' signals, MnPWM4 and MnPWM5 are produced from the pwm2A' and pwm2B' signals, and MnPWM6 and MnPWM7 are produced from the pwm3A' and pwm3B' signals.

If the Dead-Band Control mode is immediate (based on the DBCTLUPD field encoding in the PWMnCTL register), the ENABLE bit value is used immediately. If the update mode is locally synchronized, this value is used the next time the counter reaches zero. If the update mode is globally synchronized, this value is used the next time the counter reaches zero after a synchronous update has been requested through the PWM Master Control (PWMCTL) register (see page 1266). If this register is rewritten before the actual update occurs, the previous value is never used and is lost.

PWMn Dead-Band Control (PWMnDBCTL)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:1</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>0</td>
<td>ENABLE</td>
<td>RW</td>
<td>0</td>
<td>Dead-Band Generator Enable</td>
</tr>
<tr>
<td></td>
<td>Value</td>
<td></td>
<td></td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>The pwmA and pwmB signals pass through to the pwmA' and pwmB' signals unmodified.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>The dead-band generator modifies the pwmA signal by inserting dead bands into the pwmA' and pwmB' signals.</td>
</tr>
</tbody>
</table>
Register 56: PWM0 Dead-Band Rising-Edge Delay (PWM0DBRISE), offset 0x06C

Register 57: PWM1 Dead-Band Rising-Edge Delay (PWM1DBRISE), offset 0x0AC

Register 58: PWM2 Dead-Band Rising-Edge Delay (PWM2DBRISE), offset 0x0EC

Register 59: PWM3 Dead-Band Rising-Edge Delay (PWM3DBRISE), offset 0x12C

The PWMnDBRISE register contains the number of clock cycles to delay the rising edge of the pwmA signal when generating the pwmA' signal. If the dead-band generator is disabled through the PWMnDBCTL register, this register is ignored. If the value of this register is larger than the width of a High pulse on the pwmA signal, the rising-edge delay consumes the entire High time of the signal, resulting in no High time on the output. Care must be taken to ensure that the pwmA High time always exceeds the rising-edge delay.

If the Dead-Band Rising-Edge Delay mode is immediate (based on the DBRISEUPD field encoding in the PWMnCTL register), the 12-bit RISEDELAY value is used immediately. If the update mode is locally synchronized, this value is used the next time the counter reaches zero. If the update mode is globally synchronized, this value is used the next time the counter reaches zero after a synchronous update has been requested through the PWM Master Control (PWMCTL) register (see page 1266). If this register is rewritten before the actual update occurs, the previous value is never used and is lost.

### PWMn Dead-Band Rising-Edge Delay (PWMnDBRISE)

- **PWM0 base:** 0x4002.8000
- **PWM1 base:** 0x4002.9000
- **Offset:** 0x06C
- **Type:** RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11:0</td>
<td>RISEDELAY</td>
<td>RW</td>
<td>0x000</td>
<td>Dead-Band Rise Delay</td>
</tr>
</tbody>
</table>

The number of clock cycles to delay the rising edge of pwmA' after the rising edge of pwmA.
Register 60: PWM0 Dead-Band Falling-Edge-Delay (PWM0DBFALL), offset 0x070

Register 61: PWM1 Dead-Band Falling-Edge-Delay (PWM1DBFALL), offset 0x0B0

Register 62: PWM2 Dead-Band Falling-Edge-Delay (PWM2DBFALL), offset 0x0F0

Register 63: PWM3 Dead-Band Falling-Edge-Delay (PWM3DBFALL), offset 0x130

The PWMnDBFALL register contains the number of clock cycles to delay the rising edge of the pwmB signal from the falling edge of the pwmA signal. If the dead-band generator is disabled through the PWMnDBCTL register, this register is ignored. If the value of this register is larger than the width of a Low pulse on the pwmA signal, the falling-edge delay consumes the entire Low time of the signal, resulting in no Low time on the output. Care must be taken to ensure that the pwmA Low time always exceeds the falling-edge delay.

If the Dead-Band Falling-Edge-Delay mode is immediate (based on the DBFALLUP field encoding in the PWMnCTL register), the 12-bit FALLDELAY value is used immediately. If the update mode is locally synchronized, this value is used the next time the counter reaches zero. If the update mode is globally synchronized, this value is used the next time the counter reaches zero after a synchronous update has been requested through the PWM Master Control (PWMCTL) register (see page 1266). If this register is rewritten before the actual update occurs, the previous value is never used and is lost.

PWMn Dead-Band Falling-Edge-Delay (PWMnDBFALL)
PWM base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x070
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:12</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000</td>
<td>Software should not rely on the value of a reserved bit. To provide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>.0000</td>
<td>compatibility with future products, the value of a reserved bit should be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>11:0</td>
<td>FALLDELAY</td>
<td>RW</td>
<td>0x0000</td>
<td>Dead-Band Fall Delay</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The number of clock cycles to delay the falling edge of pwmB from the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>rising edge of pwmA.</td>
</tr>
</tbody>
</table>
Register 64: PWM0 Fault Source 0 (PWM0FLTSRC0), offset 0x074
Register 65: PWM1 Fault Source 0 (PWM1FLTSRC0), offset 0x0B4
Register 66: PWM2 Fault Source 0 (PWM2FLTSRC0), offset 0x0F4
Register 67: PWM3 Fault Source 0 (PWM3FLTSRC0), offset 0x134

This register specifies which fault pin inputs are used to generate a fault condition. Each bit in the following register indicates whether the corresponding fault pin is included in the fault condition. All enabled fault pins are ORed together to form the PWMnFLTSRC0 portion of the fault condition. The PWMnFLTSRC0 fault condition is then ORed with the PWMnFLTSRC1 fault condition to generate the final fault condition for the PWM generator.

If the FLTSRC bit in the PWMnCTL register (see page 1291) is clear, only the Fault0 signal affects the fault condition generated. Otherwise, sources defined in PWMnFLTSRC0 and PWMnFLTSRC1 affect the fault condition generated.

### PWMn Fault Source 0 (PWMnFLTSRC0)

**PWM0 base:** 0x4002.8000  
**PWM1 base:** 0x4002.9000  
**Offset:** 0x074  
**Type:** RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>FAULT3</td>
<td>RW</td>
<td>0</td>
<td>Fault3 Input</td>
</tr>
</tbody>
</table>

**Value Description**

- 0: The Fault3 signal is suppressed and cannot generate a fault condition.
- 1: The Fault3 signal value is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).

**Note:** The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>FAULT2</strong> Input</td>
</tr>
<tr>
<td>2</td>
<td>FAULT2</td>
<td>RW</td>
<td>0</td>
<td>The Fault2 signal is suppressed and cannot</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>generate a fault condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The Fault2 signal value is ORed with all</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>other fault condition generation inputs (Faultn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>signals and digital comparators).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The FLTSRC bit in the PWMnCTL register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>must be set for this bit to affect fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>condition generation.</td>
</tr>
<tr>
<td>1</td>
<td>FAULT1</td>
<td>RW</td>
<td>0</td>
<td>The Fault1 signal is suppressed and cannot</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>generate a fault condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The Fault1 signal value is ORed with all</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>other fault condition generation inputs (Faultn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>signals and digital comparators).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The FLTSRC bit in the PWMnCTL register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>must be set for this bit to affect fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>condition generation.</td>
</tr>
<tr>
<td>0</td>
<td>FAULT0</td>
<td>RW</td>
<td>0</td>
<td>The Fault0 signal is suppressed and cannot</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>generate a fault condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 The Fault0 signal value is ORed with all</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>other fault condition generation inputs (Faultn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>signals and digital comparators).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The FLTSRC bit in the PWMnCTL register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>must be set for this bit to affect fault</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>condition generation.</td>
</tr>
</tbody>
</table>
Register 68: PWM0 Fault Source 1 (PWM0FLTSRC1), offset 0x078
Register 69: PWM1 Fault Source 1 (PWM1FLTSRC1), offset 0x0B8
Register 70: PWM2 Fault Source 1 (PWM2FLTSRC1), offset 0x0F8
Register 71: PWM3 Fault Source 1 (PWM3FLTSRC1), offset 0x138

This register specifies which digital comparator triggers from the ADC are used to generate a fault condition. Each bit in the following register indicates whether the corresponding digital comparator trigger is included in the fault condition. All enabled digital comparator triggers are ORed together to form the PWMnFLTSRC1 portion of the fault condition. The PWMnFLTSRC1 fault condition is then ORed with the PWMnFLTSRC0 fault condition to generate the final fault condition for the PWM generator.

If the FLTSRC bit in the PWMnCTL register (see page 1291) is clear, only the PWM Fault0 pin affects the fault condition generated. Otherwise, sources defined in PWMnFLTSRC0 and PWMnFLTSRC1 affect the fault condition generated.

PWMn Fault Source 1 (PWMnFLTSRC1)
PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x078
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>7</td>
<td>DCMP7</td>
<td>RW</td>
<td>0</td>
<td>Digital Comparator 7</td>
</tr>
</tbody>
</table>

Value Description

0  The trigger from digital comparator 7 is suppressed and cannot generate a fault condition.
1  The trigger from digital comparator 7 is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).

Note: The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>DCMP6</td>
<td>RW</td>
<td>0</td>
<td>Digital Comparator 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The trigger from digital comparator 6 is suppressed and cannot generate a fault condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The trigger from digital comparator 6 is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note: The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.</td>
</tr>
<tr>
<td>5</td>
<td>DCMP5</td>
<td>RW</td>
<td>0</td>
<td>Digital Comparator 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The trigger from digital comparator 5 is suppressed and cannot generate a fault condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The trigger from digital comparator 5 is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note: The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.</td>
</tr>
<tr>
<td>4</td>
<td>DCMP4</td>
<td>RW</td>
<td>0</td>
<td>Digital Comparator 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The trigger from digital comparator 4 is suppressed and cannot generate a fault condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The trigger from digital comparator 4 is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note: The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.</td>
</tr>
<tr>
<td>3</td>
<td>DCMP3</td>
<td>RW</td>
<td>0</td>
<td>Digital Comparator 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The trigger from digital comparator 3 is suppressed and cannot generate a fault condition.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  The trigger from digital comparator 3 is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note: The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.</td>
</tr>
</tbody>
</table>
### Digital Comparator 2

**Description**: The trigger from digital comparator 2 is suppressed and cannot generate a fault condition.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The trigger from digital comparator 2 is suppressed and cannot generate a fault condition.</td>
</tr>
<tr>
<td>1</td>
<td>The trigger from digital comparator 2 is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).</td>
</tr>
</tbody>
</table>

**Note**: The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.

### Digital Comparator 1

**Description**: The trigger from digital comparator 1 is suppressed and cannot generate a fault condition.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The trigger from digital comparator 1 is suppressed and cannot generate a fault condition.</td>
</tr>
<tr>
<td>1</td>
<td>The trigger from digital comparator 1 is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).</td>
</tr>
</tbody>
</table>

**Note**: The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.

### Digital Comparator 0

**Description**: The trigger from digital comparator 0 is suppressed and cannot generate a fault condition.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The trigger from digital comparator 0 is suppressed and cannot generate a fault condition.</td>
</tr>
<tr>
<td>1</td>
<td>The trigger from digital comparator 0 is ORed with all other fault condition generation inputs (Faultn signals and digital comparators).</td>
</tr>
</tbody>
</table>

**Note**: The FLTSRC bit in the PWMnCTL register must be set for this bit to affect fault condition generation.
Register 72: PWM0 Minimum Fault Period (PWM0MINFLTPER), offset 0x07C
Register 73: PWM1 Minimum Fault Period (PWM1MINFLTPER), offset 0x0BC
Register 74: PWM2 Minimum Fault Period (PWM2MINFLTPER), offset 0x0FC
Register 75: PWM3 Minimum Fault Period (PWM3MINFLTPER), offset 0x13C

If the MINFLTPER bit in the PWMnCTL register is set, this register specifies the 16-bit time-extension value to be used in extending the fault condition. The value is loaded into a 16-bit down counter, and the counter value is used to extend the fault condition. The fault condition is released in the clock immediately after the counter value reaches 0. The fault condition is asynchronous to the PWM clock; and the delay value is the product of the PWM clock period and the (MFP field value + 1) or (MFP field value + 2) depending on when the fault condition asserts with respect to the PWM clock. The counter decrements at the PWM clock rate, without pause or condition.

### PWMn Minimum Fault Period (PWMnMINFLTPER)

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>31:16</td>
<td>reserved</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>15:0</td>
<td>MFP</td>
<td>Minimum Fault Period</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The number of PWM clocks by which a fault condition is extended when the delay is enabled by PWMnCTL MINFLTPER.</td>
</tr>
</tbody>
</table>

PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x07C
Type RW, reset 0x0000.0000

16171819202122232425262728293031
reserved

0000000000000000 Reset

302928272625242322212019181716

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MFP

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>31:16</td>
<td>reserved</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>RO</td>
<td>0x0000</td>
<td>15:0</td>
<td>MFP</td>
<td>Minimum Fault Period</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The number of PWM clocks by which a fault condition is extended when the delay is enabled by PWMnCTL MINFLTPER.</td>
</tr>
</tbody>
</table>
Register 76: PWM0 Fault Pin Logic Sense (PWM0FLTSEN), offset 0x800
Register 77: PWM1 Fault Pin Logic Sense (PWM1FLTSEN), offset 0x880
Register 78: PWM2 Fault Pin Logic Sense (PWM2FLTSEN), offset 0x900
Register 79: PWM3 Fault Pin Logic Sense (PWM3FLTSEN), offset 0x980

This register defines the PWM fault pin logic sense.

PWMn Fault Pin Logic Sense (PWMnFLTSEN)
PWM0 base: 0x4002.8000
PWM1 base: 0x4002.9000
Offset 0x800
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>FAULT3</td>
<td>RW</td>
<td>0</td>
<td>Fault3 Sense</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An error is indicated if the Fault3 signal is High.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An error is indicated if the Fault3 signal is Low.</td>
</tr>
<tr>
<td>2</td>
<td>FAULT2</td>
<td>RW</td>
<td>0</td>
<td>Fault2 Sense</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An error is indicated if the Fault2 signal is High.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An error is indicated if the Fault2 signal is Low.</td>
</tr>
<tr>
<td>1</td>
<td>FAULT1</td>
<td>RW</td>
<td>0</td>
<td>Fault1 Sense</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An error is indicated if the Fault1 signal is High.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An error is indicated if the Fault1 signal is Low.</td>
</tr>
<tr>
<td>0</td>
<td>FAULT0</td>
<td>RW</td>
<td>0</td>
<td>Fault0 Sense</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 An error is indicated if the Fault0 signal is High.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 An error is indicated if the Fault0 signal is Low.</td>
</tr>
</tbody>
</table>
Register 80: PWM0 Fault Status 0 (PWM0FLTSTAT0), offset 0x804
Register 81: PWM1 Fault Status 0 (PWM1FLTSTAT0), offset 0x884
Register 82: PWM2 Fault Status 0 (PWM2FLTSTAT0), offset 0x904
Register 83: PWM3 Fault Status 0 (PWM3FLTSTAT0), offset 0x984

Along with the PWMnFLTSTAT1 register, this register provides status regarding the fault condition inputs.

If the LATCH bit in the PWMnCTL register is clear, the contents of the PWMnFLTSTAT0 register are read-only (RO) and provide the current state of the MnFAULTn inputs.

If the LATCH bit in the PWMnCTL register is set, the contents of the PWMnFLTSTAT0 register are read / write 1 to clear (RW1C) and provide a latched version of the MnFAULTn inputs. In this mode, the register bits are cleared by writing a 1 to a set bit. The MnFAULTn inputs are recorded after their sense is adjusted in the generator.

The contents of this register can only be written if the fault source extensions are enabled (the FLTSRC bit in the PWMnCTL register is set).

**Note:** The fault status registers, PWMnFLTSTAT0 and PWMnFLTSTAT1, reflect the status of all fault sources, regardless of what fault sources are enabled for that particular generator.

**PWMn Fault Status 0 (PWMnFLTSTAT0)**

<table>
<thead>
<tr>
<th>Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>FAULT3</td>
<td>-</td>
<td>0</td>
<td>Fault Input 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the PWMnCTL register LATCH bit is clear, this bit is RO and represents the current state of the MnFAULT3 input signal after the logic sense adjustment.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the PWMnCTL register LATCH bit is set, this bit is RW1C and represents a sticky version of the MnFAULT3 input signal after the logic sense adjustment.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ If FAULT3 is set, the input transitioned to the active state previously.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ If FAULT3 is clear, the input has not transitioned to the active state since the last time it was cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ The FAULT3 bit is cleared by writing it with the value 1.</td>
</tr>
</tbody>
</table>
Fault Input 2

If the \texttt{PWMnCTL} register \texttt{LATCH} bit is clear, this bit is RO and represents the current state of the \texttt{MnFAULT2} input signal after the logic sense adjustment.

If the \texttt{PWMnCTL} register \texttt{LATCH} bit is set, this bit is RW1C and represents a sticky version of the \texttt{MnFAULT2} input signal after the logic sense adjustment.

- If \texttt{FAULT2} is set, the input transitioned to the active state previously.
- If \texttt{FAULT2} is clear, the input has not transitioned to the active state since the last time it was cleared.
- The \texttt{FAULT2} bit is cleared by writing it with the value 1.

Fault Input 1

If the \texttt{PWMnCTL} register \texttt{LATCH} bit is clear, this bit is RO and represents the current state of the \texttt{MnFAULT1} input signal after the logic sense adjustment.

If the \texttt{PWMnCTL} register \texttt{LATCH} bit is set, this bit is RW1C and represents a sticky version of the \texttt{MnFAULT1} input signal after the logic sense adjustment.

- If \texttt{FAULT1} is set, the input transitioned to the active state previously.
- If \texttt{FAULT1} is clear, the input has not transitioned to the active state since the last time it was cleared.
- The \texttt{FAULT1} bit is cleared by writing it with the value 1.

Fault Input 0

If the \texttt{PWMnCTL} register \texttt{LATCH} bit is clear, this bit is RO and represents the current state of the input signal after the logic sense adjustment.

If the \texttt{PWMnCTL} register \texttt{LATCH} bit is set, this bit is RW1C and represents a sticky version of the input signal after the logic sense adjustment.

- If \texttt{FAULT0} is set, the input transitioned to the active state previously.
- If \texttt{FAULT0} is clear, the input has not transitioned to the active state since the last time it was cleared.
- The \texttt{FAULT0} bit is cleared by writing it with the value 1.
Register 84: PWM0 Fault Status 1 (PWM0FLTSTAT1), offset 0x808  
Register 85: PWM1 Fault Status 1 (PWM1FLTSTAT1), offset 0x888  
Register 86: PWM2 Fault Status 1 (PWM2FLTSTAT1), offset 0x908  
Register 87: PWM3 Fault Status 1 (PWM3FLTSTAT1), offset 0x988

Along with the PWMnFLTSTAT0 register, this register provides status regarding the fault condition inputs.

If the LATCH bit in the PWMnCTL register is clear, the contents of the PWMnFLTSTAT1 register are read-only (RO) and provide the current state of the digital comparator triggers.

If the LATCH bit in the PWMnCTL register is set, the contents of the PWMnFLTSTAT1 register are read / write 1 to clear (RW1C) and provide a latched version of the digital comparator triggers. In this mode, the register bits are cleared by writing a 1 to a set bit. The contents of this register can only be written if the fault source extensions are enabled (the FLTSRC bit in the PWMnCTL register is set).

**Note:** The fault status registers, PWMnFLTSTAT0 and PWMnFLTSTAT1, reflect the status of all fault sources, regardless of what fault sources are enabled for that particular generator.

### PWMn Fault Status 1 (PWMnFLTSTAT1)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.00</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>DCMP7</td>
<td>-</td>
<td>0</td>
<td>Digital Comparator 7 Trigger</td>
<td></td>
</tr>
</tbody>
</table>

If the PWMnCTL register LATCH bit is clear, this bit represents the current state of the Digital Comparator 7 trigger input.

If the PWMnCTL register LATCH bit is set, this bit represents a sticky version of the trigger.

- If DCMP7 is set, the trigger transitioned to the active state previously.
- If DCMP7 is clear, the trigger has not transitioned to the active state since the last time it was cleared.
- The DCMP7 bit is cleared by writing it with the value 1.
### Description

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 6         | DCMP6| -    | 0     | Digital Comparator 6 Trigger  
If the **PWMnCTL** register **LATCH** bit is clear, this bit represents the current state of the Digital Comparator 6 trigger input.  
If the **PWMnCTL** register **LATCH** bit is set, this bit represents a sticky version of the trigger.  
  - If **DCMP6** is set, the trigger transitioned to the active state previously.  
  - If **DCMP6** is clear, the trigger has not transitioned to the active state since the last time it was cleared.  
  - The **DCMP6** bit is cleared by writing it with the value 1. |
| 5         | DCMP5| -    | 0     | Digital Comparator 5 Trigger  
If the **PWMnCTL** register **LATCH** bit is clear, this bit represents the current state of the Digital Comparator 5 trigger input.  
If the **PWMnCTL** register **LATCH** bit is set, this bit represents a sticky version of the trigger.  
  - If **DCMP5** is set, the trigger transitioned to the active state previously.  
  - If **DCMP5** is clear, the trigger has not transitioned to the active state since the last time it was cleared.  
  - The **DCMP5** bit is cleared by writing it with the value 1. |
| 4         | DCMP4| -    | 0     | Digital Comparator 4 Trigger  
If the **PWMnCTL** register **LATCH** bit is clear, this bit represents the current state of the Digital Comparator 4 trigger input.  
If the **PWMnCTL** register **LATCH** bit is set, this bit represents a sticky version of the trigger.  
  - If **DCMP4** is set, the trigger transitioned to the active state previously.  
  - If **DCMP4** is clear, the trigger has not transitioned to the active state since the last time it was cleared.  
  - The **DCMP4** bit is cleared by writing it with the value 1. |
| 3         | DCMP3| -    | 0     | Digital Comparator 3 Trigger  
If the **PWMnCTL** register **LATCH** bit is clear, this bit represents the current state of the Digital Comparator 3 trigger input.  
If the **PWMnCTL** register **LATCH** bit is set, this bit represents a sticky version of the trigger.  
  - If **DCMP3** is set, the trigger transitioned to the active state previously.  
  - If **DCMP3** is clear, the trigger has not transitioned to the active state since the last time it was cleared.  
  - The **DCMP3** bit is cleared by writing it with the value 1. |
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>DCMP2</td>
<td>-</td>
<td>0</td>
<td>Digital Comparator 2 Trigger</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the PWMnCTL register LATCH bit is clear, this bit represents the current state of the Digital Comparator 2 trigger input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the PWMnCTL register LATCH bit is set, this bit represents a sticky version of the trigger.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ If DCMP2 is set, the trigger transitioned to the active state previously.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ If DCMP2 is clear, the trigger has not transitioned to the active state since the last time it was cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ The DCMP2 bit is cleared by writing it with the value 1.</td>
</tr>
<tr>
<td>1</td>
<td>DCMP1</td>
<td>-</td>
<td>0</td>
<td>Digital Comparator 1 Trigger</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the PWMnCTL register LATCH bit is clear, this bit represents the current state of the Digital Comparator 1 trigger input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the PWMnCTL register LATCH bit is set, this bit represents a sticky version of the trigger.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ If DCMP1 is set, the trigger transitioned to the active state previously.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ If DCMP1 is clear, the trigger has not transitioned to the active state since the last time it was cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ The DCMP1 bit is cleared by writing it with the value 1.</td>
</tr>
<tr>
<td>0</td>
<td>DCMP0</td>
<td>-</td>
<td>0</td>
<td>Digital Comparator 0 Trigger</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the PWMnCTL register LATCH bit is clear, this bit represents the current state of the Digital Comparator 0 trigger input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>If the PWMnCTL register LATCH bit is set, this bit represents a sticky version of the trigger.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ If DCMP0 is set, the trigger transitioned to the active state previously.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ If DCMP0 is clear, the trigger has not transitioned to the active state since the last time it was cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>■ The DCMP0 bit is cleared by writing it with the value 1.</td>
</tr>
</tbody>
</table>
Register 88: PWM Peripheral Properties (PWMPP), offset 0xFC0

The PWMPP register provides information regarding the properties of the PWM module.

PWM Peripheral Properties (PWMPP)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>reserved</td>
<td>RO</td>
<td>0x0</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>10</td>
<td>ONE</td>
<td>RO</td>
<td>0x0</td>
<td>One-Shot Mode</td>
</tr>
<tr>
<td>9</td>
<td>EFAULT</td>
<td>RO</td>
<td>0x1</td>
<td>Extended Fault</td>
</tr>
<tr>
<td>8</td>
<td>ESYNC</td>
<td>RO</td>
<td>0x1</td>
<td>Extended Synchronization</td>
</tr>
<tr>
<td>7:4</td>
<td>FCNT</td>
<td>RO</td>
<td>0x4</td>
<td>Fault Inputs</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>GCNT</td>
<td>RO</td>
<td>0x4</td>
<td>Generators</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>No generators.</td>
</tr>
<tr>
<td>0x1</td>
<td>1 generator</td>
</tr>
<tr>
<td>0x2</td>
<td>2 generators</td>
</tr>
<tr>
<td>0x3</td>
<td>3 generators</td>
</tr>
<tr>
<td>0x4</td>
<td>4 generators</td>
</tr>
<tr>
<td>0x5-0xF</td>
<td>reserved</td>
</tr>
</tbody>
</table>

The number of PWM outputs is 2 times the number of PWM generators.
21 Quadrature Encoder Interface (QEI)

A quadrature encoder, also known as a 2-channel incremental encoder, converts linear displacement into a pulse signal. By monitoring both the number of pulses and the relative phase of the two signals, you can track the position, direction of rotation, and speed. In addition, a third channel, or index signal, can be used to reset the position counter.

The TM4C123GH6PZ microcontroller includes two quadrature encoder interface (QEI) modules. Each QEI module interprets the code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture a running estimate of the velocity of the encoder wheel.

The TM4C123GH6PZ microcontroller includes two QEI modules providing control of two motors at the same time with the following features:

- Position integrator that tracks the encoder position
- Programmable noise filter on the inputs
- Velocity capture using built-in timer
- The input frequency of the QEI inputs may be as high as 1/4 of the processor frequency (for example, 12.5 MHz for a 50-MHz system)
- Interrupt generation on:
  - Index pulse
  - Velocity-timer expiration
  - Direction change
  - Quadrature error detection

21.1 Block Diagram

Figure 21-1 on page 1331 provides an internal block diagram of a TM4C123GH6PZ QEI module. The PhA and PhB inputs shown in this diagram are the internal signals that enter the Quadrature Encoder after the external signals, PhAn and PhBn, have passed through inversion and swapping logic shown in Figure 21-2 on page 1332. The QEI module has the option of inverting and/or swapping the incoming signals.

Note: Any references in this chapter to PhA and PhB refer to the internal PhA and PhB inputs that enter the Quadrature Encoder after the external signals, PhAn and PhBn, have passed through inversion and swapping logic that is enabled through the QEI Control (QEICTL) register.
Figure 21-1. QEI Block Diagram

Figure 21-2 on page 1332 shows the logic that is provided to allow the PhAn and PhBn signals to be inverted and/or swapped.
21.2 Signal Description

The following table lists the external signals of the QEI module and describes the function of each. The QEI signals are alternate functions for some GPIO signals and default to be GPIO signals at reset. The column in the table below titled "Pin Mux/Pin Assignment" lists the possible GPIO pin placements for these QEI signals. The AFSEL bit in the GPIO Alternate Function Select (GPIOAFSEL) register (page 684) should be set to choose the QEI function. The number in parentheses is the encoding that must be programmed into the PMCn field in the GPIOPortControl (GPIOPCTL) register (page 702) to assign the QEI signal to the specified GPIO port pin. For more information on configuring GPIOs, see “General-Purpose Input/Outputs (GPIOs)” on page 659.

Table 21-1. QEI Signals (100LQFP)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDX0</td>
<td>4</td>
<td>PD3 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 index.</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>PJ2 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>PH1 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>39</td>
<td>PF4 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IDX1</td>
<td>25</td>
<td>PC4 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 index.</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>PG5 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>88</td>
<td>PG7 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PhA0</td>
<td>40</td>
<td>PF0 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase A.</td>
</tr>
<tr>
<td></td>
<td>79</td>
<td>PH4 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>99</td>
<td>PD6 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PhA1</td>
<td>24</td>
<td>PC5 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase A.</td>
</tr>
<tr>
<td></td>
<td>59</td>
<td>PG3 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>62</td>
<td>PG0 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 21-1. QEI Signals (100LQFP) (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PhB0</td>
<td>41</td>
<td>PF1 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase B.</td>
</tr>
<tr>
<td></td>
<td>78</td>
<td>PH5 (5)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>PD7 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PhB1</td>
<td>23</td>
<td>PC6 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase B.</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td>PG1 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>74</td>
<td>PG4 (6)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The TTL designation indicates the pin has TTL-compatible voltage levels.

21.3 Functional Description

The QEI module interprets the two-bit gray code produced by a quadrature encoder wheel to integrate position over time and determine direction of rotation. In addition, it can capture a running estimate of the velocity of the encoder wheel.

The position integrator and velocity capture can be independently enabled, though the position integrator must be enabled before the velocity capture can be enabled. The two phase signals, PhAn and PhBn, can be swapped before being interpreted by the QEI module to change the meaning of forward and backward and to correct for miswiring of the system. Alternatively, the phase signals can be interpreted as a clock and direction signal as output by some encoders.

The QEI module input signals have a digital noise filter on them that can be enabled to prevent spurious operation. The noise filter requires that the inputs be stable for a specified number of consecutive clock cycles before updating the edge detector. The filter is enabled by the FILTEN bit in the QEI Control (QEICTL) register. The frequency of the input update is programmable using the FILTCNT bit field in the QEICTL register.

The QEI module supports two modes of signal operation: quadrature phase mode and clock/direction mode. In quadrature phase mode, the encoder produces two clocks that are 90 degrees out of phase; the edge relationship is used to determine the direction of rotation. In clock/direction mode, the encoder produces a clock signal to indicate steps and a direction signal to indicate the direction of rotation. This mode is determined by the SIGMODE bit of the QEICTL register (see page 1337).

When the QEI module is set to use the quadrature phase mode (SIGMODE bit is clear), the capture mode for the position integrator can be set to update the position counter on every edge of the PhA signal or to update on every edge of both PhA and PhB. Updating the position counter on every PhA and PhB edge provides more positional resolution at the cost of less range in the positional counter.

When edges on PhA lead edges on PhB, the position counter is incremented. When edges on PhB lead edges on PhA, the position counter is decremented. When a rising and falling edge pair is seen on one of the phases without any edges on the other, the direction of rotation has changed.

The positional counter is automatically reset on one of two conditions: sensing the index pulse or reaching the maximum position value. The reset mode is determined by the RESMODE bit of the QEICTL register.

When RESMODE is set, the positional counter is reset when the index pulse is sensed. This mode limits the positional counter to the values [0:N-1], where N is the number of phase edges in a full revolution of the encoder wheel. The QEI Maximum Position (QEIMAXPOS) register must be programmed with N-1 so that the reverse direction from position 0 can move the position counter to N-1. In this mode, the position register contains the absolute position of the encoder relative to the index (or home) position once an index pulse has been seen.
When **RESMODE** is clear, the positional counter is constrained to the range \([0:M]\), where \(M\) is the programmable maximum value. The index pulse is ignored by the positional counter in this mode.

Velocity capture uses a configurable timer and a count register. The timer counts the number of phase edges (using the same configuration as for the position integrator) in a given time period. The edge count from the previous time period is available to the controller via the **QEI Velocity (QEISPEED)** register, while the edge count for the current time period is being accumulated in the **QEI Velocity Counter (QEICOUNT)** register. As soon as the current time period is complete, the total number of edges counted in that time period is made available in the **QEISPEED** register (overwriting the previous value), the **QEICOUNT** register is cleared, and counting commences on a new time period. The number of edges counted in a given time period is directly proportional to the velocity of the encoder.

Figure 21-3 on page 1334 shows how the TM4C123GH6PZ quadrature encoder converts the phase input signals into clock pulses, the direction signal, and how the velocity predivider operates (in Divide by 4 mode).

The following equation converts the velocity counter value into an rpm value:

\[
\text{rpm} = \left( \frac{\text{clock} \times (2^{\text{VELDIV}} \times \text{SPEED} \times 60)}{(\text{LOAD} \times \text{ppr} \times \text{edges})} \right)
\]

where:

- \(\text{clock}\) is the controller clock rate
- \(\text{ppr}\) is the number of pulses per revolution of the physical encoder
- \(\text{edges}\) is 2 or 4, based on the capture mode set in the **QEICTL** register (2 for **CAPMODE** clear and 4 for **CAPMODE** set)

For example, consider a motor running at 600 rpm. A 2048 pulse per revolution quadrature encoder is attached to the motor, producing 8192 phase edges per revolution. With a velocity predivider of +1 (**VELDIV** is clear) and clocking on both **PhA** and **PhB** edges, this results in 81,920 pulses per second (the motor turns 10 times per second). If the timer were clocked at 10,000 Hz, and the load value was 2,500 (¼ of a second), it would count 20,480 pulses per update. Using the above equation:

\[
\text{rpm} = \left( \frac{10000 \times 1 \times 20480 \times 60}{2500 \times 2048 \times 4} \right) = 600 \text{ rpm}
\]
Now, consider that the motor is sped up to 3000 rpm. This results in 409,600 pulses per second, or 102,400 every \( \frac{1}{4} \) of a second. Again, the above equation gives:

\[
\text{rpm} = \frac{10000 \times 1 \times 102400 \times 60}{2500 \times 2048 \times 4} = 3000 \text{ rpm}
\]

Care must be taken when evaluating this equation because intermediate values may exceed the capacity of a 32-bit integer. In the above examples, the clock is 10,000 and the divider is 2,500; both could be predivided by 100 (at compile time if they are constants) and therefore be 100 and 25. In fact, if they were compile-time constants, they could also be reduced to a simple multiply by 4, cancelled by the \( \div 4 \) for the edge-count factor.

**Important:** Reducing constant factors at compile time is the best way to control the intermediate values of this equation and reduce the processing requirement of computing this equation.

The division can be avoided by selecting a timer load value such that the divisor is a power of 2; a simple shift can therefore be done in place of the division. For encoders with a power of 2 pulses per revolution, the load value can be a power of 2. For other encoders, a load value must be selected such that the product is very close to a power of 2. For example, a 100 pulse-per-revolution encoder could use a load value of 82, resulting in 32,800 as the divisor, which is 0.09% above \( 2^{14} \). In this case a shift by 15 would be an adequate approximation of the divide in most cases. If absolute accuracy were required, the microcontroller's divide instruction could be used.

The QEI module can produce a controller interrupt on several events: phase error, direction change, reception of the index pulse, and expiration of the velocity timer. Standard masking, raw interrupt status, interrupt status, and interrupt clear capabilities are provided.

### 21.4 Initialization and Configuration

The following example shows how to configure the Quadrature Encoder module to read back an absolute position:

1. Enable the QEI clock using the **RCGCQEI** register in the System Control module (see page 358).

2. Enable the clock to the appropriate GPIO module via the **RCGCGPIO** register in the System Control module (see page 342).

3. In the GPIO module, enable the appropriate pins for their alternate function using the **GPIOAFSEL** register. To determine which GPIOs to configure, see Table 23-4 on page 1377.

4. Configure the \( \text{PMCn} \) fields in the **GPIOPCTL** register to assign the QEI signals to the appropriate pins (see page 702 and Table 23-5 on page 1386).

5. Configure the quadrature encoder to capture edges on both signals and maintain an absolute position by resetting on index pulses. A 1000-line encoder with four edges per line, results in 4000 pulses per revolution; therefore, set the maximum position to 3999 (0xF9F) as the count is zero-based.
   - Write the **QEICTL** register with the value of 0x0000.0018.
   - Write the **QEIMAXPOS** register with the value of 0x0000.0F9F.

6. Enable the quadrature encoder by setting bit 0 of the **QEICTL** register.
Note: Once the QEI module has been enabled by setting the ENABLE bit in the QEICTL register, it cannot be disabled. The only way to clear the ENABLE bit is to reset the module using the Quadrature Encoder Interface Software Reset (SRQEI) register.

7. Delay until the encoder position is required.

8. Read the encoder position by reading the QEI Position (QEIPOS) register value.

Note: If the application requires the quadrature encoder to have a specific initial position, this value must be programmed in the QEIPOS register after the quadrature encoder has been enabled by setting the ENABLE bit in the QEICTL register.

21.5 Register Map

Table 21-2 on page 1336 lists the QEI registers. The offset listed is a hexadecimal increment to the register's address, relative to the module's base address:

- QEI0: 0x4002.C000
- QEI1: 0x4002.D000

Note that the QEI module clock must be enabled before the registers can be programmed (see page 358). There must be a delay of 3 system clocks after the QEI module clock is enabled before any QEI module registers are accessed.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
<th>See page</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>QEICTL</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>QEI Control</td>
<td>1337</td>
</tr>
<tr>
<td>0x004</td>
<td>QEISTAT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>QEI Status</td>
<td>1340</td>
</tr>
<tr>
<td>0x008</td>
<td>QEIPOS</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>QEI Position</td>
<td>1341</td>
</tr>
<tr>
<td>0x00C</td>
<td>QEIMAXPOS</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>QEI Maximum Position</td>
<td>1342</td>
</tr>
<tr>
<td>0x010</td>
<td>QEILOAD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>QEI Timer Load</td>
<td>1343</td>
</tr>
<tr>
<td>0x014</td>
<td>QEITIME</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>QEI Timer</td>
<td>1344</td>
</tr>
<tr>
<td>0x018</td>
<td>QEICOUNT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>QEI Velocity Counter</td>
<td>1345</td>
</tr>
<tr>
<td>0x01C</td>
<td>QEISPEED</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>QEI Velocity</td>
<td>1346</td>
</tr>
<tr>
<td>0x020</td>
<td>QEIINTEN</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>QEI Interrupt Enable</td>
<td>1347</td>
</tr>
<tr>
<td>0x024</td>
<td>QEIRIS</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>QEI Raw Interrupt Status</td>
<td>1349</td>
</tr>
<tr>
<td>0x028</td>
<td>QEIISC</td>
<td>RW1C</td>
<td>0x0000.0000</td>
<td>QEI Interrupt Status and Clear</td>
<td>1351</td>
</tr>
</tbody>
</table>

21.6 Register Descriptions

The remainder of this section lists and describes the QEI registers, in numerical order by address offset.
Register 1: QEI Control (QEICTL), offset 0x000

This register contains the configuration of the QEI module. Separate enables are provided for the quadrature encoder and the velocity capture blocks; the quadrature encoder must be enabled in order to capture the velocity, but the velocity does not need to be captured in applications that do not need it. The phase signal interpretation, phase swap, Position Update mode, Position Reset mode, and velocity presdivider are all set via this register.

### QEI Control (QEICTL)

<table>
<thead>
<tr>
<th>QEIO base: 0x4002.C000</th>
<th>QEII base: 0x4002.D000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset 0x000</td>
<td></td>
</tr>
<tr>
<td>Type RW, reset 0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

#### Bit/Field | Name | Type | Reset | Description |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>19:16</td>
<td>FILTCNT</td>
<td>RW</td>
<td>0x0</td>
<td>Input Filter Prescale Count</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field controls the frequency of the input update.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When this field is clear, the input is sampled after 2 system clocks. When this field is 0x1, the input is sampled after 3 system clocks. Similarly, when this field is 0xF, the input is sampled after 17 clocks.</td>
</tr>
<tr>
<td>15:14</td>
<td>reserved</td>
<td>RO</td>
<td>0x000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>13</td>
<td>FILTEN</td>
<td>RW</td>
<td>0</td>
<td>Enable Input Filter</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The QEI inputs are not filtered.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Enables the digital noise filter on the QEI input signals. Inputs must be stable for 3 consecutive clock edges before the edge detector is updated.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>STALLEN</td>
<td>RW</td>
<td>0</td>
<td>Stall QEI</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The QEI module does not stall when the microcontroller is stopped by a debugger.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>The QEI module stalls when the microcontroller is stopped by a debugger.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Quadrature Encoder Interface (QEI)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>INVI</td>
<td>RW</td>
<td>0</td>
<td>Invert Index Pulse</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Description</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Inverts the IDX input.</td>
</tr>
<tr>
<td>10</td>
<td>INVB</td>
<td>RW</td>
<td>0</td>
<td>Invert PhB</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Inverts the PhB input.</td>
</tr>
<tr>
<td>9</td>
<td>INVA</td>
<td>RW</td>
<td>0</td>
<td>Invert PhA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Inverts the PhA input.</td>
</tr>
<tr>
<td>8:6</td>
<td>VELDIV</td>
<td>RW</td>
<td>0x0</td>
<td>Predivide Velocity</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field defines the predivider of the input quadrature pulses before being applied to the QEICOUNT accumulator.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>+1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>+2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>+4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>+8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x4</td>
<td>+16</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x5</td>
<td>+32</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x6</td>
<td>+64</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x7</td>
<td>+128</td>
</tr>
<tr>
<td>5</td>
<td>VELEN</td>
<td>RW</td>
<td>0</td>
<td>Capture Velocity</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>No effect.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>Enables capture of the velocity of the quadrature encoder.</td>
</tr>
<tr>
<td>4</td>
<td>RESMODE</td>
<td>RW</td>
<td>0</td>
<td>Reset Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>The position counter is reset when it reaches the maximum as defined by the MAXPOS field in the QEMAXPOS register.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>The position counter is reset when the index pulse is captured.</td>
</tr>
<tr>
<td>Bit/Field</td>
<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------</td>
<td>------</td>
<td>------</td>
<td>-------------</td>
</tr>
<tr>
<td>3</td>
<td>CAPMODE</td>
<td>RW</td>
<td>0</td>
<td>Capture Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> When SIGMODE=1, the CAPMODE setting is not applicable and is reserved.</td>
</tr>
<tr>
<td>Value</td>
<td>Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Only the PhA edges are counted.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The PhA and PhB edges are counted, providing twice the positional resolution but half the range.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| 2         | SIGMODE   | RW   | 0    | Signal Mode |
|           |           |      |      | **Value** |
| 0         | The internal PhA and PhB signals operate as quadrature phase signals. |
| 1         | The internal PhA input operates as the clock (CLK) signal and the internal PhB input operates as the direction (DIR) signal. |

| 1         | SWAP      | RW   | 0    | Swap Signals |
|           |           |      |      | **Value** |
| 0         | No effect. |
| 1         | Swaps the PhAn and PhBn signals. |

| 0         | ENABLE    | RW   | 0    | Enable QEI |
|           |           |      |      | **Value** |
| 0         | No effect. |
| 1         | Enables the quadrature encoder module. |

**Note:** Once the QEI module has been enabled by setting the ENABLE bit, it cannot be disabled. The only way to clear the ENABLE bit is to reset the module using the Quadrature Encoder Interface Software Reset (SRQEI) register.
Register 2: QEI Status (QEISTAT), offset 0x004

This register provides status about the operation of the QEI module.

### QEI Status (QEISTAT)

- **QE0 base**: 0x4002.C000
- **QE1 base**: 0x4002.D000
- **Offset**: 0x004
- **Type**: RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
</tbody>
</table>
| 1         | DIRECTION  | RO   | 0     | Direction of Rotation
Indicates the direction the encoder is rotating. |

- **Value Description**
  - 0: The encoder is rotating forward.
  - 1: The encoder is rotating in reverse.

| 0         | ERROR      | RO   | 0     | Error Detected                                                             |

- **Value Description**
  - 0: No error.
  - 1: An error was detected in the gray code sequence (that is, both signals changing at the same time).
Register 3: QEI Position (QEIPOS), offset 0x008

This register contains the current value of the position integrator. The value is updated by the status of the QEI phase inputs and can be set to a specific value by writing to it.

QEI Position (QEIPOS)
QE0 base: 0x4002.C000
QE1 base: 0x4002.D000
Offset 0x008
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31.0</td>
<td>POSITION</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Current Position Integrator Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The current value of the position integrator.</td>
</tr>
</tbody>
</table>
Register 4: QEI Maximum Position (QEIMAXPOS), offset 0x00C

This register contains the maximum value of the position integrator. When moving forward, the position register resets to zero when it increments past this value. When moving in reverse, the position register resets to this value when it decrements from zero.

QEI Maximum Position (QEIMAXPOS)

QEIO base: 0x4002.C000
QEII base: 0x4002.D000
Offset 0x00C
Type RW, reset 0x0000.0000

---

<table>
<thead>
<tr>
<th>MAXPOS</th>
<th>Type</th>
<th>0000.0000</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000000</td>
<td>RW</td>
<td>0x0000.0000</td>
<td></td>
</tr>
</tbody>
</table>

---

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>MAXPOS</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Maximum Position Integrator Value</td>
</tr>
</tbody>
</table>

The maximum value of the position integrator.
Register 5: QEI Timer Load (QEILOAD), offset 0x010

This register contains the load value for the velocity timer. Because this value is loaded into the timer on the clock cycle after the timer is zero, this value should be one less than the number of clocks in the desired period. So, for example, to have 2000 decimal clocks per timer period, this register should contain 1999 decimal.

QEI Timer Load (QEILOAD)
QEIO base: 0x4002.C000
QEI1 base: 0x4002.D000
Offset 0x010
Type RW, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>LOAD</td>
<td>RW</td>
<td>0x0000.0000</td>
<td>Velocity Timer Load Value</td>
</tr>
</tbody>
</table>

The load value for the velocity timer.
Register 6: QEI Timer (QEITIME), offset 0x014

This register contains the current value of the velocity timer. This counter does not increment when the VELEN bit in the QEICTL register is clear.

QEI Timer (QEITIME)
QE0 base: 0x4002.C000
QE1 base: 0x4002.D000
Offset 0x014
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>TIME</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Velocity Timer Current Value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The current value of the velocity timer.</td>
</tr>
</tbody>
</table>
Register 7: QEI Velocity Counter (QEICOUNT), offset 0x018

This register contains the running count of velocity pulses for the current time period. Because this count is a running total, the time period to which it applies cannot be known with precision (that is, a read of this register does not necessarily correspond to the time returned by the QEITIME register because there is a small window of time between the two reads, during which either value may have changed). The QEISPEED register should be used to determine the actual encoder velocity; this register is provided for information purposes only. This counter does not increment when the VELEN bit in the QEICTL register is clear.

QEI Velocity Counter (QEICOUNT)
QEI0 base: 0x4002.C000
QEI1 base: 0x4002.D000
Offset 0x018
Type RO, reset 0x0000.0000

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>COUNT</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>Velocity Pulse Count&lt;br&gt;The running total of encoder pulses during this velocity timer period.</td>
</tr>
</tbody>
</table>
Register 8: QEI Velocity (QEISPEED), offset 0x01C

This register contains the most recently measured velocity of the quadrature encoder. This value corresponds to the number of velocity pulses counted in the previous velocity timer period. This register does not update when the VELEN bit in the QEICTL register is clear.

### QEI Velocity (QEISPEED)

- **QE10 base**: 0x4002.C000
- **QE11 base**: 0x4002.D000
- **Offset 0x01C**
- **Type RO, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Description</th>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Velocity</td>
<td>31:0</td>
<td>SPEED</td>
<td>RO</td>
<td>0x0000.0000</td>
<td>The measured speed of the quadrature encoder in pulses per period.</td>
</tr>
</tbody>
</table>
Register 9: QEI Interrupt Enable (QEINTEN), offset 0x020

This register contains enables for each of the QEI module interrupts. An interrupt is asserted to the interrupt controller if the corresponding bit in this register is set.

QEI Interrupt Enable (QEINTEN)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>INTERERROR</td>
<td>RW</td>
<td>0</td>
<td>Phase Error Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>Note:</strong> The INTERERROR bit is only applicable when the QEI is operating in quadrature phase mode (SIGMODE=0) and should be masked when SIGMODE =1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The INTERERROR interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the INTERERROR bit in the QEIRIS register is set.</td>
</tr>
<tr>
<td>2</td>
<td>INTDIR</td>
<td>RW</td>
<td>0</td>
<td>Direction Change Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The INTDIR interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the INTDIR bit in the QEIRIS register is set.</td>
</tr>
<tr>
<td>1</td>
<td>INTTIMER</td>
<td>RW</td>
<td>0</td>
<td>Timer Expires Interrupt Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Value Description</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0  The INTTIMER interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1  An interrupt is sent to the interrupt controller when the INTTIMER bit in the QEIRIS register is set.</td>
</tr>
</tbody>
</table>
### Quadrature Encoder Interface (QEI)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>INTINDEX</td>
<td>RW</td>
<td>0</td>
<td>Index Pulse Detected Interrupt Enable</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The INTINDEX interrupt is suppressed and not sent to the interrupt controller.</td>
</tr>
<tr>
<td>1</td>
<td>An interrupt is sent to the interrupt controller when the INTINDEX bit in the QEI register is set.</td>
</tr>
</tbody>
</table>
Register 10: QEI Raw Interrupt Status (QEIRIS), offset 0x024

This register provides the current set of interrupt sources that are asserted, regardless of whether they cause an interrupt to be asserted to the controller (configured through the QEIINTEN register). If a bit is set, the latched event has occurred; if a bit is clear, the event in question has not occurred.

QEI Raw Interrupt Status (QEIRIS)

<table>
<thead>
<tr>
<th>Offset 0x024</th>
<th>Type RO, reset 0x0000.0000</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>INTERROR</td>
<td>RO</td>
<td>0</td>
<td>Phase Error Detected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note: The INTERROR bit is only applicable when the QEI is operating in quadrature phase mode (SIGMODE=0).</td>
</tr>
<tr>
<td>2</td>
<td>INTDIR</td>
<td>RO</td>
<td>0</td>
<td>Direction Change Detected</td>
</tr>
<tr>
<td>1</td>
<td>INTTIMER</td>
<td>RO</td>
<td>0</td>
<td>Velocity Timer Expired</td>
</tr>
</tbody>
</table>

Phase Error Detected

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the INTERROR bit in the QEIISC register.

Direction Change Detected

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the INTDIR bit in the QEIISC register.

Velocity Timer Expired

<table>
<thead>
<tr>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the INTTIMER bit in the QEIISC register.
## Quadrature Encoder Interface (QEI)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>INTINDEX</td>
<td>RO</td>
<td>0</td>
<td>Index Pulse Asserted</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An interrupt has not occurred.</td>
</tr>
<tr>
<td>1</td>
<td>The index pulse has occurred.</td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1 to the INTINDEX bit in the QEIIISC register.
Register 11: QEI Interrupt Status and Clear (QEISC), offset 0x028

This register provides the current set of interrupt sources that are asserted to the controller. If a bit is set, the latched event has occurred and is enabled to generate an interrupt; if a bit is clear the event in question has not occurred or is not enabled to generate an interrupt. This register is RW1C; writing a 1 to a bit position clears the bit and the corresponding interrupt reason.

**QEI Interrupt Status and Clear (QEISC)**

- **QEI0 base:** 0x4002.C000
- **QEI1 base:** 0x4002.D000
- **Offset 0x028**
- **Type RW1C, reset 0x0000.0000**

<table>
<thead>
<tr>
<th>Type</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:4</td>
<td>reserved</td>
<td>RO</td>
<td>0x0000.000</td>
<td>Software should not rely on the value of a reserved bit. To provide compatibility with future products, the value of a reserved bit should be preserved across a read-modify-write operation.</td>
</tr>
<tr>
<td>3</td>
<td>INTERRO</td>
<td>RW1C</td>
<td>0</td>
<td>Phase Error Interrupt</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No interrupt has occurred or the interrupt is masked.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The INTERRO bits in the QEIRIS register and the QEINTEN registers are set, providing an interrupt to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>INTDIR</td>
<td>RW1C</td>
<td>0</td>
<td>Direction Change Interrupt</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No interrupt has occurred or the interrupt is masked.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The INTDIR bits in the QEIRIS register and the QEINTEN registers are set, providing an interrupt to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>INTTIMER</td>
<td>RW1C</td>
<td>0</td>
<td>Velocity Timer Expired Interrupt</td>
</tr>
<tr>
<td></td>
<td>Value Description</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>No interrupt has occurred or the interrupt is masked.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>The INTTIMER bits in the QEIRIS register and the QEINTEN registers are set, providing an interrupt to the interrupt controller.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This bit is cleared by writing a 1. Clearing this bit also clears the INTTIMER bit in the QEIRIS register.
### Quadrature Encoder Interface (QEI)

<table>
<thead>
<tr>
<th>Bit/Field</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>INTINDEX</td>
<td>RW1C</td>
<td>0</td>
<td>Index Pulse Interrupt</td>
</tr>
</tbody>
</table>

**Value** | **Description**
---|---
0 | No interrupt has occurred or the interrupt is masked.
1 | The INTINDEX bits in the QEIRIS register and the QEINTEN registers are set, providing an interrupt to the interrupt controller.

This bit is cleared by writing a 1. Clearing this bit also clears the INTINDEX bit in the QEIRIS register.
22 Pin Diagram

The TM4C123GH6PZ microcontroller pin diagram is shown below.

Each GPIO signal is identified by its GPIO port unless it defaults to an alternate function on reset. In this case, the GPIO port name is followed by the default alternate function. To see a complete list of possible functions for each pin, see Table 23-5 on page 1386.

Figure 22-1. 100-Pin LQFP Package Pin Diagram
The following tables list the signals available for each pin. Signals are configured as GPIOs on reset, except for those noted below. Use the GPIOAMSEL register (see page 700) to select analog mode. For a GPIO pin to be used for an alternate digital function, the corresponding bit in the GPIOAFSEL register (see page 684) must be set. Further pin muxing options are provided through the PMCx bit field in the GPIOPCTL register (see page 702), which selects one of several available peripheral functions for that GPIO.

**Important:** Table 10-1 on page 660 shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (GPIOAFSEL=0, GPIODEN=0, GPIOPDR=0, GPIOPUR=0, and GPIOPCTL=0). Special consideration pins may be programed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (POR) or asserting RST returns these GPIO to their original special consideration state.

**Table 23-1. GPIO Pins With Special Considerations**

<table>
<thead>
<tr>
<th>GPIO Pins</th>
<th>Default Reset State</th>
<th>GPIOAFSEL</th>
<th>GPIODEN</th>
<th>GPIOPDR</th>
<th>GPIOPUR</th>
<th>GPIOPCTL</th>
<th>GPIOCR</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA[1:0]</td>
<td>UART0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x1</td>
<td>1</td>
</tr>
<tr>
<td>PA[5:2]</td>
<td>SSIO</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x2</td>
<td>1</td>
</tr>
<tr>
<td>PB[3:2]</td>
<td>C2I2C0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x3</td>
<td>1</td>
</tr>
<tr>
<td>PC[3:0]</td>
<td>JTAG/SWD</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0x1</td>
<td>0</td>
</tr>
<tr>
<td>PD[7]</td>
<td>GPIO8</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
<tr>
<td>PF[0]</td>
<td>GPIO8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x0</td>
<td>0</td>
</tr>
</tbody>
</table>

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the GPIOLOCK register and uncommitting it by setting the GPIOCR register.

Table 23-2 on page 1355 shows the pin-to-signal-name mapping, including functional characteristics of the signals. Each possible alternate analog and digital function is listed for each pin.

Table 23-3 on page 1366 lists the signals in alphabetical order by signal name. If it is possible for a signal to be on multiple pins, each possible pin assignment is listed. The "Pin Mux" column indicates the GPIO and the encoding needed in the PMCx bit field in the GPIOPCTL register.

Table 23-4 on page 1377 groups the signals by functionality, except for GPIOs. If it is possible for a signal to be on multiple pins, each possible pin assignment is listed.

Table 23-5 on page 1386 lists the GPIO pins and their analog and digital alternate functions. The AINx analog signals are not 5-V tolerant and go through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding DEN bit in the GPIO Digital Enable (GPIODEN) register and setting the corresponding AMSEL bit in the GPIO Analog Mode Select (GPIOAMSEL) register. Other analog signals are 5-V tolerant and are connected directly to their circuitry (C0-, C0+, C1-, C1+, C2-, C2+, USB0VBUS, USB0ID). These signals are configured by clearing the DEN bit in the GPIO Digital Enable (GPIODEN) register. The digital signals are enabled by setting the appropriate bit in the GPIO Alternate Function Select (GPIOAFSEL) and GPIODEN registers and configuring the PMCx bit field in the GPIO Port Control (GPIOPCTL) register to the numeric encoding shown in the table below. Table entries that are shaded gray are the default values for the corresponding GPIO pin.
Table 23-6 on page 1389 lists the signals based on number of possible pin assignments. This table can be used to plan how to configure the pins for a particular functionality. Application Note AN01274 Configuring Tiva™ C Series Microcontrollers with Pin Multiplexing provides an overview of the pin muxing implementation, an explanation of how a system designer defines a pin configuration, and examples of the pin configuration process.

**Note:** All digital inputs are Schmitt triggered.

### 23.1 Signals by Pin Number

Table 23-2. Signals by Pin Number

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PD0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 0.</td>
</tr>
<tr>
<td></td>
<td>AIN15</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 15.</td>
</tr>
<tr>
<td></td>
<td>I2C3SL</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>M0PWM6</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>M1PWM0</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 0. This signal is controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>SSI1Clk</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 clock.</td>
</tr>
<tr>
<td></td>
<td>SSI3Clk</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 clock.</td>
</tr>
<tr>
<td></td>
<td>WT2CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>2</td>
<td>PD1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 1.</td>
</tr>
<tr>
<td></td>
<td>AIN14</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 14.</td>
</tr>
<tr>
<td></td>
<td>I2C3SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I²C module 3 data.</td>
</tr>
<tr>
<td></td>
<td>M0PWM7</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>M1PWM1</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 1. This signal is controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>SSI1Fs</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 frame signal.</td>
</tr>
<tr>
<td></td>
<td>SSI3Fs</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 frame signal.</td>
</tr>
<tr>
<td></td>
<td>WT2CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>3</td>
<td>PD2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 2.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT0</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>SSI1Rx</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>SSI3Rx</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 3 receive.</td>
</tr>
<tr>
<td></td>
<td>USB0EPEN</td>
<td>O</td>
<td>TTL</td>
<td>Optionally used in Host mode to control an external power source to supply power to the USB bus.</td>
</tr>
<tr>
<td></td>
<td>WT3CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 0.</td>
</tr>
</tbody>
</table>
Table 23-2. Signals by Pin Number (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>PD3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 3.</td>
</tr>
<tr>
<td></td>
<td>AIN12</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 12.</td>
</tr>
<tr>
<td></td>
<td>IDX0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 index.</td>
</tr>
<tr>
<td></td>
<td>SSI1TxF</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>SSI3TxF</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 3 transmit.</td>
</tr>
<tr>
<td></td>
<td>USB0PFLT</td>
<td>I</td>
<td>TTL</td>
<td>Optionally used in Host mode by an external power source to indicate an error state by that power source.</td>
</tr>
<tr>
<td></td>
<td>WT3CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>7</td>
<td>VDDA</td>
<td>-</td>
<td>Power</td>
<td>The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in Table 24-5 on page 1397, regardless of system implementation.</td>
</tr>
<tr>
<td>8</td>
<td>VREFA+</td>
<td>-</td>
<td>Analog</td>
<td>A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with VREFA−, which specifies the minimum value. The voltage that is applied to VREFA+ is the voltage with which an AIn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in Table 24-33 on page 1426.</td>
</tr>
<tr>
<td>9</td>
<td>VREFA−</td>
<td>-</td>
<td>Analog</td>
<td>A reference voltage used to specify the input voltage at which the ADC converts to a minimum value. This pin is used in conjunction with VREFA+, which specifies the maximum value. In other words, the voltage that is applied to VREFA− is the voltage with which an AIn signal is converted to 0, while the voltage that is applied to VREFA+ is the voltage with which an AIn signal is converted to 4095. The VREFA− voltage is limited to the range specified in Table 24-33 on page 1426.</td>
</tr>
<tr>
<td>10</td>
<td>GNDA</td>
<td>-</td>
<td>Power</td>
<td>The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.</td>
</tr>
<tr>
<td>11</td>
<td>PJ2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port J bit 2.</td>
</tr>
<tr>
<td></td>
<td>IDX0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 index.</td>
</tr>
<tr>
<td></td>
<td>T2CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>U5Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 5 receive.</td>
</tr>
<tr>
<td>12</td>
<td>PE3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 3.</td>
</tr>
<tr>
<td></td>
<td>AIN0</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 0.</td>
</tr>
<tr>
<td>13</td>
<td>PE2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 2.</td>
</tr>
<tr>
<td></td>
<td>AIN1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 1.</td>
</tr>
<tr>
<td>14</td>
<td>PE1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 1.</td>
</tr>
<tr>
<td></td>
<td>AIN2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 2.</td>
</tr>
<tr>
<td></td>
<td>U7Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 7 transmit.</td>
</tr>
<tr>
<td>15</td>
<td>PE0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 0.</td>
</tr>
<tr>
<td></td>
<td>AIN3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 3.</td>
</tr>
<tr>
<td></td>
<td>U7Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 7 receive.</td>
</tr>
<tr>
<td>Pin Number</td>
<td>Pin Name</td>
<td>Pin Type</td>
<td>Buffer Type</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>----------</td>
<td>---------</td>
<td>-------------</td>
<td>-------------</td>
</tr>
<tr>
<td>16</td>
<td>PH0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 0.</td>
</tr>
<tr>
<td></td>
<td>AIN16</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 16.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT0</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>M0PWM0</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>SSI3Clk</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 clock.</td>
</tr>
<tr>
<td></td>
<td>WT2CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>17</td>
<td>PH1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 1.</td>
</tr>
<tr>
<td></td>
<td>AIN17</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 17.</td>
</tr>
<tr>
<td></td>
<td>IDX0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 index.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT1</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>M0PWM1</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>SSI3Fss</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 frame signal.</td>
</tr>
<tr>
<td></td>
<td>WT2CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>18</td>
<td>PH2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 2.</td>
</tr>
<tr>
<td></td>
<td>AIN18</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 18.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT2</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td>M0PWM2</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>SSI3Rx</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 3 receive.</td>
</tr>
<tr>
<td></td>
<td>WT5CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>19</td>
<td>PH3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 3.</td>
</tr>
<tr>
<td></td>
<td>AIN19</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 19.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT3</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 3.</td>
</tr>
<tr>
<td></td>
<td>M0PWM3</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>SSI3TX</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 3 transmit.</td>
</tr>
<tr>
<td></td>
<td>WT5CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>20</td>
<td>VDD</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>22</td>
<td>PC7</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 7.</td>
</tr>
<tr>
<td></td>
<td>C0-</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 0 negative input.</td>
</tr>
<tr>
<td></td>
<td>U3Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 3 transmit.</td>
</tr>
<tr>
<td></td>
<td>USBOFFLT</td>
<td>I</td>
<td>TTL</td>
<td>Optionally used in Host mode by an external power source to indicate an error state by that power source.</td>
</tr>
<tr>
<td></td>
<td>WT1CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 1.</td>
</tr>
</tbody>
</table>
## Table 23-2. Signals by Pin Number (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>PC6</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 6.</td>
</tr>
<tr>
<td></td>
<td>C0+</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 0 positive input.</td>
</tr>
<tr>
<td></td>
<td>PhB1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase B.</td>
</tr>
<tr>
<td></td>
<td>U3Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 3 receive.</td>
</tr>
<tr>
<td></td>
<td>USB0EPEN</td>
<td>O</td>
<td>TTL</td>
<td>Optionally used in Host mode to control an external power source to supply power to the USB bus.</td>
</tr>
<tr>
<td></td>
<td>WT1CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>24</td>
<td>PC5</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 5.</td>
</tr>
<tr>
<td></td>
<td>C1+</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 1 positive input.</td>
</tr>
<tr>
<td></td>
<td>M0PWM7</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>PhA1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase A.</td>
</tr>
<tr>
<td></td>
<td>U1CTS</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Clear To Send modem flow control input signal.</td>
</tr>
<tr>
<td></td>
<td>U1Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>U4Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 4 transmit.</td>
</tr>
<tr>
<td></td>
<td>WT0CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>C1-</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 1 negative input.</td>
</tr>
<tr>
<td></td>
<td>IDX1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 index.</td>
</tr>
<tr>
<td></td>
<td>M0PWM6</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>U1RTS</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Request to Send modem flow control output line.</td>
</tr>
<tr>
<td></td>
<td>U1Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>U4Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 4 receive.</td>
</tr>
<tr>
<td></td>
<td>WT0CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>26</td>
<td>PA0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 0.</td>
</tr>
<tr>
<td></td>
<td>CAN1Rx</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>U0Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 0 receive.</td>
</tr>
<tr>
<td>27</td>
<td>PA1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 1.</td>
</tr>
<tr>
<td></td>
<td>CAN1Tx</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>U0Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 0 transmit.</td>
</tr>
<tr>
<td>28</td>
<td>PA2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 2.</td>
</tr>
<tr>
<td></td>
<td>SSI0Clk</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 0 clock</td>
</tr>
<tr>
<td>29</td>
<td>PA3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 3.</td>
</tr>
<tr>
<td></td>
<td>SSI0Fss</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 0 frame signal</td>
</tr>
<tr>
<td>30</td>
<td>PA4</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 4.</td>
</tr>
<tr>
<td></td>
<td>SSI0Rx</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 0 receive</td>
</tr>
<tr>
<td>31</td>
<td>PA5</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 5.</td>
</tr>
<tr>
<td></td>
<td>SSI0Tx</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 0 transmit</td>
</tr>
<tr>
<td>32</td>
<td>VDD</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td>33</td>
<td>GND</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>Pin Number</td>
<td>Pin Name</td>
<td>Pin Type</td>
<td>Buffer Type</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>----------</td>
<td>----------</td>
<td>-------------</td>
<td>-------------</td>
</tr>
<tr>
<td>34</td>
<td>PA6</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 6.</td>
</tr>
<tr>
<td></td>
<td>I2C1SCL</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>M1PWM2</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 2. This signal is controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td>35</td>
<td>PA7</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 7.</td>
</tr>
<tr>
<td></td>
<td>I2C1SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 1 data.</td>
</tr>
<tr>
<td></td>
<td>M1PWM3</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 3. This signal is controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td>36</td>
<td>PF6</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 6.</td>
</tr>
<tr>
<td></td>
<td>I2C2SCL</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>T3CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>37</td>
<td>PF5</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 5.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT3</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 3.</td>
</tr>
<tr>
<td></td>
<td>T2CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>USB0PFLT</td>
<td>I</td>
<td>TTL</td>
<td>Optionally used in Host mode by an external power source to indicate an error state by that power source.</td>
</tr>
<tr>
<td>38</td>
<td>VDDC</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 24-12 on page 1410.</td>
</tr>
<tr>
<td>39</td>
<td>PF4</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 4.</td>
</tr>
<tr>
<td></td>
<td>IDX0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 index.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT2</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td>M1FAULT0</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>T2CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>TRD3</td>
<td>O</td>
<td>TTL</td>
<td>Trace data 3.</td>
</tr>
<tr>
<td></td>
<td>U1DTR</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Data Terminal Ready modem status input signal.</td>
</tr>
<tr>
<td></td>
<td>USB0EPEN</td>
<td>O</td>
<td>TTL</td>
<td>Optionally used in Host mode to control an external power source to supply power to the USB bus.</td>
</tr>
<tr>
<td>40</td>
<td>PF0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 0.</td>
</tr>
<tr>
<td></td>
<td>C0o</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 0 output.</td>
</tr>
<tr>
<td></td>
<td>CAN0Rx</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 0 receive.</td>
</tr>
<tr>
<td></td>
<td>M1PWM4</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 4. This signal is controlled by Module 1 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>NMI</td>
<td>I</td>
<td>TTL</td>
<td>Non-maskable interrupt.</td>
</tr>
<tr>
<td></td>
<td>PhA0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase A.</td>
</tr>
<tr>
<td></td>
<td>SSI1Rx</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>T0CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>TRD2</td>
<td>O</td>
<td>TTL</td>
<td>Trace data 2.</td>
</tr>
<tr>
<td></td>
<td>U1RTS</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Request to Send modem flow control output line.</td>
</tr>
</tbody>
</table>
Table 23-2. Signals by Pin Number (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>41</td>
<td>PF1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 1.</td>
</tr>
<tr>
<td></td>
<td>C1o</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 1 output.</td>
</tr>
<tr>
<td></td>
<td>M1PWM5</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 5. This signal is controlled by Module 1 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>PhB0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase B.</td>
</tr>
<tr>
<td></td>
<td>SS11Tx</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>T0CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 0 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>TRD1</td>
<td>O</td>
<td>TTL</td>
<td>Trace data 1.</td>
</tr>
<tr>
<td></td>
<td>U1CTS</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Clear To Send modem flow control input signal.</td>
</tr>
<tr>
<td>42</td>
<td>PF2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 2.</td>
</tr>
<tr>
<td></td>
<td>C2o</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 2 output.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT0</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>M1PWM6</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 6. This signal is controlled by Module 1 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>SS11Clk</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 clock.</td>
</tr>
<tr>
<td></td>
<td>T1CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>TRD0</td>
<td>O</td>
<td>TTL</td>
<td>Trace data 0.</td>
</tr>
<tr>
<td></td>
<td>U1DCD</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Data Carrier Detect modem status input signal.</td>
</tr>
<tr>
<td>43</td>
<td>PF3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 3.</td>
</tr>
<tr>
<td></td>
<td>CAN0Tx</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 0 transmit.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT1</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>M1PWM7</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 7. This signal is controlled by Module 1 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>SS11Fss</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 frame signal.</td>
</tr>
<tr>
<td></td>
<td>T1CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>TRCLK</td>
<td>O</td>
<td>TTL</td>
<td>Trace clock.</td>
</tr>
<tr>
<td></td>
<td>U1DSR</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Data Set Ready modem output control line.</td>
</tr>
<tr>
<td>44</td>
<td>VDD</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td>45</td>
<td>GND</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>46</td>
<td>PK3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port K bit 3.</td>
</tr>
<tr>
<td></td>
<td>M1FAULT3</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 3.</td>
</tr>
<tr>
<td></td>
<td>SS13Tx</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 3 transmit.</td>
</tr>
<tr>
<td>47</td>
<td>PK2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port K bit 2.</td>
</tr>
<tr>
<td></td>
<td>M1FAULT2</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td>SS13Rx</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 3 receive.</td>
</tr>
<tr>
<td>48</td>
<td>PK1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port K bit 1.</td>
</tr>
<tr>
<td></td>
<td>M1FAULT1</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>SS13Fss</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 frame signal.</td>
</tr>
<tr>
<td>49</td>
<td>PK0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port K bit 0.</td>
</tr>
<tr>
<td></td>
<td>M1FAULT0</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>SS13Clk</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 clock.</td>
</tr>
</tbody>
</table>
Table 23-2. Signals by Pin Number (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>WAKE</td>
<td>I</td>
<td>TTL</td>
<td>An external input that brings the processor out of Hibernate mode when asserted.</td>
</tr>
<tr>
<td>51</td>
<td>HB</td>
<td>O</td>
<td>TTL</td>
<td>An output that indicates the processor is in Hibernate mode.</td>
</tr>
<tr>
<td>52</td>
<td>XOSC0</td>
<td>I</td>
<td>Analog</td>
<td>Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 32.768-kHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC.</td>
</tr>
<tr>
<td>53</td>
<td>GNDX</td>
<td>-</td>
<td>Power</td>
<td>GND for the Hibernation oscillator. When using a crystal clock source, this pin should be connected to digital ground along with the crystal load capacitors. When using an external oscillator, this pin should be connected to digital ground.</td>
</tr>
<tr>
<td>54</td>
<td>XOSC1</td>
<td>O</td>
<td>Analog</td>
<td>Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.</td>
</tr>
<tr>
<td>55</td>
<td>VBAT</td>
<td>-</td>
<td>Power</td>
<td>Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.</td>
</tr>
<tr>
<td>56</td>
<td>VDD</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td>57</td>
<td>GND</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>58</td>
<td>PF7</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 7.</td>
</tr>
<tr>
<td></td>
<td>I2C2SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 2 data.</td>
</tr>
<tr>
<td></td>
<td>M1FAULT0</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>T3CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>59</td>
<td>PG3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 3.</td>
</tr>
<tr>
<td></td>
<td>I2C4SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 4 data.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT2</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td>M1PWM1</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 1. This signal is controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>PhA1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase A.</td>
</tr>
<tr>
<td></td>
<td>T5CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>60</td>
<td>PG2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 2.</td>
</tr>
<tr>
<td></td>
<td>I2C4SCL</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT1</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>M1PWM0</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 0. This signal is controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>T5CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>61</td>
<td>PG1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 1.</td>
</tr>
<tr>
<td></td>
<td>I2C3SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 3 data.</td>
</tr>
<tr>
<td></td>
<td>M1FAULT2</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td>PhB1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase B.</td>
</tr>
<tr>
<td></td>
<td>T4CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 1.</td>
</tr>
</tbody>
</table>
### Table 23-2. Signals by Pin Number (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>62</td>
<td>PG0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 0.</td>
</tr>
<tr>
<td></td>
<td>I2C3SCL</td>
<td>I/O</td>
<td>OD</td>
<td>I&lt;sup&gt;2&lt;/sup&gt;C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>M1FAULT1</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>PhA1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase A.</td>
</tr>
<tr>
<td></td>
<td>T4CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>63</td>
<td>RST</td>
<td>I</td>
<td>TTL</td>
<td>System reset input.</td>
</tr>
<tr>
<td>64</td>
<td>GND</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>65</td>
<td>OSC0</td>
<td>I</td>
<td>Analog</td>
<td>Main oscillator crystal input or an external clock reference input.</td>
</tr>
<tr>
<td>66</td>
<td>OSC1</td>
<td>O</td>
<td>Analog</td>
<td>Main oscillator crystal output. Leave unconnected when using a single-ended clock source.</td>
</tr>
<tr>
<td>67</td>
<td>VDD</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td>68</td>
<td>PJ0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port J bit 0. This pin is not 5-V tolerant.</td>
</tr>
<tr>
<td></td>
<td>T1CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>U4Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 4 receive.</td>
</tr>
<tr>
<td></td>
<td>USB0DM</td>
<td>I/O</td>
<td>Analog</td>
<td>Bidirectional differential data pin (D- per USB specification) for USB0.</td>
</tr>
<tr>
<td>69</td>
<td>PJ1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port J bit 1. This pin is not 5-V tolerant.</td>
</tr>
<tr>
<td></td>
<td>T1CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>U4Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 4 transmit.</td>
</tr>
<tr>
<td></td>
<td>USB0DP</td>
<td>I/O</td>
<td>Analog</td>
<td>Bidirectional differential data pin (D+ per USB specification) for USB0.</td>
</tr>
<tr>
<td>70</td>
<td>PB0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 0. This pin is not 5-V tolerant.</td>
</tr>
<tr>
<td></td>
<td>T2CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>U1Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>USB0ID</td>
<td>I</td>
<td>Analog</td>
<td>This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).</td>
</tr>
<tr>
<td>71</td>
<td>PB1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 1. This pin is not 5-V tolerant.</td>
</tr>
<tr>
<td></td>
<td>T2CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>U1Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>USB0VBUS</td>
<td>I/O</td>
<td>Analog</td>
<td>This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.</td>
</tr>
<tr>
<td>72</td>
<td>PB2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 2.</td>
</tr>
<tr>
<td></td>
<td>I2C0SCL</td>
<td>I/O</td>
<td>OD</td>
<td>I&lt;sup&gt;2&lt;/sup&gt;C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>T3CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>73</td>
<td>PB3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 3.</td>
</tr>
<tr>
<td></td>
<td>I2C0SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I&lt;sup&gt;2&lt;/sup&gt;C module 0 data.</td>
</tr>
<tr>
<td></td>
<td>T3CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 1.</td>
</tr>
</tbody>
</table>
Table 23-2. Signals by Pin Number (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>74</td>
<td>PG4</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 4.</td>
</tr>
<tr>
<td></td>
<td>I2C1SCL</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>M0PWM4</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>M1PWM2</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 2. This signal is controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>PhB1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase B.</td>
</tr>
<tr>
<td></td>
<td>U2Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 2 receive.</td>
</tr>
<tr>
<td></td>
<td>USB0EPEN</td>
<td>O</td>
<td>TTL</td>
<td>Optionally used in Host mode to control an external power source to supply power to the USB bus.</td>
</tr>
<tr>
<td></td>
<td>WT0CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>75</td>
<td>PG5</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 5.</td>
</tr>
<tr>
<td></td>
<td>I2C1SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 1 data.</td>
</tr>
<tr>
<td></td>
<td>IDX1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 index.</td>
</tr>
<tr>
<td></td>
<td>M0PWM5</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>M1PWM3</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 3. This signal is controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>U2Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 2 transmit.</td>
</tr>
<tr>
<td></td>
<td>USB0PFLT</td>
<td>I</td>
<td>TTL</td>
<td>Optionally used in Host mode by an external power source to indicate an error state by that power source.</td>
</tr>
<tr>
<td></td>
<td>WT0CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>76</td>
<td>PH7</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 7.</td>
</tr>
<tr>
<td></td>
<td>M0PWM7</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>SSI2Tx</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 2 transmit.</td>
</tr>
<tr>
<td></td>
<td>WT4CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>77</td>
<td>PH6</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 6.</td>
</tr>
<tr>
<td></td>
<td>M0PWM6</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>SSI2Rx</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 2 receive.</td>
</tr>
<tr>
<td></td>
<td>WT4CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>78</td>
<td>PH5</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 5.</td>
</tr>
<tr>
<td></td>
<td>M0PWM5</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>PhB0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase B.</td>
</tr>
<tr>
<td></td>
<td>SSI2Fss</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 frame signal.</td>
</tr>
<tr>
<td></td>
<td>WT3CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>79</td>
<td>PH4</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 4.</td>
</tr>
<tr>
<td></td>
<td>M0PWM4</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>PhA0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase A.</td>
</tr>
<tr>
<td></td>
<td>SSI2Clk</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 clock.</td>
</tr>
<tr>
<td></td>
<td>WT3CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 0.</td>
</tr>
</tbody>
</table>
Table 23-2. Signals by Pin Number (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>80</td>
<td>VDD</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td>81</td>
<td>GND</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>82</td>
<td>PC3</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 3.</td>
</tr>
<tr>
<td></td>
<td>SWO</td>
<td>O</td>
<td>TTL</td>
<td>JTAG TDO and SWO.</td>
</tr>
<tr>
<td></td>
<td>T5CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>TDO</td>
<td>O</td>
<td>TTL</td>
<td>JTAG TDO and SWO.</td>
</tr>
<tr>
<td>83</td>
<td>PC2</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 2.</td>
</tr>
<tr>
<td></td>
<td>T5CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>TDI</td>
<td>I</td>
<td>TTL</td>
<td>JTAG TDI.</td>
</tr>
<tr>
<td>84</td>
<td>PC1</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 1.</td>
</tr>
<tr>
<td></td>
<td>SWDIO</td>
<td>I/O</td>
<td>TTL</td>
<td>JTAG TMS and SWDIO.</td>
</tr>
<tr>
<td></td>
<td>T4CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>TMS</td>
<td>I</td>
<td>TTL</td>
<td>JTAG TMS and SWDIO.</td>
</tr>
<tr>
<td>85</td>
<td>PC0</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 0.</td>
</tr>
<tr>
<td></td>
<td>SWCLK</td>
<td>I</td>
<td>TTL</td>
<td>JTAG/SWD CLK.</td>
</tr>
<tr>
<td></td>
<td>T4CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>TCK</td>
<td>I</td>
<td>TTL</td>
<td>JTAG/SWD CLK.</td>
</tr>
<tr>
<td>86</td>
<td>VDDC</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 24-12 on page 1410.</td>
</tr>
<tr>
<td>87</td>
<td>PG6</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 6.</td>
</tr>
<tr>
<td></td>
<td>C2+</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 2 positive input.</td>
</tr>
<tr>
<td></td>
<td>I2C5SCL</td>
<td>I/O</td>
<td>OD</td>
<td>I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>M0PWM6</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>WT1CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>88</td>
<td>PG7</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 7.</td>
</tr>
<tr>
<td></td>
<td>C2−</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 2 negative input.</td>
</tr>
<tr>
<td></td>
<td>I2C5SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I^2C module 5 data.</td>
</tr>
<tr>
<td></td>
<td>IDX1</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 index.</td>
</tr>
<tr>
<td></td>
<td>M0PWM7</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>WT1CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>89</td>
<td>PE6</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 6.</td>
</tr>
<tr>
<td></td>
<td>AIN21</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 21.</td>
</tr>
<tr>
<td></td>
<td>CAN1Rx</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 1 receive.</td>
</tr>
<tr>
<td>90</td>
<td>PE7</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 7.</td>
</tr>
<tr>
<td></td>
<td>AIN20</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 20.</td>
</tr>
<tr>
<td></td>
<td>CAN1Tx</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>U1RI</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Ring Indicator modem status input signal.</td>
</tr>
<tr>
<td>Pin Number</td>
<td>Pin Name</td>
<td>Pin Type</td>
<td>Buffer Type</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>----------</td>
<td>----------</td>
<td>-------------</td>
<td>-------------</td>
</tr>
<tr>
<td>91</td>
<td>PB5</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 5.</td>
</tr>
<tr>
<td></td>
<td>AIN11</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 11.</td>
</tr>
<tr>
<td></td>
<td>CAN0Tx</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 0 transmit.</td>
</tr>
<tr>
<td></td>
<td>M0PWM3</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>SSI2Fss</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 frame signal.</td>
</tr>
<tr>
<td></td>
<td>T1CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>AIN10</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 10.</td>
</tr>
<tr>
<td></td>
<td>CAN0Rx</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 0 receive.</td>
</tr>
<tr>
<td></td>
<td>M0PWM2</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>SSI2Clk</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 clock.</td>
</tr>
<tr>
<td></td>
<td>T1CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>93</td>
<td>VDD</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td>94</td>
<td>PE4</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 4.</td>
</tr>
<tr>
<td></td>
<td>AIN9</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 9.</td>
</tr>
<tr>
<td></td>
<td>CAN0Rx</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 0 receive.</td>
</tr>
<tr>
<td></td>
<td>I2C2SCL</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>M0PWM4</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>M1PWM2</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 2. This signal is controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>U5Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 5 receive.</td>
</tr>
<tr>
<td>95</td>
<td>PE5</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 5.</td>
</tr>
<tr>
<td></td>
<td>AIN8</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 8.</td>
</tr>
<tr>
<td></td>
<td>CAN0Tx</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 0 transmit.</td>
</tr>
<tr>
<td></td>
<td>I2C2SDA</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 2 data.</td>
</tr>
<tr>
<td></td>
<td>M0PWM5</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>M1PWM3</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 3. This signal is controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>U5Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 5 transmit.</td>
</tr>
<tr>
<td>96</td>
<td>PD4</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 4.</td>
</tr>
<tr>
<td></td>
<td>AIN7</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 7.</td>
</tr>
<tr>
<td></td>
<td>U6Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 6 receive.</td>
</tr>
<tr>
<td></td>
<td>WT4CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>97</td>
<td>PD5</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 5.</td>
</tr>
<tr>
<td></td>
<td>AIN6</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 6.</td>
</tr>
<tr>
<td></td>
<td>U6Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 6 transmit.</td>
</tr>
<tr>
<td></td>
<td>WT4CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 1.</td>
</tr>
</tbody>
</table>
### Table 23-2. Signals by Pin Number (continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>99</td>
<td>PD6</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 6.</td>
</tr>
<tr>
<td></td>
<td>AIN5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 5.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT0</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>PhA0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase A.</td>
</tr>
<tr>
<td></td>
<td>U2Rx</td>
<td>I</td>
<td>TTL</td>
<td>UART module 2 receive.</td>
</tr>
<tr>
<td></td>
<td>WT5CCP0</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>100</td>
<td>PD7</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 7.</td>
</tr>
<tr>
<td></td>
<td>M0FAULT1</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>NMI</td>
<td>I</td>
<td>TTL</td>
<td>Non-maskable interrupt.</td>
</tr>
<tr>
<td></td>
<td>PhB0</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase B.</td>
</tr>
<tr>
<td></td>
<td>U2Tx</td>
<td>O</td>
<td>TTL</td>
<td>UART module 2 transmit.</td>
</tr>
<tr>
<td></td>
<td>WT5CCP1</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 1.</td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

### 23.2 Signals by Signal Name

### Table 23-3. Signals by Signal Name

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIN0</td>
<td>12</td>
<td>PE3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 0.</td>
</tr>
<tr>
<td>AIN1</td>
<td>13</td>
<td>PE2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 1.</td>
</tr>
<tr>
<td>AIN2</td>
<td>14</td>
<td>PE1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 2.</td>
</tr>
<tr>
<td>AIN3</td>
<td>15</td>
<td>PE0</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 3.</td>
</tr>
<tr>
<td>AIN4</td>
<td>100</td>
<td>PD7</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 4.</td>
</tr>
<tr>
<td>AIN5</td>
<td>99</td>
<td>PD6</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 5.</td>
</tr>
<tr>
<td>AIN6</td>
<td>98</td>
<td>PD5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 6.</td>
</tr>
<tr>
<td>AIN8</td>
<td>96</td>
<td>PE5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 8.</td>
</tr>
<tr>
<td>AIN11</td>
<td>91</td>
<td>PB5</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 11.</td>
</tr>
<tr>
<td>AIN12</td>
<td>4</td>
<td>PD3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 12.</td>
</tr>
<tr>
<td>AIN13</td>
<td>3</td>
<td>PD2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 13.</td>
</tr>
<tr>
<td>AIN14</td>
<td>2</td>
<td>PD1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 14.</td>
</tr>
<tr>
<td>AIN15</td>
<td>1</td>
<td>PD0</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 15.</td>
</tr>
<tr>
<td>AIN16</td>
<td>16</td>
<td>PH0</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 16.</td>
</tr>
<tr>
<td>AIN17</td>
<td>17</td>
<td>PH1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 17.</td>
</tr>
<tr>
<td>AIN18</td>
<td>18</td>
<td>PH2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 18.</td>
</tr>
<tr>
<td>AIN19</td>
<td>19</td>
<td>PH3</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 19.</td>
</tr>
<tr>
<td>AIN20</td>
<td>90</td>
<td>PE7</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 20.</td>
</tr>
<tr>
<td>AIN21</td>
<td>89</td>
<td>PE6</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 21.</td>
</tr>
<tr>
<td>Pin Name</td>
<td>Pin Number</td>
<td>Pin Mux / Pin Assignment</td>
<td>Pin Type</td>
<td>Buffer Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>--------------------------</td>
<td>----------</td>
<td>-------------</td>
<td>-------------</td>
</tr>
<tr>
<td>C0+</td>
<td>23</td>
<td>PC6</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 0 positive input.</td>
</tr>
<tr>
<td>C0−</td>
<td>22</td>
<td>PC7</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 0 negative input.</td>
</tr>
<tr>
<td>C0o</td>
<td>40</td>
<td>PF0 (9)</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 0 output.</td>
</tr>
<tr>
<td>C1+</td>
<td>24</td>
<td>PC5</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 1 positive input.</td>
</tr>
<tr>
<td>C1−</td>
<td>25</td>
<td>PC4</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 1 negative input.</td>
</tr>
<tr>
<td>C1o</td>
<td>41</td>
<td>PF1 (9)</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 1 output.</td>
</tr>
<tr>
<td>C2+</td>
<td>87</td>
<td>PG6</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 2 positive input.</td>
</tr>
<tr>
<td>C2−</td>
<td>88</td>
<td>PG7</td>
<td>I</td>
<td>Analog</td>
<td>Analog comparator 2 negative input.</td>
</tr>
<tr>
<td>C2o</td>
<td>42</td>
<td>PF2 (9)</td>
<td>O</td>
<td>TTL</td>
<td>Analog comparator 2 output.</td>
</tr>
<tr>
<td>CAN0Rx</td>
<td>40</td>
<td>PF0 (3)</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 0 receive.</td>
</tr>
<tr>
<td></td>
<td>92</td>
<td>PB4 (8)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>95</td>
<td>PE4 (8)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAN0Tx</td>
<td>43</td>
<td>PF3 (3)</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 0 transmit.</td>
</tr>
<tr>
<td></td>
<td>91</td>
<td>PB5 (8)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>96</td>
<td>PE5 (8)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAN1Rx</td>
<td>26</td>
<td>PA0 (8)</td>
<td>I</td>
<td>TTL</td>
<td>CAN module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>89</td>
<td>PE6 (8)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAN1Tx</td>
<td>27</td>
<td>PA1 (8)</td>
<td>O</td>
<td>TTL</td>
<td>CAN module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>90</td>
<td>PE7 (8)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>6</td>
<td>fixed</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
</tr>
<tr>
<td></td>
<td>21</td>
<td>fixed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>33</td>
<td>fixed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>45</td>
<td>fixed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>57</td>
<td>fixed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>64</td>
<td>fixed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>81</td>
<td>fixed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>94</td>
<td>fixed</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GNDX</td>
<td>53</td>
<td>fixed</td>
<td>-</td>
<td>Power</td>
<td>The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained in VDD from affecting the analog functions.</td>
</tr>
<tr>
<td>HB</td>
<td>51</td>
<td>fixed</td>
<td>O</td>
<td>TTL</td>
<td>An output that indicates the processor is in Hibernate mode.</td>
</tr>
<tr>
<td>I2C0SCL</td>
<td>72</td>
<td>PB2 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C0SDA</td>
<td>73</td>
<td>PB3 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 0 data.</td>
</tr>
<tr>
<td>I2C1SCL</td>
<td>34</td>
<td>PA6 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td></td>
<td>74</td>
<td>PG4 (3)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I2C1SDA</td>
<td>35</td>
<td>PA7 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 1 data.</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>PG5 (3)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 23-3. Signals by Signal Name (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C2SCL</td>
<td>36 95</td>
<td>PF6 (3) PE4 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C2SDA</td>
<td>58 96</td>
<td>PF7 (3) PE5 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 2 data.</td>
</tr>
<tr>
<td>I2C3SCL</td>
<td>1 62</td>
<td>PD0 (3) PG0 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C3SDA</td>
<td>2 61</td>
<td>PD1 (3) PG1 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 3 data.</td>
</tr>
<tr>
<td>I2C4SCL</td>
<td>60</td>
<td>PG2 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C4SDA</td>
<td>59</td>
<td>PG3 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 4 data.</td>
</tr>
<tr>
<td>I2C5SCL</td>
<td>87</td>
<td>PG6 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C5SDA</td>
<td>88</td>
<td>PG7 (3)</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 5 data.</td>
</tr>
<tr>
<td>IDX0</td>
<td>4 11 17 39</td>
<td>PD3 (6) PJ2 (5) PH1 (5) PF4 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 index.</td>
</tr>
<tr>
<td>IDX1</td>
<td>25 75 88</td>
<td>PC4 (6) PG5 (6) PG7 (5)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 index.</td>
</tr>
<tr>
<td>M0FAULT0</td>
<td>3 16 42 99</td>
<td>PD2 (4) PH0 (6) PF2 (4) PD6 (4)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 0.</td>
</tr>
<tr>
<td>M0FAULT1</td>
<td>17 43 60 100</td>
<td>PH1 (6) PF3 (4) PG2 (4) PD7 (4)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 1.</td>
</tr>
<tr>
<td>M0FAULT2</td>
<td>18 39 59</td>
<td>PH2 (6) PF4 (4) PG3 (4)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 2.</td>
</tr>
<tr>
<td>M0FAULT3</td>
<td>19 37</td>
<td>PH3 (6) PF5 (4)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 3.</td>
</tr>
<tr>
<td>M0PWM0</td>
<td>16</td>
<td>PH0 (4)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td>M0PWM1</td>
<td>17</td>
<td>PH1 (4)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td>M0PWM2</td>
<td>18 92</td>
<td>PH2 (4) PB4 (4)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.</td>
</tr>
<tr>
<td>M0PWM3</td>
<td>19 91</td>
<td>PH3 (4) PB5 (4)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.</td>
</tr>
<tr>
<td>M0PWM4</td>
<td>74 79 95</td>
<td>PG4 (4) PH4 (4) PE4 (4)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.</td>
</tr>
</tbody>
</table>
### Table 23-3. Signals by Signal Name (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type²</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0PWM5</td>
<td>75</td>
<td>PG5 (4) PH5 (4) PE5 (4)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>78</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>96</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM6</td>
<td>1</td>
<td>PD0 (4) PC4 (4) PH6 (4)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>77</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>87</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM7</td>
<td>2</td>
<td>PD1 (4) PC5 (4) PH7 (4)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>24</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>76</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>88</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT0</td>
<td>39</td>
<td>PF4 (5) PK0 (6) PF7 (5)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td>49</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>58</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT1</td>
<td>48</td>
<td>PK1 (6) PG0 (5)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td>62</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT2</td>
<td>47</td>
<td>PK2 (6) PG1 (5)</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1PWM0</td>
<td>1</td>
<td>PD0 (5) PG2 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 0. This signal is controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1PWM1</td>
<td>2</td>
<td>PD1 (5) PG3 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 1. This signal is controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td></td>
<td>59</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1PWM2</td>
<td>34</td>
<td>PA6 (5) PG4 (5) PE4 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 2. This signal is controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>74</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>95</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1PWM3</td>
<td>35</td>
<td>PA7 (5) PG5 (5) PE5 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 3. This signal is controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>96</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1PWM4</td>
<td>40</td>
<td>PF0 (5)</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 4. This signal is controlled by Module 1 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>41</td>
<td></td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 5. This signal is controlled by Module 1 PWM Generator 2.</td>
</tr>
<tr>
<td></td>
<td>42</td>
<td></td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 6. This signal is controlled by Module 1 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td>43</td>
<td></td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 7. This signal is controlled by Module 1 PWM Generator 3.</td>
</tr>
<tr>
<td>NMI</td>
<td>40</td>
<td>PF0 (8) PD7 (8)</td>
<td>I</td>
<td>TTL</td>
<td>Non-maskable interrupt.</td>
</tr>
<tr>
<td>OSC0</td>
<td>65</td>
<td>fixed</td>
<td>I</td>
<td>Analog</td>
<td>Main oscillator crystal input or an external clock reference input.</td>
</tr>
<tr>
<td>OSC1</td>
<td>66</td>
<td>fixed</td>
<td>O</td>
<td>Analog</td>
<td>Main oscillator crystal output. Leave unconnected when using a single-ended clock source.</td>
</tr>
<tr>
<td>PA0</td>
<td>26</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 0.</td>
</tr>
<tr>
<td>PA1</td>
<td>27</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 1.</td>
</tr>
<tr>
<td>PA2</td>
<td>28</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 2.</td>
</tr>
<tr>
<td>PA3</td>
<td>29</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 3.</td>
</tr>
<tr>
<td>PA4</td>
<td>30</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 4.</td>
</tr>
<tr>
<td>Pin Name</td>
<td>Pin Number</td>
<td>Pin Mux / Pin Assignment</td>
<td>Pin Type</td>
<td>Buffer Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>--------------------------</td>
<td>----------</td>
<td>-------------</td>
<td>------------------------------------</td>
</tr>
<tr>
<td>PA5</td>
<td>31</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 5.</td>
</tr>
<tr>
<td>PA6</td>
<td>34</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 6.</td>
</tr>
<tr>
<td>PA7</td>
<td>35</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port A bit 7.</td>
</tr>
<tr>
<td>PB0</td>
<td>70</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 0. This pin is not 5-V tolerant.</td>
</tr>
<tr>
<td>PB1</td>
<td>71</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 1. This pin is not 5-V tolerant.</td>
</tr>
<tr>
<td>PB2</td>
<td>72</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 2.</td>
</tr>
<tr>
<td>PB3</td>
<td>73</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 3.</td>
</tr>
<tr>
<td>PB4</td>
<td>92</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 4.</td>
</tr>
<tr>
<td>PB5</td>
<td>91</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port B bit 5.</td>
</tr>
<tr>
<td>PC0</td>
<td>85</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 0.</td>
</tr>
<tr>
<td>PC1</td>
<td>84</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 1.</td>
</tr>
<tr>
<td>PC2</td>
<td>83</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 2.</td>
</tr>
<tr>
<td>PC3</td>
<td>82</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 3.</td>
</tr>
<tr>
<td>PC4</td>
<td>25</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 4.</td>
</tr>
<tr>
<td>PC5</td>
<td>24</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 5.</td>
</tr>
<tr>
<td>PC6</td>
<td>23</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 6.</td>
</tr>
<tr>
<td>PC7</td>
<td>22</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port C bit 7.</td>
</tr>
<tr>
<td>PD0</td>
<td>1</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 0.</td>
</tr>
<tr>
<td>PD1</td>
<td>2</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 1.</td>
</tr>
<tr>
<td>PD2</td>
<td>3</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 2.</td>
</tr>
<tr>
<td>PD3</td>
<td>4</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 3.</td>
</tr>
<tr>
<td>PD4</td>
<td>97</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 4.</td>
</tr>
<tr>
<td>PD5</td>
<td>98</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 5.</td>
</tr>
<tr>
<td>PD6</td>
<td>99</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 6.</td>
</tr>
<tr>
<td>PD7</td>
<td>100</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port D bit 7.</td>
</tr>
<tr>
<td>PE0</td>
<td>15</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 0.</td>
</tr>
<tr>
<td>PE1</td>
<td>14</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 1.</td>
</tr>
<tr>
<td>PE2</td>
<td>13</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 2.</td>
</tr>
<tr>
<td>PE3</td>
<td>12</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 3.</td>
</tr>
<tr>
<td>PE4</td>
<td>95</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 4.</td>
</tr>
<tr>
<td>PE5</td>
<td>96</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 5.</td>
</tr>
<tr>
<td>PE6</td>
<td>89</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 6.</td>
</tr>
<tr>
<td>PE7</td>
<td>90</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port E bit 7.</td>
</tr>
<tr>
<td>PF0</td>
<td>40</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 0.</td>
</tr>
<tr>
<td>PF1</td>
<td>41</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 1.</td>
</tr>
<tr>
<td>PF2</td>
<td>42</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 2.</td>
</tr>
<tr>
<td>PF3</td>
<td>43</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 3.</td>
</tr>
<tr>
<td>PF4</td>
<td>39</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 4.</td>
</tr>
<tr>
<td>PF5</td>
<td>37</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 5.</td>
</tr>
<tr>
<td>PF6</td>
<td>36</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 6.</td>
</tr>
<tr>
<td>PF7</td>
<td>58</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port F bit 7.</td>
</tr>
</tbody>
</table>
### Table 23-3. Signals by Signal Name (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PG0</td>
<td>62</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 0.</td>
</tr>
<tr>
<td>PG1</td>
<td>61</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 1.</td>
</tr>
<tr>
<td>PG2</td>
<td>60</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 2.</td>
</tr>
<tr>
<td>PG3</td>
<td>59</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 3.</td>
</tr>
<tr>
<td>PG4</td>
<td>74</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 4.</td>
</tr>
<tr>
<td>PG5</td>
<td>75</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 5.</td>
</tr>
<tr>
<td>PG6</td>
<td>87</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 6.</td>
</tr>
<tr>
<td>PG7</td>
<td>88</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port G bit 7.</td>
</tr>
<tr>
<td>PH0</td>
<td>16</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 0.</td>
</tr>
<tr>
<td>PH1</td>
<td>17</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 1.</td>
</tr>
<tr>
<td>PH2</td>
<td>18</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 2.</td>
</tr>
<tr>
<td>PH3</td>
<td>19</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 3.</td>
</tr>
<tr>
<td>PH4</td>
<td>79</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 4.</td>
</tr>
<tr>
<td>PH5</td>
<td>78</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 5.</td>
</tr>
<tr>
<td>PH6</td>
<td>77</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 6.</td>
</tr>
<tr>
<td>PH7</td>
<td>76</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port H bit 7.</td>
</tr>
<tr>
<td>PhA0</td>
<td>40</td>
<td>PF0 (6) PH4 (5) PD6 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase A.</td>
</tr>
<tr>
<td>PhA1</td>
<td>24</td>
<td>PC5 (6) PG3 (6) PG0 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase A.</td>
</tr>
<tr>
<td>PhB0</td>
<td>41</td>
<td>PF1 (6) PH5 (5) PD7 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase B.</td>
</tr>
<tr>
<td>PhB1</td>
<td>23</td>
<td>PC6 (6) PG1 (6) PG4 (6)</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase B.</td>
</tr>
<tr>
<td>PJ0</td>
<td>68</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port J bit 0. This pin is not 5-V tolerant.</td>
</tr>
<tr>
<td>PJ1</td>
<td>69</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port J bit 1. This pin is not 5-V tolerant.</td>
</tr>
<tr>
<td>PJ2</td>
<td>11</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port J bit 2.</td>
</tr>
<tr>
<td>PK0</td>
<td>49</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port K bit 0.</td>
</tr>
<tr>
<td>PK1</td>
<td>48</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port K bit 1.</td>
</tr>
<tr>
<td>PK2</td>
<td>47</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port K bit 2.</td>
</tr>
<tr>
<td>PK3</td>
<td>46</td>
<td>-</td>
<td>I/O</td>
<td>TTL</td>
<td>GPIO port K bit 3.</td>
</tr>
<tr>
<td>RST</td>
<td>63</td>
<td>fixed</td>
<td>I</td>
<td>TTL</td>
<td>System reset input.</td>
</tr>
<tr>
<td>SSI0Clk</td>
<td>28</td>
<td>PA2 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 0 clock</td>
</tr>
<tr>
<td>SSI0Fss</td>
<td>29</td>
<td>PA3 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 0 frame signal</td>
</tr>
<tr>
<td>SSI0Rx</td>
<td>30</td>
<td>PA4 (2)</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 0 receive</td>
</tr>
<tr>
<td>SSI0Tx</td>
<td>31</td>
<td>PA5 (2)</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 0 transmit</td>
</tr>
<tr>
<td>SSI1Clk</td>
<td>1</td>
<td>PD0 (2) PD2 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 clock.</td>
</tr>
<tr>
<td>SSI1Fss</td>
<td>2</td>
<td>PD1 (2) PF3 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 frame signal.</td>
</tr>
</tbody>
</table>
Table 23-3. Signals by Signal Name (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSI1Rx</td>
<td>3</td>
<td>PD2 (2)</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>40</td>
<td>PF0 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSI1Tx</td>
<td>4</td>
<td>PD3 (2)</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>41</td>
<td>PF1 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSI2Clk</td>
<td>79</td>
<td>PH4 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 clock.</td>
</tr>
<tr>
<td></td>
<td>92</td>
<td>PB4 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSI2Fss</td>
<td>78</td>
<td>PH5 (2)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 frame signal.</td>
</tr>
<tr>
<td></td>
<td>91</td>
<td>PB5 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSI2Rx</td>
<td>77</td>
<td>PH6 (2)</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 2 receive.</td>
</tr>
<tr>
<td>SSI2Tx</td>
<td>76</td>
<td>PH7 (2)</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 2 transmit.</td>
</tr>
<tr>
<td>SSI3Clk</td>
<td>1</td>
<td>PD0 (1)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 clock.</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>PH0 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>49</td>
<td>PK0 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSI3Fss</td>
<td>2</td>
<td>PD1 (1)</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 frame signal.</td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>PH1 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>48</td>
<td>PK1 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSI3Rx</td>
<td>3</td>
<td>PD2 (1)</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 3 receive.</td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>PH2 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>47</td>
<td>PK2 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSI3Tx</td>
<td>4</td>
<td>PD3 (1)</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 3 transmit.</td>
</tr>
<tr>
<td></td>
<td>19</td>
<td>PH3 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>46</td>
<td>PK3 (2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SWCLK</td>
<td>85</td>
<td>PC0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>JTAG/SWD CLK.</td>
</tr>
<tr>
<td>SWDIO</td>
<td>84</td>
<td>PC1 (1)</td>
<td>I/O</td>
<td>TTL</td>
<td>JTAG TMS and SWDIO.</td>
</tr>
<tr>
<td>SWO</td>
<td>82</td>
<td>PC3 (1)</td>
<td>O</td>
<td>TTL</td>
<td>JTAG TDO and SWO.</td>
</tr>
<tr>
<td>T0CCP0</td>
<td>40</td>
<td>PF0 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T0CCP1</td>
<td>41</td>
<td>PF1 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 0 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T1CCP0</td>
<td>42</td>
<td>PF2 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>68</td>
<td>PJ0 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>92</td>
<td>PB4 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T1CCP1</td>
<td>43</td>
<td>PF3 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>69</td>
<td>PJ1 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>91</td>
<td>PB5 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T2CCP0</td>
<td>11</td>
<td>PJ2 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>39</td>
<td>PF4 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>70</td>
<td>PB0 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T2CCP1</td>
<td>37</td>
<td>PF5 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>71</td>
<td>PB1 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T3CCP0</td>
<td>36</td>
<td>PF6 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>72</td>
<td>PB2 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T3CCP1</td>
<td>58</td>
<td>PF7 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>73</td>
<td>PB3 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T4CCP0</td>
<td>62</td>
<td>PG0 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>85</td>
<td>PC0 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T4CCP1</td>
<td>61</td>
<td>PG1 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>84</td>
<td>PC1 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T5CCP0</td>
<td>60</td>
<td>PG2 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>83</td>
<td>PC2 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin Name</td>
<td>Pin Number</td>
<td>Pin Mux / Pin Assignment</td>
<td>Pin Type</td>
<td>Buffer Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>--------------------------</td>
<td>----------</td>
<td>-------------</td>
<td>-------------</td>
</tr>
<tr>
<td>T5CCP1</td>
<td>59/82</td>
<td>PG3 (7) PC3 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>TCK</td>
<td>85</td>
<td>PC0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>JTAG/SWD CLK.</td>
</tr>
<tr>
<td>TDI</td>
<td>83</td>
<td>PC2 (1)</td>
<td>I</td>
<td>TTL</td>
<td>JTAG TDI.</td>
</tr>
<tr>
<td>TDO</td>
<td>82</td>
<td>PC3 (1)</td>
<td>O</td>
<td>TTL</td>
<td>JTAG TDO and SWO.</td>
</tr>
<tr>
<td>TMS</td>
<td>84</td>
<td>PC1 (1)</td>
<td>I</td>
<td>TTL</td>
<td>JTAG TMS and SWDIO.</td>
</tr>
<tr>
<td>TRCLK</td>
<td>43</td>
<td>PF3 (14)</td>
<td>O</td>
<td>TTL</td>
<td>Trace clock.</td>
</tr>
<tr>
<td>TRD0</td>
<td>42</td>
<td>PF2 (14)</td>
<td>O</td>
<td>TTL</td>
<td>Trace data 0.</td>
</tr>
<tr>
<td>TRD1</td>
<td>41</td>
<td>PF1 (14)</td>
<td>I</td>
<td>TTL</td>
<td>Trace data 1.</td>
</tr>
<tr>
<td>TRD2</td>
<td>40</td>
<td>PF0 (14)</td>
<td>I</td>
<td>TTL</td>
<td>Trace data 2.</td>
</tr>
<tr>
<td>TRD3</td>
<td>39</td>
<td>PF4 (14)</td>
<td>O</td>
<td>TTL</td>
<td>Trace data 3.</td>
</tr>
<tr>
<td>U0Rx</td>
<td>26</td>
<td>PA0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 0 receive.</td>
</tr>
<tr>
<td>U0Tx</td>
<td>27</td>
<td>PA1 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 0 transmit.</td>
</tr>
<tr>
<td>U1CTS</td>
<td>24/41</td>
<td>PC5 (8) PF1 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Clear To Send modem flow control input signal.</td>
</tr>
<tr>
<td>U1DCD</td>
<td>42</td>
<td>PF2 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Data Carrier Detect modem status input signal.</td>
</tr>
<tr>
<td>U1DSR</td>
<td>43</td>
<td>PF3 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Data Set Ready modem output control line.</td>
</tr>
<tr>
<td>U1DTR</td>
<td>39</td>
<td>PF4 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Data Terminal Ready modem status input signal.</td>
</tr>
<tr>
<td>U1RI</td>
<td>90</td>
<td>PE7 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Ring Indicator modem status input signal.</td>
</tr>
<tr>
<td>U1RTS</td>
<td>25/40</td>
<td>PC4 (8) PF0 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Request to Send modem flow control output line.</td>
</tr>
<tr>
<td>U1Rx</td>
<td>25/70</td>
<td>PC4 (2) PB0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 receive.</td>
</tr>
<tr>
<td>U1Tx</td>
<td>24/71</td>
<td>PC5 (2) PB1 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 transmit.</td>
</tr>
<tr>
<td>U2Rx</td>
<td>74/99</td>
<td>PG4 (1) PD6 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 2 receive.</td>
</tr>
<tr>
<td>U2Tx</td>
<td>75/100</td>
<td>PG5 (1) PD7 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 2 transmit.</td>
</tr>
<tr>
<td>U3Rx</td>
<td>23</td>
<td>PC6 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 3 receive.</td>
</tr>
<tr>
<td>U3Tx</td>
<td>22</td>
<td>PC7 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 3 transmit.</td>
</tr>
<tr>
<td>U4Rx</td>
<td>25/68</td>
<td>PC4 (1) PJ0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 4 receive.</td>
</tr>
<tr>
<td>U4Tx</td>
<td>24/69</td>
<td>PC5 (1) PJ1 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 4 transmit.</td>
</tr>
<tr>
<td>U5Rx</td>
<td>11/95</td>
<td>PJ2 (1) PE4 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 5 receive.</td>
</tr>
<tr>
<td>U5Tx</td>
<td>96</td>
<td>PE5 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 5 transmit.</td>
</tr>
<tr>
<td>U6Rx</td>
<td>97</td>
<td>PD4 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 6 receive.</td>
</tr>
<tr>
<td>U6Tx</td>
<td>98</td>
<td>PD5 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 6 transmit.</td>
</tr>
<tr>
<td>U7Rx</td>
<td>15</td>
<td>PE0 (1)</td>
<td>I</td>
<td>TTL</td>
<td>UART module 7 receive.</td>
</tr>
<tr>
<td>Pin Name</td>
<td>Pin Number</td>
<td>Pin Mux / Pin Assignment</td>
<td>Pin Type</td>
<td>Buffer Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------</td>
<td>--------------------------</td>
<td>----------</td>
<td>-------------</td>
<td>-------------</td>
</tr>
<tr>
<td>UART module 7 transmit</td>
<td>14</td>
<td>PE1 (1)</td>
<td>O</td>
<td>TTL</td>
<td>UART module 7 transmit.</td>
</tr>
<tr>
<td>USB0DM</td>
<td>68</td>
<td>PJ0</td>
<td>I/O</td>
<td>Analog</td>
<td>Bidirectional differential data pin (D- per USB specification) for USB0.</td>
</tr>
<tr>
<td>USB0DP</td>
<td>69</td>
<td>PJ1</td>
<td>I/O</td>
<td>Analog</td>
<td>Bidirectional differential data pin (D+ per USB specification) for USB0.</td>
</tr>
<tr>
<td>USB0EPEN</td>
<td>3, 23, 39, 74</td>
<td>PD2 (8), PC6 (8), PF4 (8), PG4 (8)</td>
<td>O</td>
<td>TTL</td>
<td>Optionally used in Host mode to control an external power source to supply power to the USB bus.</td>
</tr>
<tr>
<td>USB0ID</td>
<td>70</td>
<td>PB0</td>
<td>I</td>
<td>Analog</td>
<td>This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).</td>
</tr>
<tr>
<td>USB0PFLT</td>
<td>4, 22, 37, 75</td>
<td>PD3 (8), PC7 (8), PF5 (8), PG5 (8)</td>
<td>I</td>
<td>TTL</td>
<td>Optionally used in Host mode by an external power source to indicate an error state by that power source.</td>
</tr>
<tr>
<td>USB0VBUS</td>
<td>71</td>
<td>PB1</td>
<td>I/O</td>
<td>Analog</td>
<td>This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.</td>
</tr>
<tr>
<td>VBAT</td>
<td>55</td>
<td>fixed</td>
<td>-</td>
<td>Power</td>
<td>Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.</td>
</tr>
<tr>
<td>VDD</td>
<td>5, 20, 32, 44, 56, 67, 80, 93</td>
<td>fixed</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
</tr>
<tr>
<td>VDDA</td>
<td>7</td>
<td>fixed</td>
<td>-</td>
<td>Power</td>
<td>The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in Table 24-5 on page 1397, regardless of system implementation.</td>
</tr>
<tr>
<td>VDDC</td>
<td>38, 86</td>
<td>fixed</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 24-12 on page 1410.</td>
</tr>
</tbody>
</table>
Table 23-3. Signals by Signal Name (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VREFA+</td>
<td>8</td>
<td>fixed</td>
<td>-</td>
<td>Analog</td>
<td>A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with VREFA−, which specifies the minimum value. The voltage that is applied to VREFA+ is the voltage with which an AIIn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in Table 24-33 on page 1426.</td>
</tr>
<tr>
<td>VREFA−</td>
<td>9</td>
<td>fixed</td>
<td>-</td>
<td>Analog</td>
<td>A reference voltage used to specify the input voltage at which the ADC converts to a minimum value. This pin is used in conjunction with VREFA+, which specifies the maximum value. In other words, the voltage that is applied to VREFA− is the voltage with which an AIIn signal is converted to 0, while the voltage that is applied to VREFA+ is the voltage with which an AIIn signal is converted to 4095. The VREFA− voltage is limited to the range specified in Table 24-33 on page 1426.</td>
</tr>
<tr>
<td>WAKE</td>
<td>50</td>
<td>fixed</td>
<td>I</td>
<td>TTL</td>
<td>An external input that brings the processor out of Hibernate mode when asserted.</td>
</tr>
<tr>
<td>WT0CCP0</td>
<td>25</td>
<td>PC4 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>74</td>
<td>PG4 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT0CCP1</td>
<td>24</td>
<td>PC5 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>75</td>
<td>PG5 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT1CCP0</td>
<td>23</td>
<td>PC6 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>87</td>
<td>PG6 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT1CCP1</td>
<td>22</td>
<td>PC7 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>88</td>
<td>PG7 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT2CCP0</td>
<td>1</td>
<td>PD0 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>PH0 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT2CCP1</td>
<td>2</td>
<td>PD1 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>PH1 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT3CCP0</td>
<td>3</td>
<td>PD2 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>79</td>
<td>PH4 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT3CCP1</td>
<td>4</td>
<td>PD3 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>78</td>
<td>PH5 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT4CCP0</td>
<td>77</td>
<td>PH6 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>97</td>
<td>PD4 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT4CCP1</td>
<td>76</td>
<td>PH7 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>98</td>
<td>PD5 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT5CCP0</td>
<td>18</td>
<td>PH2 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td></td>
<td>99</td>
<td>PD6 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WT5CCP1</td>
<td>19</td>
<td>PH3 (7)</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>PD7 (7)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XOSC0</td>
<td>52</td>
<td>fixed</td>
<td>I</td>
<td>Analog</td>
<td>Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 32.768-kHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC.</td>
</tr>
</tbody>
</table>
Table 23-3. Signals by Signal Name (continued)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Mux / Pin Assignment</th>
<th>Pin Type</th>
<th>Buffer Type(^a)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOSC1</td>
<td>54</td>
<td>fixed</td>
<td>O</td>
<td>Analog</td>
<td>Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.</td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.
### 23.3 Signals by Function, Except for GPIO

Table 23-4. Signals by Function, Except for GPIO

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AIN0</td>
<td>12</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 0.</td>
<td></td>
</tr>
<tr>
<td>AIN1</td>
<td>13</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 1.</td>
<td></td>
</tr>
<tr>
<td>AIN2</td>
<td>14</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 2.</td>
<td></td>
</tr>
<tr>
<td>AIN3</td>
<td>15</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 3.</td>
<td></td>
</tr>
<tr>
<td>AIN4</td>
<td>100</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 4.</td>
<td></td>
</tr>
<tr>
<td>AIN5</td>
<td>99</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 5.</td>
<td></td>
</tr>
<tr>
<td>AIN6</td>
<td>98</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 6.</td>
<td></td>
</tr>
<tr>
<td>AIN7</td>
<td>97</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 7.</td>
<td></td>
</tr>
<tr>
<td>AIN8</td>
<td>96</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 8.</td>
<td></td>
</tr>
<tr>
<td>AIN9</td>
<td>95</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 9.</td>
<td></td>
</tr>
<tr>
<td>AIN10</td>
<td>92</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 10.</td>
<td></td>
</tr>
<tr>
<td>AIN11</td>
<td>91</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 11.</td>
<td></td>
</tr>
<tr>
<td>AIN12</td>
<td>4</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 12.</td>
<td></td>
</tr>
<tr>
<td>AIN14</td>
<td>2</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 14.</td>
<td></td>
</tr>
<tr>
<td>AIN15</td>
<td>1</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 15.</td>
<td></td>
</tr>
<tr>
<td>AIN16</td>
<td>16</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 16.</td>
<td></td>
</tr>
<tr>
<td>AIN17</td>
<td>17</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 17.</td>
<td></td>
</tr>
<tr>
<td>AIN18</td>
<td>18</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 18.</td>
<td></td>
</tr>
<tr>
<td>AIN19</td>
<td>19</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 19.</td>
<td></td>
</tr>
<tr>
<td>AIN20</td>
<td>90</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 20.</td>
<td></td>
</tr>
<tr>
<td>AIN21</td>
<td>89</td>
<td>I</td>
<td>Analog</td>
<td>Analog-to-digital converter input 21.</td>
<td></td>
</tr>
<tr>
<td>VREFA+</td>
<td>8</td>
<td>-</td>
<td>Analog</td>
<td>A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with VREFA-, which specifies the minimum value. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in Table 24-33 on page 1426.</td>
<td></td>
</tr>
<tr>
<td>VREFA−</td>
<td>9</td>
<td>-</td>
<td>Analog</td>
<td>A reference voltage used to specify the input voltage at which the ADC converts to a minimum value. This pin is used in conjunction with VREFA+, which specifies the maximum value. In other words, the voltage that is applied to VREFA− is the voltage with which an AINn signal is converted to 0, while the voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA− voltage is limited to the range specified in Table 24-33 on page 1426.</td>
<td></td>
</tr>
<tr>
<td>Function</td>
<td>Pin Name</td>
<td>Pin Number</td>
<td>Pin Type</td>
<td>Buffer Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------------</td>
<td>----------</td>
<td>------------</td>
<td>----------</td>
<td>-------------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td><strong>Analog Comparators</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C0+</td>
<td>23</td>
<td>I</td>
<td>Analog</td>
<td></td>
<td>Analog comparator 0 positive input.</td>
</tr>
<tr>
<td>C0–</td>
<td>22</td>
<td>I</td>
<td>Analog</td>
<td></td>
<td>Analog comparator 0 negative input.</td>
</tr>
<tr>
<td>C0o</td>
<td>40</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>Analog comparator 0 output.</td>
</tr>
<tr>
<td>C1+</td>
<td>24</td>
<td>I</td>
<td>Analog</td>
<td></td>
<td>Analog comparator 1 positive input.</td>
</tr>
<tr>
<td>C1–</td>
<td>25</td>
<td>I</td>
<td>Analog</td>
<td></td>
<td>Analog comparator 1 negative input.</td>
</tr>
<tr>
<td>C1o</td>
<td>41</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>Analog comparator 1 output.</td>
</tr>
<tr>
<td>C2+</td>
<td>87</td>
<td>I</td>
<td>Analog</td>
<td></td>
<td>Analog comparator 2 positive input.</td>
</tr>
<tr>
<td>C2–</td>
<td>88</td>
<td>I</td>
<td>Analog</td>
<td></td>
<td>Analog comparator 2 negative input.</td>
</tr>
<tr>
<td>C2o</td>
<td>42</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>Analog comparator 2 output.</td>
</tr>
<tr>
<td><strong>Controller Area Network</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CAN0Rx</td>
<td>40/92/95</td>
<td>I</td>
<td>TTL</td>
<td></td>
<td>CAN module 0 receive.</td>
</tr>
<tr>
<td>CAN0Tx</td>
<td>43/91/96</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>CAN module 0 transmit.</td>
</tr>
<tr>
<td>CAN1Rx</td>
<td>26/89</td>
<td>I</td>
<td>TTL</td>
<td></td>
<td>CAN module 1 receive.</td>
</tr>
<tr>
<td>CAN1Tx</td>
<td>27/90</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>CAN module 1 transmit.</td>
</tr>
<tr>
<td><strong>Core</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TRCLK</td>
<td>43</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>Trace clock.</td>
</tr>
<tr>
<td>TRD0</td>
<td>42</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>Trace data 0.</td>
</tr>
<tr>
<td>TRD1</td>
<td>41</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>Trace data 1.</td>
</tr>
<tr>
<td>TRD2</td>
<td>40</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>Trace data 2.</td>
</tr>
<tr>
<td>TRD3</td>
<td>39</td>
<td>O</td>
<td>TTL</td>
<td></td>
<td>Trace data 3.</td>
</tr>
</tbody>
</table>
### Table 23-4. Signals by Function, Except for GPIO (continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T0CCP0</td>
<td></td>
<td>40</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T0CCP1</td>
<td></td>
<td>41</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 0 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T1CCP0</td>
<td></td>
<td>42 68 92</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T1CCP1</td>
<td></td>
<td>43 69 91</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T2CCP0</td>
<td></td>
<td>11 39 70</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T2CCP1</td>
<td></td>
<td>37 71</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T3CCP0</td>
<td></td>
<td>36 72</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T3CCP1</td>
<td></td>
<td>58 73</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T4CCP0</td>
<td></td>
<td>62 85</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T4CCP1</td>
<td></td>
<td>61 84</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 4 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>T5CCP0</td>
<td></td>
<td>60 83</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>T5CCP1</td>
<td></td>
<td>59 82</td>
<td>I/O</td>
<td>TTL</td>
<td>16/32-Bit Timer 5 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT0CCP0</td>
<td></td>
<td>25 74</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT0CCP1</td>
<td></td>
<td>24 75</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 0 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT1CCP0</td>
<td></td>
<td>23 87</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT1CCP1</td>
<td></td>
<td>22 88</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 1 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT2CCP0</td>
<td></td>
<td>1 16</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT2CCP1</td>
<td></td>
<td>2 17</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 2 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT3CCP0</td>
<td></td>
<td>3 79</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT3CCP1</td>
<td></td>
<td>4 78</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 3 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT4CCP0</td>
<td></td>
<td>77 97</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT4CCP1</td>
<td></td>
<td>76 98</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 4 Capture/Compare/PWM 1.</td>
</tr>
<tr>
<td>WT5CCP0</td>
<td></td>
<td>18 99</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 0.</td>
</tr>
<tr>
<td>WT5CCP1</td>
<td></td>
<td>19 100</td>
<td>I/O</td>
<td>TTL</td>
<td>32/64-Bit Wide Timer 5 Capture/Compare/PWM 1.</td>
</tr>
</tbody>
</table>
### Table 23-4. Signals by Function, Except for GPIO (continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hibernate</td>
<td>GNDX</td>
<td>53</td>
<td>-</td>
<td>Power</td>
<td>GND for the Hibernation oscillator. When using a crystal clock source, this pin should be connected to digital ground along with the crystal load capacitors. When using an external oscillator, this pin should be connected to digital ground.</td>
</tr>
<tr>
<td>Hibernate</td>
<td>HIB</td>
<td>51</td>
<td>O</td>
<td>TTL</td>
<td>An output that indicates the processor is in Hibernate mode.</td>
</tr>
<tr>
<td>Hibernate</td>
<td>VBAT</td>
<td>55</td>
<td>-</td>
<td>Power</td>
<td>Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.</td>
</tr>
<tr>
<td>Hibernate</td>
<td>WAKE</td>
<td>50</td>
<td>I</td>
<td>TTL</td>
<td>An external input that brings the processor out of Hibernate mode when asserted.</td>
</tr>
<tr>
<td>Hibernate</td>
<td>XOSC0</td>
<td>52</td>
<td>I</td>
<td>Analog</td>
<td>Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a 32.768-kHz crystal or a 32.768-kHz oscillator for the Hibernation module RTC.</td>
</tr>
<tr>
<td>Hibernate</td>
<td>XOSC1</td>
<td>54</td>
<td>O</td>
<td>Analog</td>
<td>Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C0SCL</td>
<td>72</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C0SDA</td>
<td>73</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 0 data.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C1SCL</td>
<td>34</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C1SDA</td>
<td>35</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 1 data.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C2SCL</td>
<td>36</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C2SDA</td>
<td>58</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 2 data.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C3SCL</td>
<td>1</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C3SDA</td>
<td>2</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 3 data.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C4SCL</td>
<td>60</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C4SDA</td>
<td>59</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 4 data.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C5SCL</td>
<td>87</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C5SDA</td>
<td>88</td>
<td>I/O</td>
<td>OD</td>
<td>I2C module 5 data.</td>
</tr>
</tbody>
</table>
### Table 23-4. Signals by Function, Except for GPIO (continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTAG/SWD/SWO</td>
<td>SWCLK</td>
<td>85</td>
<td>I</td>
<td>TTL</td>
<td>JTAG/SWD CLK.</td>
</tr>
<tr>
<td></td>
<td>SWDIO</td>
<td>84</td>
<td>I/O</td>
<td>TTL</td>
<td>JTAG TMS and SWDIO.</td>
</tr>
<tr>
<td></td>
<td>SWO</td>
<td>82</td>
<td>O</td>
<td>TTL</td>
<td>JTAG TDO and SWO.</td>
</tr>
<tr>
<td></td>
<td>TCK</td>
<td>85</td>
<td>I</td>
<td>TTL</td>
<td>JTAG/SWD CLK.</td>
</tr>
<tr>
<td></td>
<td>TDI</td>
<td>83</td>
<td>I</td>
<td>TTL</td>
<td>JTAG TDI.</td>
</tr>
<tr>
<td></td>
<td>TDO</td>
<td>82</td>
<td>O</td>
<td>TTL</td>
<td>JTAG TDO and SWO.</td>
</tr>
<tr>
<td></td>
<td>TMS</td>
<td>84</td>
<td>I</td>
<td>TTL</td>
<td>JTAG TMS and SWDIO.</td>
</tr>
</tbody>
</table>
## Table 23-4. Signals by Function, Except for GPIO (continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0FAULT0</td>
<td></td>
<td>3</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>42</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>99</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0FAULT1</td>
<td></td>
<td>17</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>43</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0FAULT2</td>
<td></td>
<td>18</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>39</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>59</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0FAULT3</td>
<td></td>
<td>19</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM Fault 3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>37</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM0</td>
<td></td>
<td>16</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 0. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td>M0PWM1</td>
<td></td>
<td>17</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 1. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td>M0PWM2</td>
<td></td>
<td>18</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 2. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>92</td>
<td></td>
<td></td>
<td>controlled by Module 0 PWM Generator 0.</td>
</tr>
<tr>
<td>M0PWM3</td>
<td></td>
<td>19</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 3. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>91</td>
<td></td>
<td></td>
<td>controlled by Module 0 PWM Generator 1.</td>
</tr>
<tr>
<td>M0PWM4</td>
<td></td>
<td>74</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 4. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>79</td>
<td></td>
<td></td>
<td>controlled by Module 0 PWM Generator 1.</td>
</tr>
<tr>
<td>M0PWM5</td>
<td></td>
<td>75</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 5. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>78</td>
<td></td>
<td></td>
<td>controlled by Module 0 PWM Generator 2.</td>
</tr>
<tr>
<td>M0PWM6</td>
<td></td>
<td>1</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 6. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td>controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>77</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>87</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M0PWM7</td>
<td></td>
<td>2</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 0 PWM 7. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>24</td>
<td></td>
<td></td>
<td>controlled by Module 0 PWM Generator 3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>76</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>88</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT0</td>
<td></td>
<td>39</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>49</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>58</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT1</td>
<td></td>
<td>48</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>62</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT2</td>
<td></td>
<td>47</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>61</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1FAULT3</td>
<td></td>
<td>46</td>
<td>I</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM Fault 3.</td>
</tr>
<tr>
<td>M1PWM0</td>
<td></td>
<td>1</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 0. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td>M1PWM1</td>
<td></td>
<td>2</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 1. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>59</td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 0.</td>
</tr>
<tr>
<td>M1PWM2</td>
<td></td>
<td>34</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 2. This signal is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>74</td>
<td></td>
<td></td>
<td>controlled by Module 1 PWM Generator 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>95</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1PWM3</td>
<td></td>
<td></td>
<td>O</td>
<td>TTL</td>
<td></td>
</tr>
</tbody>
</table>
### Table 23-4. Signals by Function, Except for GPIO (continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Motion Control Module 1 PWM 3. This signal is controlled by Module 1 PWM Generator 1.</td>
<td>35 75 96</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 4. This signal is controlled by Module 1 PWM Generator 2.</td>
<td></td>
</tr>
<tr>
<td>M1PWM4</td>
<td>40</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 5. This signal is controlled by Module 1 PWM Generator 2.</td>
<td></td>
</tr>
<tr>
<td>M1PWM5</td>
<td>41</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 6. This signal is controlled by Module 1 PWM Generator 3.</td>
<td></td>
</tr>
<tr>
<td>M1PWM6</td>
<td>42</td>
<td>O</td>
<td>TTL</td>
<td>Motion Control Module 1 PWM 7. This signal is controlled by Module 1 PWM Generator 3.</td>
<td></td>
</tr>
<tr>
<td>Ground reference for logic and I/O pins. Power-6</td>
<td>21 33 45 57 64 81 94</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>6 21 33 45 57 64 81 94</td>
<td>-</td>
<td>Power</td>
<td>Ground reference for logic and I/O pins.</td>
<td></td>
</tr>
<tr>
<td>GNDA</td>
<td>10</td>
<td>-</td>
<td>Power</td>
<td>The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>5 20 32 44 56 67 80 93</td>
<td>-</td>
<td>Power</td>
<td>Positive supply for I/O and some logic.</td>
<td></td>
</tr>
<tr>
<td>VDDA</td>
<td>7</td>
<td>-</td>
<td>Power</td>
<td>The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in Table 24-5 on page 1397, regardless of system implementation.</td>
<td></td>
</tr>
</tbody>
</table>
| VDDC              | 38 86    | -          | Power    | Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 24-12 on page 1410.
<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>QEI</td>
<td>IDX0</td>
<td>4 11 17 39</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 index.</td>
</tr>
<tr>
<td></td>
<td>IDX1</td>
<td>25 75 88</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 index.</td>
</tr>
<tr>
<td></td>
<td>PhA0</td>
<td>40 79 99</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase A.</td>
</tr>
<tr>
<td></td>
<td>PhA1</td>
<td>24 59 62</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase A.</td>
</tr>
<tr>
<td></td>
<td>PhB0</td>
<td>41 78 100</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 0 phase B.</td>
</tr>
<tr>
<td></td>
<td>PhB1</td>
<td>23 61 74</td>
<td>I</td>
<td>TTL</td>
<td>QEI module 1 phase B.</td>
</tr>
<tr>
<td>SSI</td>
<td>SSI0Clk</td>
<td>28</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 0 clock</td>
</tr>
<tr>
<td></td>
<td>SSI0Fss</td>
<td>29</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 0 frame signal</td>
</tr>
<tr>
<td></td>
<td>SSI0Rx</td>
<td>30</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 0 receive</td>
</tr>
<tr>
<td></td>
<td>SSI0Tx</td>
<td>31</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 0 transmit</td>
</tr>
<tr>
<td></td>
<td>SSI1Clk</td>
<td>1 42</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 clock.</td>
</tr>
<tr>
<td></td>
<td>SSI1Fss</td>
<td>2 43</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 1 frame signal.</td>
</tr>
<tr>
<td></td>
<td>SSI1Rx</td>
<td>3 40</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>SSI1Tx</td>
<td>4 41</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>SSI2Clk</td>
<td>79 92</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 clock.</td>
</tr>
<tr>
<td></td>
<td>SSI2Fss</td>
<td>78 91</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 2 frame signal.</td>
</tr>
<tr>
<td></td>
<td>SSI2Rx</td>
<td>77</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 2 receive.</td>
</tr>
<tr>
<td></td>
<td>SSI2Tx</td>
<td>76</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 2 transmit.</td>
</tr>
<tr>
<td></td>
<td>SSI3Clk</td>
<td>1 16 49</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 clock.</td>
</tr>
<tr>
<td></td>
<td>SSI3Fss</td>
<td>2 17 48</td>
<td>I/O</td>
<td>TTL</td>
<td>SSI module 3 frame signal.</td>
</tr>
<tr>
<td></td>
<td>SSI3Rx</td>
<td>3 18 47</td>
<td>I</td>
<td>TTL</td>
<td>SSI module 3 receive.</td>
</tr>
<tr>
<td></td>
<td>SSI3Tx</td>
<td>4 19 46</td>
<td>O</td>
<td>TTL</td>
<td>SSI module 3 transmit.</td>
</tr>
</tbody>
</table>
Table 23-4. Signals by Function, Except for GPIO (continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type²</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Control &amp; Clocks</td>
<td>NMI</td>
<td>40 100</td>
<td>I</td>
<td>TTL</td>
<td>Non-maskable interrupt.</td>
</tr>
<tr>
<td></td>
<td>OSC0</td>
<td>65</td>
<td>I</td>
<td>Analog</td>
<td>Main oscillator crystal input or an external clock reference input.</td>
</tr>
<tr>
<td></td>
<td>OSC1</td>
<td>66</td>
<td>O</td>
<td>Analog</td>
<td>Main oscillator crystal output. Leave unconnected when using a single-ended clock source.</td>
</tr>
<tr>
<td></td>
<td>RST</td>
<td>63</td>
<td>I</td>
<td>TTL</td>
<td>System reset input.</td>
</tr>
<tr>
<td>UART</td>
<td>U0Rx</td>
<td>26</td>
<td>I</td>
<td>TTL</td>
<td>UART module 0 receive.</td>
</tr>
<tr>
<td></td>
<td>U0Tx</td>
<td>27</td>
<td>O</td>
<td>TTL</td>
<td>UART module 0 transmit.</td>
</tr>
<tr>
<td></td>
<td>U1CTS</td>
<td>24 41</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Clear To Send modem flow control input signal.</td>
</tr>
<tr>
<td></td>
<td>U1DCD</td>
<td>42</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Data Carrier Detect modem status input signal.</td>
</tr>
<tr>
<td></td>
<td>U1DSR</td>
<td>43</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Data Set Ready modem output control line.</td>
</tr>
<tr>
<td></td>
<td>U1DTR</td>
<td>39</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Data Terminal Ready modem status input signal.</td>
</tr>
<tr>
<td></td>
<td>U1RI</td>
<td>90</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 Ring Indicator modem status input signal.</td>
</tr>
<tr>
<td></td>
<td>U1RTS</td>
<td>25 40</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 Request to Send modem flow control output line.</td>
</tr>
<tr>
<td></td>
<td>U1Rx</td>
<td>25 70</td>
<td>I</td>
<td>TTL</td>
<td>UART module 1 receive.</td>
</tr>
<tr>
<td></td>
<td>U1Tx</td>
<td>24 71</td>
<td>O</td>
<td>TTL</td>
<td>UART module 1 transmit.</td>
</tr>
<tr>
<td></td>
<td>U2Rx</td>
<td>74 99</td>
<td>I</td>
<td>TTL</td>
<td>UART module 2 receive.</td>
</tr>
<tr>
<td></td>
<td>U2Tx</td>
<td>75 100</td>
<td>O</td>
<td>TTL</td>
<td>UART module 2 transmit.</td>
</tr>
<tr>
<td></td>
<td>U3Rx</td>
<td>23</td>
<td>I</td>
<td>TTL</td>
<td>UART module 3 receive.</td>
</tr>
<tr>
<td></td>
<td>U3Tx</td>
<td>22</td>
<td>O</td>
<td>TTL</td>
<td>UART module 3 transmit.</td>
</tr>
<tr>
<td></td>
<td>U4Rx</td>
<td>25 68</td>
<td>I</td>
<td>TTL</td>
<td>UART module 4 receive.</td>
</tr>
<tr>
<td></td>
<td>U4Tx</td>
<td>24 69</td>
<td>O</td>
<td>TTL</td>
<td>UART module 4 transmit.</td>
</tr>
<tr>
<td></td>
<td>U5Rx</td>
<td>11 95</td>
<td>I</td>
<td>TTL</td>
<td>UART module 5 receive.</td>
</tr>
<tr>
<td></td>
<td>U5Tx</td>
<td>96</td>
<td>O</td>
<td>TTL</td>
<td>UART module 5 transmit.</td>
</tr>
<tr>
<td></td>
<td>U6Rx</td>
<td>97</td>
<td>I</td>
<td>TTL</td>
<td>UART module 6 receive.</td>
</tr>
<tr>
<td></td>
<td>U6Tx</td>
<td>98</td>
<td>O</td>
<td>TTL</td>
<td>UART module 6 transmit.</td>
</tr>
<tr>
<td></td>
<td>U7Rx</td>
<td>15</td>
<td>I</td>
<td>TTL</td>
<td>UART module 7 receive.</td>
</tr>
<tr>
<td></td>
<td>U7Tx</td>
<td>14</td>
<td>O</td>
<td>TTL</td>
<td>UART module 7 transmit.</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
Table 23-4. Signals by Function, Except for GPIO (continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Pin Name</th>
<th>Pin Number</th>
<th>Pin Type</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB0DM</td>
<td>68</td>
<td>I/O</td>
<td>Analog</td>
<td>Bidirectional differential data pin (D- per USB specification) for USB0.</td>
<td></td>
</tr>
<tr>
<td>USB0DP</td>
<td>69</td>
<td>I/O</td>
<td>Analog</td>
<td>Bidirectional differential data pin (D+ per USB specification) for USB0.</td>
<td></td>
</tr>
<tr>
<td>USB0EPEN</td>
<td>23 39 74</td>
<td>O</td>
<td>TTL</td>
<td>Optionally used in Host mode to control an external power source to supply power to the USB bus.</td>
<td></td>
</tr>
<tr>
<td>USB0ID</td>
<td>70</td>
<td>I</td>
<td>Analog</td>
<td>This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).</td>
<td></td>
</tr>
<tr>
<td>USB0PFLT</td>
<td>4 22 37 75</td>
<td>I</td>
<td>TTL</td>
<td>Optionally used in Host mode by an external power source to indicate an error state by that power source.</td>
<td></td>
</tr>
<tr>
<td>USB0VBUS</td>
<td>71</td>
<td>I/O</td>
<td>Analog</td>
<td>This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.</td>
<td></td>
</tr>
</tbody>
</table>

a. The TTL designation indicates the pin has TTL-compatible voltage levels.

### 23.4 GPIO Pins and Alternate Functions

#### Table 23-5. GPIO Pins and Alternate Functions

<table>
<thead>
<tr>
<th>IO</th>
<th>Pin</th>
<th>Analog Function</th>
<th>Digital Function (GPIOPCTL PMCx Bit Field Encoding)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 2 3 4 5 6 7 8 9 14 15</td>
</tr>
<tr>
<td>PA0</td>
<td>26</td>
<td>U0Rx</td>
<td>- - - - - - - - - CAN1Rx - - - -</td>
</tr>
<tr>
<td>PA1</td>
<td>27</td>
<td>U0Tx</td>
<td>- - - - - - - - - CAN1Tx - - - -</td>
</tr>
<tr>
<td>PA2</td>
<td>28</td>
<td>SS10Clk</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PA3</td>
<td>29</td>
<td>SS10Fss</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PA4</td>
<td>30</td>
<td>SS10Rx</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PA5</td>
<td>31</td>
<td>SS10Tx</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PA6</td>
<td>34</td>
<td>I2C1SCL</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PA7</td>
<td>35</td>
<td>I2C1SDA</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PB0</td>
<td>70</td>
<td>USB0ID</td>
<td>U1Rx - - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PB1</td>
<td>71</td>
<td>USB0BUS</td>
<td>U1Tx - - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PB2</td>
<td>72</td>
<td>I2C0SCL</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PB3</td>
<td>73</td>
<td>I2C0SDA</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PB4</td>
<td>92</td>
<td>AIN10</td>
<td>SS12Clk - - M0PWM2 - - - T1CCP0 CAN0Rx - - -</td>
</tr>
<tr>
<td>PB5</td>
<td>91</td>
<td>AIN11</td>
<td>SS12Fss - - M0PW3 - - - T1CCP1 CAN0Tx - - -</td>
</tr>
<tr>
<td>PC0</td>
<td>85</td>
<td>TCK SWCLK</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PC1</td>
<td>84</td>
<td>TMS SWDIO</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
<tr>
<td>PC2</td>
<td>83</td>
<td>TDI</td>
<td>- - - - - - - - - - - - - -</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
Table 23-5. GPIO Pins and Alternate Functions (continued)

<table>
<thead>
<tr>
<th>IO</th>
<th>Pin</th>
<th>Analog Function</th>
<th>Digital Function (GPIOCTL PMCx Bit Field Encoding)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>PC3</td>
<td>82</td>
<td>-</td>
<td>TDO</td>
</tr>
<tr>
<td>PC4</td>
<td>25</td>
<td>C1-</td>
<td>U4Rx</td>
</tr>
<tr>
<td>PC5</td>
<td>24</td>
<td>C1+</td>
<td>U4Tx</td>
</tr>
<tr>
<td>PC6</td>
<td>23</td>
<td>C0+</td>
<td>U3Rx</td>
</tr>
<tr>
<td>PC7</td>
<td>22</td>
<td>C0-</td>
<td>U3Tx</td>
</tr>
<tr>
<td>PD0</td>
<td>1</td>
<td>AIN15</td>
<td>SSI3Clk</td>
</tr>
<tr>
<td>PD1</td>
<td>2</td>
<td>AIN14</td>
<td>SSI3Fss</td>
</tr>
<tr>
<td>PD2</td>
<td>3</td>
<td>AIN13</td>
<td>SSI3Rx</td>
</tr>
<tr>
<td>PD3</td>
<td>4</td>
<td>AIN12</td>
<td>SSI3Tx</td>
</tr>
<tr>
<td>PD4</td>
<td>97</td>
<td>AIN7</td>
<td>U6Rx</td>
</tr>
<tr>
<td>PD5</td>
<td>98</td>
<td>AIN6</td>
<td>U6Tx</td>
</tr>
<tr>
<td>PD6</td>
<td>99</td>
<td>AIN5</td>
<td>U2Rx</td>
</tr>
<tr>
<td>PD7</td>
<td>100</td>
<td>AIN4</td>
<td>U2Tx</td>
</tr>
<tr>
<td>PE0</td>
<td>15</td>
<td>AIN3</td>
<td>U7Rx</td>
</tr>
<tr>
<td>PE1</td>
<td>14</td>
<td>AIN2</td>
<td>U7Tx</td>
</tr>
<tr>
<td>PE2</td>
<td>13</td>
<td>AIN1</td>
<td>-</td>
</tr>
<tr>
<td>PE3</td>
<td>12</td>
<td>AIN0</td>
<td>-</td>
</tr>
<tr>
<td>PE4</td>
<td>95</td>
<td>AIN9</td>
<td>U5Rx</td>
</tr>
<tr>
<td>PE5</td>
<td>96</td>
<td>AIN8</td>
<td>U5Tx</td>
</tr>
<tr>
<td>PE6</td>
<td>89</td>
<td>AIN21</td>
<td>-</td>
</tr>
<tr>
<td>PE7</td>
<td>90</td>
<td>AIN20</td>
<td>U1RI</td>
</tr>
<tr>
<td>PF0</td>
<td>40</td>
<td>-</td>
<td>U1RTS</td>
</tr>
<tr>
<td>PF1</td>
<td>41</td>
<td>-</td>
<td>U1CTS</td>
</tr>
<tr>
<td>PF2</td>
<td>42</td>
<td>-</td>
<td>U1DCD</td>
</tr>
<tr>
<td>PF3</td>
<td>43</td>
<td>-</td>
<td>U1DSR</td>
</tr>
<tr>
<td>PF4</td>
<td>39</td>
<td>-</td>
<td>U1DTR</td>
</tr>
<tr>
<td>PF5</td>
<td>37</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PF6</td>
<td>36</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PF7</td>
<td>58</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG0</td>
<td>62</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG1</td>
<td>61</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG2</td>
<td>60</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG3</td>
<td>59</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PG4</td>
<td>74</td>
<td>-</td>
<td>U2Rx</td>
</tr>
<tr>
<td>PG5</td>
<td>75</td>
<td>-</td>
<td>U2Tx</td>
</tr>
<tr>
<td>PG6</td>
<td>87</td>
<td>C2+</td>
<td>-</td>
</tr>
<tr>
<td>PG7</td>
<td>88</td>
<td>C2-</td>
<td>-</td>
</tr>
<tr>
<td>PH0</td>
<td>16</td>
<td>AIN16</td>
<td>SSI3Clk</td>
</tr>
<tr>
<td>PH1</td>
<td>17</td>
<td>AIN17</td>
<td>SSI3Fss</td>
</tr>
</tbody>
</table>
Table 23-5. GPIO Pins and Alternate Functions (continued)

<table>
<thead>
<tr>
<th>IO</th>
<th>Pin</th>
<th>Analog Function</th>
<th>Digital Function (GPIOPCTL PMCx Bit Field Encoding)(^a)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>PH2</td>
<td>18</td>
<td>AIN18</td>
<td>-</td>
</tr>
<tr>
<td>PH3</td>
<td>19</td>
<td>AIN19</td>
<td>-</td>
</tr>
<tr>
<td>PH4</td>
<td>79</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PH5</td>
<td>78</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PH6</td>
<td>77</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PH7</td>
<td>76</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PJ0</td>
<td>68</td>
<td>USB0DM</td>
<td>U4Rx</td>
</tr>
<tr>
<td>PJ1</td>
<td>69</td>
<td>USB0DP</td>
<td>U4Tx</td>
</tr>
<tr>
<td>PJ2</td>
<td>11</td>
<td>-</td>
<td>U5Rx</td>
</tr>
<tr>
<td>PK0</td>
<td>49</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PK1</td>
<td>48</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PK2</td>
<td>47</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>PK3</td>
<td>46</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

a. The digital signals that are shaded gray are the power-on default values for the corresponding GPIO pin. Encodings 10-13 are not used on this device.
### 23.5 Possible Pin Assignments for Alternate Functions

#### Table 23-6. Possible Pin Assignments for Alternate Functions

<table>
<thead>
<tr>
<th># of Possible Assignments</th>
<th>Alternate Function</th>
<th>GPIO Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>one</td>
<td>AIN0</td>
<td>PE3</td>
</tr>
<tr>
<td></td>
<td>AIN1</td>
<td>PE2</td>
</tr>
<tr>
<td></td>
<td>AIN10</td>
<td>PB4</td>
</tr>
<tr>
<td></td>
<td>AIN11</td>
<td>PB5</td>
</tr>
<tr>
<td></td>
<td>AIN12</td>
<td>PD3</td>
</tr>
<tr>
<td></td>
<td>AIN13</td>
<td>PD2</td>
</tr>
<tr>
<td></td>
<td>AIN14</td>
<td>PD1</td>
</tr>
<tr>
<td></td>
<td>AIN15</td>
<td>PD0</td>
</tr>
<tr>
<td></td>
<td>AIN16</td>
<td>PH0</td>
</tr>
<tr>
<td></td>
<td>AIN17</td>
<td>PH1</td>
</tr>
<tr>
<td></td>
<td>AIN18</td>
<td>PH2</td>
</tr>
<tr>
<td></td>
<td>AIN19</td>
<td>PH3</td>
</tr>
<tr>
<td></td>
<td>AIN2</td>
<td>PE1</td>
</tr>
<tr>
<td></td>
<td>AIN20</td>
<td>PE7</td>
</tr>
<tr>
<td></td>
<td>AIN21</td>
<td>PE6</td>
</tr>
<tr>
<td></td>
<td>AIN3</td>
<td>PE0</td>
</tr>
<tr>
<td></td>
<td>AIN4</td>
<td>PD7</td>
</tr>
<tr>
<td></td>
<td>AIN5</td>
<td>PD6</td>
</tr>
<tr>
<td></td>
<td>AIN6</td>
<td>PD5</td>
</tr>
<tr>
<td></td>
<td>AIN7</td>
<td>PD4</td>
</tr>
<tr>
<td></td>
<td>AIN8</td>
<td>PE5</td>
</tr>
<tr>
<td></td>
<td>AIN9</td>
<td>PE4</td>
</tr>
<tr>
<td></td>
<td>C0+</td>
<td>PC6</td>
</tr>
<tr>
<td></td>
<td>C0-</td>
<td>PC7</td>
</tr>
<tr>
<td></td>
<td>C0o</td>
<td>PF0</td>
</tr>
<tr>
<td></td>
<td>C1+</td>
<td>PC5</td>
</tr>
<tr>
<td></td>
<td>C1-</td>
<td>PC4</td>
</tr>
<tr>
<td></td>
<td>C1o</td>
<td>PF1</td>
</tr>
<tr>
<td></td>
<td>C2+</td>
<td>PG6</td>
</tr>
<tr>
<td></td>
<td>C2-</td>
<td>PG7</td>
</tr>
<tr>
<td></td>
<td>C2o</td>
<td>PF2</td>
</tr>
<tr>
<td></td>
<td>I2C0SCL</td>
<td>PB2</td>
</tr>
<tr>
<td></td>
<td>I2C0SDA</td>
<td>PB3</td>
</tr>
<tr>
<td></td>
<td>I2C4SCL</td>
<td>PG2</td>
</tr>
<tr>
<td></td>
<td>I2C4SDA</td>
<td>PG3</td>
</tr>
<tr>
<td></td>
<td>I2C5SCL</td>
<td>PG6</td>
</tr>
<tr>
<td></td>
<td>I2C5SDA</td>
<td>PG7</td>
</tr>
<tr>
<td></td>
<td>M0PWM0</td>
<td>PH0</td>
</tr>
<tr>
<td></td>
<td>M0PWM1</td>
<td>PH1</td>
</tr>
</tbody>
</table>
### Table 23-6. Possible Pin Assignments for Alternate Functions (continued)

<table>
<thead>
<tr>
<th># of Possible Assignments</th>
<th>Alternate Function</th>
<th>GPIO Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>M1FAULT3</td>
<td>PK3</td>
</tr>
<tr>
<td></td>
<td>M1PWM4</td>
<td>PF0</td>
</tr>
<tr>
<td></td>
<td>M1PWM5</td>
<td>PF1</td>
</tr>
<tr>
<td></td>
<td>M1PWM6</td>
<td>PF2</td>
</tr>
<tr>
<td></td>
<td>M1PWM7</td>
<td>PF3</td>
</tr>
<tr>
<td></td>
<td>SSI0Clk</td>
<td>PA2</td>
</tr>
<tr>
<td></td>
<td>SSI0Fss</td>
<td>PA3</td>
</tr>
<tr>
<td></td>
<td>SSI0Rx</td>
<td>PA4</td>
</tr>
<tr>
<td></td>
<td>SSI0Tx</td>
<td>PA5</td>
</tr>
<tr>
<td></td>
<td>SSI2Rx</td>
<td>PH6</td>
</tr>
<tr>
<td></td>
<td>SSI2Tx</td>
<td>PH7</td>
</tr>
<tr>
<td></td>
<td>SWCLK</td>
<td>PC0</td>
</tr>
<tr>
<td></td>
<td>SWDIO</td>
<td>PC1</td>
</tr>
<tr>
<td></td>
<td>SWO</td>
<td>PC3</td>
</tr>
<tr>
<td></td>
<td>TOCCP0</td>
<td>PF0</td>
</tr>
<tr>
<td></td>
<td>TOCCP1</td>
<td>PF1</td>
</tr>
<tr>
<td></td>
<td>TCK</td>
<td>PC0</td>
</tr>
<tr>
<td></td>
<td>TDI</td>
<td>PC2</td>
</tr>
<tr>
<td></td>
<td>TDO</td>
<td>PC3</td>
</tr>
<tr>
<td></td>
<td>TMS</td>
<td>PC1</td>
</tr>
<tr>
<td></td>
<td>TRCLK</td>
<td>PF3</td>
</tr>
<tr>
<td></td>
<td>TRD0</td>
<td>PF2</td>
</tr>
<tr>
<td></td>
<td>TRD1</td>
<td>PF1</td>
</tr>
<tr>
<td></td>
<td>TRD2</td>
<td>PF0</td>
</tr>
<tr>
<td></td>
<td>TRD3</td>
<td>PF4</td>
</tr>
<tr>
<td></td>
<td>U0Rx</td>
<td>PA0</td>
</tr>
<tr>
<td></td>
<td>U0Tx</td>
<td>PA1</td>
</tr>
<tr>
<td></td>
<td>U1DCD</td>
<td>PF2</td>
</tr>
<tr>
<td></td>
<td>U1DSR</td>
<td>PF3</td>
</tr>
<tr>
<td></td>
<td>U1DTR</td>
<td>PF4</td>
</tr>
<tr>
<td></td>
<td>U1RI</td>
<td>PE7</td>
</tr>
<tr>
<td></td>
<td>U3Rx</td>
<td>PC6</td>
</tr>
<tr>
<td></td>
<td>U3Tx</td>
<td>PC7</td>
</tr>
<tr>
<td></td>
<td>U5Tx</td>
<td>PE5</td>
</tr>
<tr>
<td></td>
<td>U6Rx</td>
<td>PD4</td>
</tr>
<tr>
<td></td>
<td>U6Tx</td>
<td>PD5</td>
</tr>
<tr>
<td></td>
<td>U7Rx</td>
<td>PE0</td>
</tr>
<tr>
<td></td>
<td>U7Tx</td>
<td>PE1</td>
</tr>
<tr>
<td></td>
<td>USB0DM</td>
<td>PJ0</td>
</tr>
<tr>
<td></td>
<td>USB0DP</td>
<td>PJ1</td>
</tr>
<tr>
<td></td>
<td>USB0ID</td>
<td>PB0</td>
</tr>
</tbody>
</table>
Table 23-6. Possible Pin Assignments for Alternate Functions (continued)

<table>
<thead>
<tr>
<th># of Possible Assignments</th>
<th>Alternate Function</th>
<th>GPIO Function</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>USB0VBUS</td>
<td>PB1</td>
</tr>
</tbody>
</table>
### Table 23-6. Possible Pin Assignments for Alternate Functions (continued)

<table>
<thead>
<tr>
<th># of Possible Assignments</th>
<th>Alternate Function</th>
<th>GPIO Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>two</td>
<td>CAN1Rx</td>
<td>PA0 PE6</td>
</tr>
<tr>
<td></td>
<td>CAN1Tx</td>
<td>PA1 PE7</td>
</tr>
<tr>
<td></td>
<td>I2C1SCL</td>
<td>PA6 PG4</td>
</tr>
<tr>
<td></td>
<td>I2C1SDA</td>
<td>PA7 PG5</td>
</tr>
<tr>
<td></td>
<td>I2C2SCL</td>
<td>PE4 PF6</td>
</tr>
<tr>
<td></td>
<td>I2C2SDA</td>
<td>PE5 PF7</td>
</tr>
<tr>
<td></td>
<td>I2C3SCL</td>
<td>PD0 PG0</td>
</tr>
<tr>
<td></td>
<td>I2C3SDA</td>
<td>PD1 PG1</td>
</tr>
<tr>
<td></td>
<td>M0FAULT3</td>
<td>PF5 PH3</td>
</tr>
<tr>
<td></td>
<td>M0PWM2</td>
<td>PB4 PH2</td>
</tr>
<tr>
<td></td>
<td>M0PWM3</td>
<td>PB5 PH3</td>
</tr>
<tr>
<td></td>
<td>M1FAULT1</td>
<td>PG0 PK1</td>
</tr>
<tr>
<td></td>
<td>M1FAULT2</td>
<td>PG1 PK2</td>
</tr>
<tr>
<td></td>
<td>M1PWM0</td>
<td>PD0 PG2</td>
</tr>
<tr>
<td></td>
<td>M1PWM1</td>
<td>PD1 PG3</td>
</tr>
<tr>
<td></td>
<td>NMI</td>
<td>PD7 PF0</td>
</tr>
<tr>
<td></td>
<td>SSI1Clk</td>
<td>PD0 PF2</td>
</tr>
<tr>
<td></td>
<td>SSI1Fss</td>
<td>PD1 PF3</td>
</tr>
<tr>
<td></td>
<td>SSI1Rx</td>
<td>PD2 PF0</td>
</tr>
<tr>
<td></td>
<td>SSI1Tx</td>
<td>PD3 PF1</td>
</tr>
<tr>
<td></td>
<td>SSI2Clk</td>
<td>PB4 PH4</td>
</tr>
<tr>
<td></td>
<td>SSI2Fss</td>
<td>PB5 PH5</td>
</tr>
<tr>
<td></td>
<td>T2CCP1</td>
<td>PB1 PF5</td>
</tr>
<tr>
<td></td>
<td>T3CCP0</td>
<td>PB2 PF6</td>
</tr>
<tr>
<td></td>
<td>T3CCP1</td>
<td>PB3 PF7</td>
</tr>
<tr>
<td></td>
<td>T4CCP0</td>
<td>PC0 PG0</td>
</tr>
<tr>
<td></td>
<td>T4CCP1</td>
<td>PC1 PG1</td>
</tr>
<tr>
<td></td>
<td>T5CCP0</td>
<td>PC2 PG2</td>
</tr>
<tr>
<td></td>
<td>T5CCP1</td>
<td>PC3 PG3</td>
</tr>
<tr>
<td></td>
<td>U1CTS</td>
<td>PC5 PF1</td>
</tr>
<tr>
<td></td>
<td>U1RTS</td>
<td>PC4 PF0</td>
</tr>
<tr>
<td></td>
<td>U1Rx</td>
<td>PB0 PC4</td>
</tr>
<tr>
<td></td>
<td>U1Tx</td>
<td>PB1 PC5</td>
</tr>
<tr>
<td></td>
<td>U2Rx</td>
<td>PD6 PG4</td>
</tr>
<tr>
<td></td>
<td>U2Tx</td>
<td>PD7 PG5</td>
</tr>
<tr>
<td></td>
<td>U4Rx</td>
<td>PC4 PJ0</td>
</tr>
<tr>
<td></td>
<td>U4Tx</td>
<td>PC5 PJ1</td>
</tr>
<tr>
<td></td>
<td>U5Rx</td>
<td>PE4 PJ2</td>
</tr>
<tr>
<td></td>
<td>WT0CCP0</td>
<td>PC4 PG4</td>
</tr>
<tr>
<td></td>
<td>WT0CCP1</td>
<td>PC5 PG5</td>
</tr>
<tr>
<td></td>
<td>WT1CCP0</td>
<td>PC6 PG6</td>
</tr>
</tbody>
</table>
### Table 23-6. Possible Pin Assignments for Alternate Functions (continued)

<table>
<thead>
<tr>
<th># of Possible Assignments</th>
<th>Alternate Function</th>
<th>GPIO Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>three</td>
<td>WT1CCP1</td>
<td>PC7 PG7</td>
</tr>
<tr>
<td></td>
<td>WT2CCP0</td>
<td>PD0 PH0</td>
</tr>
<tr>
<td></td>
<td>WT2CCP1</td>
<td>PD1 PH1</td>
</tr>
<tr>
<td></td>
<td>WT3CCP0</td>
<td>PD2 PH4</td>
</tr>
<tr>
<td></td>
<td>WT3CCP1</td>
<td>PD3 PH5</td>
</tr>
<tr>
<td></td>
<td>WT4CCP0</td>
<td>PD4 PH6</td>
</tr>
<tr>
<td></td>
<td>WT4CCP1</td>
<td>PD5 PH7</td>
</tr>
<tr>
<td></td>
<td>WT5CCP0</td>
<td>PD6 PH2</td>
</tr>
<tr>
<td></td>
<td>WT5CCP1</td>
<td>PD7 PH3</td>
</tr>
<tr>
<td></td>
<td>CAN0Rx</td>
<td>PB4 PE4 PF0</td>
</tr>
<tr>
<td></td>
<td>CAN0Tx</td>
<td>PB5 PE5 PF3</td>
</tr>
<tr>
<td></td>
<td>IDX1</td>
<td>PC4 PG5 PG7</td>
</tr>
<tr>
<td></td>
<td>M0FAULT2</td>
<td>PF4 PG3 PH2</td>
</tr>
<tr>
<td></td>
<td>M0PWM4</td>
<td>PE4 PG4 PH4</td>
</tr>
<tr>
<td></td>
<td>M0PWM5</td>
<td>PE5 PG5 PH5</td>
</tr>
<tr>
<td></td>
<td>M1FAULT0</td>
<td>PF4 PF7 PK0</td>
</tr>
<tr>
<td></td>
<td>M1PWM2</td>
<td>PA6 PE4 PG4</td>
</tr>
<tr>
<td></td>
<td>M1PWM3</td>
<td>PA7 PE5 PG5</td>
</tr>
<tr>
<td></td>
<td>PhA0</td>
<td>PD6 PF0 PH4</td>
</tr>
<tr>
<td></td>
<td>PhA1</td>
<td>PC5 PG0 PG3</td>
</tr>
<tr>
<td></td>
<td>PhB0</td>
<td>PD7 PF1 PH5</td>
</tr>
<tr>
<td></td>
<td>PhB1</td>
<td>PC6 PG1 PG4</td>
</tr>
<tr>
<td></td>
<td>SSI3Clk</td>
<td>PD0 PH0 PK0</td>
</tr>
<tr>
<td></td>
<td>SSI3Fss</td>
<td>PD1 PH1 PK1</td>
</tr>
<tr>
<td></td>
<td>SSI3Rx</td>
<td>PD2 PH2 PK2</td>
</tr>
<tr>
<td></td>
<td>SSI3Tx</td>
<td>PD3 PH3 PK3</td>
</tr>
<tr>
<td></td>
<td>T1CCP0</td>
<td>PB4 PF2 PJ0</td>
</tr>
<tr>
<td></td>
<td>T1CCP1</td>
<td>PB5 PF3 PJ1</td>
</tr>
<tr>
<td></td>
<td>T2CCP0</td>
<td>PB0 PF4 PJ2</td>
</tr>
<tr>
<td>four</td>
<td>IDX0</td>
<td>PD3 PF4 PH1 PJ2</td>
</tr>
<tr>
<td></td>
<td>M0FAULT0</td>
<td>PD2 PD6 PF2 PH0</td>
</tr>
<tr>
<td></td>
<td>M0FAULT1</td>
<td>PD7 PF3 PG2 PH1</td>
</tr>
<tr>
<td></td>
<td>M0PWM6</td>
<td>PC4 PD0 PG6 PH6</td>
</tr>
<tr>
<td></td>
<td>M0PWM7</td>
<td>PC5 PD1 PG7 PH7</td>
</tr>
<tr>
<td></td>
<td>USB0EPEN</td>
<td>PC6 PD2 PF4 PG4</td>
</tr>
<tr>
<td></td>
<td>USB0PFLT</td>
<td>PC7 PD3 PF5 PG5</td>
</tr>
</tbody>
</table>

#### 23.6 Connections for Unused Signals

Table 23-7 on page 1394 shows how to handle signals for functions that are not used in a particular system implementation for devices that are in a 100-pin LQFP package. Two options are shown in the table: an acceptable practice and a preferred practice for reduced power consumption and improved EMC characteristics. If a module is not used in a system, and its inputs are grounded, it
is important that the clock to the module is never enabled by setting the corresponding bit in the RCGCx register.

Table 23-7. Connections for Unused Signals (100-Pin LQFP)

<table>
<thead>
<tr>
<th>Function</th>
<th>Signal Name</th>
<th>Pin Number</th>
<th>Acceptable Practice</th>
<th>Preferred Practice</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO</td>
<td>All unused GPIOs</td>
<td>-</td>
<td>NC</td>
<td>GND</td>
</tr>
<tr>
<td>Hibernate</td>
<td>PIN</td>
<td>51</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td></td>
<td>VBAT</td>
<td>55</td>
<td>NC</td>
<td>VDD</td>
</tr>
<tr>
<td></td>
<td>WAKE</td>
<td>50</td>
<td>NC</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td>XOSC0</td>
<td>52</td>
<td>NC</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td>XOSC1</td>
<td>54</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td></td>
<td>GNDX</td>
<td>53</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>No Connects</td>
<td>NC</td>
<td>See NC pin numbers in Table 23-3 on page 1366</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>System Control</td>
<td>OSC0</td>
<td>65</td>
<td>NC</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td>OSC1</td>
<td>66</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td></td>
<td>RST</td>
<td>63</td>
<td>VDD</td>
<td>Pull up as shown in Figure 5-1 on page 215</td>
</tr>
<tr>
<td>USB</td>
<td>USB0DM</td>
<td>68</td>
<td>NC</td>
<td>GND</td>
</tr>
<tr>
<td></td>
<td>USB0DP</td>
<td>69</td>
<td>NC</td>
<td>GND</td>
</tr>
</tbody>
</table>
24 Electrical Characteristics

24.1 Maximum Ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Device reliability may be adversely affected by exposure to absolute-maximum ratings for extended periods.

Note: The device is not guaranteed to operate properly at the maximum ratings.

Table 24-1. Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} )</td>
<td>( V_{DD} ) supply voltage</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>( V_{DDA} )</td>
<td>( V_{DDA} ) supply voltage</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>( V_{BAT} )</td>
<td>( V_{BAT} ) battery supply voltage</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>( V_{BATRMP} )</td>
<td>( V_{BAT} ) battery supply voltage ramp time</td>
<td>0</td>
<td>0.7</td>
</tr>
<tr>
<td>( V_{IN,GPIO} )</td>
<td>Input voltage on GPIOs, regardless of whether the microcontroller is powered</td>
<td>-0.3</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td>Input voltage for PJ0, PJ1, PB0 and PB1 when configured as GPIO</td>
<td>-0.3</td>
<td>( V_{DD} + 0.3 )</td>
</tr>
<tr>
<td>( I_{GPIOMAX} )</td>
<td>Maximum current per output pin</td>
<td>-</td>
<td>25</td>
</tr>
<tr>
<td>( T_{S} )</td>
<td>Unpowered storage temperature range</td>
<td>-65</td>
<td>150</td>
</tr>
<tr>
<td>( T_{JMAX} )</td>
<td>Maximum junction temperature</td>
<td>-</td>
<td>150</td>
</tr>
</tbody>
</table>

a. Voltages are measured with respect to GND.

b. To ensure proper operation, VDDA must be powered before VDD if sourced from different supplies, or connected to the same supply as VDD. Note that the minimum operating voltage for VDD differs from the minimum operating voltage for VDDA. This change should be accounted for in the system design if both are sourced from the same supply. There is not a restriction on order for powering off.

c. Applies to static and dynamic signals including overshoot.

d. Refer to Figure 24-16 on page 1423 for a representation of the ESD protection on GPIOs.

e. For additional details, see the note on GPIO pad tolerance in “GPIO Module Characteristics” on page 1422.

Important: This device contains circuitry to protect the I/Os against damage due to high-static voltages; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (see “Connections for Unused Signals” on page 1393).

Table 24-2. ESD Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component-Level ESD Stress Voltage</td>
<td>( V_{ESDHBM} )</td>
<td>-</td>
<td>-</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>( V_{ESDCDM} )</td>
<td>-</td>
<td>-</td>
<td>500</td>
</tr>
</tbody>
</table>

a. Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges in device.

b. Level listed is passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

c. Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
24.2 Operating Characteristics

Table 24-3. Temperature Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient operating temperature range</td>
<td>T_A</td>
<td>-40 to +85 (industrial temp part)</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-40 to +105 (extended temp part)</td>
<td>°C</td>
</tr>
<tr>
<td>Case operating temperature range</td>
<td>T_C</td>
<td>-40 to +93 (industrial temp part)</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-40 to +114 (extended temp part)</td>
<td>°C</td>
</tr>
<tr>
<td>Junction operating temperature range</td>
<td>T_J</td>
<td>-40 to +95 (T_A=85°C)</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-40 to +116 (T_A=105°C)</td>
<td>°C</td>
</tr>
</tbody>
</table>

Table 24-4. Thermal Characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal resistance (junction to ambient)</td>
<td>Θ_JA</td>
<td>48.8</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal resistance (junction to board)</td>
<td>Θ_JB</td>
<td>26.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal resistance (junction to case)</td>
<td>Θ_JC</td>
<td>8.9</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal metric (junction to top of package)</td>
<td>Ψ_JT</td>
<td>0.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>Thermal metric (junction to board)</td>
<td>Ψ_JB</td>
<td>26.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction temperature formula</td>
<td>T_J</td>
<td>T_C + (P • Ψ_JT)</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_PCB + (P • Ψ_JB)^c</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_A + (P • Θ_JA)^3</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T_B + (P • Θ_JB)^ef</td>
<td>°C</td>
</tr>
</tbody>
</table>

a. For more details about thermal metrics and definitions, see the Semiconductor and IC Package Thermal Metrics Application Report (literature number SPRA953).
b. Junction to ambient thermal resistance (Θ_JA), junction to board thermal resistance (Θ_JB), and junction to case thermal resistance (Θ_JC) numbers are determined by a package simulator.
c. T_PCB is the temperature of the board acquired by following the steps listed in the EAI/JESD 51-8 standard summarized in the Semiconductor and IC Package Thermal Metrics Application Report (literature number SPRA953).
d. Because Θ_JA is highly variable and based on factors such as board design, chip/pad size, altitude, and external ambient temperature, it is recommended that equations containing Ψ_JT and Ψ_JB be used for best results.
e. T_B is temperature of the board.
f. Θ_JB is not a pure reflection of the internal resistance of the package because it includes the resistance of the testing board and environment. It is recommended that equations containing Ψ_JT and Ψ_JB be used for best results.
24.3 Recommended Operating Conditions

For special high-current applications, the GPIO output buffers may be used with the following restrictions. With the GPIO pins configured as 8-mA output drivers, a total of four GPIO outputs may be used to sink current loads up to 18 mA each. At 18-mA sink current loading, the $V_{OL}$ value is specified as 1.2 V. The high-current GPIO package pins must be selected such that there are only a maximum of two per side of the physical package with the total number of high-current GPIO outputs not exceeding four for the entire package.

Table 24-5. Recommended DC Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>$V_{DD}$ supply voltage</td>
<td>3.15</td>
<td>3.3</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDA}$</td>
<td>$V_{DDA}$ supply voltage</td>
<td>2.97</td>
<td>3.3</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDC}$</td>
<td>$V_{DDC}$ supply voltage</td>
<td>1.08</td>
<td>1.2</td>
<td>1.32</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDCDS}$</td>
<td>$V_{DDC}$ supply voltage, Deep-sleep mode</td>
<td>1.08</td>
<td>-</td>
<td>1.32</td>
<td>V</td>
</tr>
</tbody>
</table>

a. These values are valid when LDO is in operation.
b. There are peripheral timing restrictions for SSI and LPC in Deep-sleep mode. Please refer to those peripheral characteristic sections for more information.

Table 24-6. Recommended GPIO Pad Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{HI}$</td>
<td>GPIO high-level input voltage</td>
<td>0.65 * $V_{DD}$</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>GPIO low-level input voltage</td>
<td>0</td>
<td>-</td>
<td>0.35 * $V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{HYS}$</td>
<td>GPIO input hysteresis</td>
<td>0.2</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>GPIO high-level output voltage</td>
<td>2.4</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>GPIO low-level output voltage</td>
<td>-</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>

$I_{OH}$ High-level source current, $V_{OH}$=2.4 V

<table>
<thead>
<tr>
<th>2-mA Drive</th>
<th>4-mA Drive</th>
<th>8-mA Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4.0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8.0</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

$I_{OL}$ Low-level sink current, $V_{OL}$=0.4 V

<table>
<thead>
<tr>
<th>2-mA Drive</th>
<th>4-mA Drive</th>
<th>8-mA Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4.0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8.0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>8-mA Drive, $V_{OL}$=1.2 V</td>
<td>18.0</td>
<td>-</td>
</tr>
</tbody>
</table>

a. $I_O$ specifications reflect the maximum current where the corresponding output voltage meets the $V_{OH}/V_{OL}$ thresholds. $I_O$ current can exceed these limits (subject to absolute maximum ratings).

Table 24-7. GPIO Current Restrictions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{MAXL}$</td>
<td>Cumulative maximum GPIO current per side, left</td>
<td>-</td>
<td>-</td>
<td>70</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{MAXB}$</td>
<td>Cumulative maximum GPIO current per side, bottom</td>
<td>-</td>
<td>-</td>
<td>70</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{MAXR}$</td>
<td>Cumulative maximum GPIO current per side, right</td>
<td>-</td>
<td>-</td>
<td>75</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{MAXT}$</td>
<td>Cumulative maximum GPIO current per side, top</td>
<td>-</td>
<td>-</td>
<td>70</td>
<td>mA</td>
</tr>
</tbody>
</table>

a. Based on design simulations, not tested in production.
b. Sum of sink and source current for GPIOs as shown in Table 24-8 on page 1398.
### Table 24-8. GPIO Package Side Assignments

<table>
<thead>
<tr>
<th>Side</th>
<th>GPIOs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Left</td>
<td>PC[4-7], PD[0-3], PE[0-3], PH[0-3], PJ2</td>
</tr>
<tr>
<td>Bottom</td>
<td>PA[0-7], PF[0-6], PK[0-3]</td>
</tr>
<tr>
<td>Right</td>
<td>PB[0-3], PF7, PG[0-5], PJ[0-1]</td>
</tr>
<tr>
<td>Top</td>
<td>PB[4-5], PC[0-3], PD[4-7], PE[4-7], PG[6-7], PH[4-7]</td>
</tr>
</tbody>
</table>
24.4 Load Conditions

Unless otherwise specified, the following conditions are true for all timing measurements.

Figure 24-1. Load Conditions

```
C_L = 50 pF
```

GND
24.5 JTAG and Boundary Scan

Table 24-9. JTAG Characteristics

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1</td>
<td>F&lt;sub&gt;TCK&lt;/sub&gt;</td>
<td>TCK operational clock frequency&lt;sup&gt;a&lt;/sup&gt;</td>
<td>0</td>
<td>-</td>
<td>10</td>
<td>MHz</td>
</tr>
<tr>
<td>J2</td>
<td>T&lt;sub&gt;TCK&lt;/sub&gt;</td>
<td>TCK operational clock period</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>J3</td>
<td>T&lt;sub&gt;TCK_LOW&lt;/sub&gt;</td>
<td>TCK clock Low time</td>
<td>-</td>
<td>T&lt;sub&gt;TCK&lt;/sub&gt;/2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>J4</td>
<td>T&lt;sub&gt;TCK_HIGH&lt;/sub&gt;</td>
<td>TCK clock High time</td>
<td>-</td>
<td>T&lt;sub&gt;TCK&lt;/sub&gt;/2</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>J5</td>
<td>T&lt;sub&gt;TCK_R&lt;/sub&gt;</td>
<td>TCK rise time</td>
<td>0</td>
<td>-</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>J6</td>
<td>T&lt;sub&gt;TCK_F&lt;/sub&gt;</td>
<td>TCK fall time</td>
<td>0</td>
<td>-</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>J7</td>
<td>T&lt;sub&gt;TMS_SU&lt;/sub&gt;</td>
<td>TMS setup time to TCK rise</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>J8</td>
<td>T&lt;sub&gt;TMS_HLD&lt;/sub&gt;</td>
<td>TMS hold time from TCK rise</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>J9</td>
<td>T&lt;sub&gt;TDI_SU&lt;/sub&gt;</td>
<td>TDI setup time to TCK rise</td>
<td>18</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>J10</td>
<td>T&lt;sub&gt;TDI_HLD&lt;/sub&gt;</td>
<td>TDI hold time from TCK rise</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>J11</td>
<td>T&lt;sub&gt;TDO_ZDV&lt;/sub&gt;</td>
<td>TCK fall to Data Valid from High-Z (2-mA drive)</td>
<td>-</td>
<td>13</td>
<td>35</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to Data Valid from High-Z (4-mA drive)</td>
<td>-</td>
<td>9</td>
<td>26</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to Data Valid from High-Z (8-mA drive)</td>
<td>-</td>
<td>8</td>
<td>26</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to Data Valid from High-Z (8-mA drive with slew rate control)</td>
<td>-</td>
<td>10</td>
<td>29</td>
<td>ns</td>
</tr>
<tr>
<td>J12</td>
<td>T&lt;sub&gt;TDO_DV&lt;/sub&gt;</td>
<td>TCK fall to Data Valid from Data Valid (2-mA drive)</td>
<td>-</td>
<td>14</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to Data Valid from Data Valid (4-mA drive)</td>
<td>-</td>
<td>10</td>
<td>26</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to Data Valid from Data Valid (8-mA drive)</td>
<td>-</td>
<td>8</td>
<td>21</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to Data Valid from Data Valid (8-mA drive with slew rate control)</td>
<td>-</td>
<td>10</td>
<td>26</td>
<td>ns</td>
</tr>
<tr>
<td>J13</td>
<td>T&lt;sub&gt;TDO_DVZ&lt;/sub&gt;</td>
<td>TCK fall to High-Z from Data Valid (2-mA drive)</td>
<td>-</td>
<td>7</td>
<td>16</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to High-Z from Data Valid (4-mA drive)</td>
<td>-</td>
<td>7</td>
<td>16</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to High-Z from Data Valid (8-mA drive)</td>
<td>-</td>
<td>7</td>
<td>16</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TCK fall to High-Z from Data Valid (8-mA drive with slew rate control)</td>
<td>-</td>
<td>8</td>
<td>19</td>
<td>ns</td>
</tr>
</tbody>
</table>

<sup>a</sup> A ratio of at least 8:1 must be kept between the system clock and TCK.

Figure 24-2. JTAG Test Clock Input Timing
Figure 24-3. JTAG Test Access Port (TAP) Timing
### 24.6 Power and Brown-Out

#### Table 24-10. Power-On and Brown-Out Levels

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>$T_{\text{VDDA_RISE}}$</td>
<td>Analog Supply Voltage (VDDA) Rise Time</td>
<td>-</td>
<td>-</td>
<td>$\infty$</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>P2</td>
<td>$T_{\text{VDD_RISE}}$</td>
<td>I/O Supply Voltage (VDD) Rise Time</td>
<td>-</td>
<td>-</td>
<td>$\infty$</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>P3</td>
<td>$T_{\text{VDDC_RISE}}$ a</td>
<td>Core Supply Voltage (VDDC) Rise Time</td>
<td>10.00</td>
<td>-</td>
<td>150.00</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>P4</td>
<td>$V_{\text{POR}}$</td>
<td>Power-On Reset Threshold</td>
<td>2.00</td>
<td>2.30</td>
<td>2.60</td>
<td>$V$</td>
</tr>
<tr>
<td>P5</td>
<td>$V_{\text{VDDA_POK}}$</td>
<td>VDDA Power-OK Threshold (Rising Edge)</td>
<td>2.70</td>
<td>2.85</td>
<td>3.00</td>
<td>$V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDA Power-OK Threshold (Falling Edge)</td>
<td>2.71</td>
<td>2.80</td>
<td>2.89</td>
<td>$V$</td>
</tr>
<tr>
<td>P6</td>
<td>$V_{\text{VDD_POK}}$ b</td>
<td>VDD Power-OK Threshold (Rising Edge)</td>
<td>2.85</td>
<td>3.00</td>
<td>3.15</td>
<td>$V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDD Power-OK Threshold (Falling Edge)</td>
<td>2.70</td>
<td>2.78</td>
<td>2.87</td>
<td>$V$</td>
</tr>
<tr>
<td>P7</td>
<td>$V_{\text{VDD_BOR0}}$</td>
<td>Brown-Out 0 Reset Threshold</td>
<td>2.93</td>
<td>3.02</td>
<td>3.11</td>
<td>$V$</td>
</tr>
<tr>
<td>P8</td>
<td>$V_{\text{VDD_BOR1}}$</td>
<td>Brown-Out 1 Reset Threshold</td>
<td>2.83</td>
<td>2.92</td>
<td>3.01</td>
<td>$V$</td>
</tr>
<tr>
<td>P9</td>
<td>$V_{\text{VDDC_POK}}$</td>
<td>VDDC Power-OK Threshold (Rising Edge)</td>
<td>0.80</td>
<td>0.95</td>
<td>1.10</td>
<td>$V$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDC Power-OK Threshold (Falling Edge)</td>
<td>0.71</td>
<td>0.80</td>
<td>0.89</td>
<td>$V$</td>
</tr>
</tbody>
</table>

a. The MIN and MAX values are guaranteed by design assuming the external filter capacitor load is within the range of CLDO. Please refer to “On-Chip Low Drop-Out (LDO) Regulator” on page 1410 for the CLDO value.
b. Digital logic, Flash memory, and SRAM are all designed to operate at VDD voltages below 2.70 $V$. The internal POK reset protects the device from unpredictable operation on power down.

#### 24.6.1 VDDA Levels

The $V_{\text{DDA}}$ supply has two monitors:

- Power-On Reset (POR)
- Power-OK (POK)

The POR monitor is used to keep the analog circuitry in reset until the $V_{\text{DDA}}$ supply has reached the correct range for the analog circuitry to begin operating. The POK monitor is used to keep the digital circuitry in reset until the $V_{\text{DDA}}$ power supply is at an acceptable operational level. The digital Power-On Reset (Digital POR) is only released when the Power-On Reset has deasserted and all of the Power-OK monitors for each of the supplies indicate that power levels are in operational ranges.

Once the $V_{\text{DDA}}$ POK monitor has released the digital Power-On Reset on the initial power-up, voltage drops on the $V_{\text{DDA}}$ supply will only be reflected in the following bits. The digital Power-On Reset will not be re-asserted.

- $V_{\text{DDARIS}}$ bit in the Raw Interrupt Status (RIS) register (see page 244).
- $V_{\text{DDAMIS}}$ bit in the Masked Interrupt Status and Clear (MISC) register (see page 249). This bit is set only if the $V_{\text{DDAIM}}$ bit in the Interrupt Mask Control (IMC) register has been set.

Figure 24-4 on page 1403 shows the relationship between $V_{\text{DDA}}$, POR, POK, and an interrupt event.
24.6.2 VDD Levels

The V\textsubscript{DD} supply has three monitors:

- Power-OK (POK)
- Brown-Out Reset0 (BOR0)
- Brown-Out Reset1 (BOR1)

The POK monitor is used to keep the digital circuitry in reset until the V\textsubscript{DD} power supply is at an acceptable operational level. The digital Power-On Reset (Digital POR) is only released when the Power-On Reset has deasserted and all of the Power-OK monitors for each of the supplies indicate that power levels are in operational ranges. The BOR0 and the BOR1 monitors are used to generate a reset to the device or assert an interrupt if the V\textsubscript{DD} supply drops below its operational range. The BOR1 monitor's threshold is in between the BOR0 and POK thresholds.

If either a BOR0 event or a BOR1 event occurs, the following bits are affected:

- BOR0RIS or BOR1RIS bits in the Raw Interrupt Status (RIS) register (see page 244).
- BOR0MIS or BOR1MIS bits in the Masked Interrupt Status and Clear (MISC) register (see page 249). These bits are set only if the respective BOR0IM or BOR1IM bits in the Interrupt Mask Control (IMC) register have been set.
- BOR bit in the Reset Cause (RESC) register (see page 252). This bit is set only if either of the BOR0 or BOR1 events have been configured to initiate a reset.

In addition, the following bits control both the BOR0 and BOR1 events:

- BOR0IM or BOR1IM bits in the Interrupt Mask Control (IMC) register (see page 247).
- BOR0 or BOR1 bits in the Power-On and Brown-Out Reset Control (PBORCTL) register (see page 243).

Figure 24-5 on page 1404 shows the relationship between:
- $V_{DD}$, POK, and a BOR0 event
- $V_{DD}$, POK, and a BOR1 event

**Figure 24-5. Power and Brown-Out Assertions versus VDD Levels**

![Figure 24-5](image)

### 24.6.3 VDDC Levels

The $V_{DDC}$ supply has one monitor: the Power-OK (POK). The POK monitor is used to keep the digital circuitry in reset until the $V_{DDC}$ power supply is at an acceptable operational level. The digital Power-On Reset (digital POR) is only released when the Power-On Reset has deasserted and all of the Power-OK monitors for each of the supplies indicate that power levels are in operational ranges. Figure 24-6 on page 1405 shows the relationship between POK and $V_{DDC}$. 
Figure 24-6. POK assertion vs VDDC

24.6.4 VDD Glitches

Figure 24-7 on page 1405 shows the response of the BOR0, BOR1, and the POR circuit to glitches on the V\textsubscript{DD} supply.

Figure 24-7. POR-BOR0-BOR1 VDD Glitch Response

24.6.5 VDD Droop Response

Figure 24-8 on page 1406 shows the response of the BOR0, BOR1, and the POR monitors to a drop on the V\textsubscript{DD} supply.
Figure 24-8. POR-BOR0-BOR1 VDD Droop Response
## 24.7 Reset

### Table 24-11. Reset Characteristics

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>T&lt;sub&gt;DPORDLY&lt;/sub&gt;</td>
<td>Digital POR to Internal Reset assertion delay&lt;sup&gt;a&lt;/sup&gt;</td>
<td>0.80</td>
<td>-</td>
<td>5.35</td>
<td>µs</td>
</tr>
<tr>
<td>R2</td>
<td>T&lt;sub&gt;IRROUT&lt;/sub&gt;</td>
<td>Standard Internal Reset time</td>
<td>-</td>
<td>9</td>
<td>11.5</td>
<td>ms</td>
</tr>
<tr>
<td>R3</td>
<td>T&lt;sub&gt;BOR0DLY&lt;/sub&gt;</td>
<td>BOR0 to Internal Reset assertion delay&lt;sup&gt;a&lt;/sup&gt;</td>
<td>0.25</td>
<td>-</td>
<td>1.95</td>
<td>µs</td>
</tr>
<tr>
<td>R3</td>
<td>T&lt;sub&gt;BOR1DLY&lt;/sub&gt;</td>
<td>BOR1 to Internal Reset assertion delay&lt;sup&gt;a&lt;/sup&gt;</td>
<td>0.75</td>
<td>-</td>
<td>5.95</td>
<td>µs</td>
</tr>
<tr>
<td>R4</td>
<td>T&lt;sub&gt;RSTMIN&lt;/sub&gt;</td>
<td>Minimum RST pulse width</td>
<td>-</td>
<td>250</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>R5</td>
<td>T&lt;sub&gt;IRWDR&lt;/sub&gt;</td>
<td>RST to Internal Reset assertion delay</td>
<td>-</td>
<td>250</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>R6</td>
<td>T&lt;sub&gt;IRSWR&lt;/sub&gt;</td>
<td>Internal reset timeout after software-initiated system reset</td>
<td>-</td>
<td>2.07</td>
<td>-</td>
<td>µs</td>
</tr>
<tr>
<td>R7</td>
<td>T&lt;sub&gt;IRWDR&lt;/sub&gt;</td>
<td>Internal reset timeout after Watchdog reset</td>
<td>-</td>
<td>2.10</td>
<td>-</td>
<td>µs</td>
</tr>
<tr>
<td>R8</td>
<td>T&lt;sub&gt;IRMFR&lt;/sub&gt;</td>
<td>Internal reset timeout after MOSC failure reset</td>
<td>-</td>
<td>1.92</td>
<td>-</td>
<td>µs</td>
</tr>
</tbody>
</table>

<sup>a</sup> Timing values are dependent on the V<sub>DD</sub> power-down ramp rate.

<sup>b</sup> This parameter applies only in situations where a power-loss or brown-out event occurs during an EEPROM program or erase operation, and EEPROM needs to be repaired (which is a rare case). For all other sequences, there is no impact to normal Power-On Reset (POR) timing. This delay is in addition to other POR delays.

<sup>c</sup> This value represents the maximum internal reset time when the EEPROM reaches its endurance limit.

---

### Figure 24-9. Digital Power-On Reset Timing

Note: The digital Power-On Reset is only released when the analog Power-On Reset has deasserted and all of the Power-OK monitors for each of the supplies indicate that power levels are in operational ranges.
**Figure 24-10. Brown-Out Reset Timing**

![Brown-Out Reset Timing Diagram](image)

**Figure 24-11. External Reset Timing (RST)**

![External Reset Timing Diagram](image)

**Figure 24-12. Software Reset Timing**

![Software Reset Timing Diagram](image)

**Figure 24-13. Watchdog Reset Timing**

![Watchdog Reset Timing Diagram](image)
Figure 24-14. MOSC Failure Reset Timing

MOSC Fail
Reset

Reset (Internal)

R_8
## 24.8 On-Chip Low Drop-Out (LDO) Regulator

Table 24-12. LDO Regulator Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{\text{LDO}}$</td>
<td>External filter capacitor size for internal power supply$^a$</td>
<td>2.5</td>
<td>-</td>
<td>4.0</td>
<td>μF</td>
</tr>
<tr>
<td>ESR</td>
<td>Filter capacitor equivalent series resistance</td>
<td>10</td>
<td>-</td>
<td>100</td>
<td>mΩ</td>
</tr>
<tr>
<td>ESL</td>
<td>Filter capacitor equivalent series inductance</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>nH</td>
</tr>
<tr>
<td>$V_{LDO}$</td>
<td>LDO output voltage</td>
<td>1.08</td>
<td>1.2</td>
<td>1.32</td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{INRUSH}}$</td>
<td>Inrush current</td>
<td>50</td>
<td>-</td>
<td>250</td>
<td>mA</td>
</tr>
</tbody>
</table>

$^a$ The capacitor should be connected as close as possible to pin 86.
24.9 Clocks

The following sections provide specifications on the various clock sources and mode.

24.9.1 PLL Specifications

The following tables provide specifications for using the PLL.

Table 24-13. Phase Locked Loop (PLL) Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>F&lt;sub&gt;REF_XTAL&lt;/sub&gt;</td>
<td>Crystal reference</td>
<td>25&lt;sup&gt;a&lt;/sup&gt;</td>
<td>-</td>
<td>25</td>
<td>MHz</td>
</tr>
<tr>
<td>F&lt;sub&gt;REF_EXT&lt;/sub&gt;</td>
<td>External clock reference&lt;sup&gt;a&lt;/sup&gt;</td>
<td>25&lt;sup&gt;a&lt;/sup&gt;</td>
<td>-</td>
<td>25</td>
<td>MHz</td>
</tr>
<tr>
<td>F&lt;sub&gt;PLL&lt;/sub&gt;</td>
<td>PLL frequency&lt;sup&gt;b&lt;/sup&gt;</td>
<td>-</td>
<td>400</td>
<td>-</td>
<td>MHz</td>
</tr>
<tr>
<td>T&lt;sub&gt;READY&lt;/sub&gt;</td>
<td>PLL lock time, enabling the PLL</td>
<td>-</td>
<td>-</td>
<td>512 * (N+1)&lt;sup&gt;c&lt;/sup&gt;</td>
<td>reference clocks&lt;sup&gt;d&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>PLL lock time, changing the XTAL field in the RCC/RCC2 register or changing the OSCSRC between MOSC and PIOSC</td>
<td>-</td>
<td>-</td>
<td>128 * (N+1)&lt;sup&gt;c&lt;/sup&gt;</td>
<td>reference clocks&lt;sup&gt;d&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

a. If the PLL is not used, the minimum input frequency can be 4 MHz.
b. PLL frequency is automatically calculated by the hardware based on the XTAL field of the RCC register. The PLL frequency that is set by the hardware can be calculated using the values in the PLLFREQ0 and PLLFREQ1 registers.
c. N is the value in the N field in the PLLFREQ1 register.
d. A reference clock is the clock period of the crystal being used, which can be MOSC or PIOSC. For example, a 16-MHz crystal connected to MOSC yields a reference clock of 62.5 ns.

Table 24-14 on page 1411 shows the actual frequency of the PLL based on the crystal frequency used (defined by the XTAL field in the RCC register).

Table 24-14. Actual PLL Frequency

<table>
<thead>
<tr>
<th>XTAL</th>
<th>Crystal Frequency (MHz)</th>
<th>MINT</th>
<th>MFRAC</th>
<th>Q</th>
<th>N</th>
<th>PLL Multiplier</th>
<th>PLL Frequency (MHz)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x09</td>
<td>5.0</td>
<td>0x50</td>
<td>0x0</td>
<td>0x0</td>
<td>0x0</td>
<td>80</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x0A</td>
<td>5.12</td>
<td>0x9C</td>
<td>0x100</td>
<td>0x0</td>
<td>0x1</td>
<td>156.25</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x0B</td>
<td>6.0</td>
<td>0xC8</td>
<td>0x0</td>
<td>0x0</td>
<td>0x2</td>
<td>200</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x0C</td>
<td>6.144</td>
<td>0xC3</td>
<td>0x140</td>
<td>0x0</td>
<td>0x2</td>
<td>195.3125</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x0D</td>
<td>7.3728</td>
<td>0xA2</td>
<td>0x30A</td>
<td>0x0</td>
<td>0x2</td>
<td>162.7598</td>
<td>399.9984</td>
<td>0.0004%</td>
</tr>
<tr>
<td>0x0E</td>
<td>8.0</td>
<td>0x32</td>
<td>0x0</td>
<td>0x0</td>
<td>0x0</td>
<td>50</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x0F</td>
<td>8.192</td>
<td>0xC3</td>
<td>0x140</td>
<td>0x0</td>
<td>0x3</td>
<td>195.3125</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x10</td>
<td>10.0</td>
<td>0x50</td>
<td>0x0</td>
<td>0x0</td>
<td>0x1</td>
<td>80</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x11</td>
<td>12.0</td>
<td>0xC8</td>
<td>0x0</td>
<td>0x0</td>
<td>0x5</td>
<td>200</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x12</td>
<td>12.288</td>
<td>0xC3</td>
<td>0x140</td>
<td>0x0</td>
<td>0x5</td>
<td>195.3125</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x13</td>
<td>13.56</td>
<td>0xB0</td>
<td>0x3F6</td>
<td>0x0</td>
<td>0x5</td>
<td>176.9902</td>
<td>399.9979</td>
<td>0.0005%</td>
</tr>
<tr>
<td>0x14</td>
<td>14.318</td>
<td>0xC3</td>
<td>0x238</td>
<td>0x0</td>
<td>0x6</td>
<td>195.5547</td>
<td>399.9982</td>
<td>0.0005%</td>
</tr>
<tr>
<td>0x15</td>
<td>16.0</td>
<td>0x32</td>
<td>0x0</td>
<td>0x0</td>
<td>0x1</td>
<td>50</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x16</td>
<td>16.384</td>
<td>0xC3</td>
<td>0x140</td>
<td>0x0</td>
<td>0x7</td>
<td>195.3125</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x17</td>
<td>18.0</td>
<td>0xC8</td>
<td>0x0</td>
<td>0x0</td>
<td>0x8</td>
<td>200</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x18</td>
<td>20.0</td>
<td>0x50</td>
<td>0x0</td>
<td>0x0</td>
<td>0x3</td>
<td>80</td>
<td>400</td>
<td>-</td>
</tr>
<tr>
<td>0x19</td>
<td>24.0</td>
<td>0x32</td>
<td>0x0</td>
<td>0x0</td>
<td>0x2</td>
<td>50</td>
<td>400</td>
<td>-</td>
</tr>
</tbody>
</table>
Table 24-14. Actual PLL Frequency (continued)

<table>
<thead>
<tr>
<th>XTAL</th>
<th>Crystal Frequency (MHz)</th>
<th>MINT</th>
<th>MFRAC</th>
<th>Q</th>
<th>N</th>
<th>PLL Multiplier</th>
<th>PLL Frequency (MHz)</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1A</td>
<td>25</td>
<td>0x50</td>
<td>0x0</td>
<td>0x0</td>
<td>0x4</td>
<td>80</td>
<td>400</td>
<td>-</td>
</tr>
</tbody>
</table>

### 24.9.2 PIOSC Specifications

Table 24-15. PIOSC Clock Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>F&lt;sub&gt;PIOSC&lt;/sub&gt;</td>
<td>Factory calibration: Internal 16-MHz precision oscillator frequency variance across the specified voltage and temperature range when factory calibration is used</td>
<td>-</td>
<td>-</td>
<td>±3%</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Recalibration: Internal 16-MHz precision oscillator frequency variance when 7-bit recalibration is used</td>
<td>-</td>
<td>-</td>
<td>±1%</td>
<td>-</td>
</tr>
<tr>
<td>T&lt;sub&gt;START&lt;/sub&gt;</td>
<td>PIOSC startup time&lt;sup&gt;b&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>1µs</td>
<td>-</td>
</tr>
</tbody>
</table>

<sup>a</sup> ±1% is only guaranteed at the specific voltage/temperature condition where the recalibration occurs.

<sup>b</sup> PIOSC startup time is part of reset and is included in the internal reset timeout value (T<sub>RTOUT</sub>) given in Table 24-11 on page 1407. Note that the T<sub>START</sub> value is based on simulation.

### 24.9.3 Low-Frequency Internal Oscillator (LFIOSC) Specifications

Table 24-16. Low-Frequency internal Oscillator Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>F&lt;sub&gt;LFIOSC&lt;/sub&gt;</td>
<td>Low-frequency internal oscillator (LFIOSC) frequency</td>
<td>10</td>
<td>33</td>
<td>90</td>
<td>KHz</td>
</tr>
</tbody>
</table>

### 24.9.4 Hibernation Clock Source Specifications

Table 24-17. Hibernation Oscillator Input Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>F&lt;sub&gt;HIBLFIOSC&lt;/sub&gt;</td>
<td>Hibernation low frequency internal oscillator (HIB LFIOSC) frequency</td>
<td>10</td>
<td>33</td>
<td>90</td>
<td>KHz</td>
</tr>
<tr>
<td>C&lt;sub&gt;1&lt;/sub&gt;, C&lt;sub&gt;2&lt;/sub&gt;</td>
<td>External load capacitance on XOSC0, XOSC1 pins&lt;sup&gt;a&lt;/sup&gt;</td>
<td>12</td>
<td>-</td>
<td>24</td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;INSE&lt;/sub&gt;</td>
<td>Input capacitance of XOSC0 in single-ended mode</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;PKG&lt;/sub&gt;</td>
<td>Device package stray shunt capacitance&lt;sup&gt;a&lt;/sup&gt;</td>
<td>-</td>
<td>0.5</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;PCB&lt;/sub&gt;</td>
<td>PCB package stray shunt capacitance&lt;sup&gt;a&lt;/sup&gt;</td>
<td>-</td>
<td>0.5</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>C&lt;sub&gt;SHUNT&lt;/sub&gt;</td>
<td>Total shunt capacitance&lt;sup&gt;a&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>4</td>
<td>pF</td>
</tr>
<tr>
<td>ESR</td>
<td>Crystal effective series resistance, OSCDRV = 0&lt;sup&gt;b&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>kΩ</td>
</tr>
<tr>
<td>DL</td>
<td>Oscillator output drive level</td>
<td>-</td>
<td>-</td>
<td>0.25</td>
<td>µW</td>
</tr>
<tr>
<td>T&lt;sub&gt;START&lt;/sub&gt;</td>
<td>Oscillator startup time, when using a crystal&lt;sup&gt;c&lt;/sup&gt;</td>
<td>-</td>
<td>600</td>
<td>1500</td>
<td>ms</td>
</tr>
<tr>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>CMOS input high level, when using an external oscillator with Supply &gt; 3.3 V</td>
<td>2.64</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>CMOS input high level, when using an external oscillator with 1.8 V ≤ Supply ≤ 3.3 V</td>
<td>0.8</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>

<sup>a</sup> ±1% is only guaranteed at the specific voltage/temperature condition where the recalibration occurs.

<sup>b</sup> ±1% is only guaranteed at the specific voltage/temperature condition where the recalibration occurs.

<sup>c</sup> ±1% is only guaranteed at the specific voltage/temperature condition where the recalibration occurs.

June 12, 2014

Texas Instruments-Production Data
Table 24-17. Hibernation Oscillator Input Characteristics (continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>CMOS input low level, when using an external oscillator with $1.8 \text{ V} \leq \text{Supply} \leq 3.63 \text{ V}$</td>
<td>-</td>
<td>-</td>
<td>0.2 * Supply</td>
<td>V</td>
</tr>
<tr>
<td>$V_{HYS}$</td>
<td>CMOS input buffer hysteresis, when using an external oscillator with $1.8 \text{ V} \leq \text{Supply} \leq 3.63 \text{ V}$</td>
<td>360</td>
<td>960</td>
<td>1390</td>
<td>mV</td>
</tr>
<tr>
<td>$D_{CHIBOSC_EXT}$</td>
<td>External clock reference duty cycle</td>
<td>30</td>
<td>-</td>
<td>70</td>
<td>%</td>
</tr>
</tbody>
</table>

a. See information below table.
b. Crystal ESR specified by crystal manufacturer.
c. Oscillator startup time is specified from the time the oscillator is enabled to when it reaches a stable point of oscillation such that the internal clock is valid.
d. Only valid for recommended supply conditions. Measured with $\text{OSCDRV}$ bit set (high drive strength enabled, 24 pF).
e. Specification is relative to the larger of $V_{DD}$ or $V_{BAT}$.

The load capacitors added on the board, $C_1$ and $C_2$, should be chosen such that the following equation is satisfied (see Table 24-17 on page 1412 for typical values).

- $C_L = \text{load capacitance specified by crystal manufacturer}$
- $C_L = (C_1*C_2)/(C_1+C_2) + C_{PKG} + C_{PCB}$
- $C_{SHUNT} = C_{PKG} + C_{PCB} + C_0$ (total shunt capacitance seen across $\text{XOSC0, XOSC1}$)
- $C_{PKG}, C_{PCB}$ as measured across the $\text{XOSC0, XOSC1}$ pins excluding the crystal
- Clear the $\text{OSCDRV}$ bit in the $\text{Hibernation Control (HIBCTL)}$ register for $C_{1,2} \leq 18 \text{ pF}$; set the $\text{OSCDRV}$ bit for $C_{1,2} > 18 \text{ pF}$.
- $C_0 = \text{Shunt capacitance of crystal specified by the crystal manufacturer}$

24.9.5 Main Oscillator Specifications

Table 24-18. Main Oscillator Input Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{MOSC}$</td>
<td>Parallel resonance frequency</td>
<td>4$^b$</td>
<td>-</td>
<td>25</td>
<td>MHz</td>
</tr>
<tr>
<td>$C_1, C_2$</td>
<td>External load capacitance on $\text{OSC0, OSC1}$ pins$^b$</td>
<td>10</td>
<td>-</td>
<td>24</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{PKG}$</td>
<td>Device package stray shunt capacitance$^b$</td>
<td>-</td>
<td>0.5</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{PCB}$</td>
<td>PCB stray shunt capacitance$^b$</td>
<td>-</td>
<td>0.5</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{SHUNT}$</td>
<td>Total shunt capacitance$^b$</td>
<td>-</td>
<td>-</td>
<td>4</td>
<td>pF</td>
</tr>
<tr>
<td>ESR</td>
<td>Crystal effective series resistance, 4 MHz$^{cd}$</td>
<td>-</td>
<td>-</td>
<td>300</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Crystal effective series resistance, 6 MHz$^{cd}$</td>
<td>-</td>
<td>-</td>
<td>200</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Crystal effective series resistance, 8 MHz$^{cd}$</td>
<td>-</td>
<td>-</td>
<td>130</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Crystal effective series resistance, 12 MHz$^{cd}$</td>
<td>-</td>
<td>-</td>
<td>120</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Crystal effective series resistance, 16 MHz$^{cd}$</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Crystal effective series resistance, 25 MHz$^{cd}$</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>Ω</td>
</tr>
<tr>
<td>DL</td>
<td>Oscillator output drive level$^e$</td>
<td>-</td>
<td>$\text{OSCPWR}$</td>
<td>-</td>
<td>mW</td>
</tr>
<tr>
<td>$T_{START}$</td>
<td>Oscillator startup time, when using a crystal$^f$</td>
<td>-</td>
<td>-</td>
<td>18</td>
<td>ms</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>CMOS input high level, when using an external oscillator</td>
<td>0.65 * $V_{DD}$</td>
<td>-</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
</tbody>
</table>

June 12, 2014

Texas Instruments-Production Data
Table 24-18. Main Oscillator Input Characteristics (continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>CMOS input low level, when using an external oscillator</td>
<td>GND</td>
<td>-</td>
<td>0.35 $\times V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{HYS}$</td>
<td>CMOS input buffer hysteresis, when using an external oscillator</td>
<td>150</td>
<td>-</td>
<td>-</td>
<td>mV</td>
</tr>
<tr>
<td>$DC_{OSC_EXT}$</td>
<td>External clock reference duty cycle</td>
<td>45</td>
<td>-</td>
<td>55</td>
<td>%</td>
</tr>
</tbody>
</table>

a. 5 MHz is the minimum when using the PLL.
b. See information below table.
c. Crystal ESR specified by crystal manufacturer.
d. Crystal vendors can be contacted to confirm these specifications are met for a specific crystal part number if the vendors
generic crystal datasheet show limits outside of these specifications.
e. $OSC_{PWR} = (2 \times pi \times F_P \times C_L \times 2.5)^2 \times ESR / 2$. An estimation of the typical power delivered to the crystal is based on the
$C_L$, $F_P$ and ESR parameters of the crystal in the circuit as calculated by the $OSC_{PWR}$ equation. Ensure that the value
calculated for $OSC_{PWR}$ does not exceed the crystal's drive-level maximum.
f. Oscillator startup time is specified from the time the oscillator is enabled to when it reaches a stable point of oscillation
such that the internal clock is valid.

The load capacitors added on the board, $C_1$ and $C_2$, should be chosen such that the following
equation is satisfied (see Table 24-18 on page 1413 for typical values and Table 24-19 on page 1415
detailed crystal parameter information).

- $C_L = $ load capacitance specified by crystal manufacturer
- $C_L = (C_1 \times C_2) / (C_1 + C_2) + C_{SHUNT}$
- $C_{SHUNT} = C_0 + C_{PKG} + C_{PCB}$ (total shunt capacitance seen across OSC0, OSC1 crystal inputs)
- $C_{PKG}$, $C_{PCB} = $ the mutual caps as measured across the OSC0,OSC1 pins excluding the crystal.
- $C_0 = $ Shunt capacitance of crystal specified by the crystal manufacturer

Table 24-19 on page 1415 lists part numbers of crystals that have been simulated and confirmed to
operate within the specifications in Table 24-18 on page 1413. Other crystals that have nearly identical
crystal parameters can be expected to work as well.

In the table below, the crystal parameters labeled $C_0$, $C_1$ and $L_1$ are values that are obtained from
the crystal manufacturer. These numbers are usually a result of testing a relevant batch of crystals
on a network analyzer. The parameters labeled $ESR$, $DL$ and $C_L$ are maximum numbers usually
available in the data sheet for a crystal.

The table also includes three columns of Recommended Component Values. These values apply
to system board components. $C_1$ and $C_2$ are the values in pico Farads of the load capacitors that
should be put on each leg of the crystal pins to ensure oscillation at the correct frequency. $Rs$ is the
value in kΩ of a resistor that is placed in series with the crystal between the $OSC1$ pin and the crystal
pin. $Rs$ dissipates some of the power so the Max $DI$ crystal parameter is not exceeded. Only use
the recommended $C_1$, $C_2$, and $Rs$ values with the associated crystal part. The values in the table
were used in the simulation to ensure crystal startup and to determine the worst case drive level
(WC $DI$). The value in the WC $DI$ column should not be greater than the Max $DI$ Crystal parameter.
The WC $DI$ value can be used to determine if a crystal with similar parameter values but a lower
Max $DI$ value is acceptable.
<table>
<thead>
<tr>
<th>MFG</th>
<th>MFG Part#</th>
<th>Holder</th>
<th>PKG Size (mm x mm)</th>
<th>Freq (MHz)</th>
<th>Crystal Spec (Tolerance / Stability)</th>
<th>Crystal Parameters</th>
<th>Recommended Component Values</th>
<th>WC DI (μW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Typical Values</td>
<td>Max Values</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C0 (pF)</td>
<td>C1 (pF)</td>
<td>L1 (mH)</td>
</tr>
<tr>
<td>NDK</td>
<td>NX8045GB-4.000M-STD-CJL-5</td>
<td>NX8045GB</td>
<td>8 x 4.5</td>
<td>4</td>
<td>30/50 ppm</td>
<td>1.00</td>
<td>2.70</td>
<td>598.10</td>
</tr>
<tr>
<td>FOX</td>
<td>FQ1045A-4</td>
<td>2-SMD</td>
<td>10 x 4.5</td>
<td>4</td>
<td>30/30 ppm</td>
<td>1.18</td>
<td>4.05</td>
<td>396.00</td>
</tr>
<tr>
<td>NDK</td>
<td>NX8045GB-5.000M-STD-CSF-4</td>
<td>NX8045GB</td>
<td>8 x 4.5</td>
<td>5</td>
<td>30/50 ppm</td>
<td>1.00</td>
<td>2.80</td>
<td>356.50</td>
</tr>
<tr>
<td>NDK</td>
<td>NX8045GB-6.000M-STD-CSF-4</td>
<td>NX8045GB</td>
<td>8 x 4.5</td>
<td>6</td>
<td>30/50 ppm</td>
<td>1.30</td>
<td>4.10</td>
<td>173.20</td>
</tr>
<tr>
<td>FOX</td>
<td>FQ7050B-8</td>
<td>4-SMD</td>
<td>7 x 5</td>
<td>8</td>
<td>30/30 ppm</td>
<td>1.95</td>
<td>6.69</td>
<td>59.10</td>
</tr>
<tr>
<td>ECS</td>
<td>ECS-80-16-28A-TR</td>
<td>HC49/US</td>
<td>12.5 x 4.85</td>
<td>8</td>
<td>50/30 ppm</td>
<td>1.82</td>
<td>4.90</td>
<td>85.70</td>
</tr>
<tr>
<td>Abracon</td>
<td>AABMM-12.0000MHz-10-D-1-X-T</td>
<td>ABMM</td>
<td>7.2 x 5.2</td>
<td>12</td>
<td>10/20 ppm</td>
<td>2.37</td>
<td>8.85</td>
<td>20.5</td>
</tr>
<tr>
<td>NDK</td>
<td>NX3225GA-12.000MHZ-STD-CRG-2</td>
<td>NX3225GA</td>
<td>3.2 x 2.5</td>
<td>12</td>
<td>20/30 ppm</td>
<td>0.70</td>
<td>2.20</td>
<td>81.00</td>
</tr>
<tr>
<td>NDK</td>
<td>NX5032GA-12.000MHZ-LN-CD-1</td>
<td>NX5032GA</td>
<td>5 x 3.2</td>
<td>12</td>
<td>30/50 ppm</td>
<td>0.93</td>
<td>3.12</td>
<td>56.40</td>
</tr>
<tr>
<td>FOX</td>
<td>FQ5032B-12</td>
<td>4-SMD</td>
<td>5 x 3.2</td>
<td>12</td>
<td>30/30 ppm</td>
<td>1.16</td>
<td>4.16</td>
<td>42.30</td>
</tr>
<tr>
<td>Abracon</td>
<td>AABMM-16.0000MHz-10-D-1-X-T</td>
<td>ABMM</td>
<td>7.2 x 5.2</td>
<td>16</td>
<td>10/20 ppm</td>
<td>3.00</td>
<td>11.00</td>
<td>9.30</td>
</tr>
<tr>
<td>Eclip tek</td>
<td>ECX-6595-16.000M</td>
<td>HC49/UP</td>
<td>13.3 x 4.85</td>
<td>16</td>
<td>15/30 ppm</td>
<td>3.00</td>
<td>12.7</td>
<td>8.1</td>
</tr>
<tr>
<td>NDK</td>
<td>NX3225GA-16.000MHZ-STD-CRG-2</td>
<td>NX3225GA</td>
<td>3.2 x 2.5</td>
<td>16</td>
<td>20/30 ppm</td>
<td>1.00</td>
<td>2.90</td>
<td>33.90</td>
</tr>
<tr>
<td>NDK</td>
<td>NX5032GA-16.000MHZ-LN-CD-1</td>
<td>NX5032GA</td>
<td>5 x 3.2</td>
<td>16</td>
<td>30/50ppm</td>
<td>1.02</td>
<td>3.82</td>
<td>25.90</td>
</tr>
</tbody>
</table>
Table 24-19. Crystal Parameters (continued)

<table>
<thead>
<tr>
<th>MFG</th>
<th>MFG Part#</th>
<th>Holder</th>
<th>PKG Size (mm x mm)</th>
<th>Freq (MHz)</th>
<th>Crystal Spec (Tolerance / Stability)</th>
<th>Crystal Parameters</th>
<th>Recommended Component Values</th>
<th>WC DL (µW)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>C0 (pF)</td>
<td>C1 (pF)</td>
<td>L1 (mH)</td>
</tr>
<tr>
<td>ECS</td>
<td>ECS-160-9-42-CKM-TR</td>
<td>ECX-42</td>
<td>4 x 2.5</td>
<td>16</td>
<td>10/10 ppm</td>
<td>1.47</td>
<td>3.90</td>
<td>25.84</td>
</tr>
<tr>
<td>Abracon</td>
<td>AABMM-25.000MHz-10-D-1-X-T</td>
<td>ABMM</td>
<td>7.2 x 5.2</td>
<td>25</td>
<td>10/20 ppm</td>
<td>3.00</td>
<td>11.00</td>
<td>3.70</td>
</tr>
<tr>
<td>Ecliptek</td>
<td>ECX-6593-25.000M</td>
<td>HC-49/UP</td>
<td>13.3 x 4.85</td>
<td>25</td>
<td>15/30 ppm</td>
<td>3.00</td>
<td>12.8</td>
<td>3.2</td>
</tr>
<tr>
<td>NDK</td>
<td>NX3225GA-25.000MHz-STD-CRG-2</td>
<td>NX3225GA</td>
<td>3.2 x 2.5</td>
<td>25</td>
<td>20/30 ppm</td>
<td>1.10</td>
<td>4.70</td>
<td>8.70</td>
</tr>
<tr>
<td>NDK</td>
<td>NX5032GA-25.000MHz-LD-CD-1</td>
<td>NX5032GA</td>
<td>5 x 3.2</td>
<td>25</td>
<td>30/50 ppm</td>
<td>1.3</td>
<td>5.1</td>
<td>7.1</td>
</tr>
<tr>
<td>AURIS</td>
<td>Q-25.000MHz-HC3225/4-F-30-30-E-12-TR</td>
<td>HC3225/4</td>
<td>3.2 x 2.5</td>
<td>25</td>
<td>30/30 ppm</td>
<td>1.58</td>
<td>5.01</td>
<td>8.34</td>
</tr>
<tr>
<td>FOX</td>
<td>FQ50328-25</td>
<td>4-SMD</td>
<td>5 x 3.2</td>
<td>25</td>
<td>30/30 ppm</td>
<td>1.69</td>
<td>7.92</td>
<td>5.13</td>
</tr>
<tr>
<td>TXC</td>
<td>7A2570018</td>
<td>NX5032GA</td>
<td>5 x 3.2</td>
<td>25</td>
<td>20/25 ppm</td>
<td>2.0</td>
<td>6.7</td>
<td>6.1</td>
</tr>
</tbody>
</table>

a. Rs values as low as 0 Ohms can be used. Using a lower Rs value will result in the WC DL to increase towards the Max DL of the crystal.
b. Although this ESR value is outside of the recommended crystal ESR maximum for this frequency, this crystal has been simulated to confirm proper operation and is valid for use with this device.
c. Rs values as low as 500 Ohms can be used. Using a lower Rs value will result in the WC DL to increase towards the Max DL of the crystal.

Table 24-20. Supported MOSC Crystal Frequencies*

<table>
<thead>
<tr>
<th>Value</th>
<th>Crystal Frequency (MHz) Not Using the PLL</th>
<th>Crystal Frequency (MHz) Using the PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00-0x5</td>
<td>reserved</td>
<td>reserved</td>
</tr>
<tr>
<td>0x06</td>
<td>4 MHz</td>
<td>reserved</td>
</tr>
<tr>
<td>0x07</td>
<td>4.096 MHz</td>
<td>reserved</td>
</tr>
<tr>
<td>0x08</td>
<td>4.9152 MHz</td>
<td>reserved</td>
</tr>
<tr>
<td>0x09</td>
<td>5 MHz (USB)</td>
<td>5 MHz (USB)</td>
</tr>
<tr>
<td>0x0A</td>
<td>5.12 MHz</td>
<td>5.12 MHz</td>
</tr>
<tr>
<td>0x0B</td>
<td>6 MHz (USB)</td>
<td>6 MHz (USB)</td>
</tr>
<tr>
<td>0x0C</td>
<td>6.144 MHz</td>
<td>6.144 MHz</td>
</tr>
<tr>
<td>0x0D</td>
<td>7.3728 MHz</td>
<td>7.3728 MHz</td>
</tr>
<tr>
<td>0x0E</td>
<td>8 MHz (USB)</td>
<td>8 MHz (USB)</td>
</tr>
<tr>
<td>0x0F</td>
<td>8.192 MHz</td>
<td>8.192 MHz</td>
</tr>
<tr>
<td>0x10</td>
<td>10.0 MHz (USB)</td>
<td>10.0 MHz (USB)</td>
</tr>
</tbody>
</table>

*Reserved values are not supported. **Only one value per column is supported at a time. ***Values are subject to change. **Use of recommended components is recommended for best performance.
Table 24-20. Supported MOSC Crystal Frequencies (continued)

<table>
<thead>
<tr>
<th>Value</th>
<th>Crystal Frequency (MHz) Not Using the PLL</th>
<th>Crystal Frequency (MHz) Using the PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x11</td>
<td>12.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x12</td>
<td>12.288 MHz</td>
<td></td>
</tr>
<tr>
<td>0x13</td>
<td>13.56 MHz</td>
<td></td>
</tr>
<tr>
<td>0x14</td>
<td>14.31818 MHz</td>
<td></td>
</tr>
<tr>
<td>0x15</td>
<td>16.0 MHz (reset value) (USB)</td>
<td></td>
</tr>
<tr>
<td>0x16</td>
<td>16.384 MHz</td>
<td></td>
</tr>
<tr>
<td>0x17</td>
<td>18.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x18</td>
<td>20.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x19</td>
<td>24.0 MHz (USB)</td>
<td></td>
</tr>
<tr>
<td>0x1A</td>
<td>25.0 MHz (USB)</td>
<td></td>
</tr>
</tbody>
</table>

a. Frequencies that may be used with the USB interface are indicated in the table.

24.9.6 System Clock Specification with ADC Operation

Table 24-21. System Clock Characteristics with ADC Operation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fsysadc</td>
<td>System clock frequency when the ADC module is operating (when PLL is bypassed).</td>
<td>15.9952</td>
<td>16</td>
<td>16.0048</td>
<td>MHz</td>
</tr>
</tbody>
</table>

a. Clock frequency (plus jitter) must be stable inside specified range. ADC can be clocked from the PLL, directly from an external clock source, or from the PIOSC, as long as frequency absolute precision is inside specified range.

24.9.7 System Clock Specification with USB Operation

Table 24-22. System Clock Characteristics with USB Operation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fsysusb</td>
<td>System clock frequency when the USB module is operating (note that MOSC must be the clock source, either with or without using the PLL)</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>MHz</td>
</tr>
</tbody>
</table>
24.10 Sleep Modes

Table 24-23. Sleep Modes AC Characteristics\(^a\)

<table>
<thead>
<tr>
<th>Parameter No</th>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>(T_{\text{WAKE_S}})</td>
<td>Time to wake from interrupt in sleep mode(^b)</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>system clocks</td>
</tr>
<tr>
<td></td>
<td>(T_{\text{WAKE_DS}})</td>
<td>Time to wake from interrupt in deep-sleep mode, using PIOSC for both Run mode and Deep-sleep mode(^b)(^c)</td>
<td>-</td>
<td>1.25</td>
<td>-</td>
<td>(\mu s)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Time to wake from interrupt in deep-sleep mode, using PIOSC for Run mode and LFIOSC for Deep-sleep mode(^b)(^c)</td>
<td>-</td>
<td>350</td>
<td>-</td>
<td>(\mu s)</td>
</tr>
<tr>
<td>D2</td>
<td>(T_{\text{WAKE_PLL_DS}})</td>
<td>Time to wake from interrupt in deep-sleep mode when using the PLL(^b)</td>
<td>-</td>
<td>-</td>
<td>(T_{\text{READY}})</td>
<td>ms</td>
</tr>
</tbody>
</table>

\(^a\) Values in this table assume the LFIOSC is the clock source during sleep or deep-sleep mode.

\(^b\) Specified from registering the interrupt to first instruction.

\(^c\) If the main oscillator is used for run mode, add the main oscillator startup time, \(T_{\text{START}}\).

Table 24-24. Time to Wake with Respect to Low-Power Modes\(^ab\)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Run Mode Clock/Frequency</th>
<th>Sleep/Deep-Sleep Mode Clock/Frequency</th>
<th>FLASHPM</th>
<th>SRAMPM</th>
<th>Time to Wake</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep</td>
<td>MOSC, PLL on - 80MHz</td>
<td>MOSC, PLL on - 80MHz</td>
<td>0x0</td>
<td>0x0</td>
<td>0.28</td>
<td>0.30</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>0x1</td>
<td>33.57</td>
<td>35.00</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>0x3</td>
<td>33.75</td>
<td>35.05</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>0x2</td>
<td>105.02</td>
<td>109.23</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>0x1</td>
<td>137.85</td>
<td>143.93</td>
<td>(\mu s)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>0x3</td>
<td>138.06</td>
<td>143.86</td>
<td>(\mu s)</td>
<td></td>
</tr>
</tbody>
</table>
Table 24-24. Time to Wake with Respect to Low-Power Modes (continued)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Run Mode Clock/Frequency</th>
<th>Sleep/Deep-Sleep Mode Clock/Frequency</th>
<th>FLASHPM</th>
<th>SRAMP</th>
<th>Time to Wake</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>MOSC, PLL on - 80MHz</td>
<td>PIOSC - 16MHz</td>
<td></td>
<td>0x0</td>
<td>2.47</td>
<td>2.60</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>35.31</td>
<td>36.35</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>35.40</td>
<td>36.76</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>0x0</td>
<td>107.05</td>
<td>111.54</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>139.34</td>
<td>145.64</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>140.41</td>
<td>145.53</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>0x0</td>
<td>0x0</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>0x1</td>
<td>0x1</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>0x3</td>
<td>0x3</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>0x2</td>
<td>0x2</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>0x0</td>
<td>0x0</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>0x1</td>
<td>0x1</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>0x3</td>
<td>0x3</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>0x2</td>
<td>0x2</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0</td>
<td>0x0</td>
<td>0x0</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1</td>
<td>0x1</td>
<td>0x1</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3</td>
<td>0x3</td>
<td>0x3</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2</td>
<td>0x2</td>
<td>0x2</td>
<td>μs</td>
</tr>
</tbody>
</table>

Deep-Sleep

|      |                         |                                      | 0x0     | 415.06| 728.38       | μs   |
|      |                         |                                      | 0x1     | 436.60| 740.88       | μs   |
|      |                         |                                      | 0x3     | 433.80| 755.32       | μs   |
|      |                         |                                      | 0x2     | 0x0   | 503.73       | 812.82 | μs |
|      |                         |                                      | 0x1     | 537.72| 846.23       | μs   |
|      |                         |                                      | 0x3     | 536.10| 839.25       | μs   |
|      |                         |                                      | 0x0     | 0x0   | 0x0          | μs   |
|      |                         |                                      | 0x1     | 0x1   | 0x1          | μs   |
|      |                         |                                      | 0x3     | 0x3   | 0x3          | μs   |
|      |                         |                                      | 0x2     | 0x2   | 0x2          | μs   |
|      |                         |                                      | 0x0     | 0x0   | 0x0          | μs   |
|      |                         |                                      | 0x1     | 0x1   | 0x1          | μs   |
|      |                         |                                      | 0x3     | 0x3   | 0x3          | μs   |
|      |                         |                                      | 0x2     | 0x2   | 0x2          | μs   |
|      |                         |                                      | 0x0     | 0x0   | 0x0          | μs   |
|      |                         |                                      | 0x1     | 0x1   | 0x1          | μs   |
|      |                         |                                      | 0x3     | 0x3   | 0x3          | μs   |
|      |                         |                                      | 0x2     | 0x2   | 0x2          | μs   |

MOSC, PLL on - 80MHz

|      |                         |                                      | 0x0     | 18.95 | 19.55       | ms   |
|      |                         |                                      | 0x1     | 18.94 | 19.54       | ms   |
|      |                         |                                      | 0x3     | 18.95 | 19.53       | ms   |
|      |                         |                                      | 0x2     | 0x0   | 18.95       | 19.54 | ms |
|      |                         |                                      | 0x1     | 18.94 | 19.53       | ms   |
|      |                         |                                      | 0x3     | 18.95 | 19.54       | ms   |
|      |                         |                                      | 0x2     | 0x2   | 0x2          | ms   |
|      |                         |                                      | 0x0     | 0x0   | 0x0          | ms   |
|      |                         |                                      | 0x1     | 0x1   | 0x1          | ms   |
|      |                         |                                      | 0x3     | 0x3   | 0x3          | ms   |
|      |                         |                                      | 0x2     | 0x2   | 0x2          | ms   |

- Time from wake event to first instruction of code execution.
- If the LDO voltage is adjusted, it will take an extra 4 μs to wake up from Sleep or Deep-sleep mode.
- PIO is turned off by setting the PIOUSPD bit in the DSLPCLKCFG register.
24.11 Hibernation Module

The Hibernation module requires special system implementation considerations because it is intended to power down all other sections of its host device, refer to “Hibernation Module” on page 503.

Table 24-25. Hibernation Module Battery Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nominal</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BAT}$</td>
<td>Battery supply voltage</td>
<td>1.8</td>
<td>3.0</td>
<td>3.6$^a$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{BATRMP}^b$</td>
<td>$V_{BAT}$ battery supply voltage ramp time</td>
<td>0</td>
<td>-</td>
<td>0.7</td>
<td>V/μs</td>
</tr>
<tr>
<td>$V_{LOWBAT}$</td>
<td>Low battery detect voltage, $V_{BATSEL}=0x0$</td>
<td>1.8</td>
<td>1.9</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Low battery detect voltage, $V_{BATSEL}=0x1$</td>
<td>2.0</td>
<td>2.1</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Low battery detect voltage, $V_{BATSEL}=0x2$</td>
<td>2.2</td>
<td>2.3</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Low battery detect voltage, $V_{BATSEL}=0x3$</td>
<td>2.4</td>
<td>2.5</td>
<td>2.6</td>
<td>V</td>
</tr>
</tbody>
</table>

a. To ensure proper functionality, any voltage input within the range of $3.6 \, V < V_{BAT} \leq 4 \, V$ must be connected through a diode.

b. For recommended $V_{BAT}$ RC circuit values, refer to the diagrams located in “Hibernation Clock Source” on page 506.

Table 24-26. Hibernation Module AC Characteristics

<table>
<thead>
<tr>
<th>Parameter No</th>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1</td>
<td>$T_{WAKE}$</td>
<td>WAKE assertion time</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>H2</td>
<td>$T_{WAKE_TO_HIB}$</td>
<td>WAKE assert to HIB desassert (wake up time)</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>hibernation clock period</td>
</tr>
<tr>
<td>H3</td>
<td>$T_{VDD_RAMP}$</td>
<td>$V_{DD}$ ramp to 3.0 V</td>
<td>-</td>
<td>Depends on characteristics of power supply</td>
<td>-</td>
<td>µs</td>
</tr>
<tr>
<td>H4</td>
<td>$T_{VDD_CODE}$</td>
<td>$V_{DD}$ at 3.0 V to internal POR deassert; first instruction executes</td>
<td>-</td>
<td>-</td>
<td>500</td>
<td>µs</td>
</tr>
</tbody>
</table>

Figure 24-15. Hibernation Module Timing
## 24.12 Flash Memory and EEPROM

### Table 24-27. Flash Memory Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{PE\text{CYC}}$</td>
<td>Number of program/erase cycles before failure $^a$</td>
<td>100,000</td>
<td>-</td>
<td>-</td>
<td>cycles</td>
</tr>
<tr>
<td>$T_{RE}t$</td>
<td>Data retention, -40°C to +85°C</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>years</td>
</tr>
<tr>
<td>$T_{RET\text{TEMP}}$</td>
<td>Data retention, 105°C</td>
<td>11</td>
<td>-</td>
<td>-</td>
<td>years</td>
</tr>
<tr>
<td>$T_{PRG64}$</td>
<td>Program time for double-word-aligned 64 bits of data $^a$</td>
<td>30</td>
<td>50</td>
<td>300</td>
<td>µs</td>
</tr>
<tr>
<td>$T_{ERASE}$</td>
<td>Page erase time, &lt;1k cycles</td>
<td>-</td>
<td>8</td>
<td>15</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Page erase time, 10k cycles</td>
<td>-</td>
<td>15</td>
<td>40</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Page erase time, 100k cycles</td>
<td>-</td>
<td>75</td>
<td>500</td>
<td>ms</td>
</tr>
<tr>
<td>$T_{ME}$</td>
<td>Mass erase time, &lt;1k cycles</td>
<td>-</td>
<td>10</td>
<td>25</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Mass erase time, 10k cycles</td>
<td>-</td>
<td>20</td>
<td>70</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Mass erase time, 100k cycles</td>
<td>-</td>
<td>300</td>
<td>2500</td>
<td>ms</td>
</tr>
</tbody>
</table>

*a. A program/erase cycle is defined as switching the bits from 1-> 0 -> 1.

*b. If programming fewer than 64 bits of data, the programming time is the same. For example, if only 32 bits of data need to be programmed, the other 32 bits are masked off.

### Table 24-28. EEPROM Characteristics $^a$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$EPE_{CYC}$$^b$</td>
<td>Number of mass program/erase cycles of a single word before failure $^c$</td>
<td>500,000</td>
<td>-</td>
<td>-</td>
<td>cycles</td>
</tr>
<tr>
<td>$ET_{RE}t$</td>
<td>Data retention, -40°C to +85°C</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>years</td>
</tr>
<tr>
<td>$ET_{PROG}$</td>
<td>Program time for 32 bits of data - space available</td>
<td>-</td>
<td>110</td>
<td>600</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>Program time for 32 bits of data - requires a copy to the copy buffer, copy buffer has space and less than 10% of EEPROM endurance used</td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Program time for 32 bits of data - requires a copy to the copy buffer, copy buffer has space and greater than 90% of EEPROM endurance used</td>
<td>-</td>
<td>-</td>
<td>900</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Program time for 32 bits of data - requires an erase and less than 10% of EEPROM endurance used</td>
<td>-</td>
<td>60</td>
<td>-</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Program time for 32 bits of data - requires an erase and greater than 90% of EEPROM endurance used</td>
<td>-</td>
<td>-</td>
<td>1800</td>
<td>ms</td>
</tr>
<tr>
<td>$ET_{READ}$</td>
<td>Read access time</td>
<td>-</td>
<td>4</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td>$ET_{ME}$</td>
<td>Mass erase time, &lt;1k cycles</td>
<td>-</td>
<td>8</td>
<td>15</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Mass erase time, 10k cycles</td>
<td>-</td>
<td>15</td>
<td>40</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>Mass erase time, 100k cycles</td>
<td>-</td>
<td>75</td>
<td>500</td>
<td>ms</td>
</tr>
</tbody>
</table>

*a. Because the EEPROM operates as a background task and does not prevent the CPU from executing from Flash memory, the operation will complete within the maximum time specified provided the EEPROM operation is not stalled by a Flash memory program or erase operation.

*b. One word can be written more than 500K times, but these writes impact the endurance of the words in the meta-block that the word is within. Different words can be written such that any or all words can be written more than 500K times when write counts per word stay about the same. See the section called “Endurance” on page 548 for more information.

*c. A program/erase cycle is defined as switching the bits from 1-> 0 -> 1.
24.13 Input/Output Pin Characteristics

24.13.1 GPIO Module Characteristics

Note: All GPIO signals are 5-V tolerant when configured as inputs except for PJ0, PJ1, PB0 and PB1, which are limited to 3.6 V. See “Signal Description” on page 659 for more information on GPIO configuration.

Note: GPIO pads are tolerant to 5-V digital inputs without creating reliability issues, as long as the supply voltage, VDD, is present. There are limitations to how long a 5-V input can be present on any given I/O pad if VDD is not present. Not meeting these conditions will affect reliability of the device and affect the GPIO characteristics specifications.

- If the voltage applied to a GPIO pad is in the high voltage range (5V +/- 10%) while VDD is not present, such condition should be allowed for a maximum of 10,000 hours at 27°C or 5,000 hours at 85°C, over the lifetime of the device.

- If the voltage applied to a GPIO pad is in the normal voltage range (3.3V +/- 10%) while VDD is not present or if the voltage applied is in the high voltage range (5V +/- 10%) while VDD is present, there are no constraints on the lifetime of the device.

Table 24-29. GPIO Module Characteristics\(^a\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{\text{GPIO}} )</td>
<td>GPIO Digital Input Capacitance</td>
<td>-</td>
<td>8</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>( R_{\text{GPIO PU}} )</td>
<td>GPIO internal pull-up resistor</td>
<td>13</td>
<td>20</td>
<td>30</td>
<td>kΩ</td>
</tr>
<tr>
<td>( R_{\text{GPIO PD}} )</td>
<td>GPIO internal pull-down resistor</td>
<td>13</td>
<td>20</td>
<td>35</td>
<td>kΩ</td>
</tr>
<tr>
<td>( I_{\text{LG}} )</td>
<td>GPIO input leakage current, ( 0 \leq V_{\text{IN}} \leq V_{\text{DD}} ), GPIO pins(^b)</td>
<td>-</td>
<td>-</td>
<td>1.0</td>
<td>µA</td>
</tr>
<tr>
<td>( I_{\text{LG}} )</td>
<td>GPIO input leakage current, ( 0 &lt; V_{\text{IN}} &lt; V_{\text{DD}} ), GPIO pins configured as ADC or analog comparator inputs</td>
<td>-</td>
<td>-</td>
<td>2.0</td>
<td>µA</td>
</tr>
<tr>
<td>( T_{\text{GPIO R}} )</td>
<td>GPIO rise time, 2-mA drive(^c)</td>
<td>14.2</td>
<td>16.1</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{GPIO R}} )</td>
<td>GPIO rise time, 4-mA drive(^c)</td>
<td>11.9</td>
<td>15.5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{GPIO R}} )</td>
<td>GPIO rise time, 8-mA drive(^c)</td>
<td>8.1</td>
<td>11.2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{GPIO R}} )</td>
<td>GPIO rise time, 8-mA drive with slew rate control(^c)</td>
<td>9.5</td>
<td>11.8</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{GPIO F}} )</td>
<td>GPIO fall time, 2-mA drive(^d)</td>
<td>-</td>
<td>25.2</td>
<td>29.4</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{GPIO F}} )</td>
<td>GPIO fall time, 4-mA drive(^d)</td>
<td>13.3</td>
<td>16.8</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{GPIO F}} )</td>
<td>GPIO fall time, 8-mA drive(^d)</td>
<td>8.6</td>
<td>11.2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{GPIO F}} )</td>
<td>GPIO fall time, 8-mA drive with slew rate control(^d)</td>
<td>11.3</td>
<td>12.9</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

\(^a\) V_{\text{DD}} must be within the range specified in Table 24-5 on page 1397.

\(^b\) The leakage current is measured with \( V_{\text{IN}} \) applied to the corresponding pin(s). The leakage of digital port pins is measured individually. The port pin is configured as an input and the pull-up/pull-down resistor is disabled.

\(^c\) Time measured from 20% to 80% of V_{\text{DD}}.

\(^d\) Time measured from 80% to 20% of V_{\text{DD}}.

24.13.2 Types of I/O Pins and ESD Protection

With respect to ESD and leakage current, three types of I/O pins exist on the device: Power I/O pins, I/O pins with fail-safe ESD protection (GPIOs other than PJ0 and PJ1, and XOSC\(n\) pins) and I/O pins with non-fail-safe ESD protection (any non-power, non-GPIO (other than PJ0 and PJ1) and...
non-XOSCn pins). This section covers I/O pins with fail-safe ESD protection and I/O pins with
non-fail-safe ESD protection. Power I/O pin voltage and current limitations are specified in
“Recommended Operating Conditions” on page 1397.

24.13.2.1 Fail-Safe Pins

GPIOs other than PJ0 and PJ1, pins for the Hibernate 32-kHz oscillator (XOSCn), Hibernate input
pins, and I/O pins for the USB PHY use ESD protection as shown in Figure 24-16 on page 1423.

An unpowered device cannot be parasitically powered through any of these pins. This ESD protection
prevents a direct path between these I/O pads and any power supply rails in the device. GPIO/XOSCn
pad input voltages should be kept inside the maximum ratings specified in Table 24-1 on page 1395
to ensure current leakage and current injections are within acceptable range. Current leakages and
current injection for these pins are specified in Table 24-29 on page 1422.

Figure 24-16 on page 1423 shows a diagram of the ESD protection on fail-safe pins.

Some GPIOs when configured as inputs require a strong pull-up resistor to maintain a threshold
above the minimum value of VIH during power-on. See Table 24-31 on page 1424.

Figure 24-16. ESD Protection on Fail-Safe Pins

![ESD Protection Diagram](image)

Table 24-30. Pad Voltage/Current Characteristics for Fail-Safe Pins

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I&lt;sub&gt;LKG+&lt;/sub&gt;</td>
<td>GPIO input leakage current, V&lt;sub&gt;DD&lt;/sub&gt;≤ V&lt;sub&gt;IN&lt;/sub&gt; ≤ 4.5 V&lt;sup&gt;3b&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>700</td>
<td>μA</td>
</tr>
<tr>
<td>I&lt;sub&gt;LKG&lt;/sub&gt;</td>
<td>GPIO input leakage current, 4.5 V &lt; V&lt;sub&gt;IN&lt;/sub&gt; ≤ 5.5 V&lt;sup&gt;3c&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td>I&lt;sub&gt;LKG&lt;/sub&gt;</td>
<td>GPIO input leakage current, V&lt;sub&gt;IN&lt;/sub&gt; &lt; -0.3 V&lt;sup&gt;3d&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>I&lt;sub&gt;LKG&lt;/sub&gt;</td>
<td>GPIO input leakage current, -0.3 V ≤ V&lt;sub&gt;IN&lt;/sub&gt; &lt; 0 V&lt;sup&gt;3d&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>I&lt;sub&gt;INJ+&lt;/sub&gt;</td>
<td>DC injection current, V&lt;sub&gt;DD&lt;/sub&gt; &lt; V&lt;sub&gt;IN&lt;/sub&gt; ≤ 5.5 V&lt;sup&gt;6&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>μA</td>
</tr>
<tr>
<td>I&lt;sub&gt;INJ&lt;/sub&gt;</td>
<td>DC injection current, V&lt;sub&gt;IN&lt;/sub&gt; ≤ 0 V&lt;sup&gt;6&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>0.5</td>
<td>mA</td>
</tr>
</tbody>
</table>

a. VIN must be within the range specified in Table 24-1 on page 1395.
b. To protect internal circuitry from over-voltage, the GPIOs have an internal voltage clamp that limits internal swings to V<sub>DD</sub> without affecting swing at the I/O pad. This internal clamp starts turning on while V<sub>DD</sub> < V<sub>IN</sub> < 4.5 V and causes a somewhat larger (but bounded) current draw. To save power, static input voltages between V<sub>DD</sub> and 4.5 V should be avoided.
c. Leakage current above maximum voltage (V<sub>IN</sub> = 5.5V) is not guaranteed, this condition is not allowed and can result in permanent damage to the device.
d. Leakage outside the minimum range (-0.3V) is unbounded and must be limited to I<sub>INJ</sub> using an external resistor.
e. In this case, I<sub>LKG</sub> is unbounded and must be limited to I<sub>INJ</sub>, using an external resistor.
f. Current injection is internally bounded for GPIOs, and maximum current into the pin is given by $I_{LKG+}$ for $V_{DD} < V_{IN} < 5.5$ V.

g. If the I/O pad is not voltage limited, it should be current limited (to $I_{INJ+}$ and $I_{INJ-}$) if there is any possibility of the pad voltage exceeding the $V_{IO}$ limits (including transient behavior during supply ramp up, or at any time when the part is unpowered).

Table 24-31. Fail-Safe GPIOs that Require an External Pull-up

<table>
<thead>
<tr>
<th>GPIO</th>
<th>Pin</th>
<th>Pull-Up Resistor Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB0</td>
<td>70</td>
<td>1k ≤ R ≤ 10k</td>
<td>Ω</td>
</tr>
<tr>
<td>PB1</td>
<td>71</td>
<td>1k ≤ R ≤ 10k</td>
<td>Ω</td>
</tr>
<tr>
<td>PE3</td>
<td>12</td>
<td>1k ≤ R ≤ 10k</td>
<td>Ω</td>
</tr>
</tbody>
</table>

24.13.2.2 Non-Fail-Safe Pins

The ADC external voltage reference input pins, the Main Oscillator (MOSC) crystal connection pins and GPIO pins PJ0 and PJ1 have ESD protection as shown in Figure 24-17 on page 1424. These pins have a potential path between the I/O pad and an internal power rail if either one of the ESD diodes is accidentally forward biased. The voltage and current of these pins should follow the specifications in Table 24-32 on page 1424 to prevent potential damage to the device. In addition to the specifications outlined in Table 24-32 on page 1424, it is recommended that the ADC external reference specifications in Table 24-33 on page 1426 be adhered to in order to prevent any gain error.

Figure 24-17 on page 1424 shows a diagram of the ESD protection on non-fail-safe pins.

![ESD Protection on Non-Fail-Safe Pins](image)

Table 24-32. Non-Fail-Safe I/O Pad Voltage/Current Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IO}$</td>
<td>IO pad voltage limits</td>
<td>-0.3</td>
<td>$V_{DD}$</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{LKG+}$</td>
<td>Positive IO leakage for $V_{IO} \text{Max}^{\text{ref}}$</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{LKG-}$</td>
<td>Negative IO leakage for $V_{IO} \text{Min}^{\text{ef}}$</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{INJ+}$</td>
<td>Max positive injection$^2$</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{INJ-}$</td>
<td>Max negative injection if not voltage protected$^2$</td>
<td>-</td>
<td>-</td>
<td>-0.5</td>
<td>mA</td>
</tr>
</tbody>
</table>

a. $V_{IN}$ must be within the range specified in Table 24-1 on page 1395. Leakage current outside of this maximum voltage is not guaranteed and can result in permanent damage of the device.

b. $V_{DD}$ must be within the range specified in Table 24-5 on page 1397.
c. To avoid potential damage to the part, either the voltage or current on the ESD-protected, non-Power, non-Hibernate/XOSC input/outputs should be limited externally as shown in this table.

d. I/O pads should be protected if at any point the IO voltage has a possibility of going outside the limits shown in the table. If the part is unpowered, the IO pad Voltage or Current must be limited (as shown in this table) to avoid powering the part through the IO pad, causing potential irreversible damage.

e. This value applies to an I/O pin that is voltage-protected within the Min and Max $V_{\text{IO}}$ ratings. Leakage outside the specified voltage range is unbounded and must be limited to $I_{\text{INJ}}$, using an external resistor.

f. MIN and MAX leakage current for the case when the I/O is voltage-protected to $V_{\text{IO}}$ Min or $V_{\text{IO}}$ Max.

g. If an I/O pin is not voltage-limited, it should be current-limited (to $I_{\text{INJ}^+}$ and $I_{\text{INJ}^-}$) if there is any possibility of the pad voltage exceeding the $V_{\text{IO}}$ limits (including transient behavior during supply ramp up, or at any time when the part is unpowered).
## 24.14 Analog-to-Digital Converter (ADC)

### Table 24-33. ADC Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Parameter</th>
<th>Unit</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>( V_\text{DDA} )</th>
<th>( V_\text{DDA} )</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>POWER SUPPLY REQUIREMENTS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_\text{DDA} )</td>
<td>ADC supply voltage</td>
<td>-</td>
<td>2.97</td>
<td>3.3</td>
<td>3.63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>ADC ground voltage</td>
<td>-</td>
<td>-</td>
<td>0</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>VDDA / GNDA VOLTAGE REFERENCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_\text{REF} )</td>
<td>Voltage reference decoupling capacitance</td>
<td>-</td>
<td>-</td>
<td>1.0 // 0.01&lt;sup&gt;c&lt;/sup&gt;</td>
<td>-</td>
<td></td>
<td>µF</td>
</tr>
<tr>
<td><strong>EXTERNAL VOLTAGE REFERENCE INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{REFA}+} )</td>
<td>Positive external voltage reference for ADC, when ( V_\text{REF} ) field in the ADCCTL register is not 0x0&lt;sup&gt;d&lt;/sup&gt;</td>
<td>2.4</td>
<td></td>
<td></td>
<td></td>
<td>( V_\text{DDA} )</td>
<td>( V_\text{DDA} )</td>
</tr>
<tr>
<td>( V_{\text{REFA}-} )</td>
<td>Negative external voltage reference for ADC, when ( V_\text{REF} ) field in the ADCCTL register is not 0x0&lt;sup&gt;d&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GNDA</td>
<td>GNDA</td>
</tr>
<tr>
<td>( I_{\text{VREF}} )</td>
<td>Current on ( V_\text{REF}+ ) input, using external ( V_\text{REF}+ = 3.3 ) V</td>
<td>-</td>
<td>330.5</td>
<td>440</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( I_{\text{LVREF}} )</td>
<td>DC leakage current on ( V_\text{REF}+ ) input when external VREF disabled</td>
<td>-</td>
<td>-</td>
<td>2.0</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( C_\text{REF} )</td>
<td>External reference decoupling capacitance&lt;sup&gt;d&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>1.0 // 0.01&lt;sup&gt;e&lt;/sup&gt;</td>
<td>-</td>
<td></td>
<td>µF</td>
</tr>
<tr>
<td><strong>ANALOG INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{ADCIN}} )</td>
<td>Single-ended, full-scale analog input voltage, internal reference&lt;sup&gt;g&lt;/sup&gt;</td>
<td>0</td>
<td>-</td>
<td></td>
<td>( V_\text{DDA} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Differential, full-scale analog input voltage, internal reference&lt;sup&gt;h&lt;/sup&gt;</td>
<td>-( V_\text{DDA} )</td>
<td>-</td>
<td></td>
<td>( V_\text{DDA} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Single-ended, full-scale analog input voltage, external reference&lt;sup&gt;g&lt;/sup&gt;</td>
<td>( V_{\text{REFA}-} )</td>
<td>-</td>
<td>-</td>
<td>( V_{\text{REFA}+} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Differential, full-scale analog input voltage, external reference&lt;sup&gt;d&lt;/sup&gt;</td>
<td>- (( V_{\text{REFA}+} - V_{\text{REFA}-} ))</td>
<td>-</td>
<td>-</td>
<td>( V_{\text{REFA}+} - V_{\text{REFA}-} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{INCM}} )</td>
<td>Input common mode voltage, differential mode&lt;sup&gt;j&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td></td>
<td>(( V_{\text{REFP}} + V_{\text{REFN}} ) / 2 ± 25)</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( I_{\text{IL}} )</td>
<td>ADC input leakage current&lt;sup&gt;k&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td></td>
<td>2.0</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( R_{\text{ADC}} )</td>
<td>ADC equivalent input resistance&lt;sup&gt;k&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td></td>
<td>2.5</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>( C_{\text{ADC}} )</td>
<td>ADC equivalent input capacitance&lt;sup&gt;k&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td></td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( R_{\text{S}} )</td>
<td>Analog source resistance&lt;sup&gt;k&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td></td>
<td>500</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td><strong>SAMPLING DYNAMICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( F_{\text{ADC}} )</td>
<td>ADC conversion clock frequency&lt;sup&gt;j&lt;/sup&gt;</td>
<td>-</td>
<td>16</td>
<td>-</td>
<td>-</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>( F_{\text{CONV}} )</td>
<td>ADC conversion rate</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td></td>
<td>MspS</td>
</tr>
<tr>
<td>( T_{\text{S}} )</td>
<td>ADC sample time</td>
<td>-</td>
<td>250</td>
<td>-</td>
<td>-</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{C}} )</td>
<td>ADC conversion time&lt;sup&gt;m&lt;/sup&gt;</td>
<td>-</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td></td>
<td>µS</td>
</tr>
<tr>
<td>( T_{\text{LT}} )</td>
<td>Latency from trigger to start of conversion</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td></td>
<td>ADC clocks</td>
</tr>
<tr>
<td><strong>SYSTEM PERFORMANCE when using external reference&lt;sup&gt;g&lt;/sup&gt;</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( N )</td>
<td>Resolution</td>
<td>12</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
<td>bits</td>
</tr>
<tr>
<td>( \text{INL} )</td>
<td>Integral nonlinearity error, over full input range</td>
<td>-</td>
<td>±1.5</td>
<td>-</td>
<td>±3.0</td>
<td></td>
<td>LSB</td>
</tr>
</tbody>
</table>

<sup>a</sup>Values specified for use with external reference.<br>
<sup>b</sup>Unit is °C unless specifically noted.<br>
<sup>c</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) or \( V_\text{REF}+ \) inputs, whichever is lower.<br>
<sup>d</sup>When \( V_\text{REF} \) field in the ADCCTL register is not 0x0.<br>
<sup>e</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.<br>
<sup>f</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.<br>
<sup>g</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.<br>
<sup>h</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.<br>
<sup>i</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.<br>
<sup>j</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.<br>
<sup>k</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.<br>
<sup>l</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.<br>
<sup>m</sup>Reference decoupling capacitance values are for use with \( V_\text{REF}+ \) input, whichever is lower.
Table 24-33. ADC Electrical Characteristics (continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DNL</td>
<td>Differential nonlinearity error, over full input range</td>
<td>-</td>
<td>±0.8</td>
<td>+2.0/-1.0</td>
<td>LSB</td>
</tr>
<tr>
<td>E₀</td>
<td>Offset error</td>
<td>-</td>
<td>±1.0</td>
<td>±3.0</td>
<td>LSB</td>
</tr>
<tr>
<td>E₇</td>
<td>Gain errorᵢ</td>
<td>-</td>
<td>±2.0</td>
<td>±3.0</td>
<td>LSB</td>
</tr>
<tr>
<td>E₇</td>
<td>Total unadjusted error, over full input rangeᵢ</td>
<td>-</td>
<td>±2.5</td>
<td>±4.0</td>
<td>LSB</td>
</tr>
</tbody>
</table>

SYSTEM PERFORMANCE when using internal reference

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>Resolution</td>
<td>12</td>
</tr>
<tr>
<td>INL</td>
<td>Integral nonlinearity error, over full input range</td>
<td>-</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential nonlinearity error, over full input range</td>
<td>-</td>
</tr>
<tr>
<td>E₀</td>
<td>Offset error</td>
<td>-</td>
</tr>
<tr>
<td>E₇</td>
<td>Gain errorᵢ</td>
<td>-</td>
</tr>
<tr>
<td>E₇</td>
<td>Total unadjusted error, over full input rangeᵢ</td>
<td>-</td>
</tr>
</tbody>
</table>

DYNAMIC CHARACTERISTICSᵢᵢ

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR₀</td>
<td>Signal-to-noise-ratio, Differential input, V_ADCIN⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻ᵢᵢ</td>
<td>70</td>
</tr>
<tr>
<td>SDR₀</td>
<td>Signal-to-distortion ratio, Differential input, V_ADCIN⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻ᵢᵢ</td>
<td>72</td>
</tr>
<tr>
<td>SNDR₀</td>
<td>Signal-to-Noise+Distortion ratio, Differential input, V_ADCIN⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻ᵢᵢ</td>
<td>68</td>
</tr>
<tr>
<td>SNRS</td>
<td>Signal-to-noise-ratio, Single-ended input, V_ADCIN⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻ᵢᵢ</td>
<td>60</td>
</tr>
<tr>
<td>SDRₛ</td>
<td>Signal-to-distortion ratio, Single-ended input, V_ADCIN⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻ᵢᵢ</td>
<td>70</td>
</tr>
<tr>
<td>SNDRₛ</td>
<td>Signal-to-Noise+Distortion ratio, Single-ended input, V_ADCIN⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻⁻ᵢᵢ</td>
<td>60</td>
</tr>
</tbody>
</table>

TEMPERATURE SENSOR

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTSENS</td>
<td>Temperature sensor voltage, junction temperature 25 °C</td>
<td>-</td>
</tr>
<tr>
<td>STSENS</td>
<td>Temperature sensor slope</td>
<td>-</td>
</tr>
<tr>
<td>ETSENS</td>
<td>Temperature sensor accuracyᵢᵢᵢᵢ</td>
<td>-</td>
</tr>
</tbody>
</table>

a. V_REF+ = 3.3V, F_ADC = 16 MHz unless otherwise noted.
b. Best design practices suggest that static or quiet digital I/O signals be configured adjacent to sensitive analog inputs to reduce capacitive coupling and cross talk. Analog signals configured adjacent to ADC input channels should meet the same source resistance and bandwidth limitations that apply to the ADC input signals.
c. Two capacitors in parallel.
d. Assumes external filtering network between VREF and VREF- as shown in Figure 24-18 on page 1428. External reference noise level must be under 12bit (-74 dB) of Full Scale input, over input bandwidth, measured at VREF+/ - VREF-.
e. Two capacitors in parallel.
f. Internal reference is connected directly between VDDA and GND (VREF = VDDA - GND). In this mode, E₀, E₇, E₇, and dynamic specifications are adversely affected due to internal voltage drop and noise on VDDA and GND. Internal reference voltage is selected when VREF field in the ADCCTL register is 0x0.
g. V_ADCIN = V_INP - V_INN
h. With signal common mode as VDDA/2.
i. With signal common mode as (VREF+ + VREF-)/2.
j. This parameter is defined as the average of the differential inputs.
k. As shown in Figure 24-19 on page 1429, $R_{ADC}$ is the total equivalent resistance in the input line all the way up to the sampling node at the input of the ADC.
l. See “System Clock Specification with ADC Operation” on page 1417 for full ADC clock frequency specification.
m. ADC conversion time ($T_c$) includes the ADC sample time ($T_s$).
n. Low noise environment is assumed in order to obtain values close to spec. Board must have good ground isolation between analog and digital grounds, a clean reference voltage is assumed, and input signal must be bandlimited to Nyquist bandwidth. No anti-aliasing filter is provided internally.
o. ADC static measurements taken by averaging over several samples. At least 20-sample averaging is assumed to obtain expected typical or maximum spec values.
p. 12-bit DNL
q. Gain error is measured at max code after compensating for offset. Gain error is equivalent to “Full Scale Error.” It can be given in % of slope error, or in LSB, as done here.
r. Total Unadjusted Error is the maximum error at any one code versus the ideal ADC curve. It includes all other errors (offset error, gain error and INL) at any given ADC code.
s. A low-noise environment is assumed in order to obtain values close to spec. The board must have good ground isolation between analog and digital grounds and a clean reference voltage. The input signal must be band-limited to Nyquist bandwidth. No anti-aliasing filter is provided internally.
t. ADC dynamic characteristics are measured using low-noise board design, with low-noise reference voltage ( < -74dB noise level in signal BW) and low-noise analog supply voltage. Board noise and ground bouncing couple into the ADC and affect dynamic characteristics. Clean external reference must be used to achieve shown specs.
u. Differential signal with correct common mode, applied between two ADC inputs.
v. SDR = -THD in dB.
w. For higher frequency inputs, degradation in SDR should be expected.
x. SNDR = $S/(N+D) = \text{SINAD (in dB)}$
y. Effective number of bits (ENOB) can be calculated from SNDR: \(\text{ENOB} = (\text{SNDR} - 1.76) / 6.02\).
z. Single-ended inputs are more sensitive to board and trace noise than differential inputs; SNR and SNDR measurements on single-ended inputs are highly dependent on how clean the test set-up is. If the input signal is not well-isolated on the board, higher noise than specified could potentially be seen at the ADC output.

aa. Note that this parameter does not include ADC error.

**Figure 24-18. ADC External Reference Filtering**
Figure 24-19. ADC Input Equivalency Diagram
24.15 Synchronous Serial Interface (SSI)

Table 24-34. SSI Characteristics

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>T_CLK_PER</td>
<td>SSIClk cycle time, as master&lt;sup&gt;a&lt;/sup&gt;</td>
<td>40</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SSIClk cycle time, as slave&lt;sup&gt;b&lt;/sup&gt;</td>
<td>150</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S2</td>
<td>T_CLK_HIGH</td>
<td>SSIClk high time, as master</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SSIClk high time, as slave</td>
<td>75</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S3</td>
<td>T_CLK_LOW</td>
<td>SSIClk low time, as master</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SSIClk low time, as slave</td>
<td>75</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S4</td>
<td>T_CLKR</td>
<td>SSIClk rise time&lt;sup&gt;c&lt;/sup&gt;</td>
<td>1.25</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S5</td>
<td>T_CLKF</td>
<td>SSIClk fall time&lt;sup&gt;c&lt;/sup&gt;</td>
<td>1.25</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S6</td>
<td>T_TXDMOV</td>
<td>Master Mode: Master Tx Data Output (to slave)</td>
<td>-</td>
<td>-</td>
<td>15.7</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Valid Time from edge of SSIClk</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S7</td>
<td>T_TXDMOH</td>
<td>Master Mode: Master Tx Data Output (to slave)</td>
<td>0.31</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hold Time from next SSIClk</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S8</td>
<td>T_RXDMS</td>
<td>Master Mode: Master Rx Data In (from slave) setup</td>
<td>17.15</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S9</td>
<td>T_RXDMH</td>
<td>Master Mode: Master Rx Data In (from slave) hold</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S10</td>
<td>T_TXDsov</td>
<td>Slave Mode: Master Tx Data Output (to Master)</td>
<td>-</td>
<td>-</td>
<td>77.74&lt;sup&gt;d&lt;/sup&gt;</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Valid Time from edge of SSIClk</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S11</td>
<td>T_TXDSOH</td>
<td>Slave Mode: Slave Tx Data Output (to Master)</td>
<td>55.5&lt;sup&gt;e&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hold Time from edge of SSIClk</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S12</td>
<td>T_RXDSU</td>
<td>Slave Mode: Rx Data In (from master) setup time</td>
<td>0</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S13</td>
<td>T_RXDSH</td>
<td>Slave Mode: Rx Data In (from master) hold time</td>
<td>51.55&lt;sup&gt;f&lt;/sup&gt;</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

a. In master mode, the system clock must be at least twice as fast as the SSIClk.
b. In slave mode, the system clock must be at least 12 times faster than the SSIClk.
c. Note that the delays shown are using 8-mA drive strength.
d. This MAX value is for the minimum T<sub>SYSCLK</sub> (12.5 ns). To find the MAX T<sub>TXDSOV</sub> value for a larger T<sub>SYSCLK</sub>, use the equation: 4*<sub>T_SysClk</sub>+27.74.
e. This MIN value is for the minimum slave mode T<sub>SYSCLK</sub> (12.5 ns). To find the MIN T<sub>TXDSOH</sub> value for a larger T<sub>SYSCLK</sub>, use the equation: 4*<sub>T_SysClk</sub>+5.50.
f. This MIN value is for the minimum slave mode T<sub>SYSCLK</sub> (12.5 ns). To find the MIN T<sub>RXDSH</sub> value for a larger T<sub>SYSCLK</sub>, use the equation: 4*<sub>T_SysClk</sub>+1.55.
Figure 24-20. SSI Timing for TI Frame Format (FRF=01), Single Transfer Timing Measurement

Figure 24-21. SSI Timing for MICROWIRE Frame Format (FRF=10), Single Transfer
Figure 24-22. Master Mode SSI Timing for SPI Frame Format (FRF=00), with SPH=1

Figure 24-23. Slave Mode SSI Timing for SPI Frame Format (FRF=00), with SPH=1
# 24.16 Inter-Integrated Circuit ($I^2$C) Interface

## Table 24-35. $I^2$C Characteristics

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>11&lt;sup&gt;a&lt;/sup&gt;</td>
<td>$T_{SCH}$</td>
<td>Start condition hold time</td>
<td>36</td>
<td>-</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td>12&lt;sup&gt;a&lt;/sup&gt;</td>
<td>$T_{LP}$</td>
<td>Clock Low period</td>
<td>36</td>
<td>-</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td>13&lt;sup&gt;a&lt;/sup&gt;</td>
<td>$T_{SRT}$</td>
<td>$I^2$CSCL/$I^2$CSDA rise time ($V_{IL}=0.5$ V to $V_{IH}=2.4$ V)</td>
<td>-</td>
<td>-</td>
<td>(see note b)</td>
<td>ns</td>
</tr>
<tr>
<td>14</td>
<td>$T_{DH}$</td>
<td>Data hold time (slave)</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data hold time (master)</td>
<td>-</td>
<td>7</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td>15&lt;sup&gt;c&lt;/sup&gt;</td>
<td>$T_{SFT}$</td>
<td>$I^2$CSCL/$I^2$CSDA fall time ($V_{IH}=2.4$ V to $V_{IL}=0.5$ V)</td>
<td>-</td>
<td>9</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>16&lt;sup&gt;a&lt;/sup&gt;</td>
<td>$T_{HT}$</td>
<td>Clock High time</td>
<td>24</td>
<td>-</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td>17</td>
<td>$T_{DS}$</td>
<td>Data setup time</td>
<td>18</td>
<td>-</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td>18&lt;sup&gt;a&lt;/sup&gt;</td>
<td>$T_{SCSR}$</td>
<td>Start condition setup time (for repeated start condition only)</td>
<td>36</td>
<td>-</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td>19&lt;sup&gt;a&lt;/sup&gt;</td>
<td>$T_{SCS}$</td>
<td>Stop condition setup time</td>
<td>24</td>
<td>-</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td>10</td>
<td>$T_{DV}$</td>
<td>Data Valid (slave)</td>
<td>-</td>
<td>2</td>
<td>-</td>
<td>system clocks</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Data Valid (master)</td>
<td>-</td>
<td>(6 * (1 + TPR)) + 1</td>
<td>-</td>
<td>system clocks</td>
</tr>
</tbody>
</table>

a. Values depend on the value programmed into the TPR bit in the $I^2$C Master Timer Period ($I^2$CMTPR) register; a TPR programmed for the maximum $I^2$CSCL frequency (TPR=0x2) results in a minimum output timing as shown in the table above. The $I^2$C interface is designed to scale the actual data transition time to move it to the middle of the $I^2$CSCL Low period. The actual position is affected by the value programmed into the TPR; however, the numbers given in the above values are minimum values.

b. Because $I^2$CSCL and $I^2$CSDA operate as open-drain-type signals, which the controller can only actively drive Low, the time $I^2$CSCL or $I^2$CSDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

c. Specified at a nominal 50 pF load.

## Figure 24-24. $I^2$C Timing
24.17 Universal Serial Bus (USB) Controller

The TM4C123GH6PZ USB controller electrical specifications are compliant with the *Universal Serial Bus Specification Rev. 2.0* (full-speed and low-speed support) and the *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.0*. Some components of the USB system are integrated within the TM4C123GH6PZ microcontroller and specific to the TM4C123GH6PZ microcontroller design.
### 24.18 Analog Comparator

#### Table 24-36. Analog Comparator Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{INP}$-$V_{INN}$</td>
<td>Input voltage range</td>
<td>GNDA</td>
<td>-</td>
<td>$V_{DDA}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CM}$</td>
<td>Input common mode voltage range</td>
<td>GNDA</td>
<td>-</td>
<td>$V_{DDA}$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input offset voltage</td>
<td>-</td>
<td>±10</td>
<td>±50$^2$</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{INP}$-$I_{INN}$</td>
<td>Input leakage current over full voltage range</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>µA</td>
</tr>
<tr>
<td>$C_{CMR}$</td>
<td>Common mode rejection ratio</td>
<td>-</td>
<td>50</td>
<td>2.0</td>
<td>µA</td>
</tr>
<tr>
<td>$T_{RT}$</td>
<td>Response time</td>
<td>-</td>
<td>-</td>
<td>1.0$^8$</td>
<td>µs</td>
</tr>
<tr>
<td>$T_{MC}$</td>
<td>Comparator mode change to Output Valid</td>
<td>-</td>
<td>-</td>
<td>10</td>
<td>µs</td>
</tr>
</tbody>
</table>

a. Best design practices suggest that static or quiet digital I/O signals be configured adjacent to sensitive analog inputs to reduce capacitive coupling and cross talk.

b. To achieve best analog results, the source resistance driving the analog inputs, $V_{INP}$ and $V_{INN}$, should be kept low.

c. The external voltage inputs to the Analog Comparator are designed to be highly sensitive and can be affected by external noise on the board. For this reason, $V_{INP}$ and $V_{INN}$ must be set to different voltage levels during idle states to ensure the analog comparator triggers are not enabled. If an internal voltage reference is used, it should be set to a mid-supply level. When operating in Sleep/Deep-Sleep modes, the Analog Comparator module external voltage inputs set to different levels (greater than the input offset voltage) to achieve minimum current draw.

d. Measured at VREF=100 mV.

e. Measured at external VREF=100 mV, input signal switching from 75 mV to 125 mV.

#### Table 24-37. Analog Comparator Voltage Reference Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{HR}$</td>
<td>Resolution in high range</td>
<td>-</td>
<td>$V_{DDA}/29.4$</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$R_{LR}$</td>
<td>Resolution in low range</td>
<td>-</td>
<td>$V_{DDA}/22.12$</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$A_{HR}$</td>
<td>Absolute accuracy high range</td>
<td>-</td>
<td>-</td>
<td>±$R_{HR}/2$</td>
<td>V</td>
</tr>
<tr>
<td>$A_{LR}$</td>
<td>Absolute accuracy low range</td>
<td>-</td>
<td>-</td>
<td>±$R_{LR}/2$</td>
<td>V</td>
</tr>
</tbody>
</table>

#### Table 24-38. Analog Comparator Voltage Reference Characteristics, $V_{DDA} = 3.3V$, EN= 1, and RNG = 0

<table>
<thead>
<tr>
<th>VREF Value</th>
<th>$V_{REF}$ Min</th>
<th>Ideal $V_{REF}$</th>
<th>$V_{REF}$ Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0.731</td>
<td>0.786</td>
<td>0.841</td>
<td>V</td>
</tr>
<tr>
<td>0x1</td>
<td>0.843</td>
<td>0.898</td>
<td>0.953</td>
<td>V</td>
</tr>
<tr>
<td>0x2</td>
<td>0.955</td>
<td>1.010</td>
<td>1.065</td>
<td>V</td>
</tr>
<tr>
<td>0x3</td>
<td>1.067</td>
<td>1.122</td>
<td>1.178</td>
<td>V</td>
</tr>
<tr>
<td>0x4</td>
<td>1.180</td>
<td>1.235</td>
<td>1.290</td>
<td>V</td>
</tr>
<tr>
<td>0x5</td>
<td>1.292</td>
<td>1.347</td>
<td>1.402</td>
<td>V</td>
</tr>
<tr>
<td>0x6</td>
<td>1.404</td>
<td>1.459</td>
<td>1.514</td>
<td>V</td>
</tr>
<tr>
<td>0x7</td>
<td>1.516</td>
<td>1.571</td>
<td>1.627</td>
<td>V</td>
</tr>
<tr>
<td>0x8</td>
<td>1.629</td>
<td>1.684</td>
<td>1.739</td>
<td>V</td>
</tr>
<tr>
<td>0x9</td>
<td>1.741</td>
<td>1.796</td>
<td>1.851</td>
<td>V</td>
</tr>
<tr>
<td>0xA</td>
<td>1.853</td>
<td>1.908</td>
<td>1.963</td>
<td>V</td>
</tr>
<tr>
<td>0xB</td>
<td>1.965</td>
<td>2.020</td>
<td>2.076</td>
<td>V</td>
</tr>
<tr>
<td>0xC</td>
<td>2.078</td>
<td>2.133</td>
<td>2.188</td>
<td>V</td>
</tr>
</tbody>
</table>
Table 24-38. Analog Comparator Voltage Reference Characteristics, \( V_{DDA} = 3.3V, \text{EN}= 1, \text{and} \ R\text{NG} = 0 \) (continued)

<table>
<thead>
<tr>
<th>( \text{VREF Value} )</th>
<th>( V_{\text{REF Min}} )</th>
<th>( \text{Ideal} V_{\text{REF}} )</th>
<th>( V_{\text{REF Max}} )</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xD</td>
<td>2.190</td>
<td>2.245</td>
<td>2.300</td>
<td>V</td>
</tr>
<tr>
<td>0xE</td>
<td>2.302</td>
<td>2.357</td>
<td>2.412</td>
<td>V</td>
</tr>
<tr>
<td>0xF</td>
<td>2.414</td>
<td>2.469</td>
<td>2.525</td>
<td>V</td>
</tr>
</tbody>
</table>

Table 24-39. Analog Comparator Voltage Reference Characteristics, \( V_{DDA} = 3.3V, \text{EN}= 1, \text{and} \ R\text{NG} = 1 \)

<table>
<thead>
<tr>
<th>( \text{VREF Value} )</th>
<th>( V_{\text{REF Min}} )</th>
<th>( \text{Ideal} V_{\text{REF}} )</th>
<th>( V_{\text{REF Max}} )</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0.000</td>
<td>0.000</td>
<td>0.074</td>
<td>V</td>
</tr>
<tr>
<td>0x1</td>
<td>0.076</td>
<td>0.149</td>
<td>0.223</td>
<td>V</td>
</tr>
<tr>
<td>0x2</td>
<td>0.225</td>
<td>0.298</td>
<td>0.372</td>
<td>V</td>
</tr>
<tr>
<td>0x3</td>
<td>0.374</td>
<td>0.448</td>
<td>0.521</td>
<td>V</td>
</tr>
<tr>
<td>0x4</td>
<td>0.523</td>
<td>0.597</td>
<td>0.670</td>
<td>V</td>
</tr>
<tr>
<td>0x5</td>
<td>0.672</td>
<td>0.746</td>
<td>0.820</td>
<td>V</td>
</tr>
<tr>
<td>0x6</td>
<td>0.822</td>
<td>0.895</td>
<td>0.969</td>
<td>V</td>
</tr>
<tr>
<td>0x7</td>
<td>0.971</td>
<td>1.044</td>
<td>1.118</td>
<td>V</td>
</tr>
<tr>
<td>0x8</td>
<td>1.120</td>
<td>1.193</td>
<td>1.267</td>
<td>V</td>
</tr>
<tr>
<td>0x9</td>
<td>1.269</td>
<td>1.343</td>
<td>1.416</td>
<td>V</td>
</tr>
<tr>
<td>0xA</td>
<td>1.418</td>
<td>1.492</td>
<td>1.565</td>
<td>V</td>
</tr>
<tr>
<td>0xB</td>
<td>1.567</td>
<td>1.641</td>
<td>1.715</td>
<td>V</td>
</tr>
<tr>
<td>0xC</td>
<td>1.717</td>
<td>1.790</td>
<td>1.864</td>
<td>V</td>
</tr>
<tr>
<td>0xD</td>
<td>1.866</td>
<td>1.939</td>
<td>2.013</td>
<td>V</td>
</tr>
<tr>
<td>0xE</td>
<td>2.015</td>
<td>2.089</td>
<td>2.162</td>
<td>V</td>
</tr>
<tr>
<td>0xF</td>
<td>2.164</td>
<td>2.238</td>
<td>2.311</td>
<td>V</td>
</tr>
</tbody>
</table>

24.19 Pulse-Width Modulator (PWM)

Table 24-40. PWM Timing Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_{\text{FLTMIN}} )</td>
<td>MnFAULTn De-Assertion to PWM Active(^a)</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{FLTMAX}} )</td>
<td>MnFAULTn Assertion to PWM Inactive(^a)</td>
<td>-</td>
<td>-</td>
<td>27 + (1 PWM clock)</td>
<td>ns</td>
</tr>
<tr>
<td>( T_{\text{FLTMIN}} )</td>
<td>Minimum Fault Pulse Width</td>
<td>2</td>
<td>-</td>
<td>-</td>
<td>PWM clock periods</td>
</tr>
</tbody>
</table>

a. This parameter value can vary depending on the PWM clock frequency which is controlled by the System Clock and a programmable divider field in the PWMCC register.

b. The latch and minimum fault period functions that can be enabled in the PWMnCTL register can change the timing of this parameter.
## 24.20 Current Consumption

Table 24-41. Current Consumption

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Conditions</th>
<th>System Clock</th>
<th>Nom</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Frequency</td>
<td>Clock Source</td>
<td>-40°C</td>
</tr>
<tr>
<td>I_{DD RUN}</td>
<td>Run mode (Flash loop)</td>
<td>$V_{DD} = 3.3 \text{ V}$ $V_{DDA} = 3.3 \text{ V}$ Peripherals = All ON</td>
<td>80 MHz MOSC with PLL</td>
<td>45.0</td>
<td>45.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>40 MHz MOSC with PLL</td>
<td>31.9</td>
<td>32.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>16 MHz MOSC with PLL</td>
<td>19.6</td>
<td>19.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>16 MHz PIOCSC</td>
<td>17.5</td>
<td>17.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 MHz PIOCSC</td>
<td>10.0</td>
<td>10.1</td>
</tr>
<tr>
<td></td>
<td>Run mode (SRAM loop)</td>
<td>$V_{DD} = 3.3 \text{ V}$ $V_{DDA} = 3.3 \text{ V}$ Peripherals = All OFF</td>
<td>80 MHz MOSC with PLL</td>
<td>24.5</td>
<td>24.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>40 MHz MOSC with PLL</td>
<td>19.6</td>
<td>19.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>16 MHz MOSC with PLL</td>
<td>12.1</td>
<td>12.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>16 MHz PIOCSC</td>
<td>10.1</td>
<td>10.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 MHz PIOCSC</td>
<td>5.45</td>
<td>5.50</td>
</tr>
<tr>
<td>I_{DD A}</td>
<td>Run, Sleep and Deep-sleep mode</td>
<td>$V_{DD} = 3.3 \text{ V}$ $V_{DDA} = 3.3 \text{ V}$ Peripherals = All ON</td>
<td>MOSC with PLL</td>
<td>2.71</td>
<td>2.71</td>
</tr>
<tr>
<td></td>
<td>Deep-Sleep mode</td>
<td>30 kHz LFIOSC</td>
<td>2.54</td>
<td>2.54</td>
<td>2.54</td>
</tr>
<tr>
<td></td>
<td>Run, Sleep and Deep-sleep mode</td>
<td>$V_{DD} = 3.3 \text{ V}$ $V_{DDA} = 3.3 \text{ V}$ Peripherals = All OFF</td>
<td>-</td>
<td>0.28</td>
<td>0.28</td>
</tr>
<tr>
<td>Parameter</td>
<td>Parameter Name</td>
<td>Conditions</td>
<td>System Clock</td>
<td>Nom</td>
<td>Max</td>
</tr>
<tr>
<td>-----------</td>
<td>----------------</td>
<td>------------</td>
<td>--------------</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Frequency</td>
<td>Clock Source</td>
<td>-40°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.3 V</td>
<td>80 MHz</td>
<td>MOSC with PLL</td>
<td>29.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V</td>
<td>40 MHz</td>
<td>MOSC with PLL</td>
<td>19.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peripherals = All ON</td>
<td>16 MHz</td>
<td>MOSC with PLL</td>
<td>13.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDO = 1.2 V</td>
<td>16 MHz</td>
<td>PIOCSC&lt;sup&gt;c&lt;/sup&gt;</td>
<td>11.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sleep mode</td>
<td>1 MHz</td>
<td>PIOCSC&lt;sup&gt;c&lt;/sup&gt;</td>
<td>7.01</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(FLASHPM = 0x0)</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.3 V</td>
<td>80 MHz</td>
<td>MOSC with PLL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V</td>
<td>40 MHz</td>
<td>MOSC with PLL</td>
<td>7.49</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peripherals = All OFF</td>
<td>16 MHz</td>
<td>MOSC with PLL</td>
<td>6.22</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDO = 1.2 V</td>
<td>16 MHz</td>
<td>PIOCSC&lt;sup&gt;c&lt;/sup&gt;</td>
<td>4.28</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sleep mode</td>
<td>1 MHz</td>
<td>PIOCSC&lt;sup&gt;c&lt;/sup&gt;</td>
<td>3.52</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(FLASHPM = 0x2)</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.3 V</td>
<td>80 MHz</td>
<td>MOSC with PLL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V</td>
<td>40 MHz</td>
<td>MOSC with PLL</td>
<td>18.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peripherals = All ON</td>
<td>16 MHz</td>
<td>MOSC with PLL</td>
<td>12.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDO = 1.2 V</td>
<td>16 MHz</td>
<td>PIOCSC&lt;sup&gt;c&lt;/sup&gt;</td>
<td>10.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sleep mode</td>
<td>1 MHz</td>
<td>PIOCSC&lt;sup&gt;c&lt;/sup&gt;</td>
<td>7.09</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(FLASHPM = 0x2)</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.3 V</td>
<td>80 MHz</td>
<td>MOSC with PLL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DDA&lt;/sub&gt; = 3.3 V</td>
<td>40 MHz</td>
<td>MOSC with PLL</td>
<td>6.55</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peripherals = All OFF</td>
<td>16 MHz</td>
<td>MOSC with PLL</td>
<td>5.27</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LDO = 1.2 V</td>
<td>16 MHz</td>
<td>PIOCSC&lt;sup&gt;c&lt;/sup&gt;</td>
<td>3.34</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 MHz</td>
<td>PIOCSC&lt;sup&gt;c&lt;/sup&gt;</td>
<td>2.58</td>
</tr>
</tbody>
</table>
## Table 24-41. Current Consumption (continued)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Name</th>
<th>Conditions</th>
<th>System Clock</th>
<th>Nom</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Frequency</td>
<td>Clock Source</td>
<td>-40°C</td>
<td>25°C</td>
</tr>
<tr>
<td>I_DD_DEEPSLEEP</td>
<td>Deep-sleep mode (FLASHPM = 0x0)</td>
<td>V_DD = 3.3 V</td>
<td>16 MHz</td>
<td>PIOSC</td>
<td>9.29</td>
<td>9.29</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDA = 3.3 V</td>
<td>30 kHz</td>
<td>LFIOSC</td>
<td>5.10</td>
<td>5.10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peripherals = All ON LDO = 1.2 V</td>
<td>V_DD = 3.3 V</td>
<td>PIOSC</td>
<td>3.51</td>
<td>3.51</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDA = 3.3 V</td>
<td>30 kHz</td>
<td>LFIOSC</td>
<td>2.00</td>
<td>2.00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peripherals = All OFF LDO = 1.2 V</td>
<td>V_DD = 3.3 V</td>
<td>PIOSC</td>
<td>8.34</td>
<td>8.36</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DDA = 3.3 V</td>
<td>30 kHz</td>
<td>LFIOSC</td>
<td>4.14</td>
<td>4.18</td>
</tr>
<tr>
<td>I_HIB_NOTC</td>
<td>Hibernate mode (external wake, RTC disabled)</td>
<td>V_BAT = 3.0 V</td>
<td>-</td>
<td>-</td>
<td>1.23</td>
<td>1.38</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD = 0 V</td>
<td>V_DDA = 0 V</td>
<td>System Clock = OFF Hibernate Module = 32.768 kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_HIB_RTC</td>
<td>Hibernate mode (RTC enabled)</td>
<td>V_BAT = 3.0 V</td>
<td>-</td>
<td>-</td>
<td>1.27</td>
<td>1.40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD = 0 V</td>
<td>V_DDA = 0 V</td>
<td>System Clock = OFF Hibernate Module = 32.768 kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_HIB_VDD3ON</td>
<td>Hibernate mode (VDD3ON mode, RTC on)</td>
<td>V_BAT = 3.0 V</td>
<td>-</td>
<td>-</td>
<td>3.17</td>
<td>4.49</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD = 3.3 V</td>
<td>V_DDA = 3.3 V</td>
<td>System Clock = OFF Hibernate Module = 32.768 kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hibernate mode (VDD3ON mode, RTC off)</td>
<td>V_BAT = 3.0 V</td>
<td>-</td>
<td>-</td>
<td>3.16</td>
<td>4.33</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD = 3.3 V</td>
<td>V_DDA = 3.3 V</td>
<td>System Clock = OFF Hibernate Module = 32.768 kHz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Applicable for extended temperature devices only.
- The value for I_DDA is included in the above values for I_DD_RUN, I_DD_SLEEP, and I_DD_DEEPSLEEP.
- Note that if the MOSC is the source of the Run-mode system clock and is powered down in Sleep mode, wake time is increased by T_MOSC_SETTLE.
A Package Information

A.1 Orderable Devices

The figure below defines the full set of orderable part numbers for the TM4C123x Series. See the Package Option Addendum for the complete list of valid orderable part numbers for the TM4C123GH6PZ microcontroller.

Figure A-1. Key to Part Numbers

Prefix
   T = Qualified Device
   X = Experimental Device

Core
   M4 = ARM® Cortex™-M4

Tiva Series
   C = Connected MCUs

Family

Part Number
   SSS = Series identifier

Program Memory
   C = 32 KB
   D = 64 KB
   E = 128 KB
   H = 256 KB

Data Memory
   3 = 12 KB
   5 = 24 KB
   6 = 32 KB

Package
   PZ = 100-pin LQFP
   PGE = 144-pin LQFP
   ZRB = 157-ball BGA

Temperature
   I = –40°C to +85°C
   T = –40°C to +105°C

Shipping Medium
   R = Tape-and-reel
   Omitted = Default shipping (tray or tube)

Revision

Special Codes
   Optional

A.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microcontroller (MCU) devices. Each Tiva™ C Series family member has one of two prefixes: XM4C or TM4C. These prefixes represent evolutionary stages of product development from engineering prototypes (XM4C) through fully qualified production devices (TM4C).

Device development evolutionary flow:

- XM4C — Experimental device that is not necessarily representative of the final device’s electrical specifications and may not use production assembly flow.

- TM4C — Production version of the silicon die that is fully qualified.

XM4C devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TM4C devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI’s standard warranty applies.

Predictions show that prototype devices (XM4C) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.
A.3 Device Markings

The figure below shows an example of the Tiva™ microcontroller package symbolization.

This identifying number contains the following information:

- **Lines 1 and 5:** Internal tracking numbers
- **Lines 2 and 3:** Part number

For example, TM4C123G on the second line followed by H6PGEI7 on the third line indicates orderable part number TM4C123GH6PGEI7. The silicon revision number is the last number in the part number, in this example, 7. The DID0 register also identifies the version of the microcontroller, as shown in the table below. Combined, the MAJOR and MINOR bit fields indicate the die revision and part revision numbers.

<table>
<thead>
<tr>
<th>MAJOR Bitfield Value</th>
<th>MINOR Bitfield Value</th>
<th>Die Revision</th>
<th>Part Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0x0</td>
<td>A0</td>
<td>1</td>
</tr>
<tr>
<td>0x0</td>
<td>0x1</td>
<td>A1</td>
<td>2</td>
</tr>
<tr>
<td>0x0</td>
<td>0x2</td>
<td>A2</td>
<td>3</td>
</tr>
<tr>
<td>0x0</td>
<td>0x3</td>
<td>A3</td>
<td>4</td>
</tr>
<tr>
<td>0x1</td>
<td>0x0</td>
<td>B0</td>
<td>5</td>
</tr>
<tr>
<td>0x1</td>
<td>0x1</td>
<td>B1</td>
<td>6</td>
</tr>
<tr>
<td>0x1</td>
<td>0x2</td>
<td>B2</td>
<td>7</td>
</tr>
</tbody>
</table>

- **Line 4:** Date code

The first two characters on the fourth line indicate the date code, followed by internal tracking numbers. The two-digit date code YM indicates the last digit of the year, then the month. For example, a 34 for the first two digits of the fourth line indicates a date code of April 2013.
A.4 Packaging Diagram

Figure A-2. TM4C123GH6PZ 100-Pin LQFP Package Diagram

MECHANICAL DATA

PZ (S-PQFP-G100) PLASTIC QUAD FLATPACK

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Texas Instruments-Production Data
June 12, 2014

1442
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TM4C123GH6PZI7</td>
<td>ACTIVE</td>
<td>LQFP</td>
<td>PZ</td>
<td>100</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>TM4C123G H6PZI7</td>
<td></td>
</tr>
<tr>
<td>TM4C123GH6PZI7R</td>
<td>ACTIVE</td>
<td>LQFP</td>
<td>PZ</td>
<td>100</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>TM4C123G H6PZI7</td>
<td></td>
</tr>
<tr>
<td>TM4C123GH6PZT7</td>
<td>ACTIVE</td>
<td>LQFP</td>
<td>PZ</td>
<td>100</td>
<td>90</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 105</td>
<td>TM4C123G H6PZT7</td>
<td></td>
</tr>
<tr>
<td>TM4C123GH6PZT7R</td>
<td>ACTIVE</td>
<td>LQFP</td>
<td>PZ</td>
<td>100</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 105</td>
<td>TM4C123G H6PZT7</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
- **TBD**: The Pb-Free/Green conversion plan has not been defined.
- **Pb-Free (RoHS)**: TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
- **Pb-Free (RoHS Exempt)**: This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
- **Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
IMPORTANT NOTICE AND DISCLAIMER

TI provides technical and reliability data (including datasheets), design resources (including reference designs), application or other design advice, web tools, safety information, and other resources “as is” and with all faults, and disclaims all warranties, express and implied, including without limitation any implied warranties of merchantability, fitness for a particular purpose or non-infringement of third party intellectual property rights.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated